# Design

The design goal for the 1-bit full Subtractor is high speed. The implementation of the 1-bit subtractor is represented in Figure1 below with 4 different types of gates as INVERTER, AND, 3-input OR, and XOR.



Figure Schematic for 1-bit Subtractor

The critical path of this design is the path of two XORs which takes the longest propagation delay. So as to achieve the high speed requirement, the speed of XOR needs to be high. Therefore, the design of XOR in the previous section is used. In the convenience of design, the ratio and NWIDTH value is kept the same for other gates design. The schematic of these gates are shown below.



Figure Schematic for INVERTER



Figure Schematic for AND gate



Figure Schematic for 3-input OR

In order to speed up the output of the Subtractor, buffers which are made up of two inverters are added into the design as can be seen in the Figure below.



Figure Schematic for 1-bit Subtractor with buffer.

In the case that all schematic design is completed as the value of P/NWIDTH is configured, the layout of each gates are produced as following and the combination of gates for subtractor with buffers added is presented in the last.



Figure INVERTER Layout



Figure AND Layout



Figure 3-input OR Layout



Figure Subtractor with Buffer Layout

# Testing

For testing the function of the design, transient analysis is used and the results are shown in the figures below. From this figure, it is available to get a truth table showing the correct operation of the design.

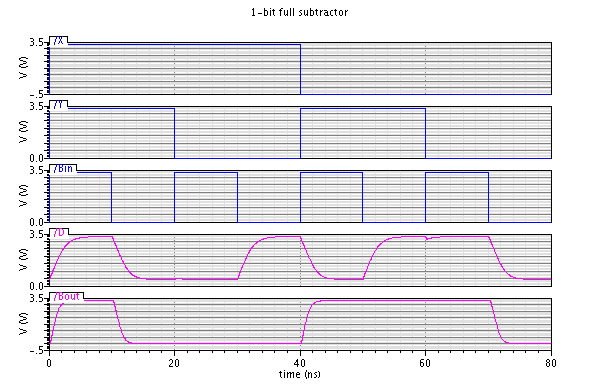


Figure Subtractor Schematic Simulation

Another transient analysis is launched to compare the performance of the subtractor with buffers against the original subtractor. The results are shown below and it can be easily found that the one with buffers works much faster especially for the output speed of D which is the combination of two XOR gates.

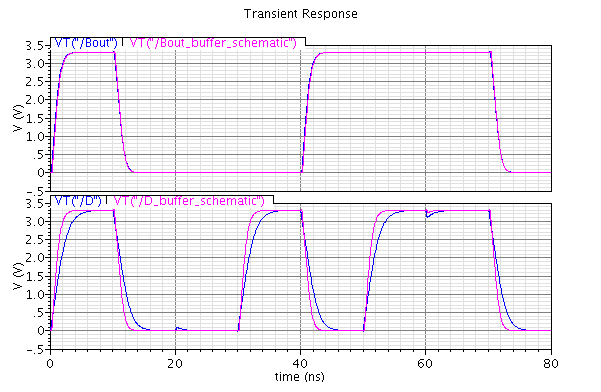


Figure Comparisons of Subtractor and Subtractor\_buffer

The simulation Figure 12 below shows the output of Layout against the output of Schematic under transient analysis sharing the same results and are very close to each other which indicates the correct operation and good design of Layout.

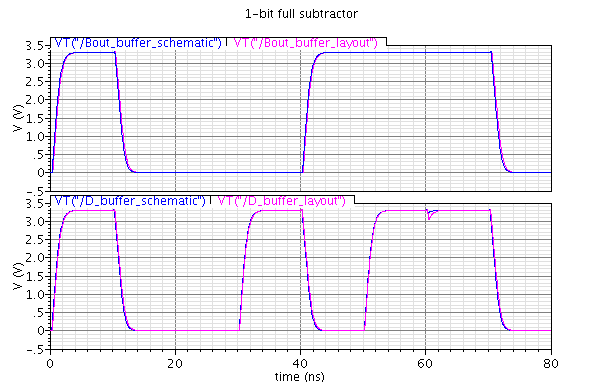


Figure Subtractor Layout Simulation

# Impact of Variability

## Temperature Variations

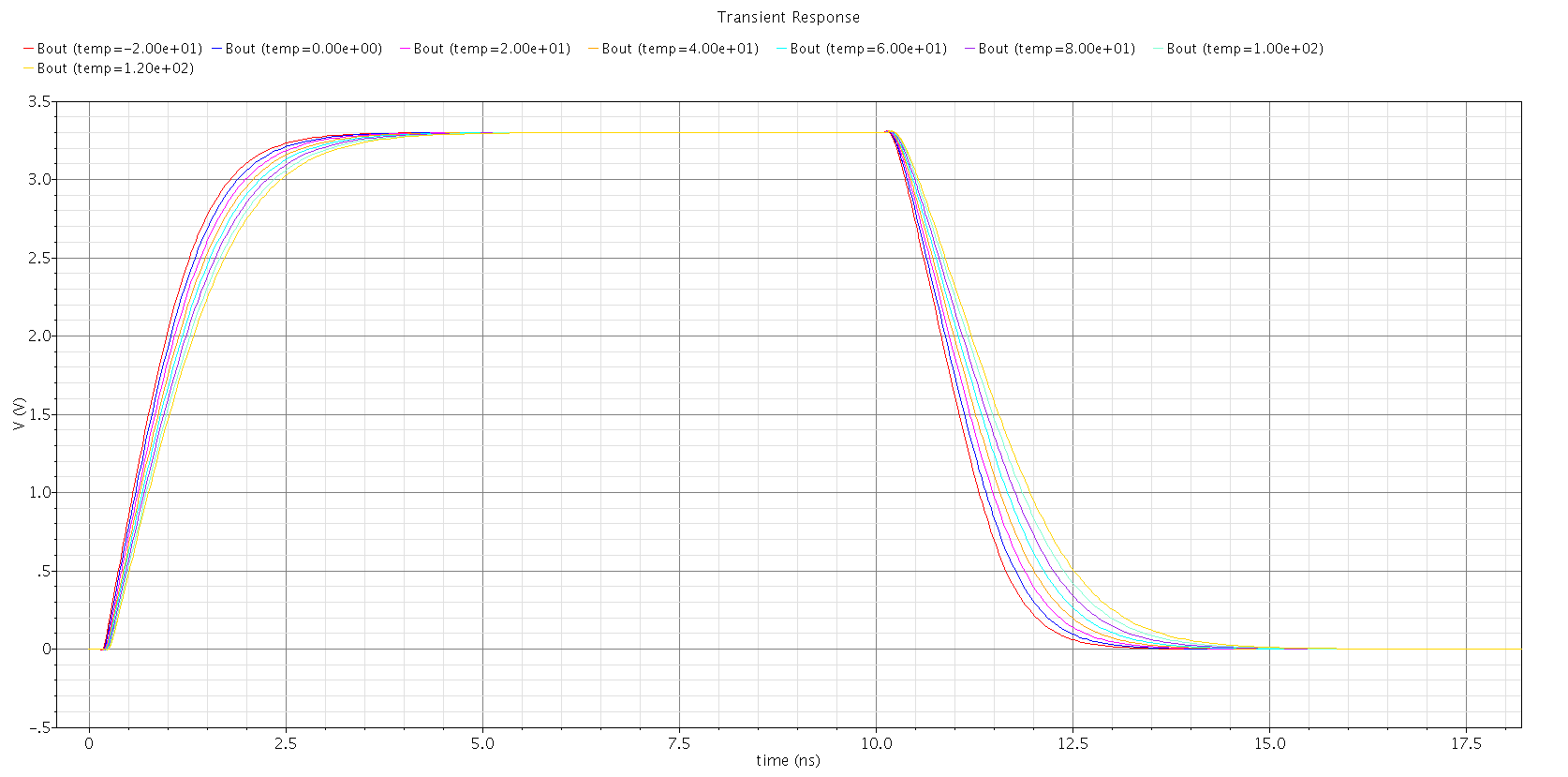


Figure Transient Simulation with Temperature Swapping for Subtractor

This Figure shows the performance of rise and fall time under different temperature. It is indicated that the value of rise and fall time differs with the change of temperature. And with a higher temperature the rise time and fall time increases leading to a longer propagation delay.

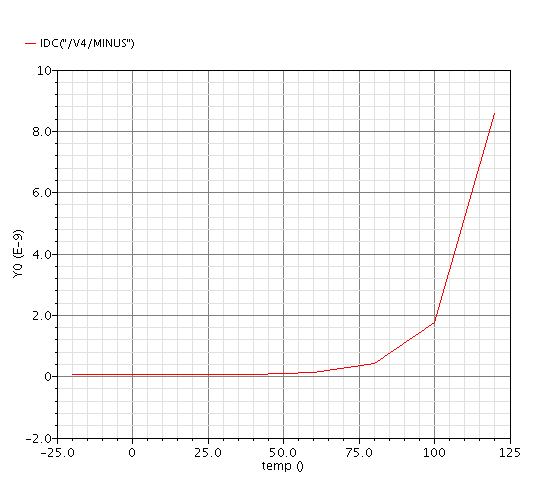


Figure DC simulation with Temperature Swapping for Subtractor

The Figure indicates that the current supply goes extremely high when the temperature is over 75 degrees.

## Power supply Variations

As the design is required to achieve high speed, the different value of supply voltage will not influence the performance of the design as is described in the previous XOR design. Unlike the XOR design, as can been seen from the Figure below, the change of power supply does not influence much the current supply of the circuit as well. This might because of the buffer balancing the performance of the design.

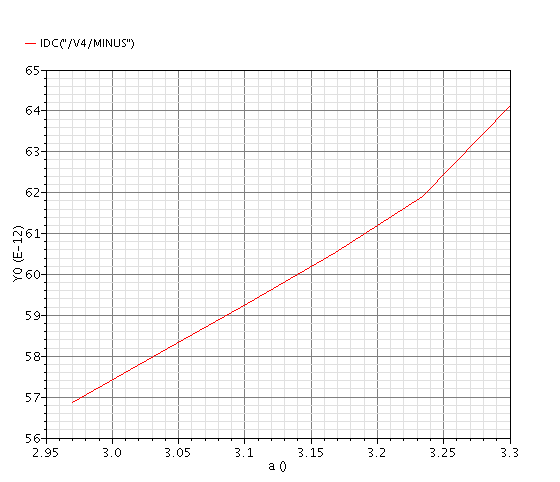


Figure 15 DC simulation with VDD Swapping for Subtractor