# Design

The design goal for the XOR2 is high speed. The first design attempt is to use pass-transistor logic (PTL) as shown in Figure1 where the source side of the MOS transistor is connected to an input line instead of being connected to the power lines and this saves sufficient amount of transistors.



Figure Schematic of PTL design for XOR

However, in this design, problem encountered is the threshold loss at the output node leading to a non-full voltage swing at the output node. The reduction in output voltage swing, on one hand, is useful to power consumption which is not required for the design. On the other hand, this may lead to slow switching in the operation which should be avoided for the design. Therefore, the PTL design is abandoned and the option of complementary CMOS design is considered and found to be better. The Static CMOS XOR is shown in Figure 2.



Figure Schematic of Static CMOS XOR

The ratio between width of PMOS and NMOS is chosen by swapping the ratio to achieve the best results for rise and fall time matching under the circumstance of fan out 2. The configuring method and the results are in the figures below. And the ratio of 3 is chosen.



Figure Test circuit to find out ratio

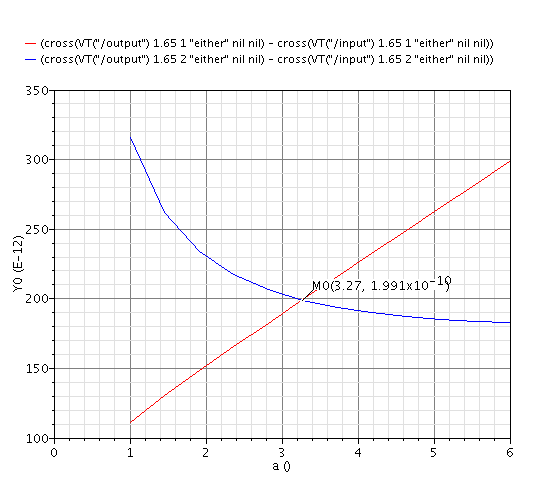


Figure Test results for the ratio

To find out the value of NWIDTH to achieve the design goal of high speed, a ring oscillator with fan out 2 based on XOR is built and tested as shown in figure 5 and 6. The frequency of the RO suggests the propagation delay of the elements.



Figure XOR based RO

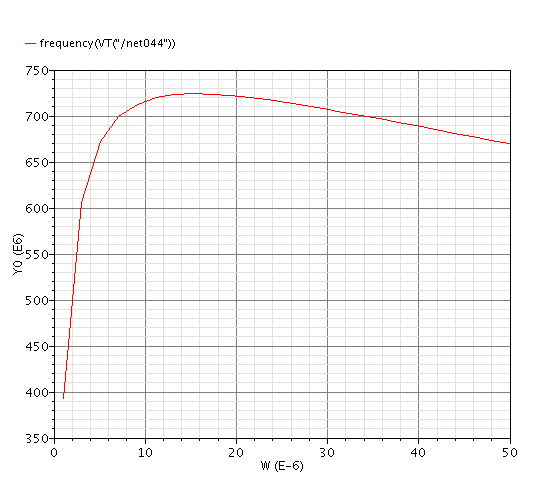


Figure Test results of XOR based RO

As can be seen from the test results, the ring oscillator achieves the highest frequency when the NWIDTH is of 14um. However, comparing this highest point with the point where NWIDTH is 4um, it can be found that, when NWIDTH is 4um, a lot of area is saved with only a little sacrifice of speed. Therefore, the NWIDTH of 4um is chosen and the PWIDTH of 12um is chosen as 3 times the value of NWIDTH. The final layout of XOR is then produced in the Figure below.



Figure XOR Layout

# Testing

For testing the function of both schematic and layout, transient analysis is used and the results are shown in the figures below. For XOR gate, in principle, output goes high if inputs are different. Thus the simulation figures show that the XOR gate designed has the correct operation.

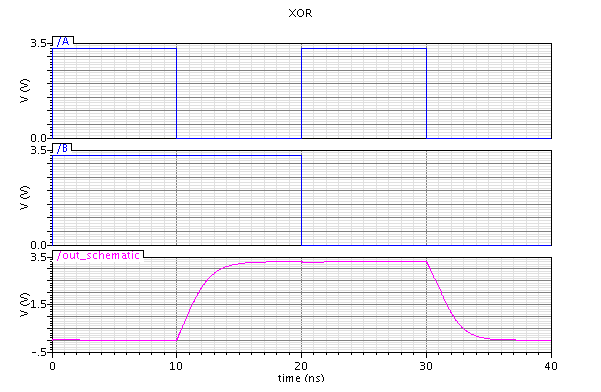


Figure 8 XOR Schematic Simulation

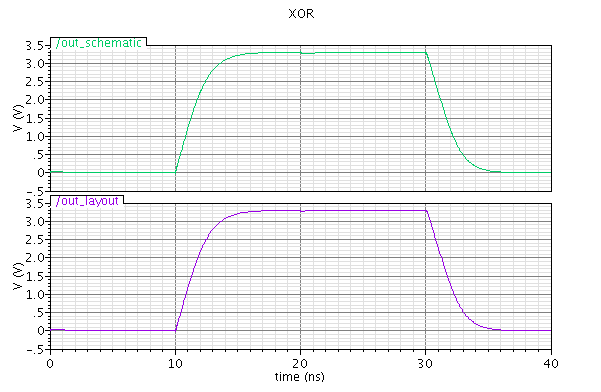


Figure 9 XOR Layout Simulation

# Impact of Variability

## Temperature Variations

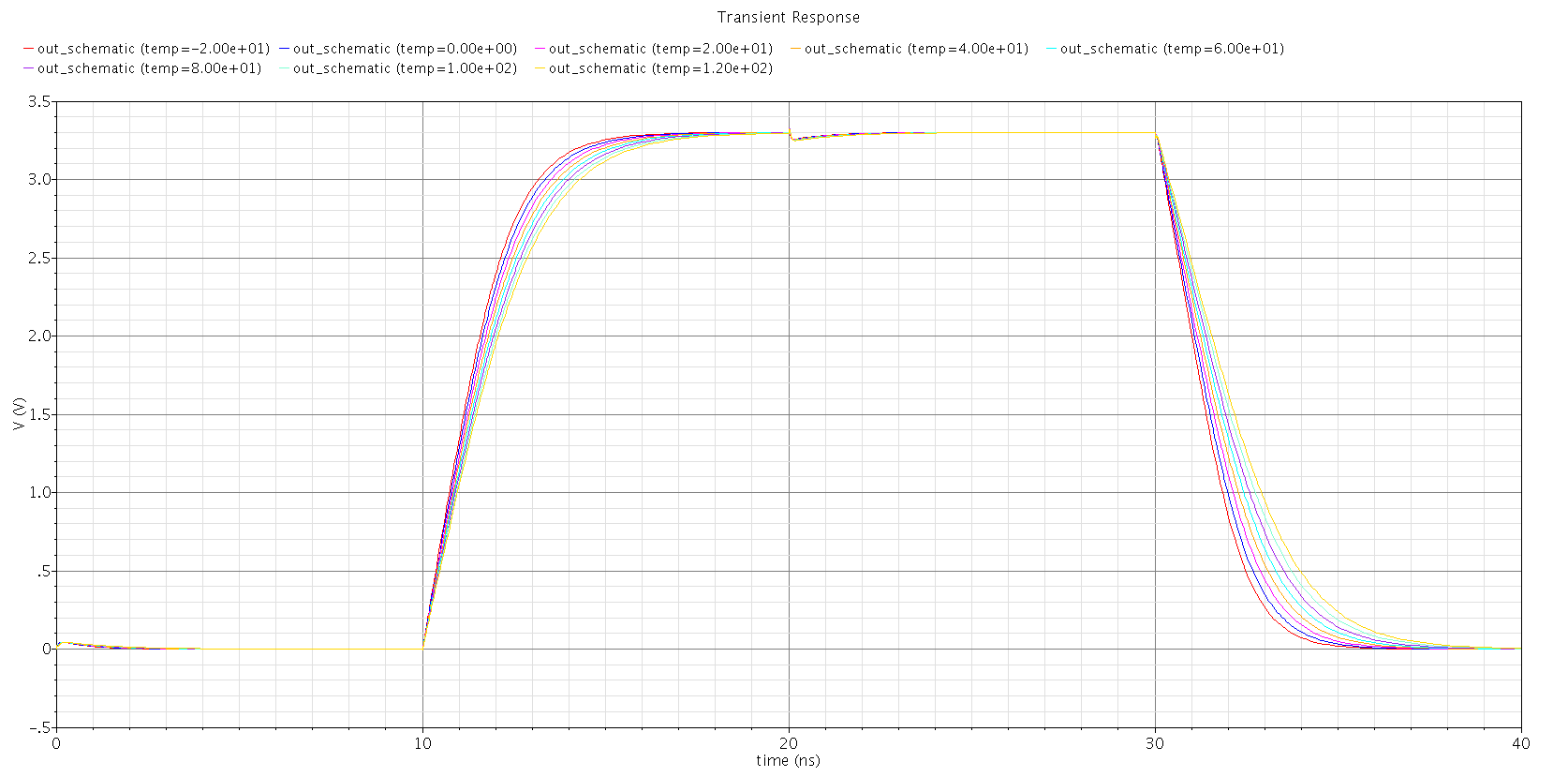


Figure 10 Transient Simulation with Temperature Swapping for XOR

This Figure indicates the rise and fall time differs under different temperature. It is indicated that with a higher temperature the rise time and fall time increases leading to a longer propagation delay.

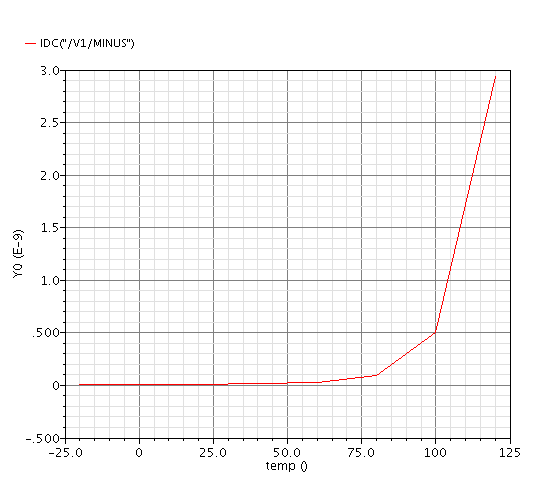


Figure 11 DC simulation with Temperature Swapping for XOR

This Figure shows that the current supply goes extremely high when the temperature goes over 75 degrees.

## Power supply Variations

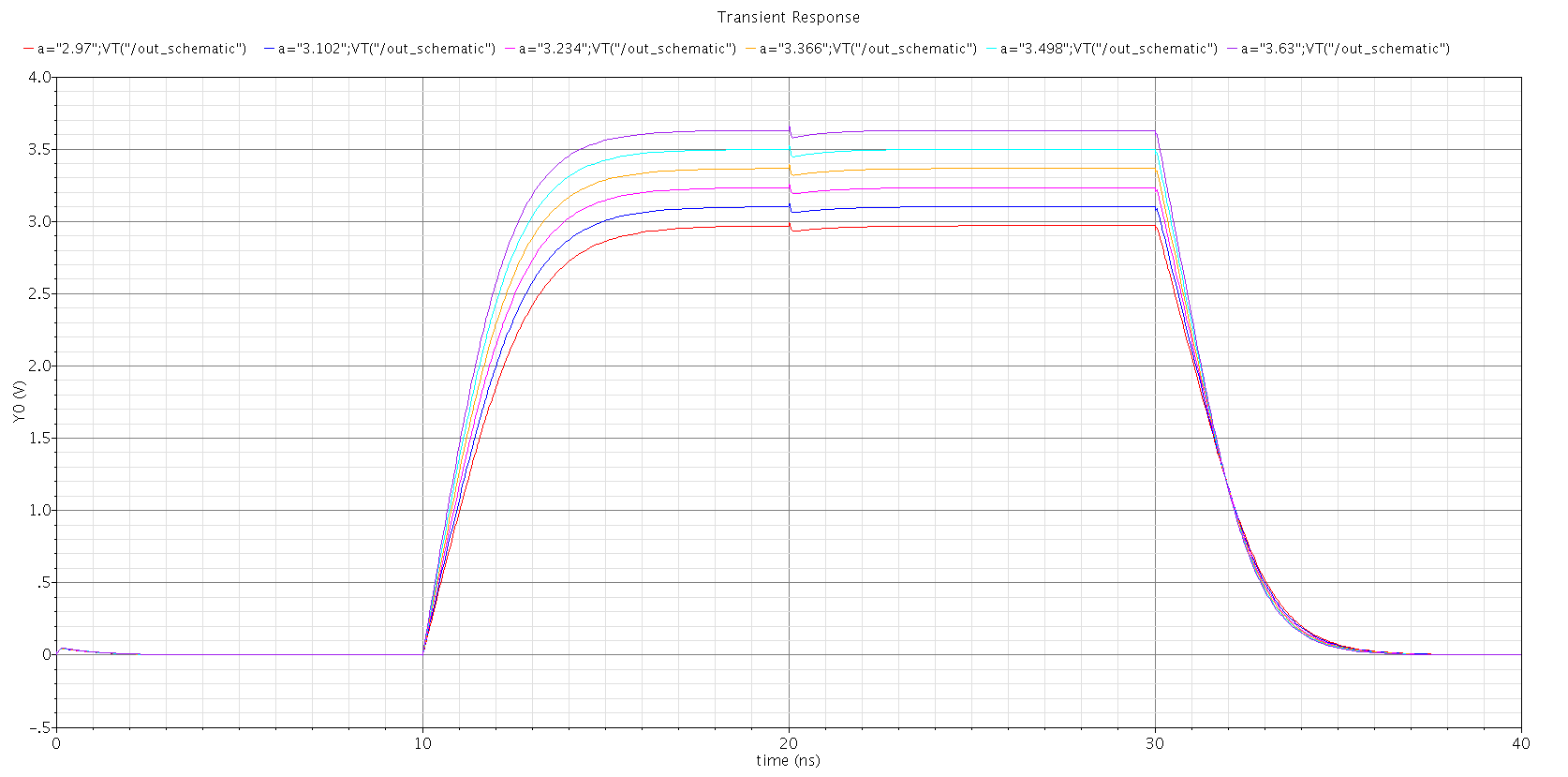


Figure 12 Transient Simulation with VDD Swapping for XOR

As the design goal of the circuit is high speed, the different value of supply voltage will not influence the performance of the gate as can been seen in Figure12.

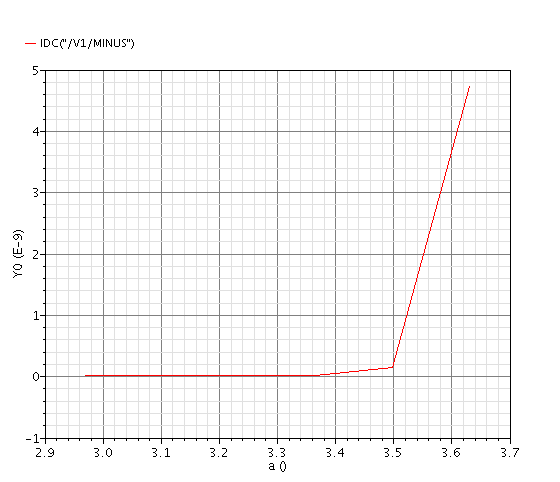


Figure 13 DC simulation with VDD Swapping for XOR

The change of power supply influences the current supply of the circuit. It is suggested by the figure above that the current supply goes extremely high after 3.5V of power supply.