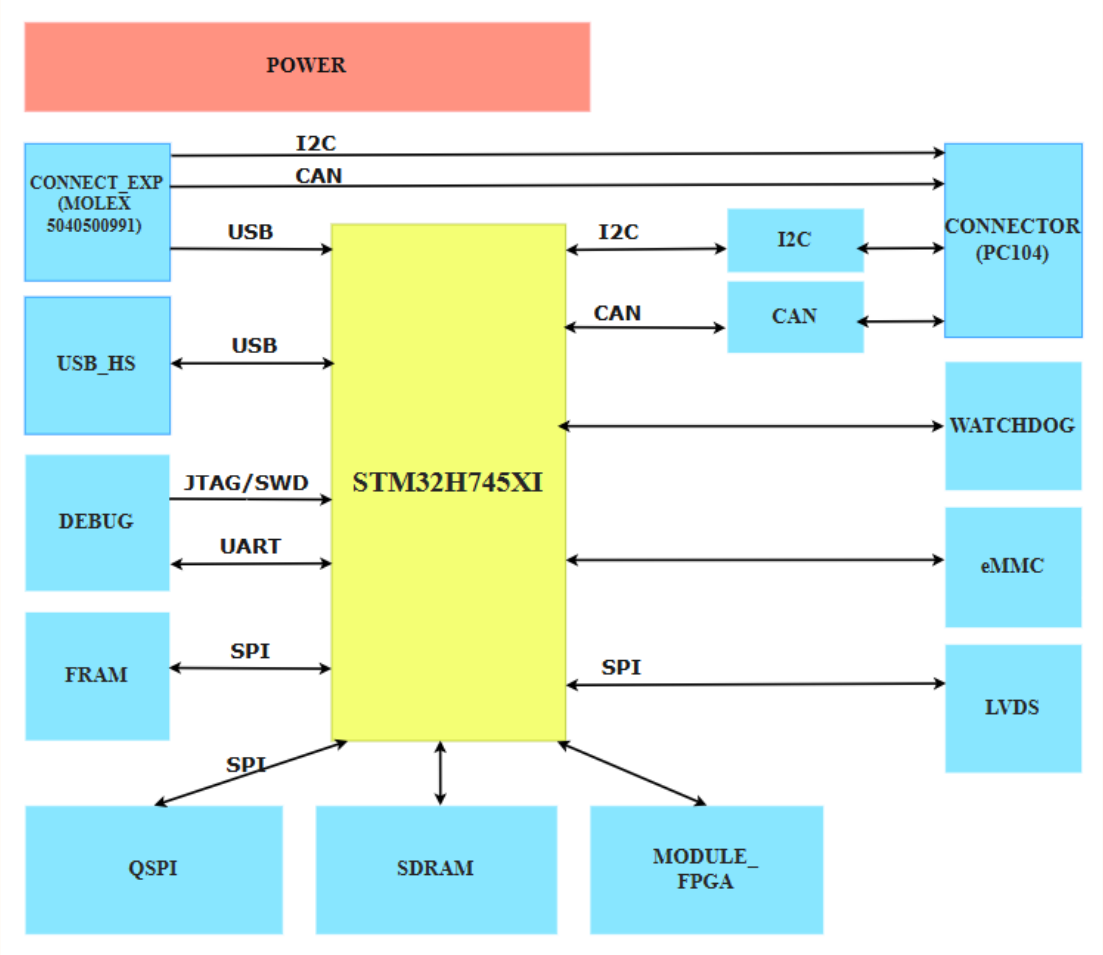
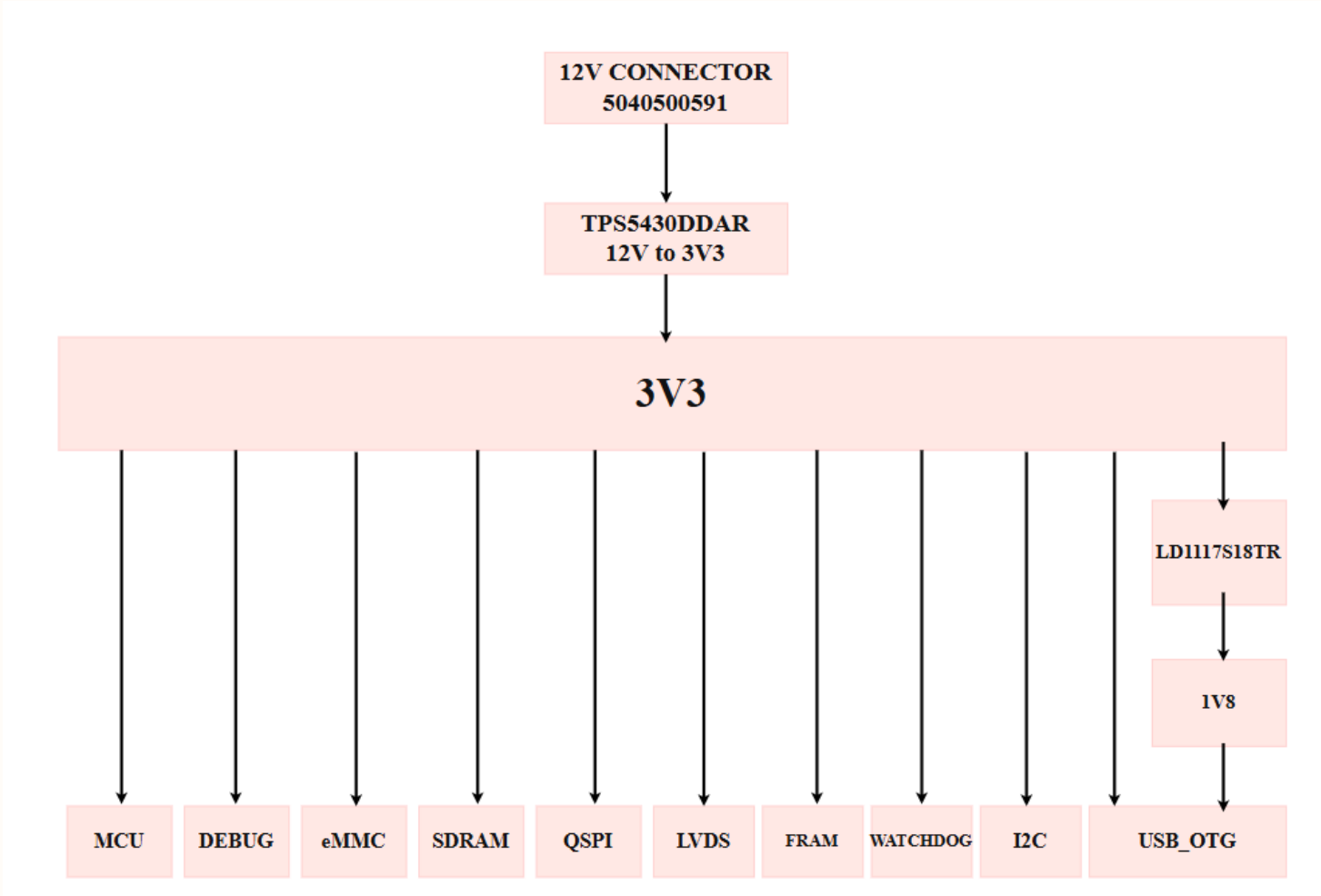
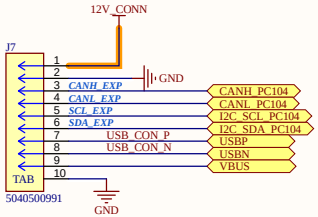


Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: BLOCK_DIAGRAM.SchDoc	Sheet 1 of 16
Checked by: BAO BUI Q.	Document No: 1	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

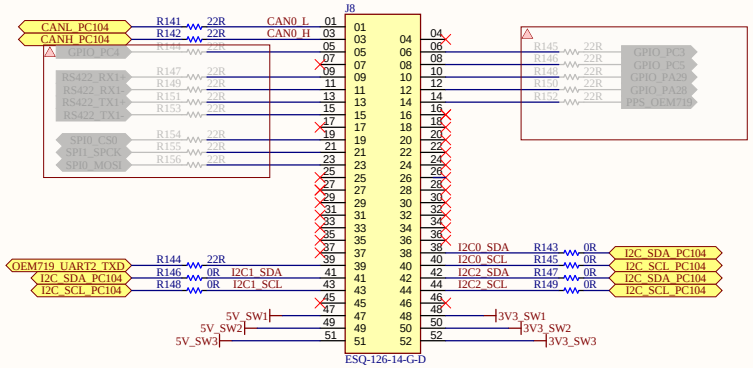


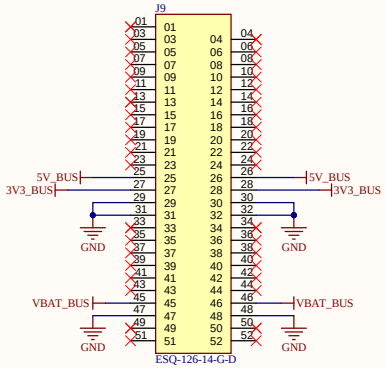
Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: POWER_TREE.SchDoc	Sheet 2 of 16
Checked by: BAO BUI Q.	Document No: 2	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

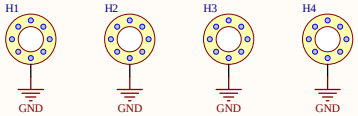
CONNECT BETWEEN EXP AND COMM



PC104

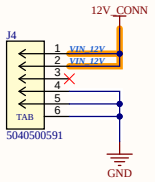




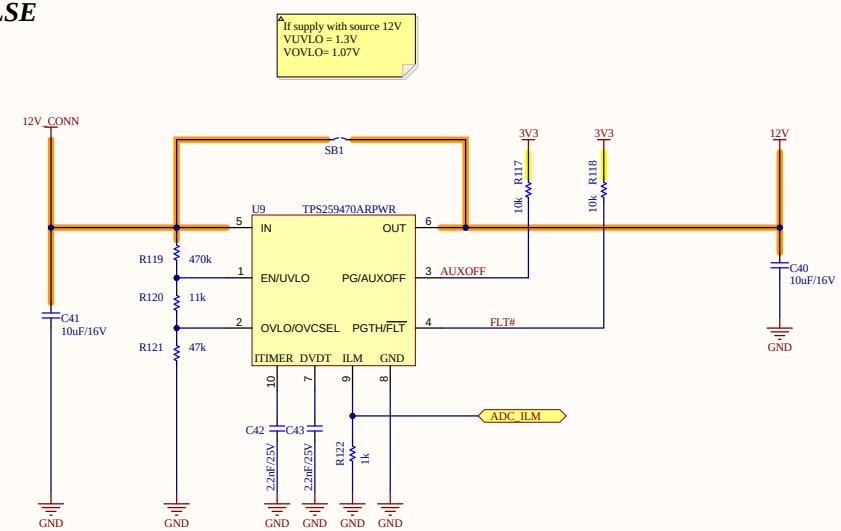


Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: CONNECTOR.SchDoc	Sheet 3 of 16
Checked by: BAO BUI Q.	Document No: 3	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

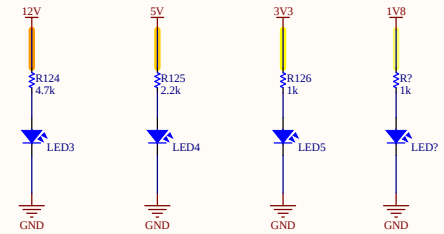
POWER_INPUT



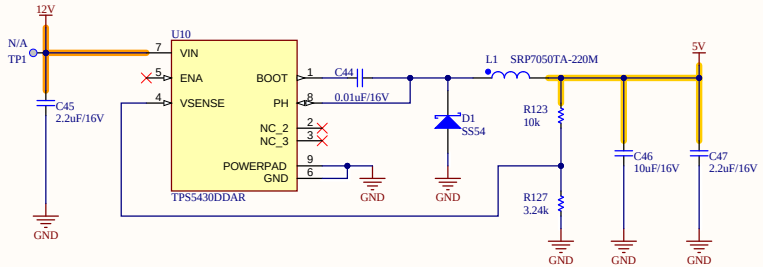
eFULSE



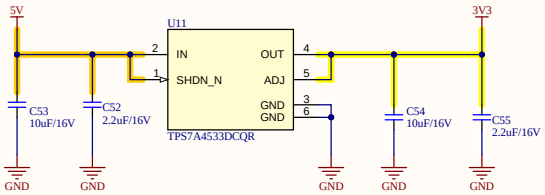
STATUS POWER LED



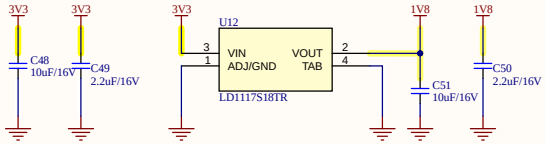
BUCK 12V TO 5V



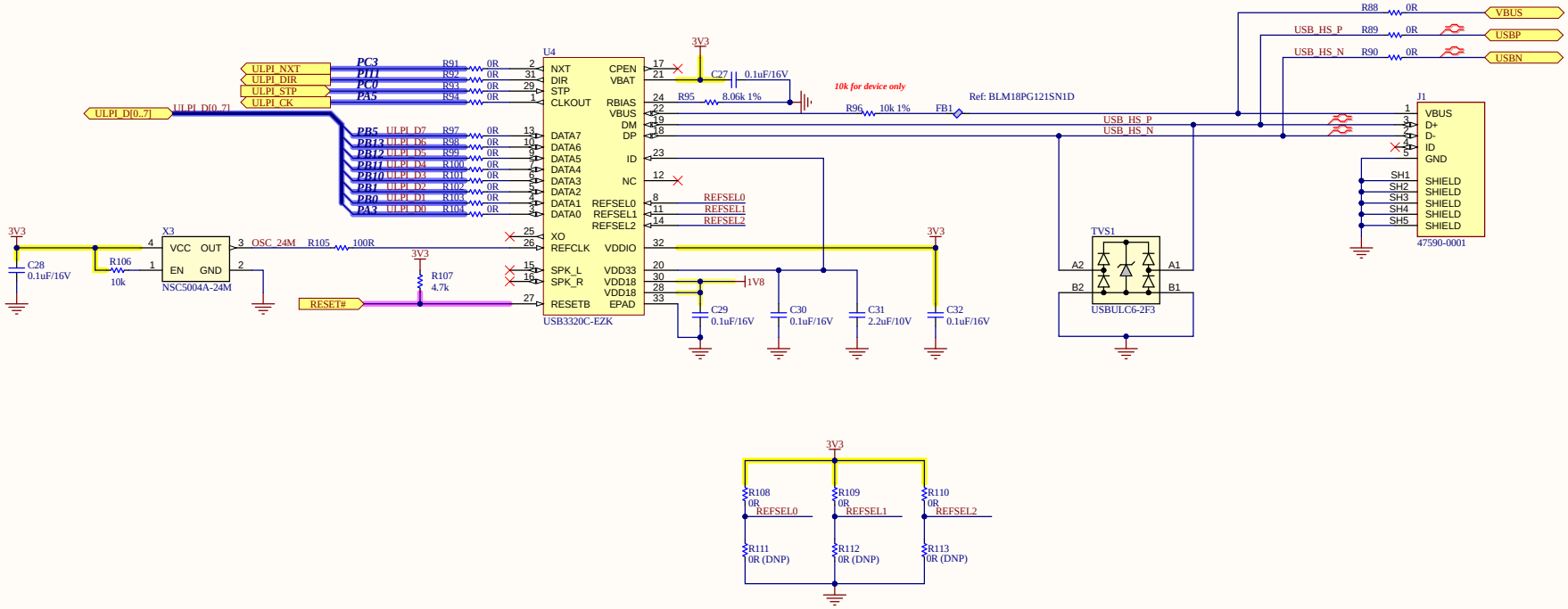
LDO 5V TO 3V3



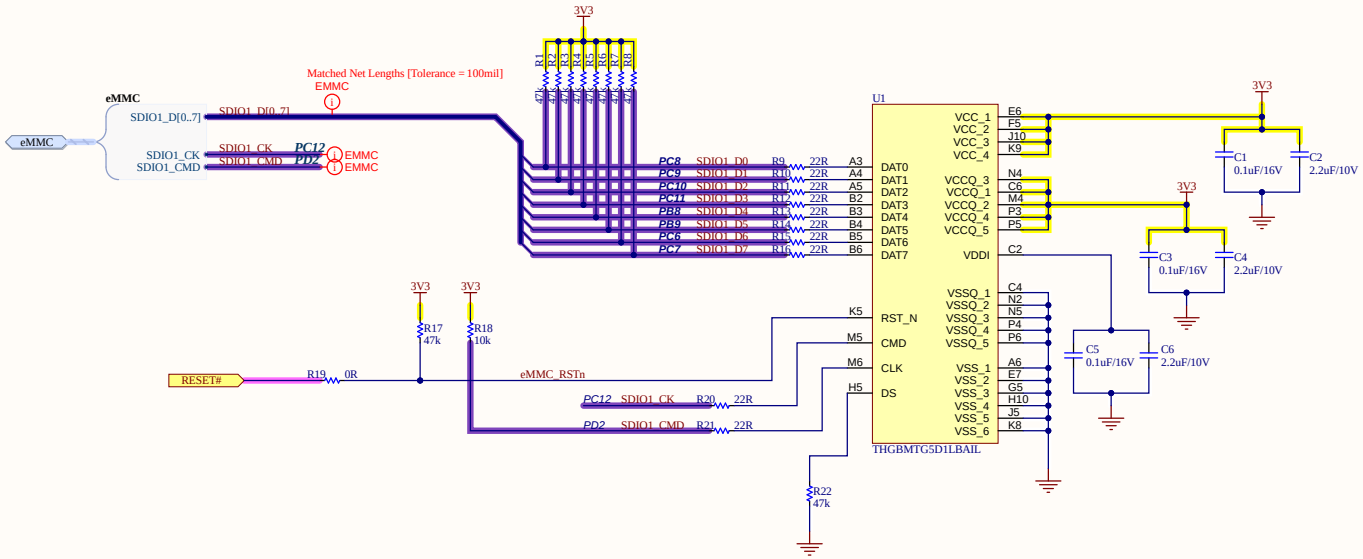
LDO 3V3 TO 1V8



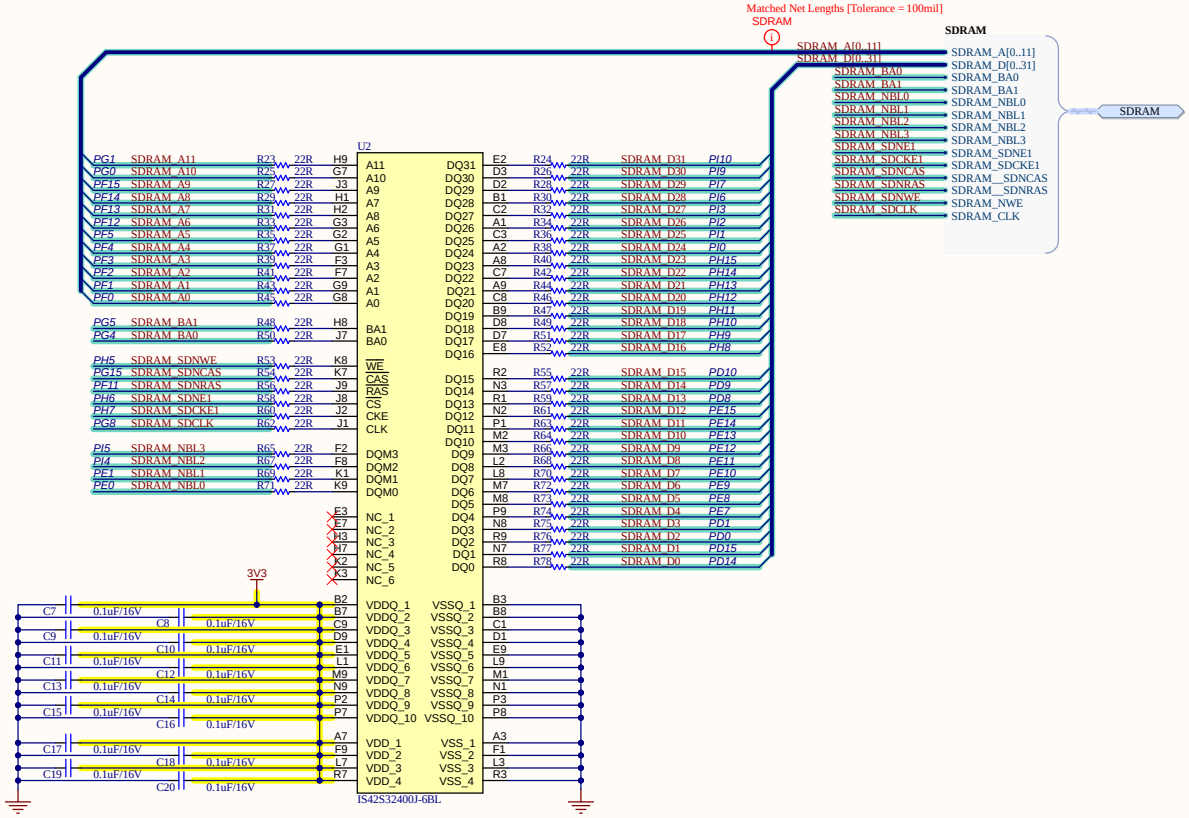
Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: POWER.SchDoc	Sheet 4 of 16
Checked by: BAO BUI Q.	Document No: 4	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



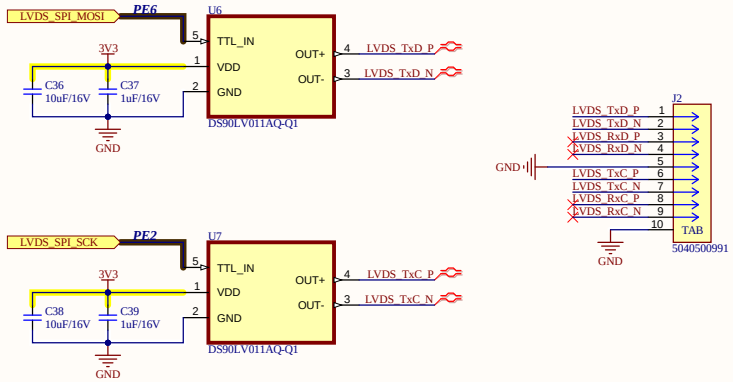
Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: USB_HS_DEVICE.SchDoc	Sheet 5 of 16
Checked by: BAO BUI Q.	Document No: 5	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: eMMC.SchDoc	Sheet 6 of 16
Checked by: BAO BUI Q.	Document No: 6	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

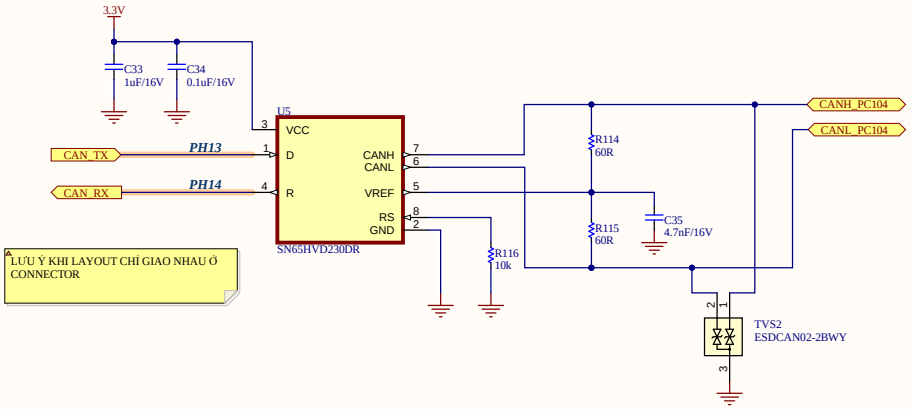


Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: SDRAM.SchDoc	Sheet 7 of 16
Checked by: BAO BUI Q.	Document No: 7	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

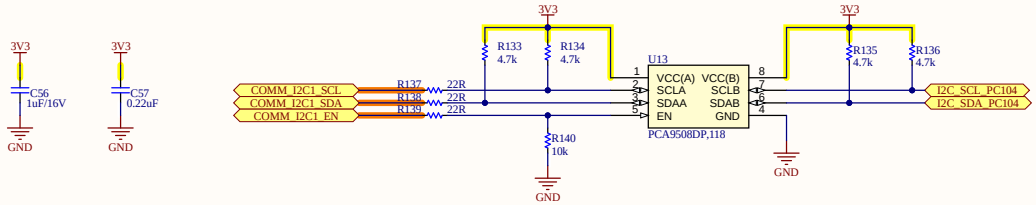


Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: LVDS.SchDoc	Sheet 8 of 16
Checked by: BAO BUI Q.	Document No: 8	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

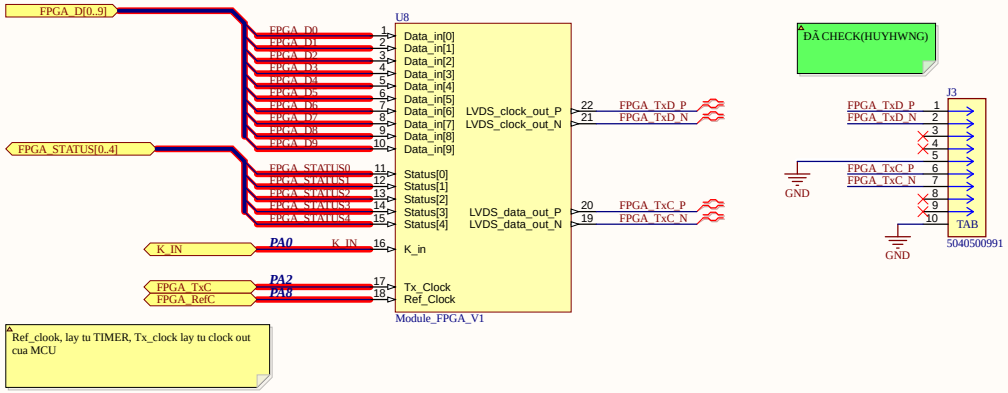
LVDS
HuyHwng



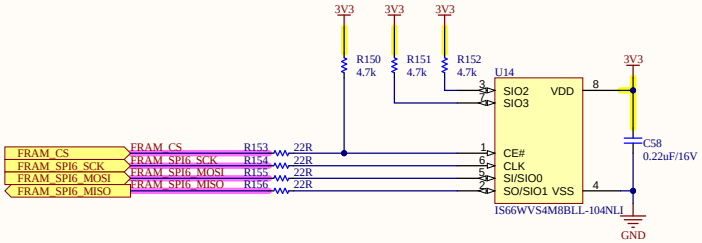
Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: CAN.SchDoc	Sheet 9 of 16
Checked by: BAO BUI Q.	Document No: 9	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



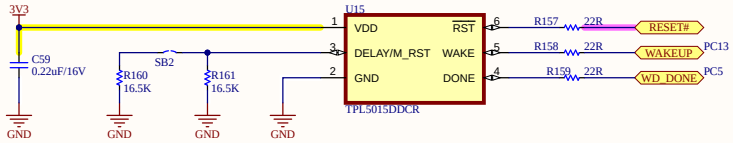
Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: I2C.SchDoc	Sheet 10 of 16
Checked by: BAO BUI Q.	Document No: 10	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: MODULE_FPGA.SchDoc	Sheet 11 of 16
Checked by: BAO BUI Q.	Document No: 11	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

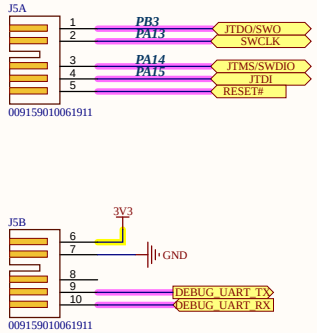


Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: FRAM.SchDoc	Sheet 12 of 16
Checked by: BAO BUI Q.	Document No: 12	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: WATCHDOG.SchDoc	Sheet 13 of 16
Checked by: BAO BUI Q.	Document No: 13	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025

STLink-V3 MINIE



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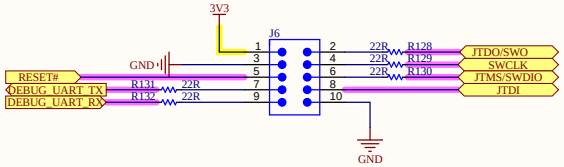
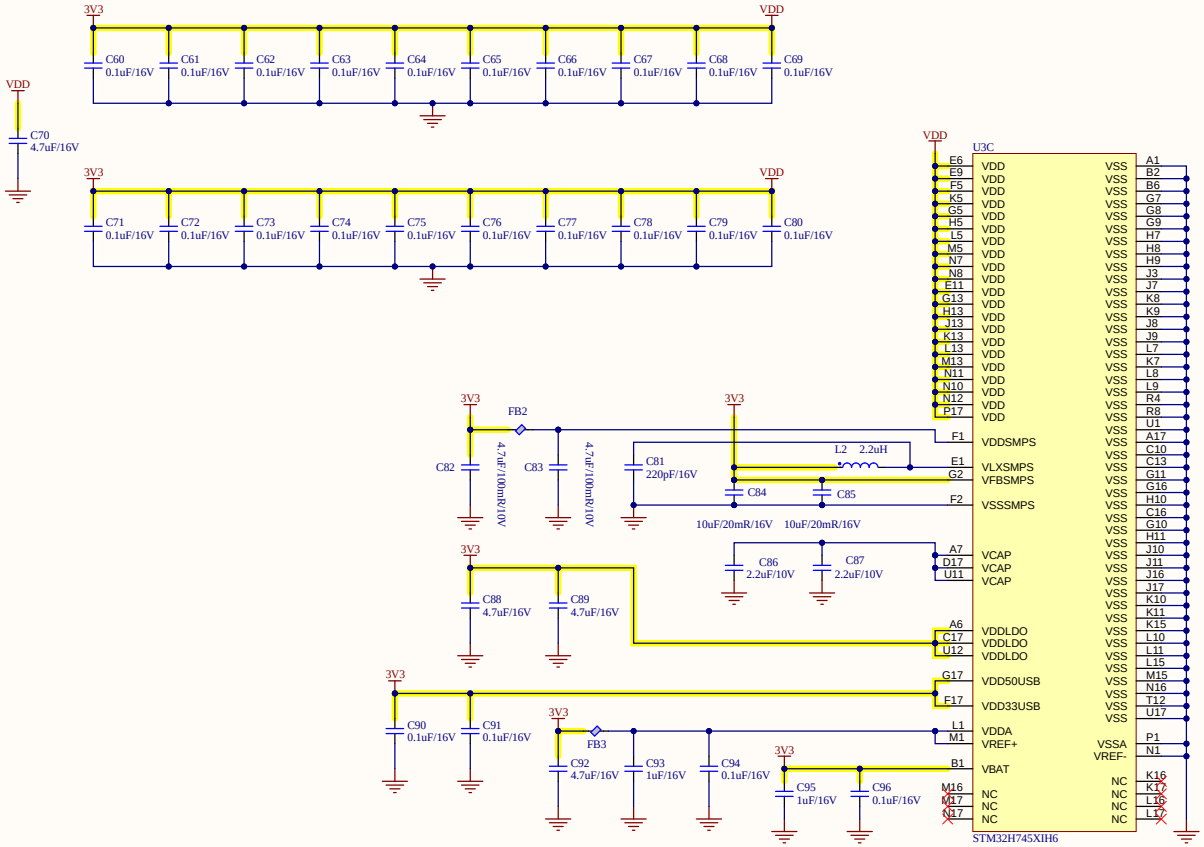
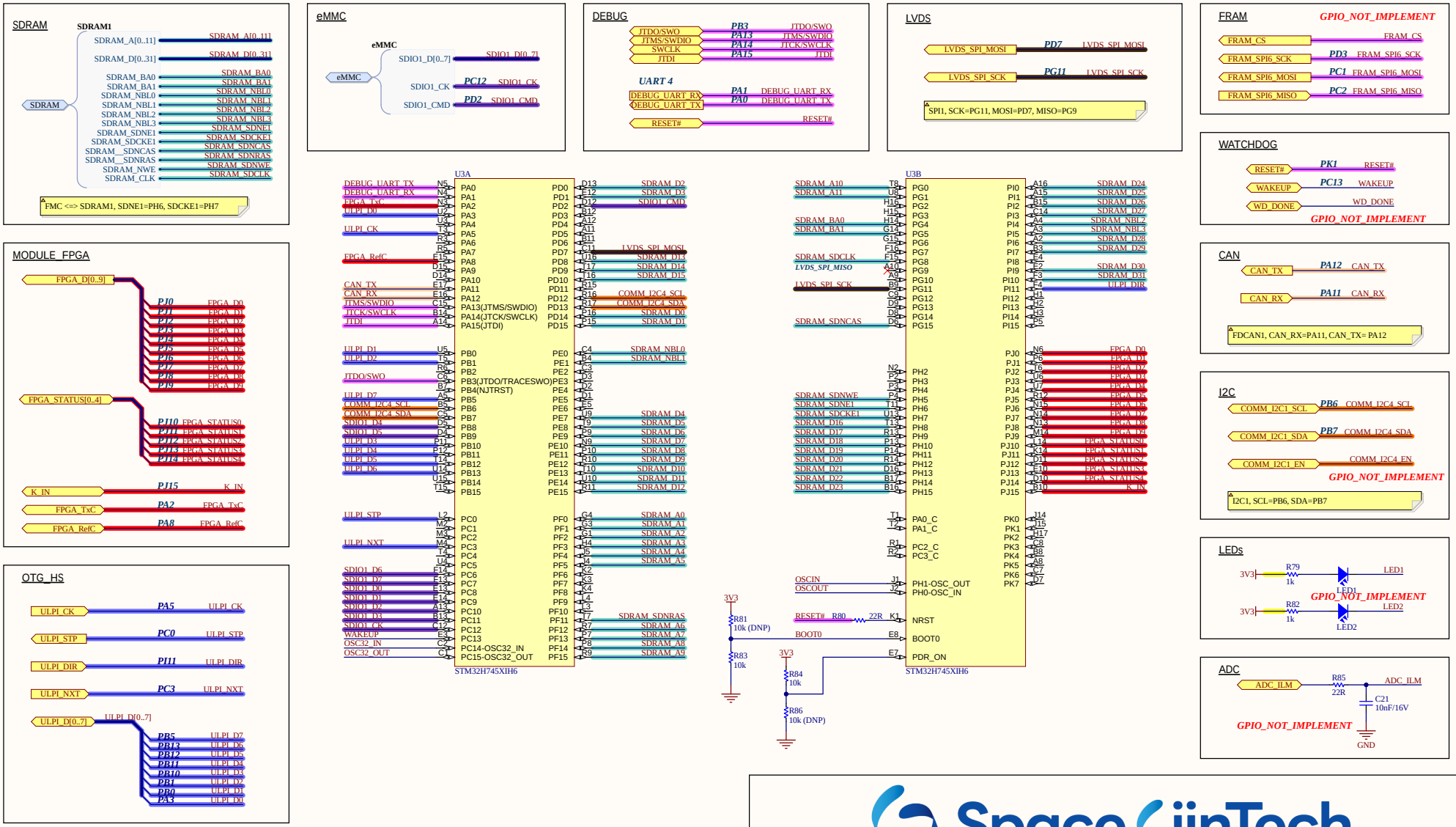
HEADER 5X2 EXPAND FOR DEBUG



Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: DEBUG.SchDoc	Sheet 14 of 16
Checked by: BAO BUI Q.	Document No: 14	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025



Project: BEE-PC1	Sub-system: NANORACK_EXP_CONTROLLER	
Design by: SANG HUYNH	Sheet title: MCU_POWER.SchDoc	Sheet 15 of 16
Checked by: BAO BUI Q.	Document No: 15	Size: A3
Approved by: VU PHAM	Revision: V1.2.2	Date: 8/27/2025


SDRAM
SDRAM1
SDRAM_A[0..11]
SDRAM_D[0..31]
SDRAM_BA0
SDRAM_BA1
SDRAM_NBL0
SDRAM_NBL1
SDRAM_NBL2
SDRAM_NBL3
SDRAM_SDNE1
SDRAM_SDCKE1
SDRAM__SDNCAS
SDRAM__SDNRAS
SDRAM_NWE
SDRAM_CLK
FMC <=> SDRAM1, SDNE1=PH6, SDCKE1=PH7
eMMC
SDIO1_D[0..7]
SDIO1_CK
SDIO1_CMD
PC12
PD2
DEBUG
JTDO/SWO
JTMS/SWDIO
SWCLK
JTDI
PB3
PA13
PA14
PA15
UART 4
DEBUG_UART_RX
DEBUG_UART_TX
PA1
PA0
RESET#
LVDS
LVDS_SPI_MOSI
LVDS_SPI_SCK
PD7
PG11
SPI1, SCK=PG11, MOSI=PD7, MISO=PG9
FRAM
GPIO_NOT_IMPLEMENT
FRAM_CS
FRAM_SPI6_SCK
FRAM_SPI6_MOSI
FRAM_SPI6_MISO
PD3
PC1
PC2
WATCHDOG
WAKEUP
WD_DONE
PK1
PC13
CAN
CAN_TX
CAN_RX
PA12
PA11
FDCAN1, CAN_RX=PA11, CAN_TX= PA12
I2C
COMM_I2C1_SCL
COMM_I2C1_SDA
COMM_I2C1_EN
PB6
PB7
I2C1, SCL=PB6, SDA=PB7
MODULE_FPGA
FPGA_D[0..9]
FPGA_STATUS[0..4]
K_IN
FPGA_TxC
FPGA_RefC
PA2
PA8
PJ15
LEDs
3V3
R79
1k
LED1
R82
LED2
OTG_HS
ULPI_CK
ULPI_STP
ULPI_DIR
ULPI_NXT
ULPI_D[0..7]
PA5
PC0
PI11
PC3
PB5
PB13
PB12
PB11
PB10
PB1
PB0
PA3
ADC
ADC_ILM
R85
22R
C21
10nF/16V
GND
U3A
U3B
STM32H745XIH6
OSC_32M
OSC32_IN
OSC32_OUT
X2
MU00525-32.768K
C25
1.5pF/50V
C26
1.5pF/50V
OSC_25M
OSCIN
OSCOUT
X1
C22
12pF/10V
C23
12pF/10V
BT_NRST
BT1
R87
10k
C24
0.1uF/16V
Project: BEE-PC1
Sub-system: NANORACK_EXP_CONTROLLER
Design by: SANG HUYNH
Sheet title: MCU.SchDoc
Sheet 16 of 16
Checked by: BAO BUI Q.
Document No: 16
Size: A3
Approved by: VU PHAM
Revision: V1.2.2
Date: 8/27/2025