VIET NAM NATIONAL UNIVERSITY HO CHI MINH CITY - UNIVERSITY OF TECHNOLOGY

FACULTY OF ELECTRICAL

AND ELECTRONICS ENGINEERING

ELECTRONIC CIRCUITS

PROJECT OF AMPLIFIER CIRCUIT

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# Chapter 1 – Technical Requirements

## 1.1. Technical Specifications

### 1.1.1 Input Specifications

Because this is an audio amplifier, the audio source level can vary significantly across devices. Therefore, explicitly defining input specifications is critical to determine the required output power.

|  |  |
| --- | --- |
| Parameter | Value |
|  | 15 V |
| (max) | 500 mV |
|  | → > 10 kΩ |
|  | 20 Hz – 20 kHz |

Table 2.1: Input specifications

### 1.1.2. Output Specifications

The output load is a loudspeaker that must be driven by the amplifier. Output specifications are defined as follows:

|  |  |
| --- | --- |
| Parameter | Value |
|  | 4 Ω |
| (max) | 2 W |
|  | → <1kΩ |
|  | 20 Hz – 20 kHz |

Table 2.2: Output specifications

### 1.1.3. Input–Output Relationship

After identifying the required specifications, the input–output relationship is determined.

To amplify the power up to 2 W, the group uses:

= (Eq. 2.1)

From calculation (including possible transmission losses), the circuit voltage gain is estimated to be approximately 25, so the summarized targets are:

|  |  |
| --- | --- |
| Parameter | Value |
|  | 25 |
| Q-point | Located at the middle of the load line |

Table 2.3: Input–output relationship

## 1.2 Block Diagram

To build a complete circuit that satisfies input and output requirements, the design is divided into three main blocks.

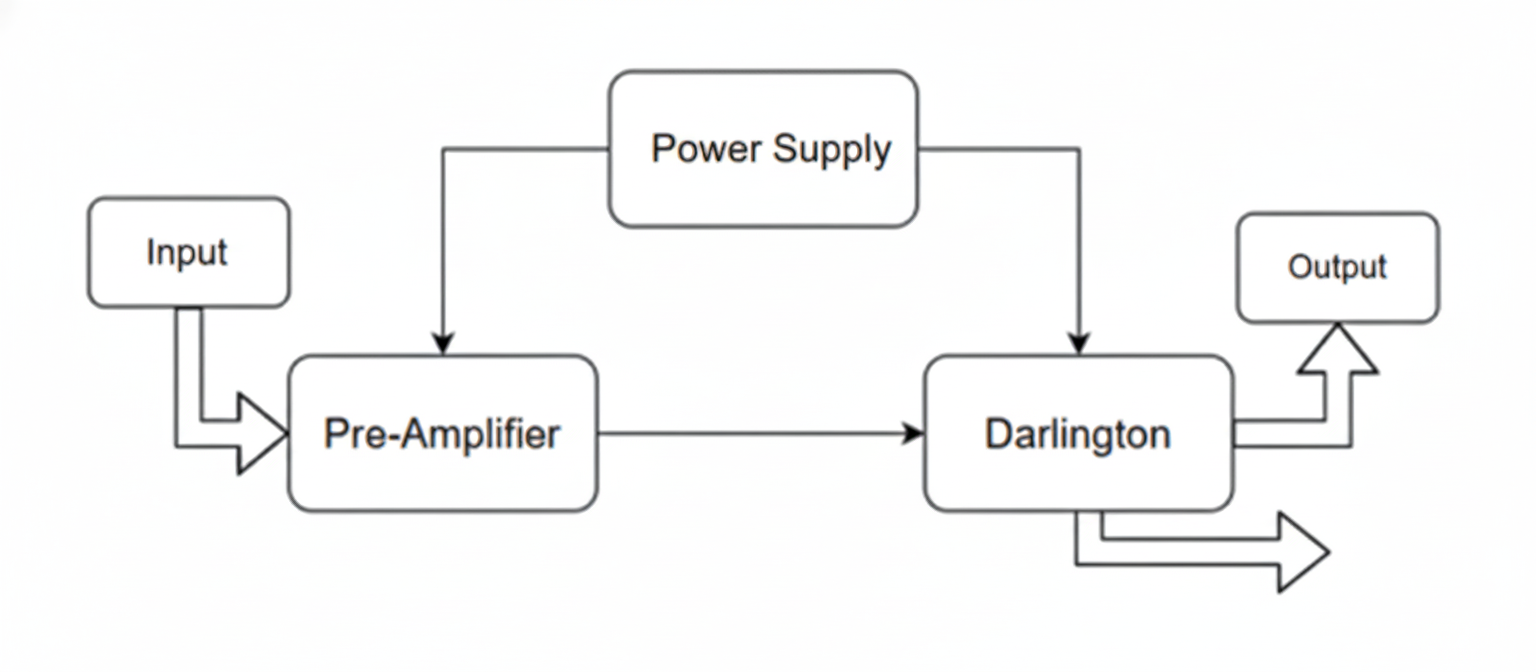
Functions of each block:

Power supply block: provides a stable DC supply for the remaining blocks.

Pre-amplifier block: provides voltage gain according to the requirements when the load is not connected.

Darlington block: maintains voltage gain when the load is connected, ensuring the gain is preserved.

Note: The original report includes a block diagram figure; this translation preserves the described functions.



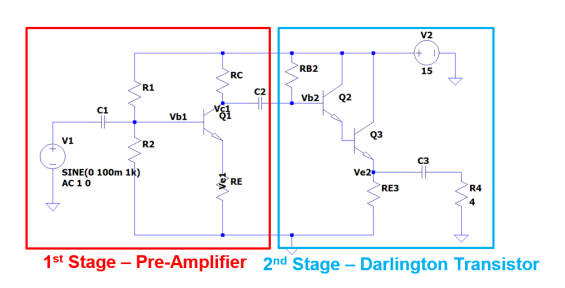
# Chapter 2 – Block Design

## 2.1 Overall Circuit Diagram

To perform component calculations, the group constructs the overall circuit

Unknowns to be determined: , , , , , , , , , , , .

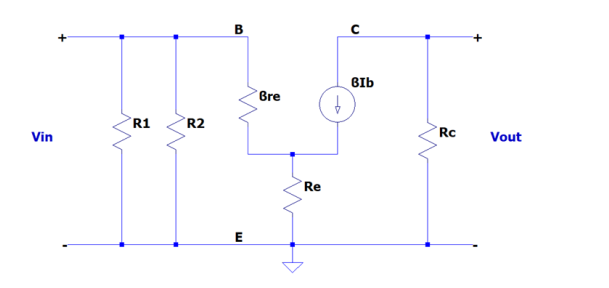
For calculation, the circuit is separated into two main blocks and analyzed as follows.



## 2.2 Pre-Amplifier

The first stage is a common-emitter amplifier with voltage-divider bias. In the small-signal model:

### 2.2.1 Small-Signal Analysis

 = (Eq. 4.1)

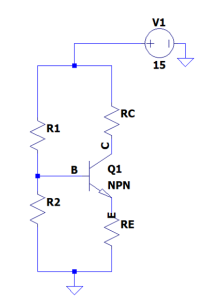
Design target: || = 25.

Assume >> , then:

= 25 (Eq. 4.2)

Select commercial resistor values: = 12 kΩ, = 470 Ω.

### 2.2.2 Large-Signal Analysis



Applying KVL to the CE loop yields the DC load-line equation:

= (Eq. 4.3)

To place the Q-point at the middle of the load line, require:

= · = · (Eq. 4.4)

= · = · (Eq. 4.5)

Substituting values gives: = 0.6 mA (Eq. 4.6)

### 2.2.3 BJT Selection

To compute R1 and R2, the group selects a BJT after obtaining , preferring a device with higher current gain (β).

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | 2N2222 | 2N5551 | 2N5401 |
|  | 30 V | 160 V | 150 V |
|  | 600 mA | 300 mA | 600 mA |
| β Range | 100–300 | 80–250 | 60–240 |
| β (25°C) | 160 | 122 | 72 |

Table 4.1: BJT comparison

Based on the –β relationship (as surveyed by the group), 2N2222 provides the most favorable β, so it is selected.

### 2.2.4 Calculation of R1 and R2

With >> , the input impedance is approximated as:

= // // β· (Eq. 4.7)

Input requirement: ≥ 10 kΩ. Therefore:

≥ 10.6 kΩ (Eq. 4.8)

From large-signal analysis:

= ·= 0.6 mA · 470 Ω = 0.282 V (Eq. 4.9)

= + = 0.282 + 0.7 = 0.982 V (Eq. 4.10)

= · (Eq. 4.11)

Thus: = = (Eq. 4.12)

Combining Eqs. (4.8) and (4.12), choose commercial values:

= 200 kΩ, = 15 kΩ (Eq. 4.13)

## 2.3 Darlington Stage

### 2.3.1 BJT Selection

The group selects:

• : 2N2222A, = 160 (same as ).

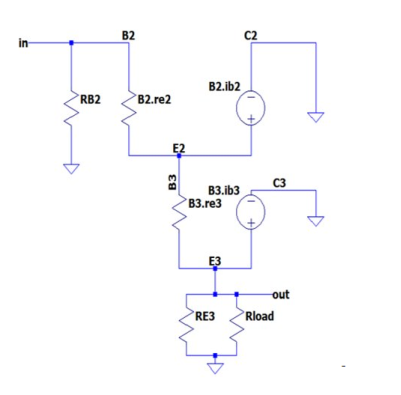
• : 2SD882, = 200, for the following reasons:

DC current gain is less dependent on collector current.

Higher absolute maximum ratings (to handle power dissipation on ).

Less dependent on temperature.

### 2.3.2 Small-Signal Analysis



From the small-signal model, the stage gains are:

= (Eq. 4.14)

= (Eq. 4.15)

### 2.3.3 Large-Signal Analysis



Applying KVL to the BE loop:

= (Eq. 4.16)

Applying KVL to the loop:

= (Eq. 4.17)

Solving yields: = 26026.67 (Eq. 4.19)

With = = 0.00347· and = = 0.694·, then:

= (Eq. 4.20)

To make Av2 ≈ 1, choose a small power resistor: RE3 = 10 Ω, then RB2 = 330 kΩ.

## 2.4 Frequency Response

Computed impedances:

• = // // β· = 11.77 kΩ

• = = 12 kΩ

• = // ·( // ) = 34.12 kΩ

• = + = 0.0689 kΩ

For a low cutoff frequency fL ≤ 20 Hz, required coupling capacitors are:

C1 ≥ 1 / [2π·20 Hz·] = 0.68 µF

C2 ≥ 1 / [2π·20 Hz·(+ )] = 0.173 µF

C3 ≥ 1 / [2π·20 Hz·(+ )] = 1955 µF

Selected values: C1 = 1 µF, C2 = 1 µF, C3 = 2.2 mF.

## 2.5 Overall Voltage Gain

When combining both blocks, the effective gains become:

Av1(with Zin2) = − (RC // Zin2) / (Eq. 4.21)

Av2(with Zout1) = β3·( // RLoad) / [β3·(RE3 // RLoad) + β3·re3 + re2] (Eq. 4.22)

Overall gain: Avoverall = Av1(with Zin2) · Av2(with Zout1) (Eq. 4.23)

Result: Avoverall = 18.49.

The change in overall gain is attributed to the interaction between output and input impedances between stages.

# Chapter 3 – Circuit Implementation

## 3.1. LTSpice Simulation

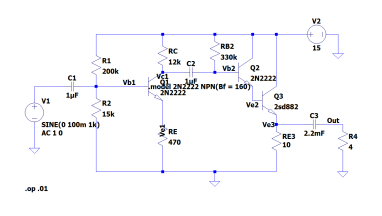
### 3.1.1 Simulation Circuit

The circuit is simulated in LTSpice using the following component parameters:

|  |  |
| --- | --- |
| Parameter / Component | Value |
| 2N2222 | β = 160 |
| 2SD882 | β = 200 |
| VCC | 15 V |
|  | 200 kΩ |
|  | 15 kΩ |
|  | 470 Ω |
|  | 12 kΩ |
|  | 330 kΩ |
|  | 10 Ω |
| C1 | 1 µF |
| C2 | 1 µF |

C3 = 2.2 mF

Table 5.1: Component parameters



LTSpice schematic figure (Figure 5.1).

### 3.1.2 Operating Point (Q Point)

To test the Qpoint operating point, the team performed DC simulations for the circuit and obtained the following results:

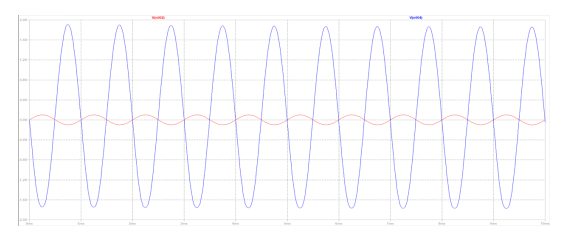
|  |  |
| --- | --- |
| V(n002): 0  V(vb1): 1.00146  V(n001): 15  V(ve1): 0.244313  V(vc1): 8.80096  V(ve3): 6.33925  V(out): 5.57854e-1  V(vb2): 7.8812  V(ve2): 7.07493  Ic(Q1): 0.00051658  Ib(Q1): 3.22866e-06  Ie(Q1): -0.000519816  Ic(Q2): 0.00345154  Ib(Q2): 2.15721e-05  Ie(Q2): -0.00347311  Ic(Q3): 0.630452  Ib(Q3): 0.00347311  Ie(Q3): -0.633925  I(C1): 1.00146e-18  I(C2): -9.19758e-19  I(C3): -1.39464e-14  I(): 6.99927e-05  I(): 6.6764e-05  I(): 0.000519816  I(): 0.000516587  I(): 0.633925  I(R4): 1.39464e-14  I(Rb2): 2.15721e-05  I(V1): 1.00146e-18  I(V2): -0.634512 | voltage voltage voltage voltage voltage voltage voltage voltage voltage devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent devicecurrent |

Based on several parameters, we can compare them with the following calculations.

|  |  |  |
| --- | --- | --- |
| parameter | calculate | Simulate |
| *VCEQ*1  *ICQ*1  *VCEQ*2  *ICQ*2  *VCEQ*3  *ICQ*3 | 7.5V  0.6mA  7.5V  3.75mA  7.5V  0.75V | 8.6V 0.51mA 7.93V 3.45mA 8.67V 0.63V |

### 3.1.3 Output Signal Analysis

To test the output signal, the team performed AC simulations for the circuit and obtained the following results:



Based on the graph above:

• The input signal is represented by the red line.

• The output signal is represented by the blue line.

Observation: The input signal is amplified in opposite phase, with each cycle relative to the output signal.

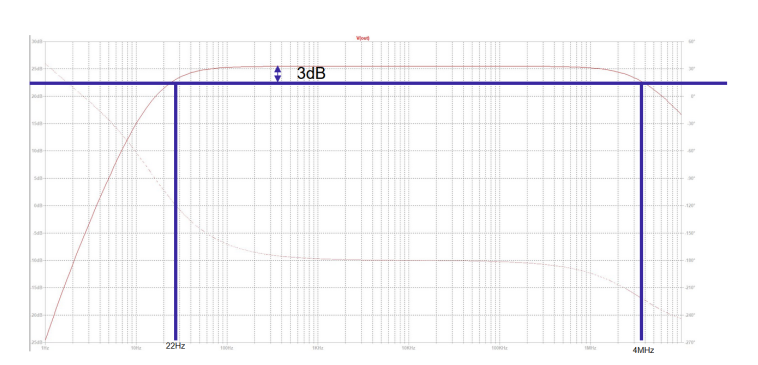
Calculating the gain based on the simulation graph:

• Maximum output signal value: 1.84V.

• Maximum input value: 0.1V

• Gain: *|Av|* = *|- Vout / V in |* = *|-* 1.84 / 0.1 *|* = 18*.*4

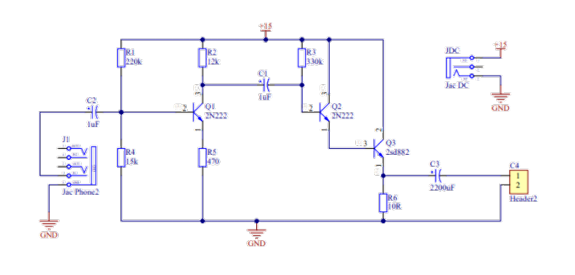
### 3.1.4 Bode Plot



Using the Bode plot, the operating frequency range of the circuit is determined to be between 22Hz and 4MHz. While this differs from the initial requirement, it can be seen that the circuit is still within the audible range with a maximum value of 25dB. The Av value can be calculated as follows:

20*log*(*Av*) = 25*dB → Av ≈* 17*.*78

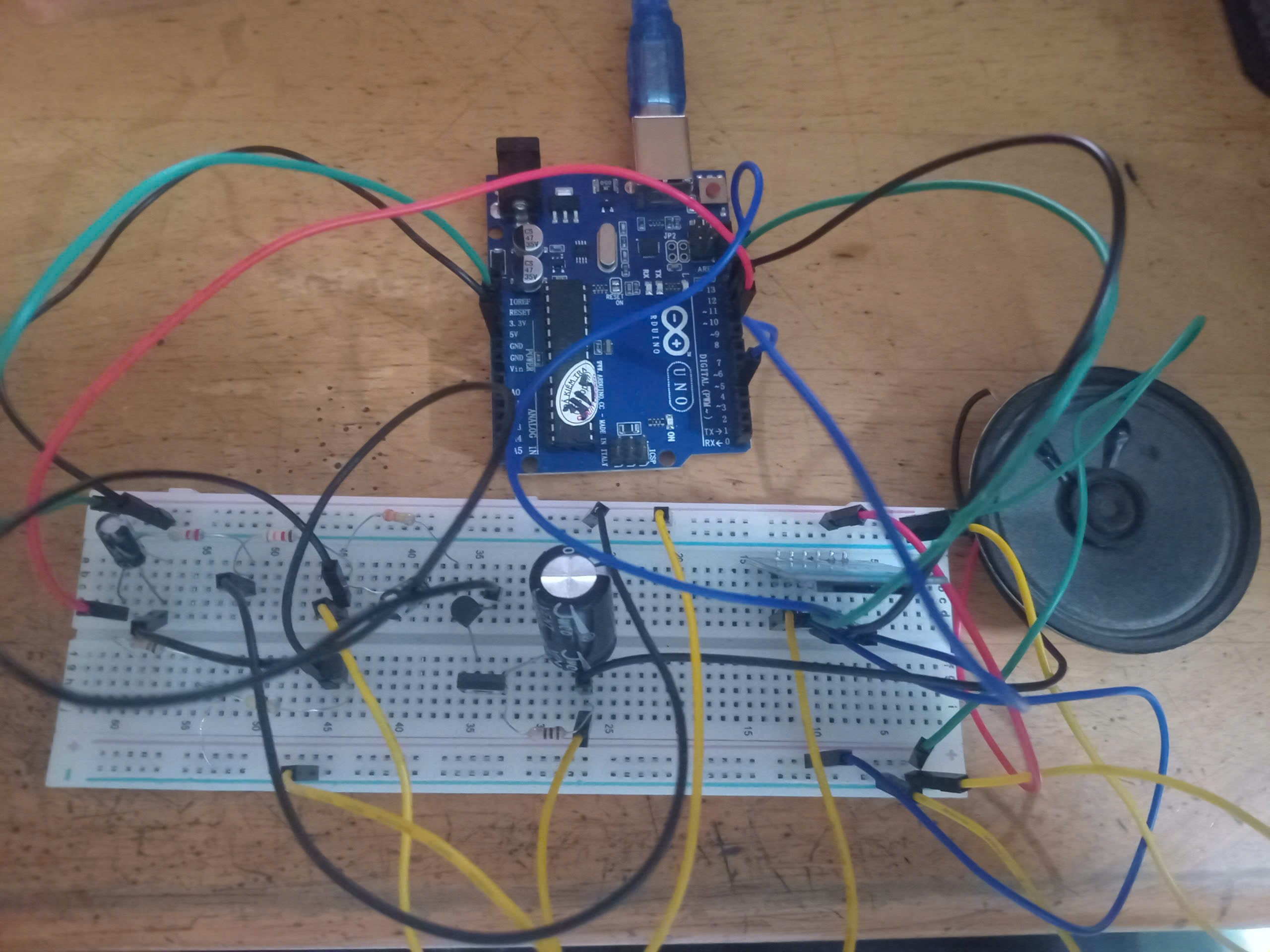
## 3.2 Hardware Design in Altium and Breadboard Implementation

The audio amplifier circuit was first redrawn and verified in Altium Designer based on the calculated component values. The schematic was used as the reference for wiring and component placement during the hardware implementation. 

In the hardware setup, the J1 (audio input) and JDC (DC input) connectors were not implemented as physical jack connectors. Instead, the circuit was wired directly on a breadboard according to the Altium schematic. The input signal is provided by the Arduino system (reading audio data from a microSD card module), and the DC supply is connected through the breadboard power rails with a shared ground between the Arduino and the amplifier.

# 

## 3.3 Hardware Construction with arduino and input signal from microSD card module

The audio amplifier circuit using Arduino and a microSD card module is designed to play back digital audio signals stored on the memory card. In this system, the Arduino acts as the main controller, communicating with the microSD module via the SPI interface to read audio data. The digital audio signal is then processed and converted into an analog signal using the Arduino’s output stage, which is subsequently fed into an audio power amplifier. The amplifier increases the signal amplitude to a level sufficient to drive a loudspeaker. This system is suitable for applications such as audio playback, announcement systems, and embedded sound devices.

# 4. Conclusion:

This report defined the technical specifications for an audio amplifier circuit, including , an input signal amplitude up to , input impedance , a loudspeaker load, a target output power of , and an operating audio band of 20 Hz–20 kHz.

The initial target voltage gain was estimated at approximately 25.

In the design and simulation results, the overall voltage gain after cascading stages reached ; the report attributes this reduction to loading effects caused by the interaction between stage output and input impedances.

The output waveform analysis from simulation also indicates based on the amplitude ratio .

From the Bode plot, the obtained operating range is approximately 22 Hz to 4 MHz; the report notes that the lower cutoff (22 Hz) slightly deviates from the 20 Hz requirement but remains within the audible region.

For hardware implementation, the circuit was recreated and verified in Altium Designer as the basis for wiring, and then assembled on a breadboard. The input connector (J1) and DC connector (JDC) were not implemented as physical jacks; instead, an Arduino with a microSD module was used to provide the input signal, and power was supplied via the breadboard power rails with a common ground between the Arduino and the amplifier circuit.