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Your task is to find the maximal delay of this design – i.e. determine the delays of $S_{0\text{-}31}$ and C_{32} – the maximal delay of these outputs will be the maximal delay of the design. Fill in the values in the table on the following page to receive full credit (and to help with possible partial credit).

Output	Delay	
G0	2T	*(2 points)*
P0	2T	*(2 points)*
Gα	12T	*(2 points)*
Pα	7T	*(2 points)*
C12	10T	*(2 points)*
C15	30T	*(2 points)*
C16	24T	*(2 points)*
S15	32T	*(2 points)*
C20	16T	*(2 points)*
S19	14T	*(2 points)*
C24	30T	*(2 points)*
C31	54T	*(2 points)*
C32 (after mux)	62T	*(2 points)*
S31 (after mux)	60T	*(2 points)*

Find the maximum delay **in terms of T** of the 32-bit adder – take the maximum of all output bits – including the sum bits (S_0-S_{31}) and the final carry out (C_{32}). Show your work clearly in the table above. The two figures on the following pages are taken from the class notes, if you need to refer to them.

Maximal Delay: 62T. *(2 points)*

C_{24} =

S_{31}