TEXAS INSTRUMENTS

TPA3116D2, TPA3118D2, TPA3130D2

具有 AM 抑制功能的 TPA3116D2 15W、30W、50W 无滤波器 D 类立体声放大器系列

1 特性

- 支持多个输出配置
  - 21V 电压、4Ω BTL 负载条件下的功率为 2 × 50W (TPA3116D2)
  - 24V 电压、8Ω BTL 负载条件下的功率为 2 × 30W (TPA3118D2)
  - 15V 电压、8Ω BTL 负载条件下的功率为 2 × 15W (TPA3130D2)
- 宽电压范围：4.5V 至 26V
- 高效 D 类运行
  - 大于 90% 的电源效率加之较低空闲损耗，大幅减小了散热器尺寸
  - 高级调制方案
- 多重开关频率
  - AM 抑制
  - 主从同步
  - 高达 1.2MHz 的开关频率
- 采用具有高 PSRR 的反馈功率级架构，降低了 PSU 要求
- 可编程功率限制
- 差分和单端输入
- 立体声模式和单声道模式（采用单滤波器单声道配置）
- 采用单电源供电，减少了组件数量
- 集成式自保护电路，包括过压、欠压、过热、直流检测和短路等保护，并且具有错误报告功能
- 热增强型封装
  - DAD（32 引脚 HTSSOP 封装，焊盘朝上）
  - DAP（32 引脚 HTSSOP 封装，焊盘朝下）
- -40°C 至 85°C 环境温度范围

2 应用

- 小型-微型组件、条形音箱、扩展坞
- 汽车零件市场
- CRT TV
- 消费类音频 应用

3 说明

TPA31xxD2 系列是高效的立体声数字放大器功率级，用于在单声道模式下驱动高达 100W/2Ω 的扬声器。TPA3130D2 的效率非常高，可在单层 PCB 上提供 2 × 15W 的功率，且无需外部散热器。TPA3118D2 甚至可以在不使用外部散热器的情况下在双层 PCB 上提供 2 × 30W/8Ω 的功率。如果需要更高的功率，可以选用 TPA3116D2，这款器件在其顶层 PowerPAD 上连接一个小型散热器后可提供 2 × 50W/4Ω 的功率。这三款器件的大小相同，这样一来，使用单个 PCB 即可满足不同功率级的需求。

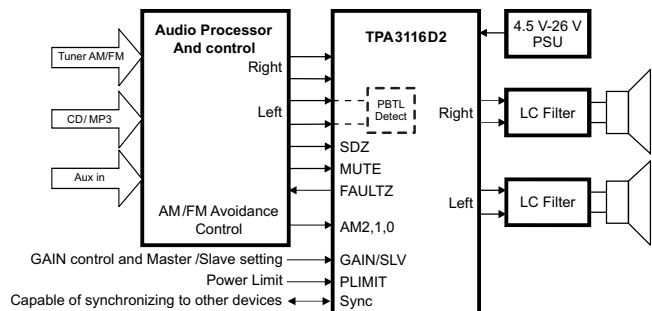TPA31xxD2 高级振荡器/PLL 电路采用了一个多开关频率选项来抑制 AM 干扰；搭配选择使用主从选项时，还可使多个器件实现同步。

TPA31xxD2 器件具有短路保护和热保护以及过压、欠压和直流保护，可全面防止出现故障。在过载情况下，器件会将故障情况反馈给处理器，从而避免自身遭到损坏。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPA3116D2 中的器件型号 TPA3116D2 的封装 DAP (32)	DAD (32)	11.00mm x 6.20mm
TPA3118D2 TPA3130D2	DAP (32)	11.00mm x 6.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用电路

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4 修订历史记录

Changes from Revision F (February 2017) to Revision G   **Page**

- Changed R to GND column row 1 From: "Short" To: "Open" in 表 3 16
- Changed R to GVDD column row 1 From: "Open" To: "Short" in 表 3 16
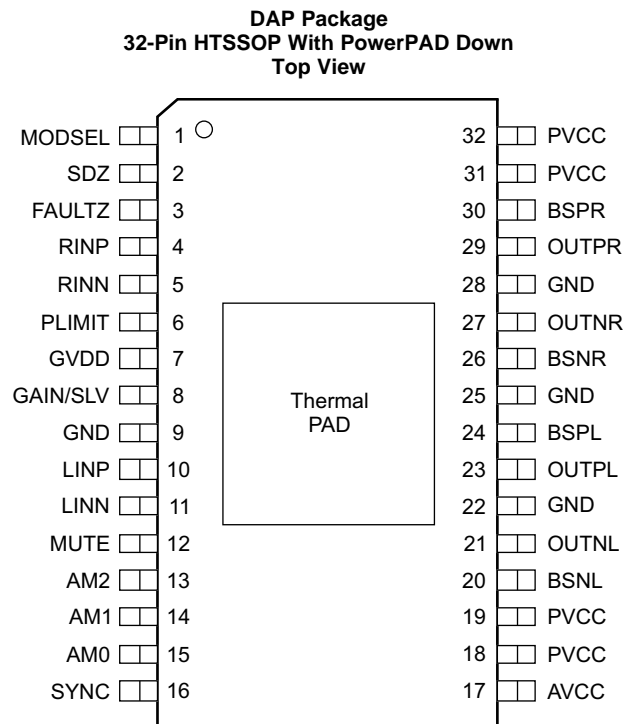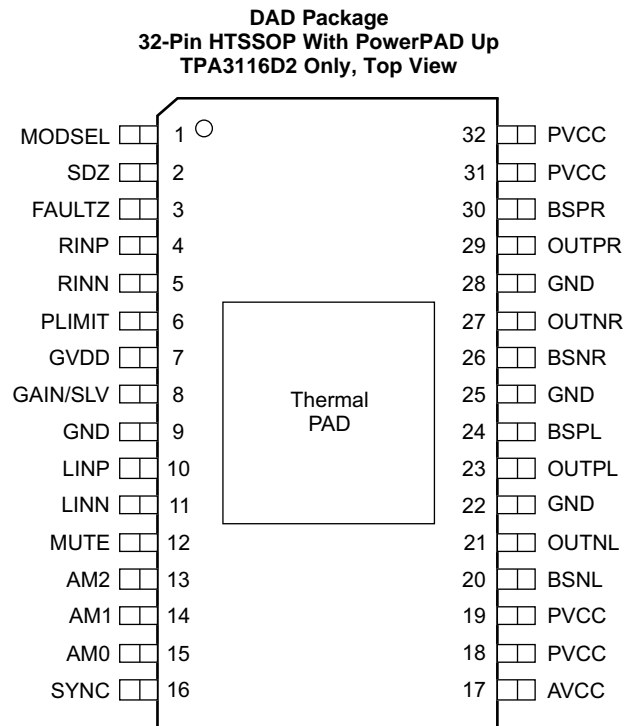
Changes from Revision E (September 2015) to Revision F   **Page**

- Changed pin 20 Description From: ceramic cap to OUTPL To: ceramic cap to OUTNL in the *Pin Functions* table 4
- Changed pin 24 Description From: ceramic cap to OUTNL To: ceramic cap to OUTPL in the *Pin Functions* table 4
- Changed 2.3 Hz To 1.9 Hz for HIGH-PASS FILTER in 表 2 14

Changes from Revision D (January 2015) to Revision E   **Page**

- 删除了器件信息 表 1

Changes from Revision C (April 2012) to Revision D   **Page**

- 已添加 引脚配置和功能 部分、*ESD* 额定值 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 1

Changes from Revision B (May 2012) to Revision C   **Page**

- Changed Notes 2 and 3 of the *Thermal Information Table*. 6
- Changed the Gain (BTL) Test Condition values for R1 and R2 6
- Changed the Gain (SLV) Test Condition values for R1 and R2 6
- Changed the *System Block Diagram* 13

5 Pin Configuration and Functions

DAD Package
32-Pin HTSSOP With PowerPAD Up
TPA3116D2 Only, Top View

Pin	Left Signal	Pin	Right Signal
1	MODSEL	32	PVCC
2	SDZ	31	PVCC
3	FAULTZ	30	BSPR
4	RINP	29	OUTPR
5	RINN	28	GND
6	PLIMIT	27	OUTNR
7	GVDD	26	BSNR
8	GAIN/SLV	25	GND
9	GND	24	BSPL
10	LINP	23	OUTPL
11	LINN	22	GND
12	MUTE	21	OUTNL
13	AM2	20	BSNL
14	AM1	19	PVCC
15	AM0	18	PVCC
16	SYNC	17	AVCC

Thermal PAD

DAP Package
32-Pin HTSSOP With PowerPAD Down
Top View

Pin	Left Signal	Pin	Right Signal
1	MODSEL	32	PVCC
2	SDZ	31	PVCC
3	FAULTZ	30	BSPR
4	RINP	29	OUTPR
5	RINN	28	GND
6	PLIMIT	27	OUTNR
7	GVDD	26	BSNR
8	GAIN/SLV	25	GND
9	GND	24	BSPL
10	LINP	23	OUTPL
11	LINN	22	GND
12	MUTE	21	OUTNL
13	AM2	20	BSNL
14	AM1	19	PVCC
15	AM0	18	PVCC
16	SYNC	17	AVCC

Thermal PAD

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Mode selection logic input (LOW = BD mode, HIGH = 1 SPW mode). TTL logic levels with compliance to AVCC.
2	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO	General fault reporting including Over-temp, DC Detect. Open drain. FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	RINP	I	Positive audio input for right channel. Biased at 3 V.
5	RINN	I	Negative audio input for right channel. Biased at 3 V.
6	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers.
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9	GND	G	Ground
10	LINP	I	Positive audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
11	LINN	I	Negative audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
12	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	I	AM Avoidance Frequency Selection
14	AM1	I	AM Avoidance Frequency Selection
15	AM0	I	AM Avoidance Frequency Selection
16	SYNC	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal.
17	AVCC	P	Analog Supply
18	PVCC	P	Power supply
19	PVCC	P	Power supply
20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL
21	OUTNL	PO	Negative left channel output
22	GND	G	Ground
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
25	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR
27	OUTNR	PO	Negative right channel output
28	GND	G	Ground
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR
31	PVCC	P	Power supply
32	PVCC	P	Power supply
33	PowerPAD	G	Connect to GND for best system performance. If not connected to GND, leave floating.

(1) **TYPE**: DO = Digital Output, I = Analog Input, G = General Ground, PO = Power Output, BST = Boot Strap.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	−0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	−0.3	6.3	V
	PLIMIT, GAIN / SLV, SYNC	−0.3	GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	−0.3	PVCC+0.3	V
Slew rate, maximum[2]	AM0, AM1, AM2, MUTE, SDZ, MODSEL		10	V/ms
Operating free-air temperature, T_A		−40	85	°C
Operating junction temperature , T_J		−40	150	°C
Storage temperature, T_{stg}		−40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 100 kΩ series resistor is needed if maximum slew rate is exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}		4.5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL		2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL				0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V				0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)				50	µA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 µH, C = 680 nF	TPA3116D2, TPA3118D2	3.2	4		Ω
			TPA3130D2	5.6	8		
R_L(PBTL)		Output filter: L = 10 µH, C = 1 µF	TPA3116D2, TPA3118D2	1.6			
			TPA3130D2	3.2	4		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition		1			µH

6.4 Thermal Information

THERMAL METRIC[1]		TPA3130D2	TPA3118D2	TPA3116D2	UNIT
		DAP[2]	DAP[3]	DAD[4]	
		32 PINS	32 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	22	14	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	5.9	4.7	5.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For the PCB layout please see the TPA3130D2EVM user guide.
(3) For the PCB layout please see the TPA3118D2EVM user guide.
(4) The heat sink drawing used for the thermal model data are shown in the application section, size: 14mm wide, 50mm long, 25mm high.

6.5 DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB		1.5	15	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, No load or filter, PV_{CC} = 12 V		20	35	mA
		SDZ = 2 V, No load or filter, PV_{CC} = 24 V		32	50	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, No load or filter, PV_{CC} = 12 V		<50		μA
		SDZ = 0.8 V, No load or filter, PV_{CC} = 24 V		50	400	
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C		120		mΩ
G	Gain (BTL)	R1 = 5.6 kΩ, R2 = Open	19	20	21	dB
		R1 = 20 kΩ, R2 = 100 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 47 kΩ, R2 = 75 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 75 kΩ, R2 = 47 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 100 kΩ, R2 = 16 kΩ	35	36	37	
t_{on}	Turn-on time	SDZ = 2 V		10		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V		2		μs
GVDD	Gate drive supply	IGVDD < 200 μA	6.4	6.9	7.4	V
V_O	Output voltage maximum under PLIMIT control	V(PLIMIT) = 2 V; V_I = 1 V_{rms}	6.75	7.90	8.75	V

6.6 AC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV$_{PP}$ ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to GND		–70		dB
P$_O$	Continuous output power	THD+N = 10%, f = 1 kHz, PV$_{CC}$ = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, PV$_{CC}$ = 21 V		50		
THD+N	Total harmonic distortion + noise	V$_{CC}$ = 21 V, f = 1 kHz, P$_O$ = 25 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V$_O$ = 1 V$_{rms}$, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f$_{OSC}$	Oscillator frequency	AM2=0, AM1=0, AM0=0	376	400	424	kHz
		AM2=0, AM1=0, AM0=1	470	500	530	
		AM2=0, AM1=1, AM0=0	564	600	636	
		AM2=0, AM1=1, AM0=1	940	1000	1060	
		AM2=1, AM1=0, AM0=0	1128	1200	1278	
		AM2=1, AM1=0, AM0=1				
		AM2=1, AM1=1, AM0=0		Reserved		
		AM2=1, AM1=1, AM0=1				
	Thermal trip point			150+		°C
	Thermal hysteresis			15		°C
	Over current trip point	TPA3130D2		4.5		A
		TPA3118D2, TPA3116D2		7.5		

6.7 Typical Characteristics

f_s = 400 kHz, BD Mode (unless otherwise noted)
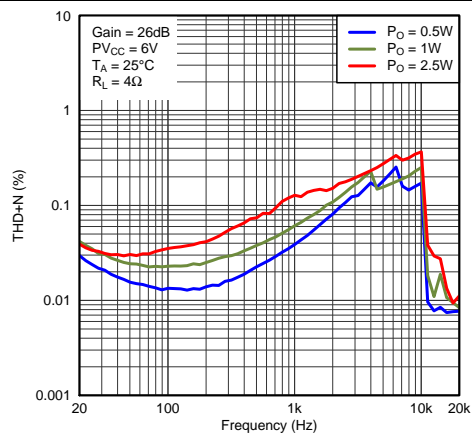
图 1. Total Harmonic Distortion + Noise (BTL) vs Frequency
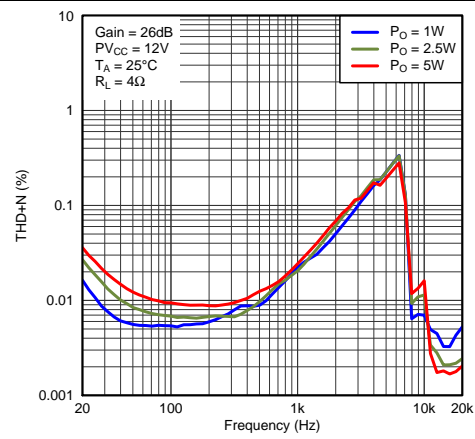
图 2. Total Harmonic Distortion + Noise (BTL) vs Frequency
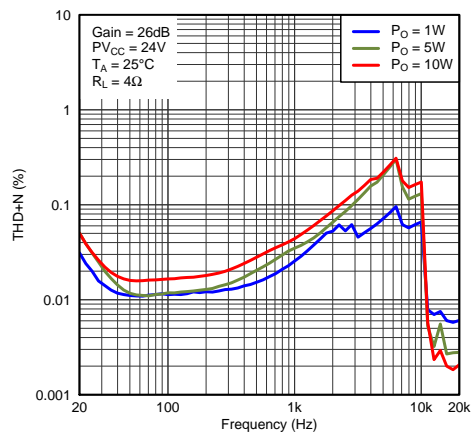
图 3. Total Harmonic Distortion + Noise (BTL) vs Frequency
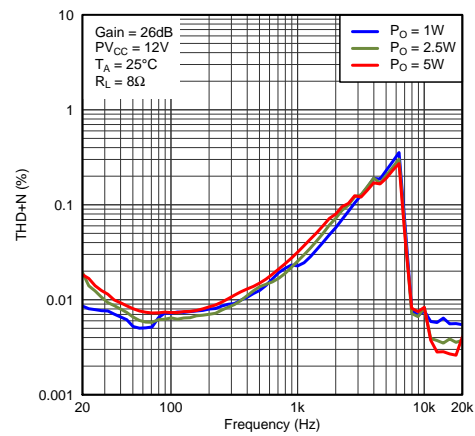
图 4. Total Harmonic Distortion + Noise (BTL) vs Frequency
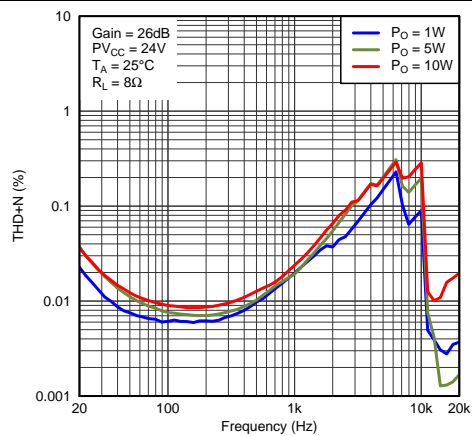
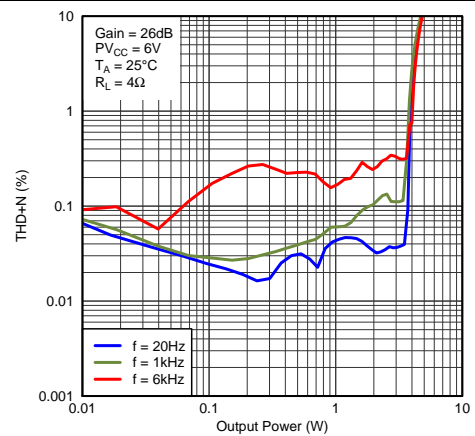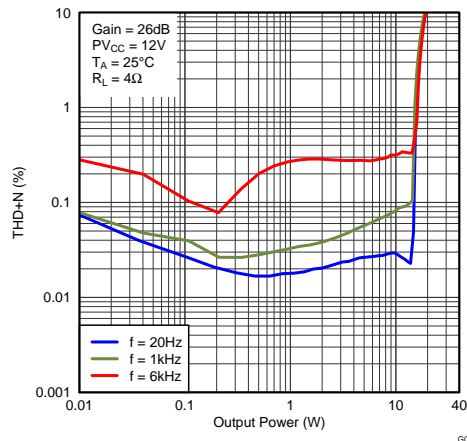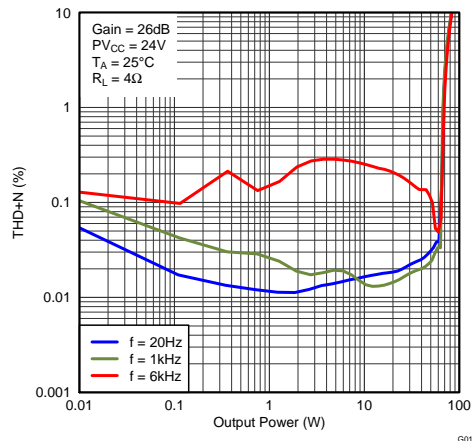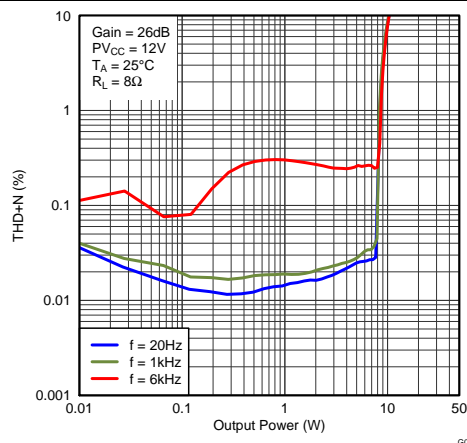图 5. Total Harmonic Distortion + Noise (BTL) vs Frequency

图 6. Total Harmonic Distortion + Noise (BTL) vs Output Power

Typical Characteristics (接下页)

f_s = 400 kHz, BD Mode (unless otherwise noted)

图 7. Total Harmonic Distortion + Noise (BTL) vs Output Power

图 8. Total Harmonic Distortion + Noise (BTL) vs Output Power

图 9. Total Harmonic Distortion + Noise (BTL) vs Output Power
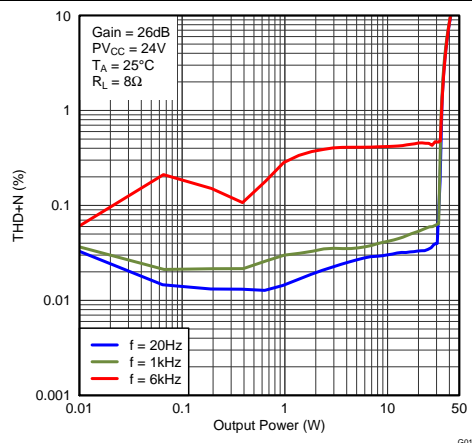
图 10. Total Harmonic Distortion + Noise (BTL) vs Output Power
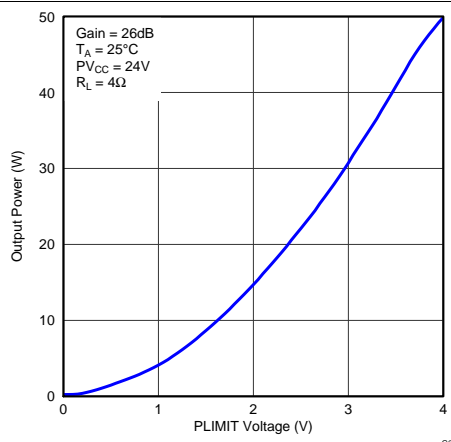
图 11. Output Power (BTL) vs Plimit Voltage
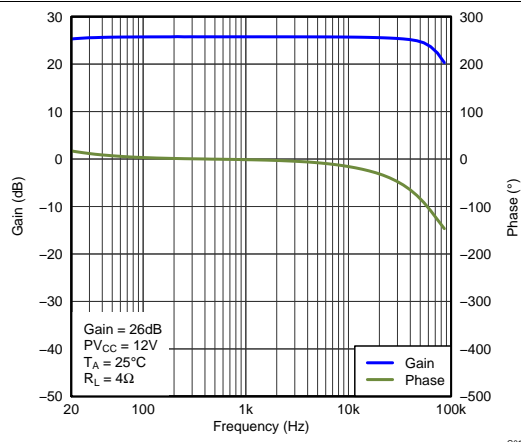
图 12. Gain/Phase (BTL) vs Frequency

TPA3116D2, TPA3118D2, TPA3130D2

ZHCS891G – APRIL 2012 – REVISED DECEMBER 2017

Typical Characteristics (接下页)

f_s = 400 kHz, BD Mode (unless otherwise noted)
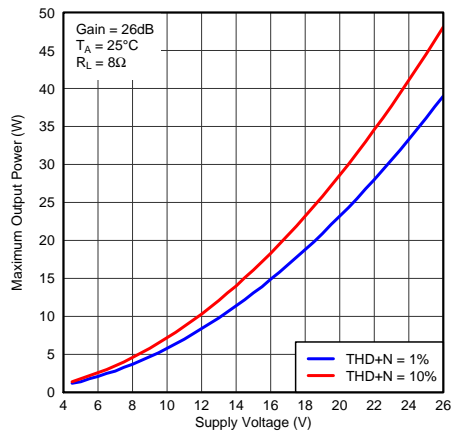
图 13. Maximum Output Power (BTL) vs Supply Voltage
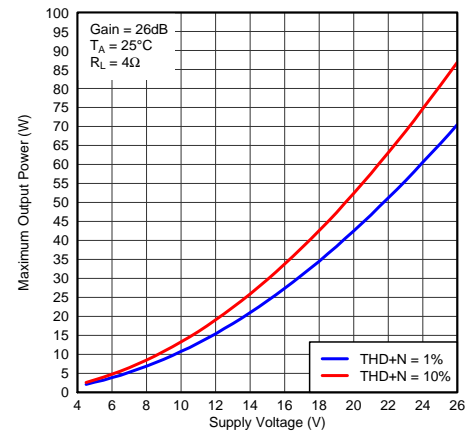
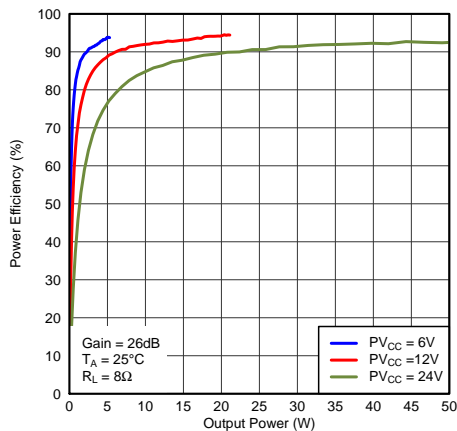图 14. Maximum Output Power (BTL) vs Supply Voltage
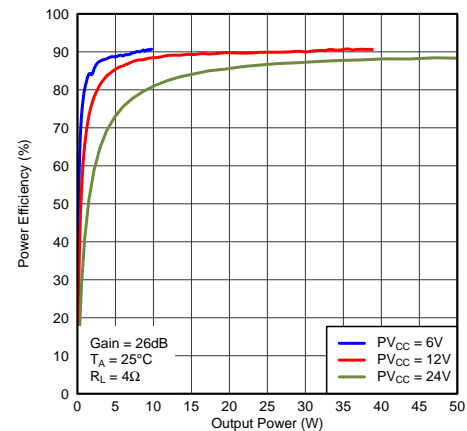

图 15. Power Efficiency (BTL) vs Output Power
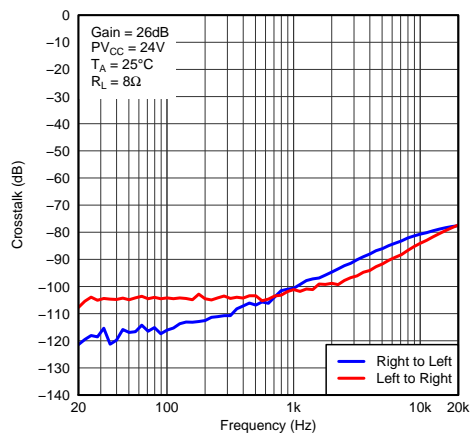

图 16. Power Efficiency (BTL) vs Output Power

图 17. Crosstalk vs Frequency
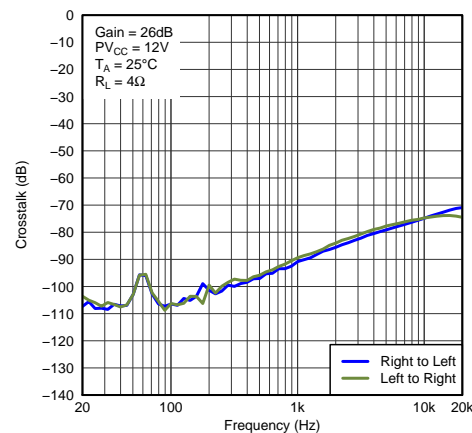

图 18. Crosstalk vs Frequency

Typical Characteristics (接下页)

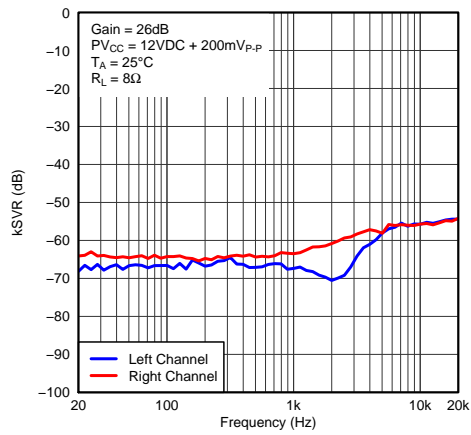f_s = 400 kHz, BD Mode (unless otherwise noted)
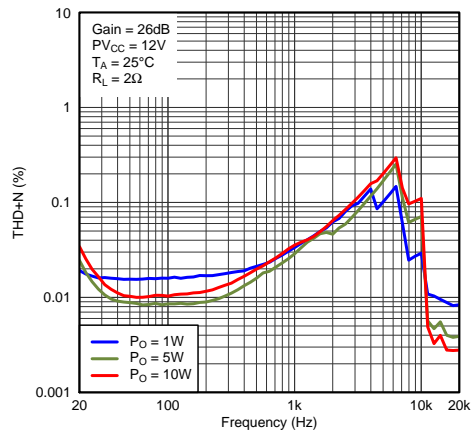
图 19. Supply Ripple Rejection Ratio (BTL) vs Frequency

图 20. Total Harmonic Distortion + Noise (PBTL) vs Frequency

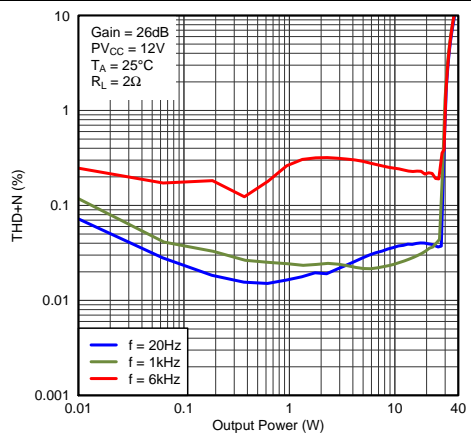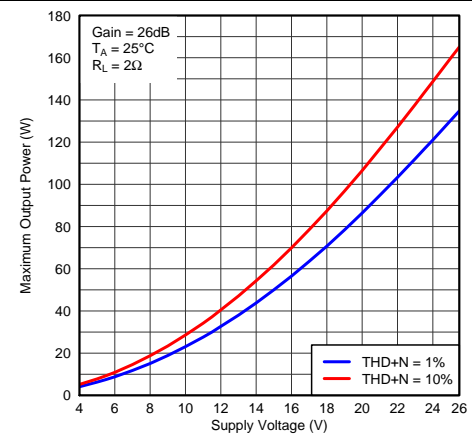图 21. Total Harmonic Distortion + Noise (PBTL) vs Output Power

图 22. Maximum Output Power (PBTL) vs Supply Voltage

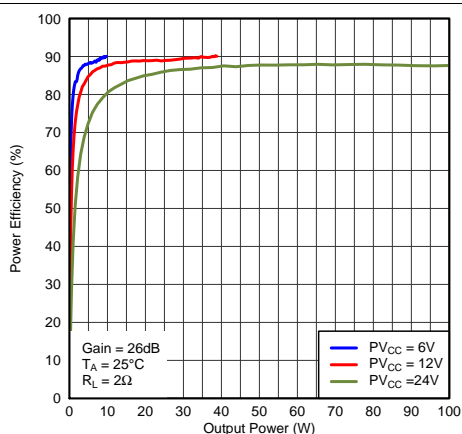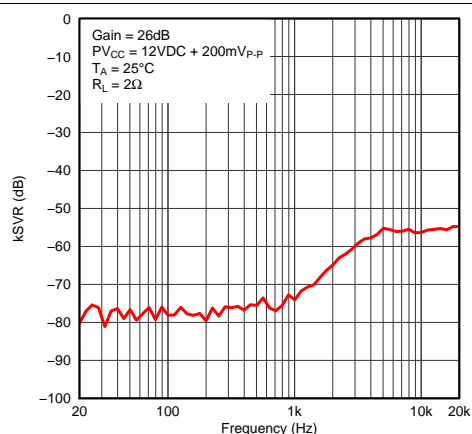图 23. Power Efficiency (PBTL) vs Output Power

图 24. Supply Ripple Rejection Ratio (PBTL) vs Frequency

Typical Characteristics (接下页)

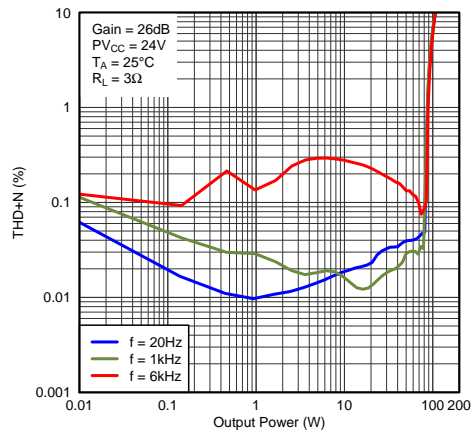f$_s$ = 400 kHz, BD Mode (unless otherwise noted)

图 25. Total Harmonic Distortion + Noise (PBTL) vs Output Power
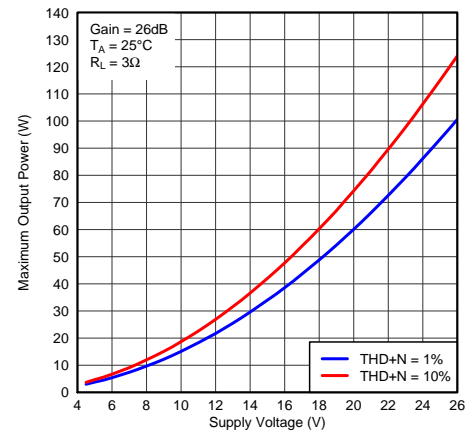
图 26. Maximum Output Power (PBTL) vs Supply Voltage

7 Detailed Description

7.1 Overview

The TPA31xxD2 device is a highly efficient Class D audio amplifier with integrated 120m Ohms MOSFET that allows output currents up to 7.5 A. The high efficiency allows the amplifier to provide an excellent audio performance without the need for a bulky heat sink.

The device can be configured for either master or slave operation by using the SYNC pin. This helps to prevent audible beats noise.

7.2 Functional Block Diagram

Copyright © 2016, Texas Instruments Incorporated
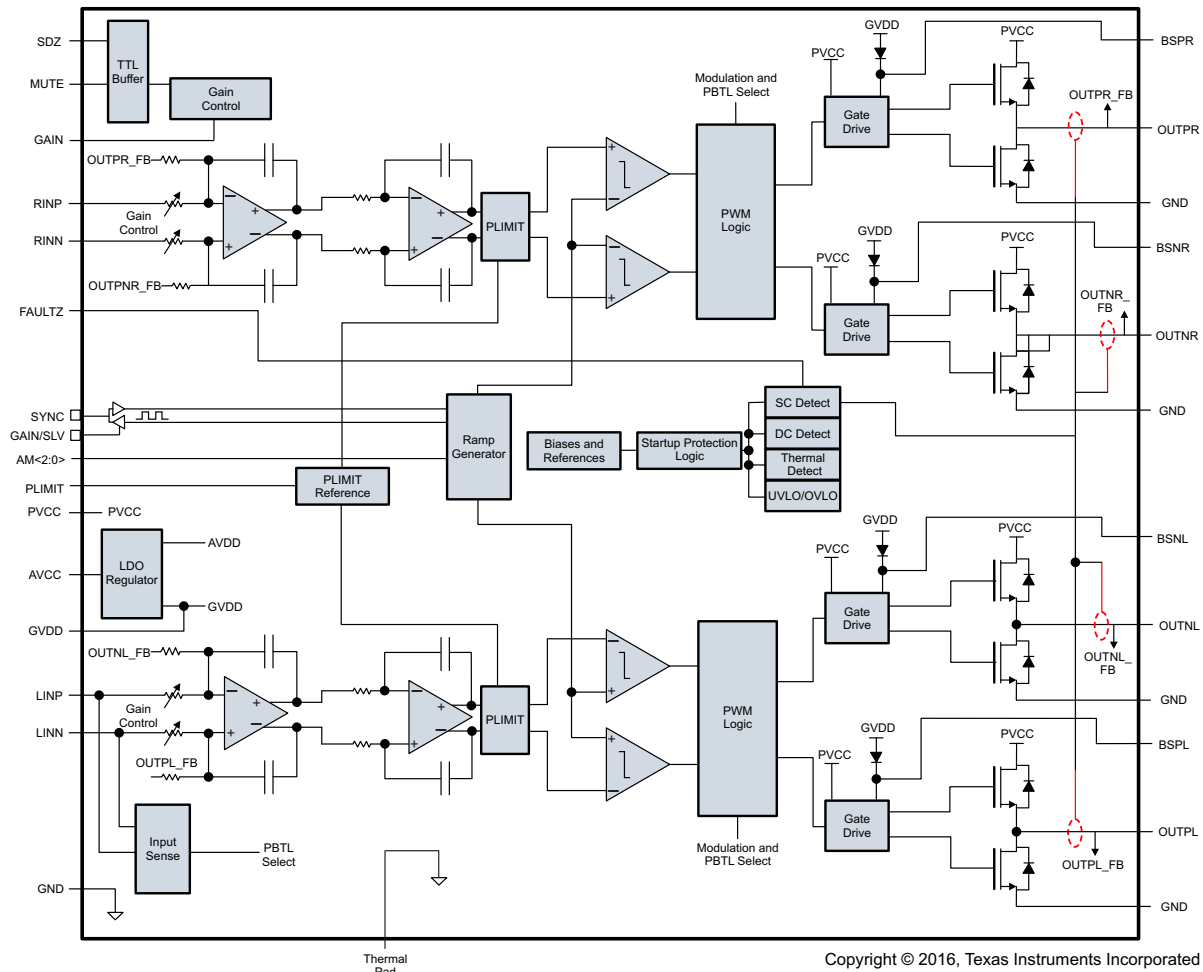
7.3 Feature Description

7.3.1 Gain Setting and Master and Slave

The gain of the TPA31xxD2 family is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. 表 1 lists the recommended resistor values and the state and gain:

Feature Description (接下页)

表 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)[1]	R2 (to GVDD)[1]	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1)   Resistor tolerance should be 5% or better.
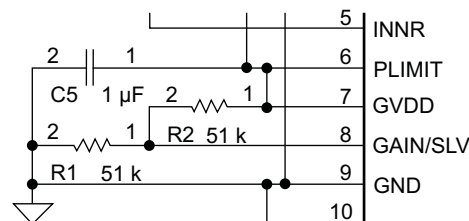
图 27. Gain, Master/Slave

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

7.3.2 Input Impedance

The TPA31xxD2 family input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. 表 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs need to be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

$$f = \frac{1}{2\pi Z_i C_i}$$

(1)

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. 表 2 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1 µF can be used.

表 2. Recommended Input AC-Coupling Capacitors

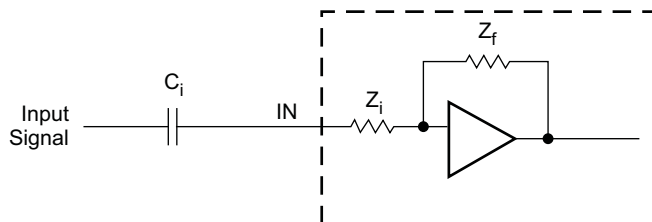| GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	1.9 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

图 28. Input Impedance

The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum or ceramic. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

7.3.3 Startup and Shutdown Operation

The TPA31xxD2 family employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power-up.

7.3.4 PLIMIT Operation

The TPA31xxD2 family has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1 µF capacitor from pin PLIMIT to ground to ensure stability. It is recommended to connect PLIMIT to GVDD when using 1SPW-modulation mode.
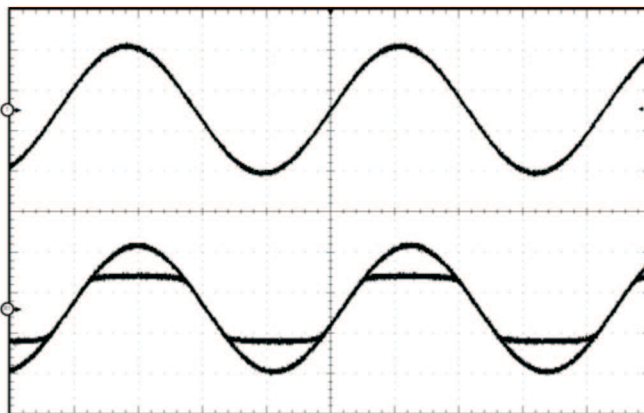
图 29. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is approximately 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10% THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude
- V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P (2)

表 3. Power Limit Example

PV$_{CC}$ (V)	PLIMIT VOLTAGE (V)[1]	R to GND	R to GVDD	OUTPUT VOLTAGE (V$_{rms}$)
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9
12 V	1.5	18 kΩ	68 kΩ	6.3

(1) PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V$_{rms}$.

7.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X5R ceramic 1 µF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

7.3.6 BSPx AND BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220 nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in 图 37.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

7.3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA31xxD2 family with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the TPA31xxD2 family with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 10 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

7.3.8 Device Protection System

The TPA31xxD2 family contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to 表 4:

表 4. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED/SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	$T_j > 150°C$	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

7.3.9 DC Detect Protection

The TPA31xxD2 family has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. Table x below shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

表 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 420 ms to trigger the DC detect.

表 5. DC Detect Threshold

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	0.96
6	1.3
12	2.6
18	3.9

7.3.10 Short-Circuit Protection and Automatic Recovery Feature

The TPA31xxD2 family has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

In systems where a possibility of a permanent short from the output to PVDD or to a high voltage battery like a car battery can occur, pull the MUTE pin low with the FAULTZ signal with a inverting transistor to ensure a high-Z restart, like shown in the figure below:
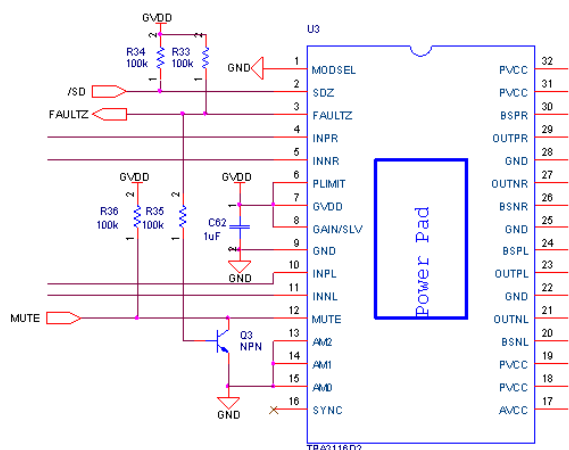
图 30. MUTE Driven by Inverted FAULTZ

图 31. Timing Requirement for SDZ

7.3.11 Thermal Protection

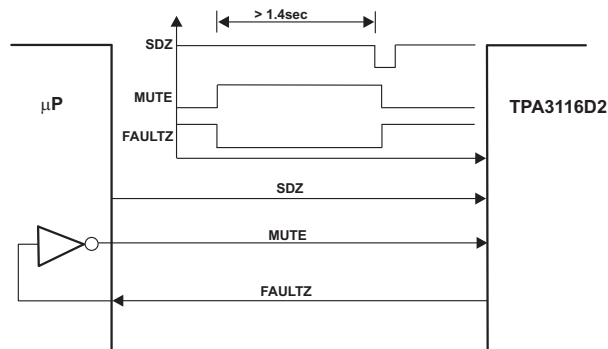Thermal protection on the TPA31xxD2 family prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

7.3.12 Device Modulation Scheme

The TPA31xxD2 family has the option of running in either BD modulation or 1SPW modulation; this is set by the MODSEL pin.

7.3.12.1 MODSEL = GND: BD-Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^{2}R losses in the load.
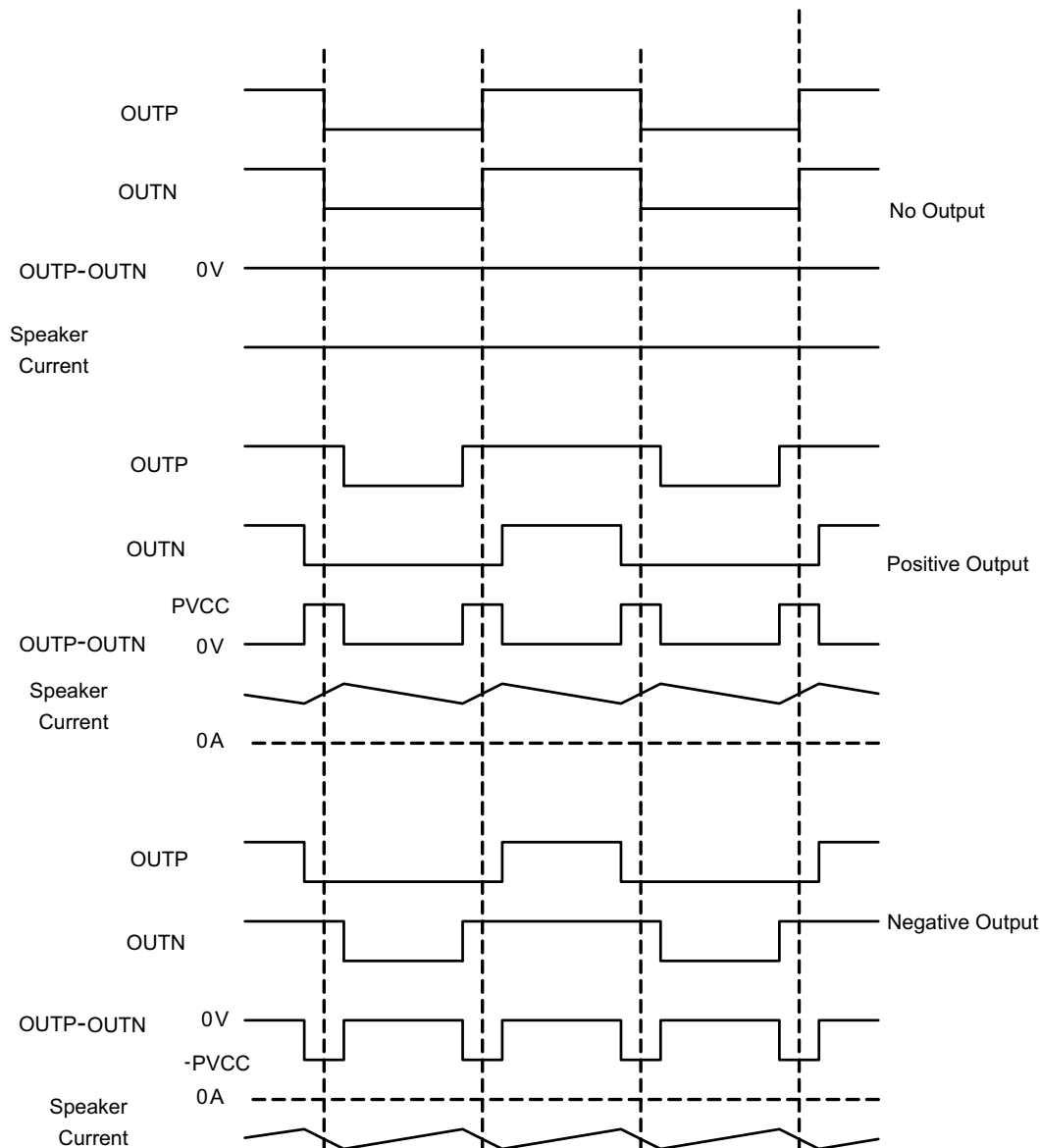
图 32. BD Mode Modulation

7.3.12.2   MODSEL = HIGH: 1SPW-modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

图 33. 1SPW Mode Modulation

7.3.13 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier-based on AD modulation needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, b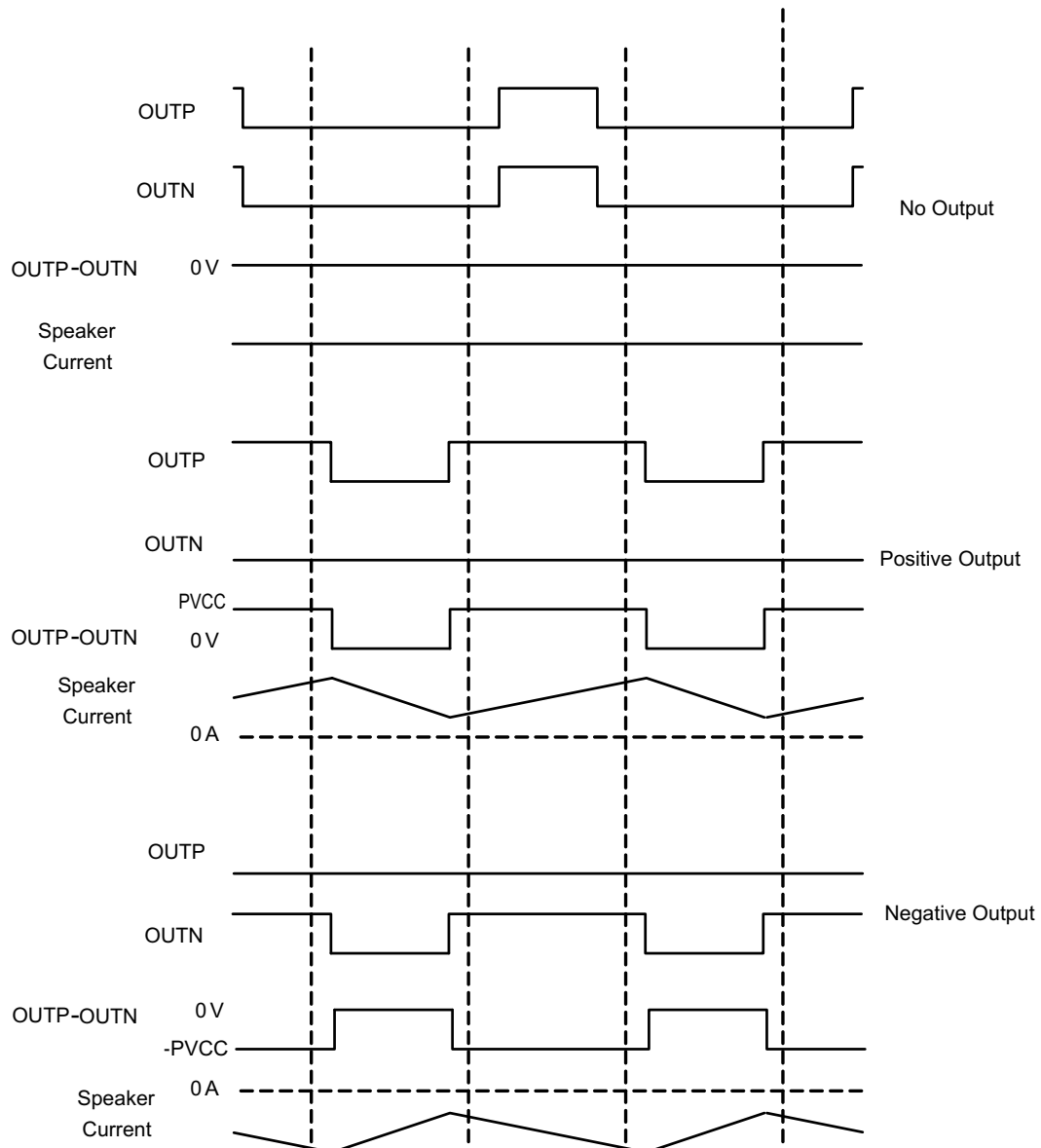ecause the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3116D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

7.3.14 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3116D2 amplifier it is possible to design a high efficiency class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3130D2 can be seen in the TPA3130D2EVM user guide SLOU341.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.
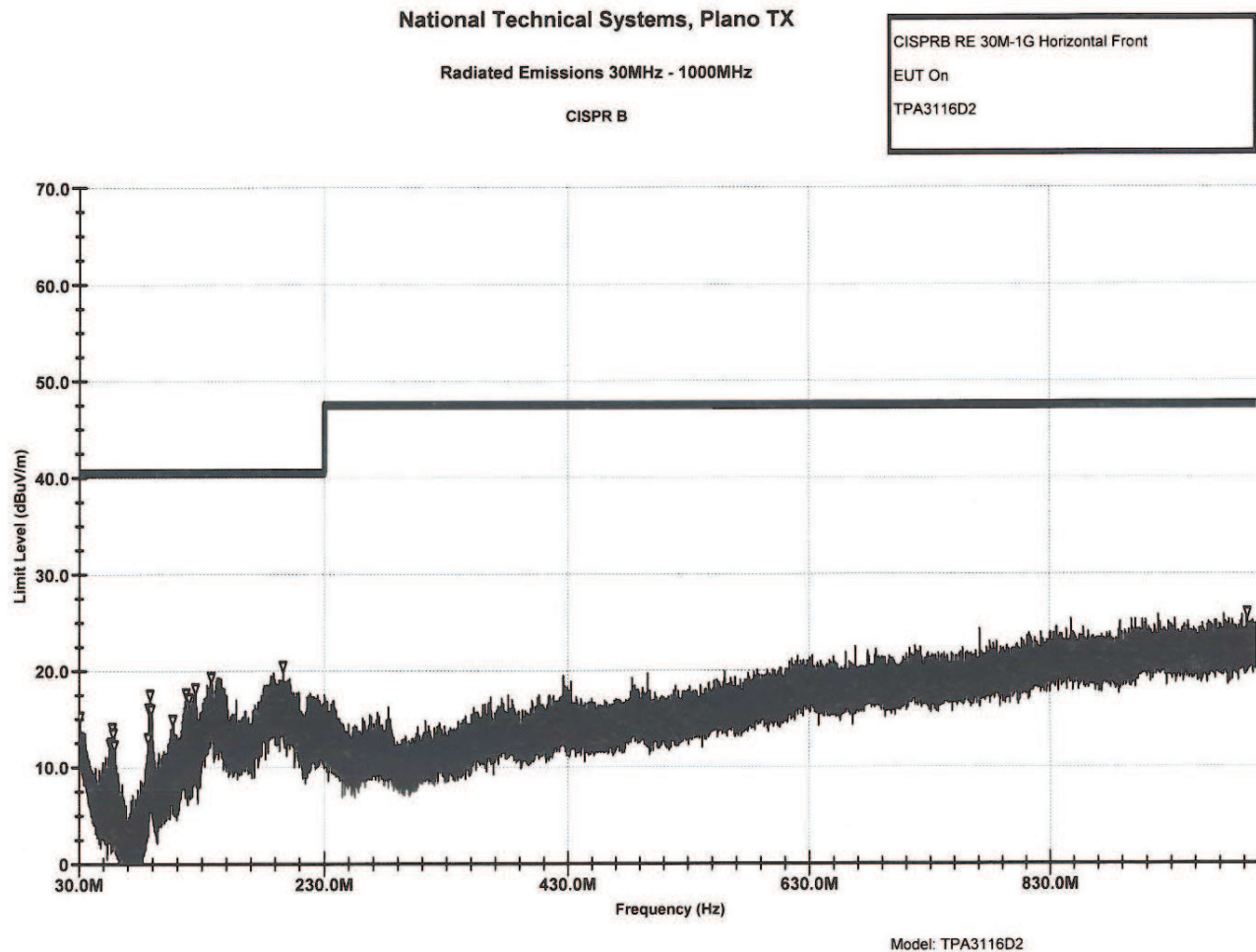
图 34. **TPA311xD2 Radiated Emissions**

7.3.15 When to Use an Output Filter for EMI Suppression

The TPA3116D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3116D2 EVM passes FCC class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.
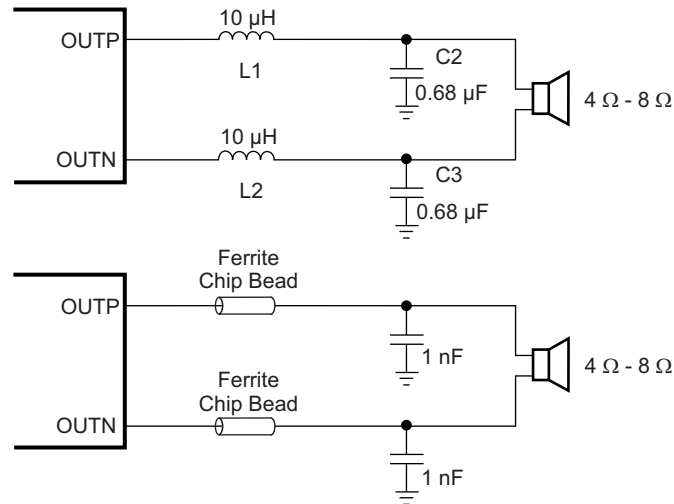
图 35. TPA31xxD2 Output Filters

7.3.16 AM Avoidance EMI Reduction

To reduce interference in the AM radio band, the TPA3116D2 has the ability to change the switching frequency via AM<2:0> pins. The recommended frequencies are listed in 表 6. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

表 6. AM Frequencies

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
	522-540				
540-917	540-914	500	0	0	1
917-1125	914-1122	600 (or 400)	0	1	0
			0	0	0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600 (or 400)	0	1	0
			0	0	0
1547-1700	1548-1701	600 (or 500)	0	1	0
			0	0	1

7.4 Device Functional Modes

7.4.1 Mono Mode (PBTL)

The TPA31xxD2 family can be connected in MONO mode enabling up to 100W output power. This is done by:
- Connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin.
- Analog input signal is applied to INPR and INNR.
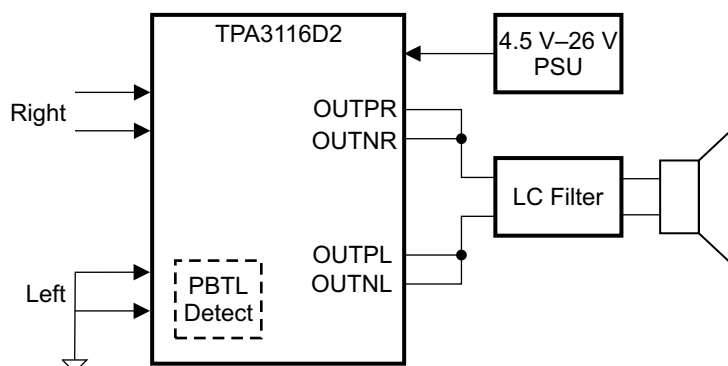
图 36. **Mono Mode**

8   Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1   Application Information

This section describes a 2.1 Master and Slave application. The Master is configured as stereo outputs and the Slave is configured as mono PBTL output.

8.2   Typical Application

A 2.1 solution, U1 TPA3116D2 in Master mode 400 kHz, BTL, gain if 20 dB, power limit not implemented. U2 in Slave, PBTL mode gain of 20 dB. Inputs are connected for differential inputs.

Typical Application (接下页)
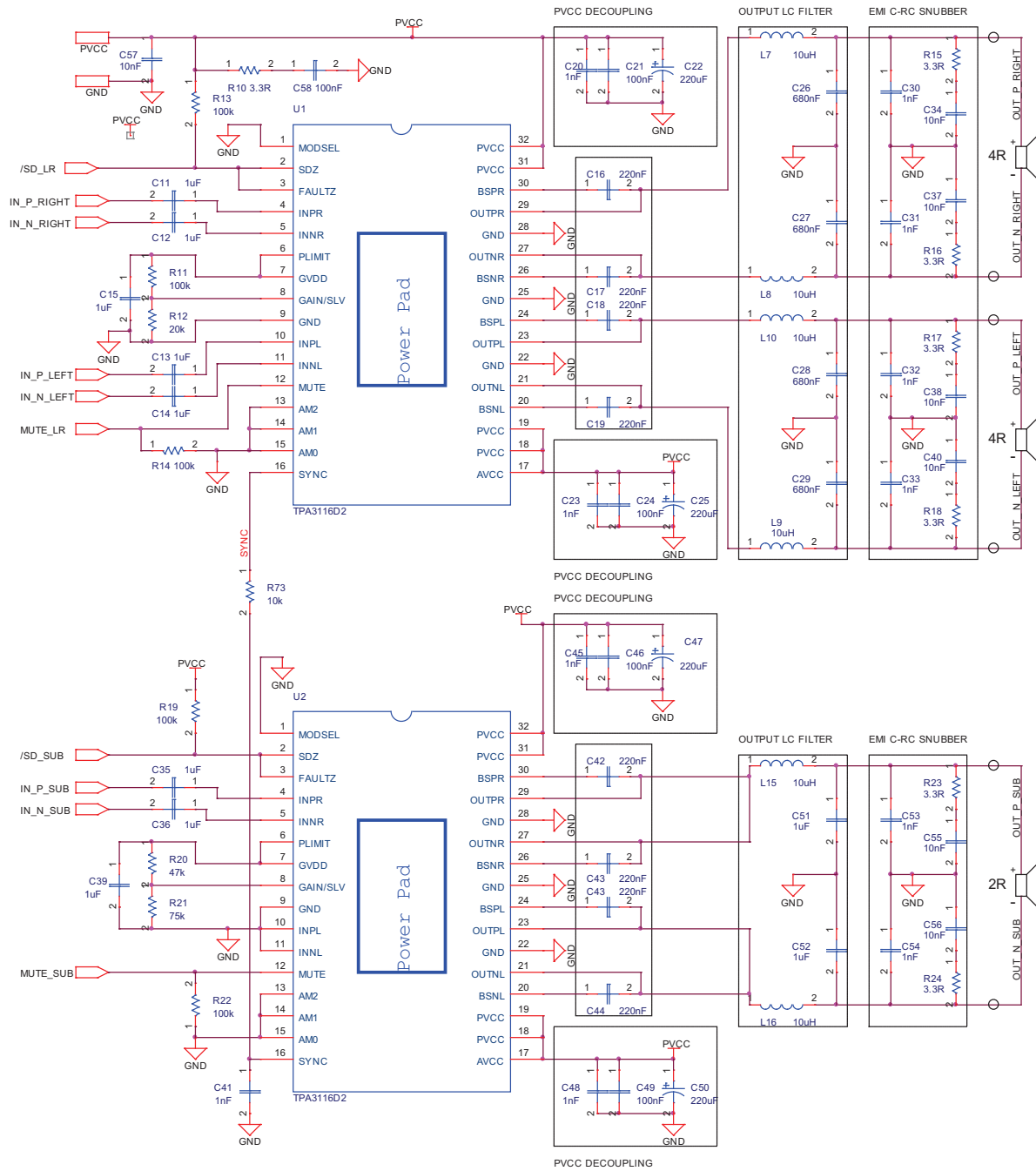
Copyright © 2016, Texas Instruments Incorporated

图 37. Schematic

Typical Application (接下页)

8.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	4.5 V to 26 V
PWM output frequencies	400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	50 W

8.2.2 Detailed Design Procedure

The TPA31xxD2 family is a very flexible and easy to use Class D amplifier; therefore the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Desired PWM frequency

8.2.2.1 Select the PWM Frequency

Set the PWM frequency by using AM0, AM1 and AM2 pins.

8.2.2.2 Select the Amplifier Gain and Master/Slave Mode

In order to select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain and master/slave mode can be set by selecting the voltage divider resistors (R1 and R2) on the Gain/SLV pin.

8.2.2.3 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 100-μF, 50-V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a high-speed switching application.

8.2.2.4 Select Decoupling Capacitors

Good quality decoupling capacitors need to be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

8.2.2.5 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-μF, 25-V capacitors of X5R quality or better.

8.2.3 Application Curves

图 38. Total Harmonic Distortion + Noise (BTL) vs Output Power

图 39. Total Harmonic Distortion + Noise (BTL) vs Output Power
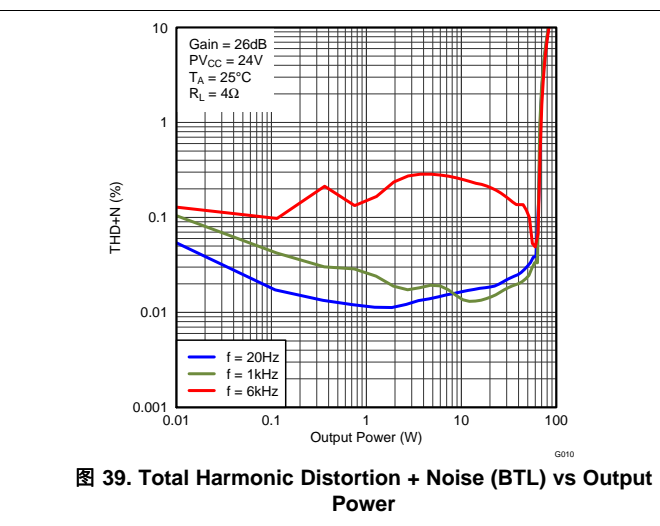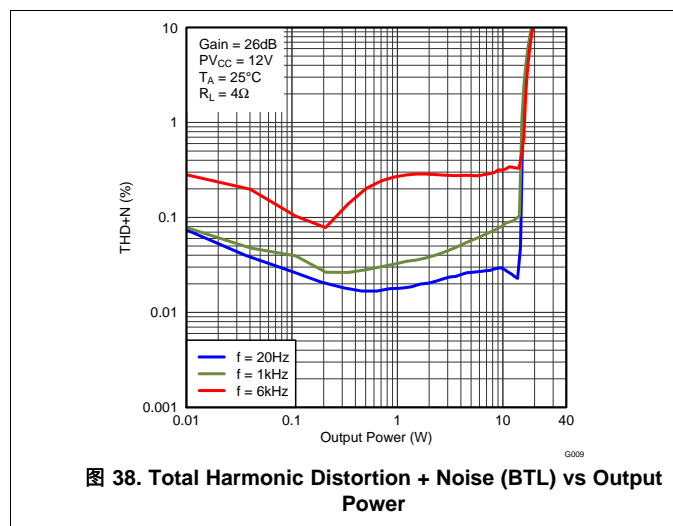
9 Power Supply Recommendations

The power supply requirements for the TPA3116D2 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TPA3116D2 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high voltage supply, between 4.5 V and 26 V, supplies the analog circuitry (AVCC) and the power stage (PVCC). The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

10 Layout

10.1 Layout Guidelines

The TPA3116D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3116D2 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 μF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA3116D2.
- Output filter — The ferrite EMI filter (see 图 35) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

Layout Guidelines (接下页)

For an example layout, see the TPA3116D2 Evaluation Module (TPA3116D2EVM) User Guide (SLOU336). Both the EVM user manual and the thermal pad application reports, SLMA002 and SLMA004, are available on the TI Web site at http://www.ti.com.

10.2 Layout Example

Lots of via's to connect top and bottom layer

Wide open areas for thermal flow. No wires cutting the GND layer obstructing the thermal flow

Top layer is filled with GND

Bulk cap for good audio decoupling

Direct low impedance traces for PVCC and output traces

Ceramic SMD caps close to GVDD, PVCC pins

Output filters placed close to the output pins to minimize return loop

图 40. Layout Example Top

Layout Example (接下页)

Via's along the PCB edge

Solid GND plane for low impedance return path

Lots of via's to connect top and bottom layer

Bottom layer is filled with GND
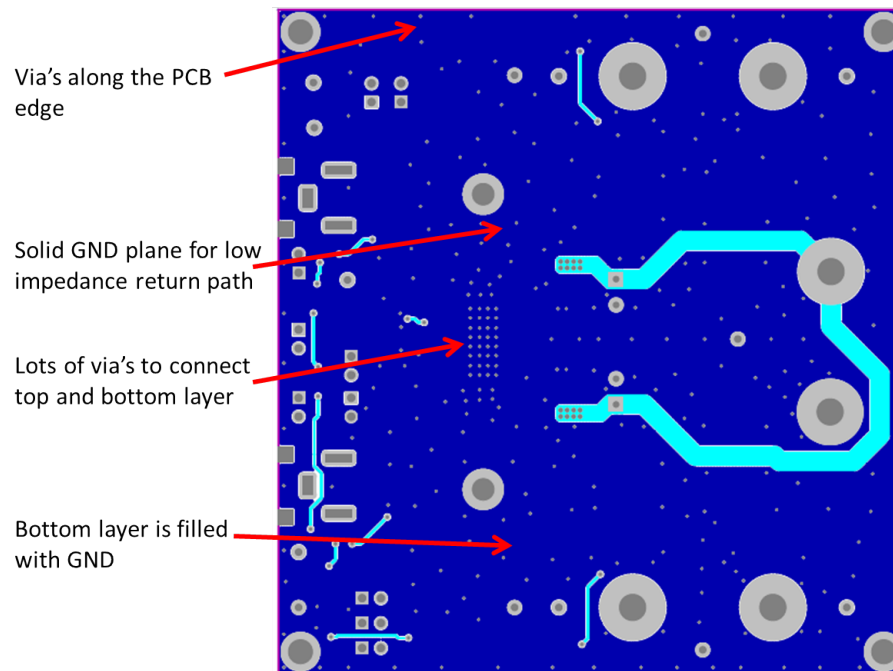
图 41. Layout Example Bottom

10.3 Heat Sink Used on the EVM

The heat sink (part number ATS-TI 10 OP-521-C1-R1) used on the EVM is an 14x25x50 mm extruded aluminum heat sink with three fins (see drawing below). For additional information on the heat sink, go to www.qats.com.
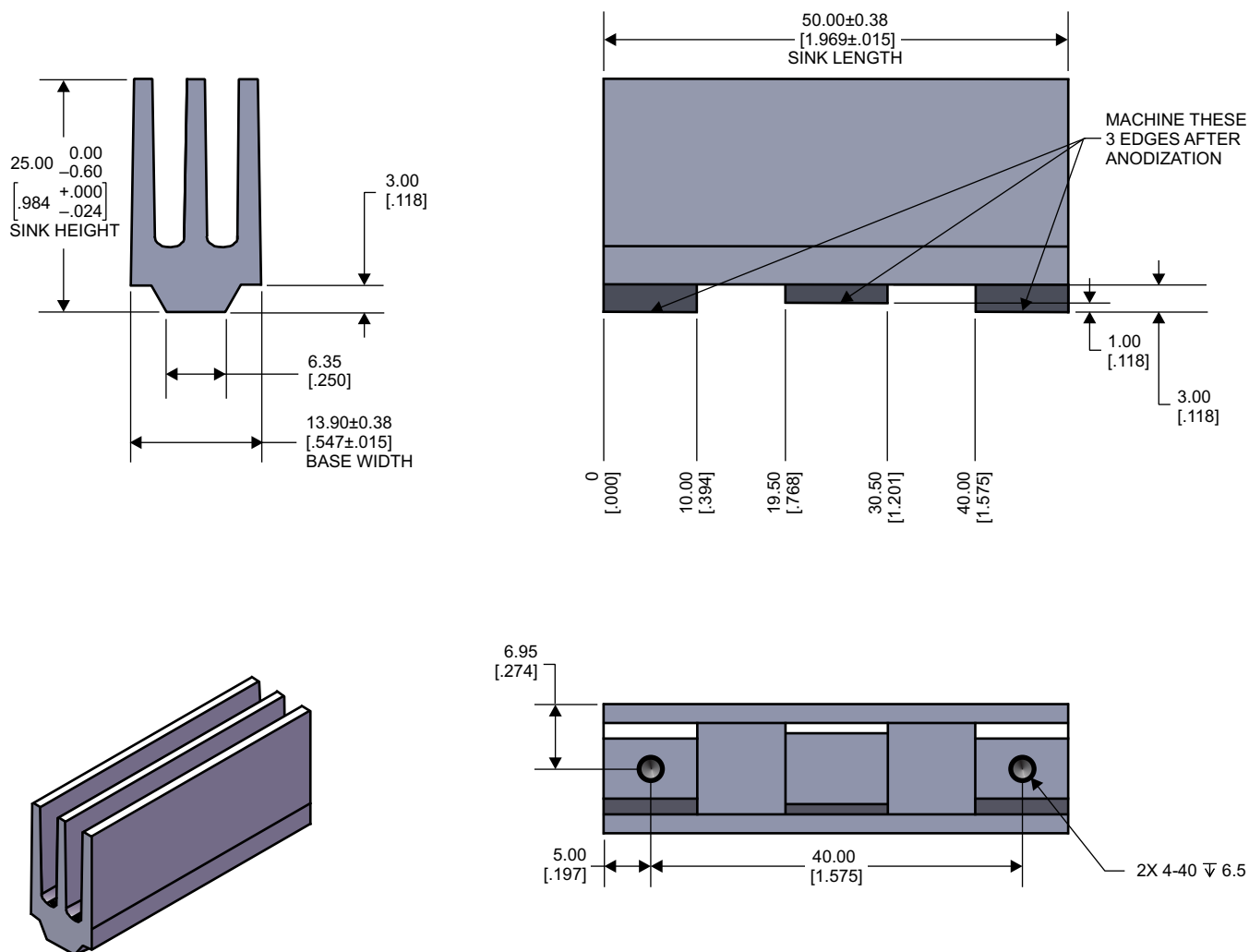
图 42. EVM Heatsink

This size heat sink has shown to be sufficient for continuous output power. The crest factor of music and having airflow will lower the requirement for the heat sink size and smaller types can be used.

11 器件和文档支持

11.1 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 7. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPA3116D2	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPA3118D2	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPA3130D2	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

要接收文档更新通知，请转至 ti.com 上您的器件的产品文件夹。请在右上角单击*通知我* 按钮进行注册，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区。*此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3116D2DAD	ACTIVE	HTSSOP	DAD	32	46	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	TPA 3116 D2	Samples
TPA3116D2DADR	ACTIVE	HTSSOP	DAD	32	2000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	TPA 3116 D2	Samples
TPA3118D2DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3118	Samples
TPA3118D2DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3118	Samples
TPA3130D2DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3130	Samples
TPA3130D2DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3130	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPA3116D2, TPA3118D2 :

● Automotive : TPA3116D2-Q1, TPA3118D2-Q1

NOTE: Qualified Version Definitions:

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3116D2DADR	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3116D2DADR	HTSSOP	DAD	32	2000	350.0	350.0	43.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3116D2DAD	DAD	HTSSOP	32	46	530	11.89	3600	4.9
TPA3118D2DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TPA3130D2DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9

DAD 32
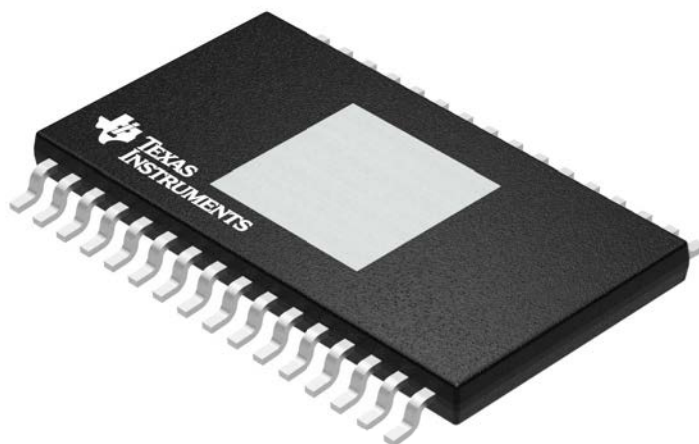
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073258-2/G

8.3 / 7.9 TYP

A

PIN 1 ID AREA

32

30X 0.65

EXPOSED
THERMAL PAD

11.1
10.9
NOTE 3

4.36
3.26

2X
9.75

1

16

17

32X 0.30 / 0.19

⊕ 0.1 Ⓜ C AⓈ BⓈ

4.11
3.31

B

6.2
6.0

C

SEATING PLANE

⌂ 0.1 C

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.75
0.50

1.15
1.00

0.15
0.05

DETAIL A
TYPICAL

4222646/B   02/2020

PowerPAD is a trademark of Texas Instruments.
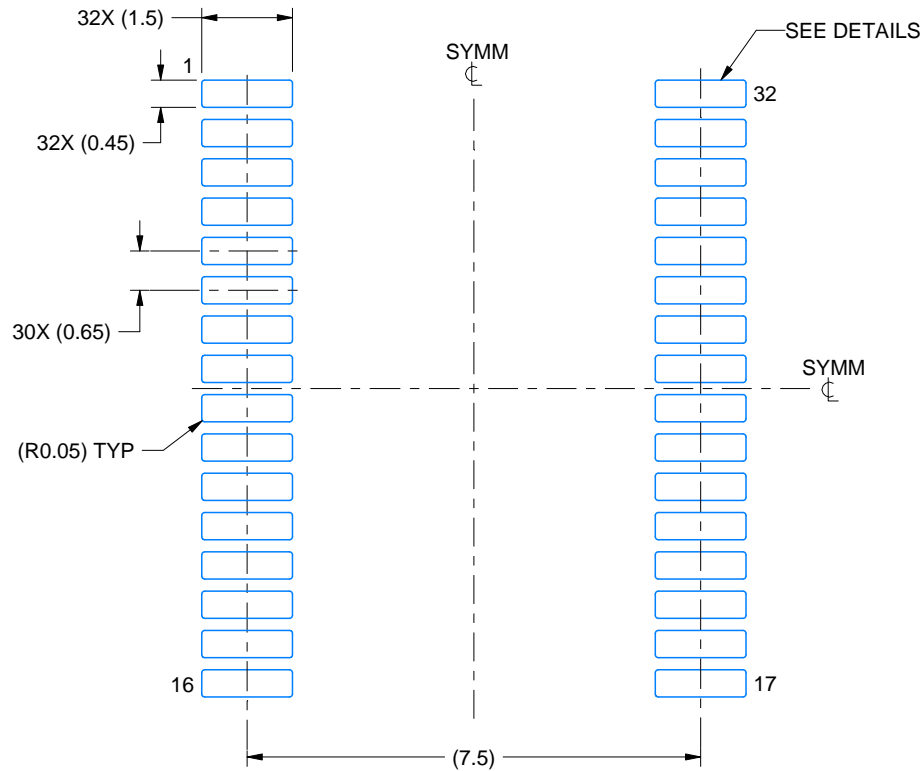
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

DAD0032A

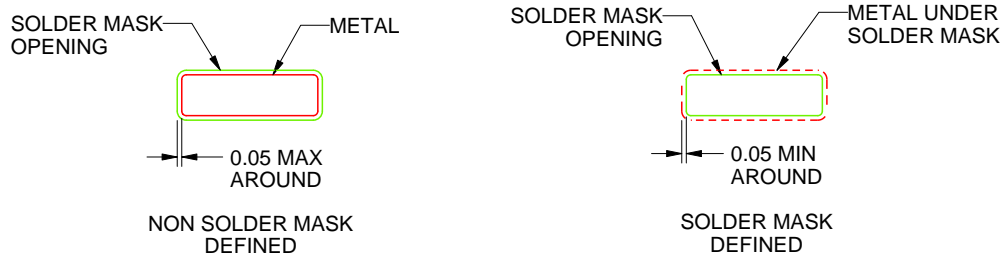### PowerPAD ™TSSOP - 1.15 mm max height

32X (1.5)

1

32X (0.45)

30X (0.65)

(R0.05) TYP

SYMM

SEE DETAILS

32

SYMM

16

17

(7.5)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.05 MAX
AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

0.05 MIN
AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
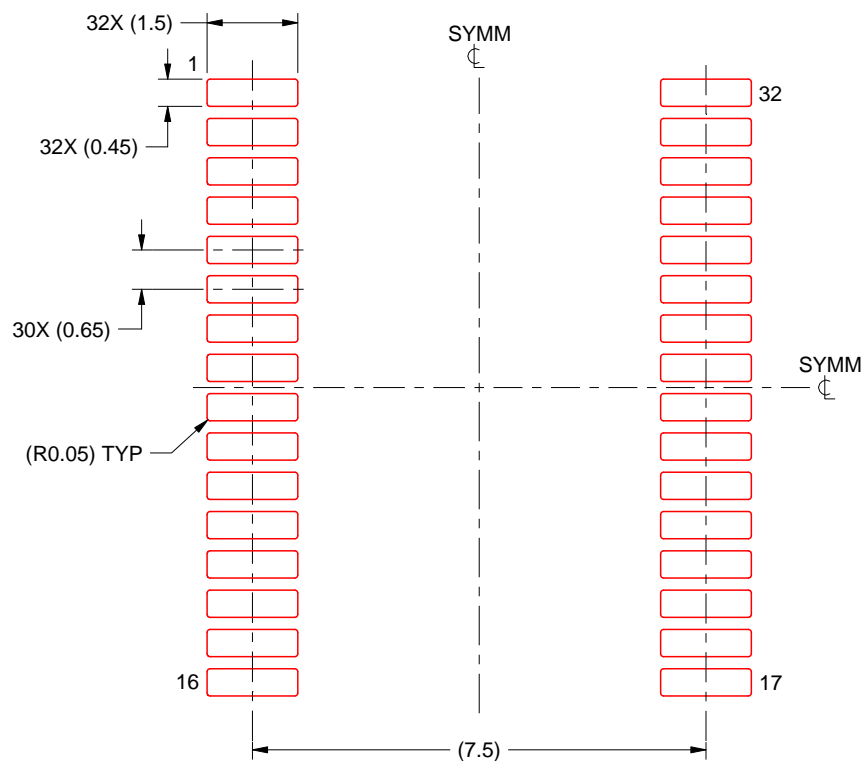NOT TO SCALE

4222646/B   02/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS
INSTRUMENTS
www.ti.com

DAD0032A

PowerPAD ™TSSOP - 1.15 mm max height

PLASTIC SMALL OUTLINE

32X (1.5)

1

SYMM

32X (0.45)

30X (0.65)

(R0.05) TYP

16

SYMM

32

SYMM

17

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222646/B 02/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
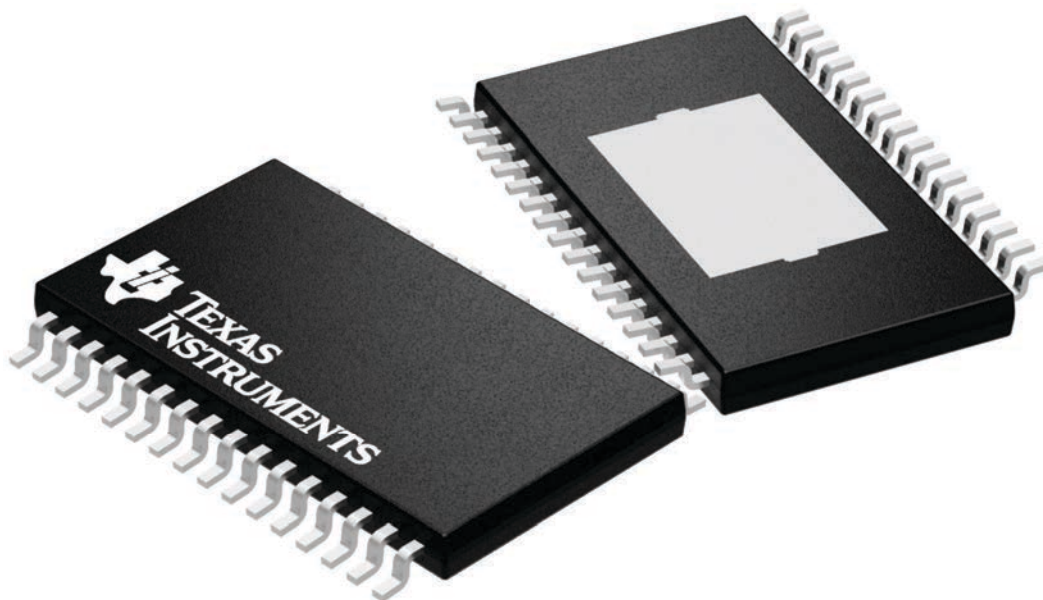8. Board assembly site may have different recommendations for stencil design.

DAP 32

PowerPAD™ TSSOP - 1.2 mm max height
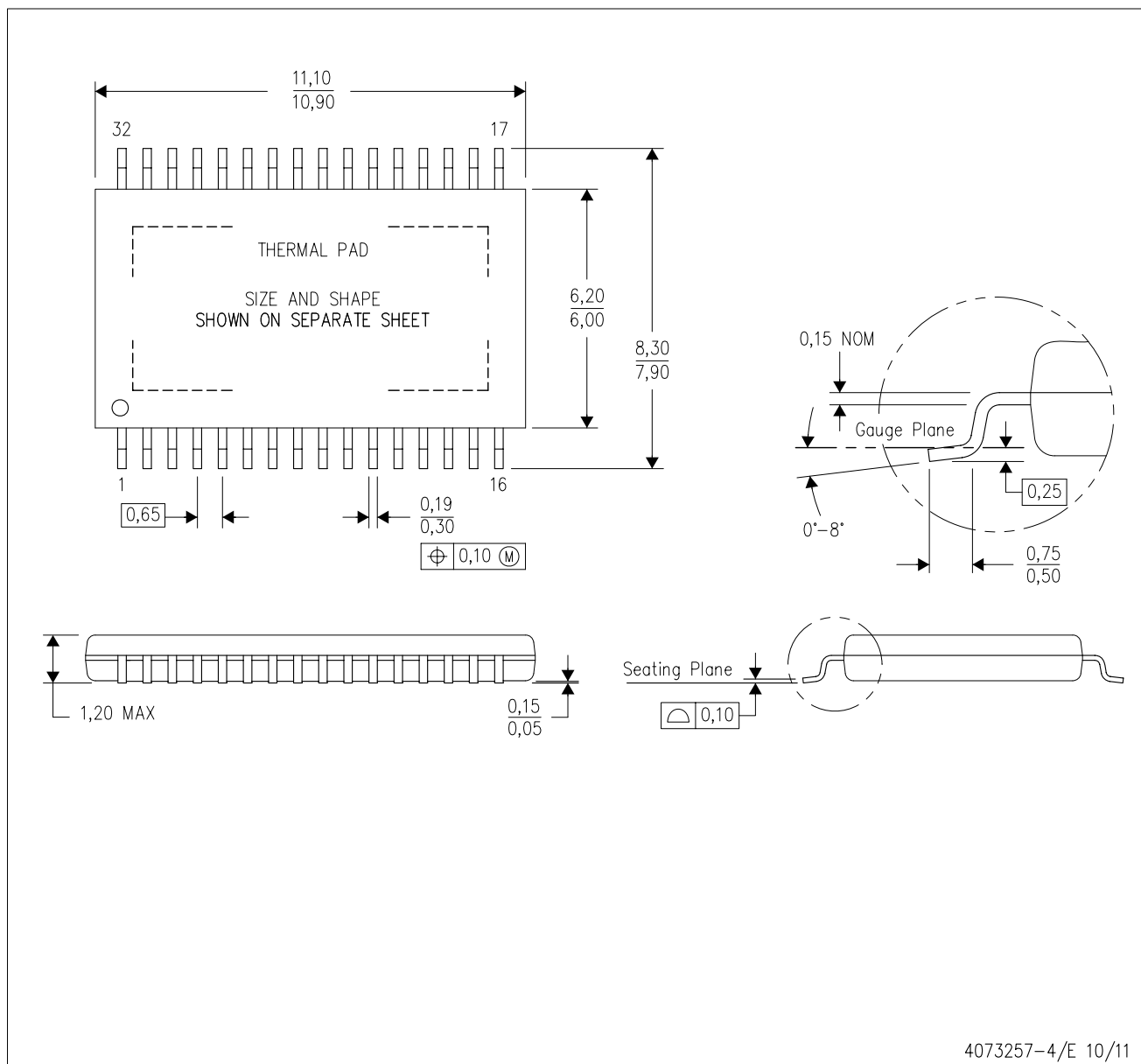
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225303/A

DAP (R−PDSO−G32)   PowerPAD™ PLASTIC SMALL−OUTLINE PACKAGE

$\frac{11,10}{10,90}$

32   17

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

$\frac{6,20}{6,00}$

$\frac{8,30}{7,90}$

1   16

| 0,65 |

$\frac{0,19}{0,30}$

⊕ | 0,10 Ⓜ |

0,15 NOM

Gauge Plane

| 0,25 |

0°−8°

$\frac{0,75}{0,50}$

1,20 MAX

$\frac{0,15}{0,05}$

Seating Plane

◁ | 0,10 |

4073257−4/E 10/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.
         F.   Falls within JEDEC MO−153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.
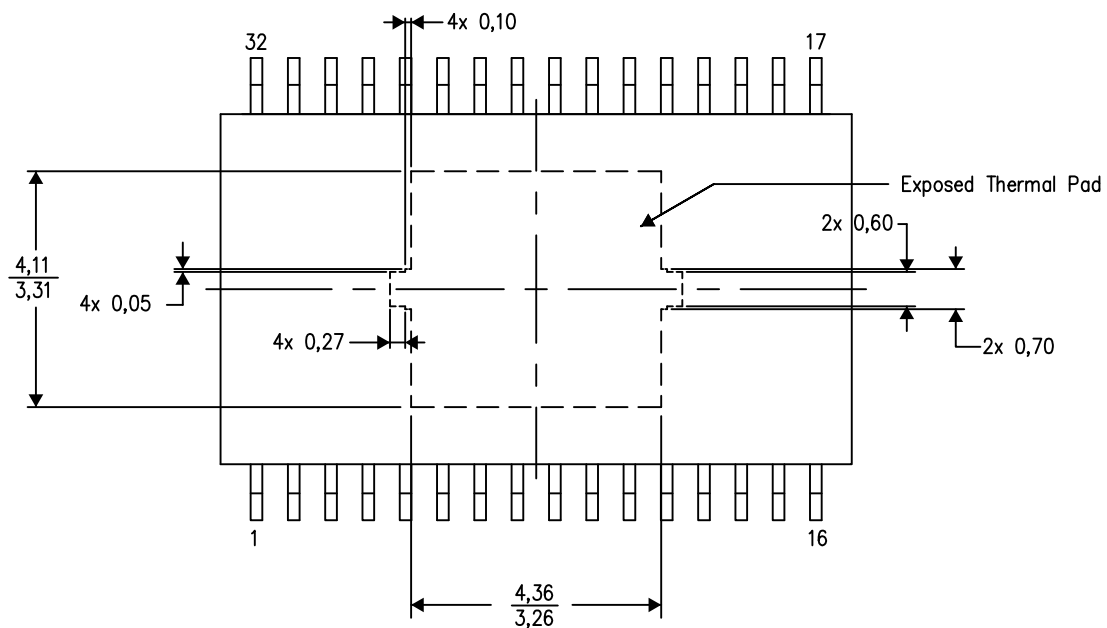
TEXAS INSTRUMENTS
www.ti.com

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

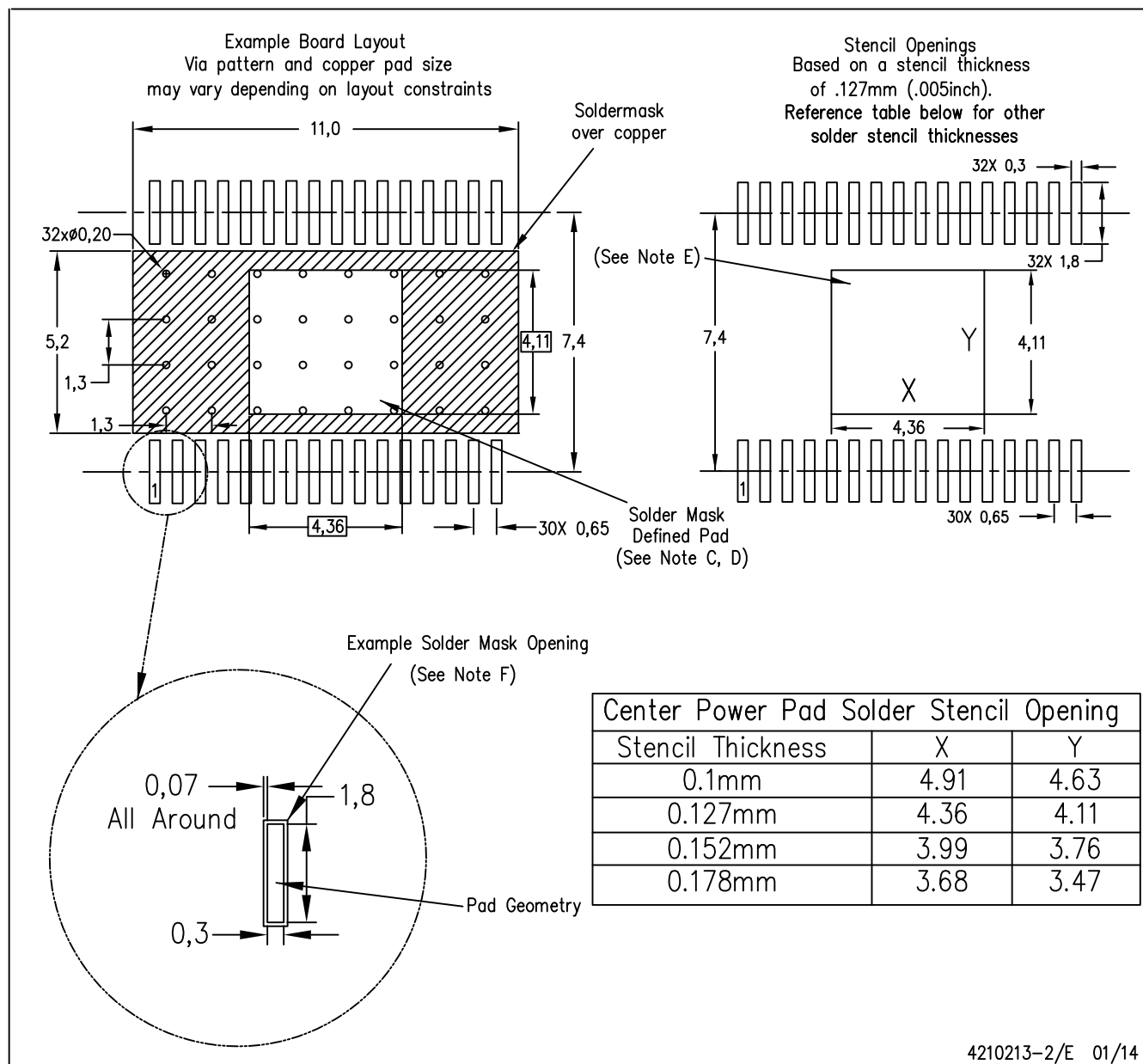Top View
Exposed Thermal Pad Dimensions

4206319-3/M 09/13

NOTE: All linear dimensions are in millimeters

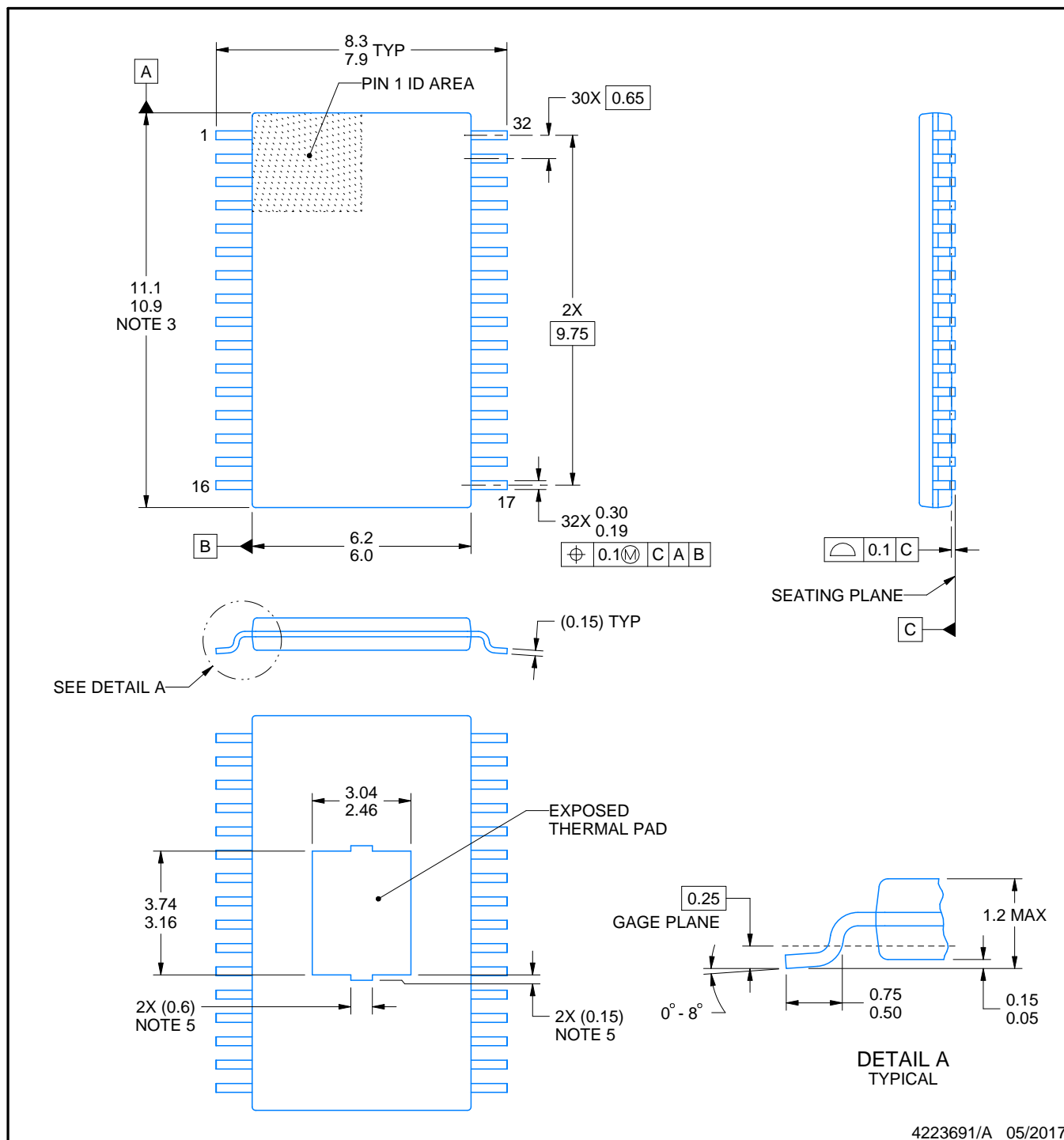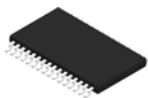**PowerPAD is a trademark of Texas Instruments.**

TEXAS INSTRUMENTS
www.ti.com

DAP (R−PDSO−G32)   PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Soldermask
over copper

11,0

32xØ0,20

5,2

1,3

1,3

4,11 7,4

(See Note E)

Solder Mask
Defined Pad
(See Note C, D)

4,36

30X 0,65

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

32X 0,3

32X 1,8

7,4

Y

X

4,11

4,36

30X 0,65

Example Solder Mask Opening
(See Note F)

0,07
All Around

1,8

0,3

Pad Geometry

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

4210213−2/E 01/14

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
             Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout. These documents are available at
             www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         F. Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments

![Texas Instruments logo]
**TEXAS
INSTRUMENTS**
www.ti.com

8.3 / 7.9 TYP

A

PIN 1 ID AREA

30X 0.65

32

1

11.1 / 10.9 NOTE 3

2X 9.75

16

17

B

6.2 / 6.0

32X 0.30 / 0.19

⊕ 0.1 Ⓜ C A B

⌓ 0.1 C

SEATING PLANE

C

SEE DETAIL A

(0.15) TYP

3.04 / 2.46

EXPOSED THERMAL PAD

3.74 / 3.16

2X (0.6) NOTE 5

2X (0.15) NOTE 5

0.25

GAGE PLANE

1.2 MAX

0° - 8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
TYPICAL

4223691/A   05/2017

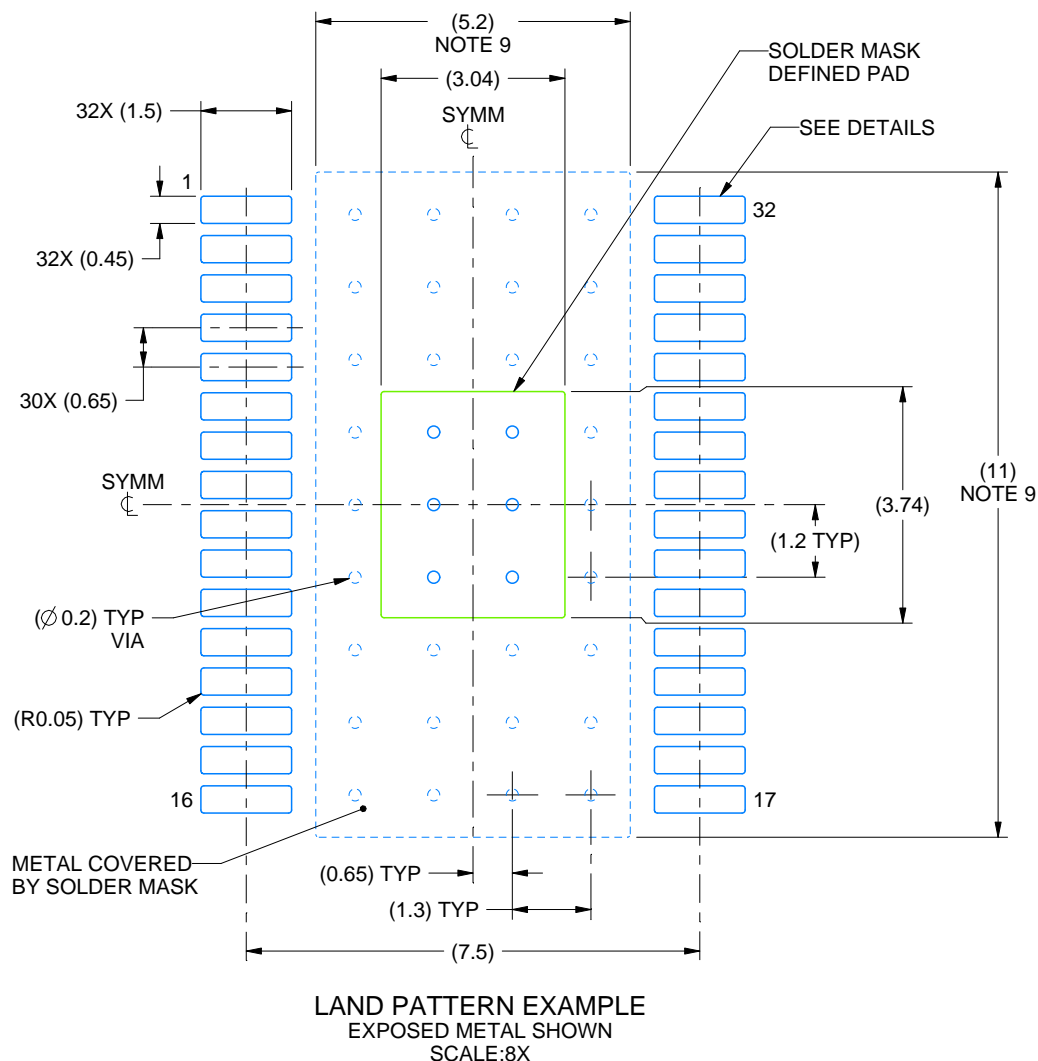PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

DAP0032C

SOLDER MASK
DEFINED PAD

SEE DETAILS

(5.2)
NOTE 9

(3.04)
SYMM

32X (1.5)

1

32X (0.45)

30X (0.65)

SYMM

(∅ 0.2) TYP
VIA

(R0.05) TYP

METAL COVERED
BY SOLDER MASK

32

17

16

(11)
NOTE 9

(3.74)

(1.2 TYP)

(0.65) TYP

(1.3) TYP

(7.5)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223691/A   05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

DAP0032C

PowerPAD™   TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE
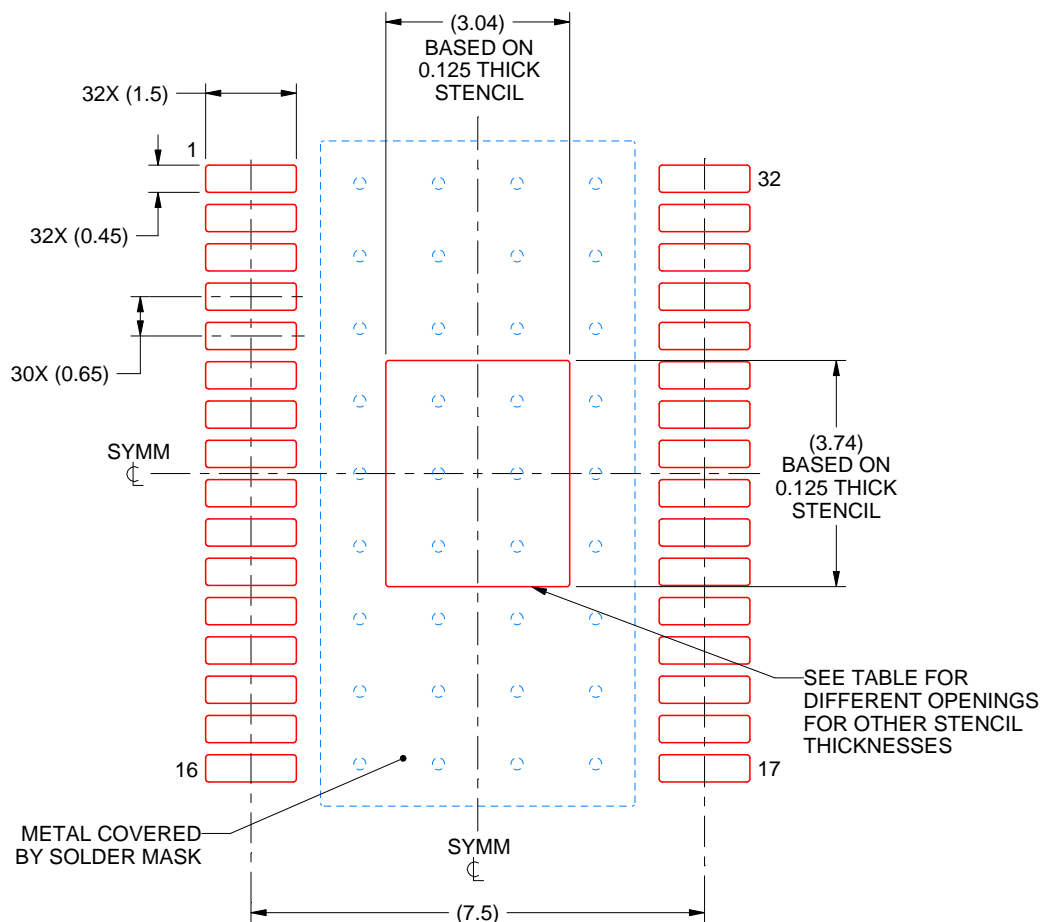
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A   05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明