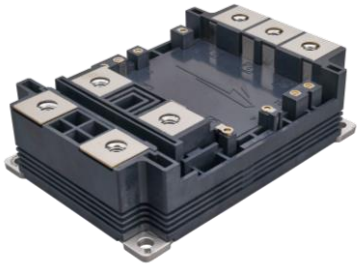
CAB600M33LM3

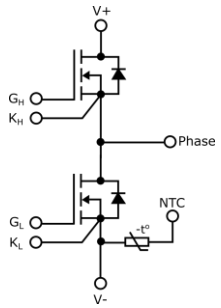
3300 V, 2.7 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	3300 V
I_{DS}	600 A

Technical Features

- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Low Stray Inductance (9.5 nH)
- AlSiC Baseplate
- High Thermal Conductivity Silicon Nitride Substrate
- Increased Thermal-Mechanical Performance
- 3300 V Drain-Source Voltage





System Benefits

- Reduced Volume, Weight Overall System Level Cost
- Higher Reliability
- Higher System Efficiency
- Reduced Cooling Requirements
- Improved Thermal Cycling and Longer Lifetime

Typical Applications

- Heavy-Duty E-Mobility: Transportation and Mining
- Ultra-Fast DC Chargers
- Industrial Motor Drives
- Industrial Uninterruptable Power Supply (UPS) Systems
- Marine and Aerospace Propulsion
- Terrestrial Power Distribution Systems
- HVDC and FACTS Controllers

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Voltage	V_{DS}			3300	V	T_C = 25 °C	
Maximum Gate-Source Voltage	$V_{GS\,max}$	-10		+20		Transient	Note 1 Fig. 33
Operational Gate-Source Voltage	$V_{GS\,op}$		-5/+15			Static	
DC Continuous Drain Current ($T_{VJ} \leq 175$ °C)	I_D			770	A	V_{GS} = 15 V, T_C = 25 °C, $T_{VJ} \leq 175$ °C	Notes 2, 3, 4 Fig. 20
			580			V_{GS} = 15 V, T_C = 90 °C, $T_{VJ} \leq 175$ °C	
Pulsed Drain Current	I_{DM}		1540			t_{pmax} limited by $T_{VJ\,max}$ V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		4050		W	T_C = 25 °C, $T_{VJ} \leq 175$ °C	Note 5 Fig. 21
Operating Virtual Junction Temperature	$T_{VJ\,op}$	-55		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with ±5% regulation tolerance
Note (2): Current limit T_C = 25 °C imposed by package
Note (3): Current limit T_C = 90 °C calculated by $I_{D(max)}=\sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$
Note (4): Verified by design
Note (5): $P_D = (T_{VJ} - T_C)/R_{TH(JC,\,Typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	3300			V	V_{GS} = 0 V, T_{VJ} = -55 °C	
Gate Threshold Voltage	$V_{GS(th)}$	2.6	3.5	4.5	V	V_{DS} = V_{GS}, I_{DS} = 530 mA	
			2.6			V_{DS} = V_{GS}, I_{DS} = 530 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		100	600	µA	V_{GS} = 0 V, V_{DS} = 3300 V	
Gate-Source Leakage Current	I_{GSS}		200	5000	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (MOSFET only)	$R_{DS(on)}$		2.7	3.4	mΩ	V_{GS} = 15 V, I_{DS} = 600 A	Fig. 2 Fig. 3
			6.8			V_{GS} = 15 V, I_{DS} = 600 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		448		S	V_{DS} = 20 V, I_{DS} = 600 A	Fig. 4
			536			V_{DS} = 20 V, I_{DS} = 600 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		170 167 193		mJ	V_{DD} = 1800 V, I_D = 600 A, V_{GS} = -5 V/15 V, $R_{G-ON(ext)}$ = 2.5 Ω, $R_{G-OFF(ext)}$ = 1 Ω, L_σ = 7 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		40 37 41				
Internal Gate Resistance	$R_{G(int)}$		0.5		Ω	f = 100 kHz, V_{AC} = 25 mV	
Input Capacitance	C_{iss}		146		nF	V_{GS} = 0 V, V_{DS} = 3000 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.8				
Reverse Transfer Capacitance	C_{rss}		53		pF		
Gate to Source Charge	Q_{GS}		2620		nC	V_{DS} = 2000 V, V_{GS} = -5 V/+15 V I_D = 1000 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		375				
Total Gate Charge	Q_G		5120				
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.037		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Body Diode Forward Voltage	V_{SD}		6.0		V	V_{GS} = -5 V, I_{SD} = 600 A	Fig. 7
			5.3		V	V_{GS} = -5 V, I_{SD} = 600 A, T_{VJ} = 175 °C	
Reverse Recovery Time	t_{RR}		238		ns	V_{GS} = -5 V, I_{SD} = 600 A, V_R = 1800 V; di_f/dt = 6.5 A/ns, $R_{G(ON)}$ = 2.5 Ω, T_{VJ} = 175 °C,	
Reverse Recovery Charge	Q_{RR}		38		µC		
Peak Reverse Recovery Current	I_{RRM}		255		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		1.0 24.4 53.1		mJ	V_{DD} = 1800 V, I_D = 600 A, V_{GS} = -5 V/15 V, $R_{G-ON(ext)}$ = 2.5 Ω, L_σ = 7 nH	Fig. 14

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25 °C	R_{25}		4700		Ω	T_{NTC} = 25 °C
Tolerance of R_{25}				±1	%	
Beta Value for 25 °C to 85 °C	$B_{25/85}$		3435		K	
Beta Value for 0 °C to 100 °C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$				±1	%	
Maximum Power Dissipation	P_{25}			50	mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Characteristics Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	R_{1-3}		0.28		mΩ	T_C = 125 °C, Note 6 & 7
Package Resistance, M2 (Low-Side)	R_{3-6}		0.55		mΩ	T_C = 125 °C, Note 6 & 7
Stray Inductance	L_{Stray}		9.5		nH	Between Terminals 1 & 6, f = 10 MHz
Case Temperature	T_C	-55		150	°C	
Storage Temperature	T_{stg}	-55		150	°C	
Mounting Torque	M	3.5	4.5	5.5	N-m	Baseplate, M6 bolts
		12	14	16	N-m	Power Terminals, M8 bolts
		0.5	0.7	1.3	N-m	Auxiliary Terminals, M3 bolts
Weight	W		745		g	
Case Isolation Voltage	6.0				kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance		11			mm	Terminal to Terminal
		33			mm	Terminal to Baseplate
Creepage Distance		23			mm	Terminal to Terminal
		45			mm	Terminal to Baseplate

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(ON)}$ + Switch Position Package Resistance
Note (7): Numbers reference the connections from the Schematics and Pin Out section of this document

Typical Performance

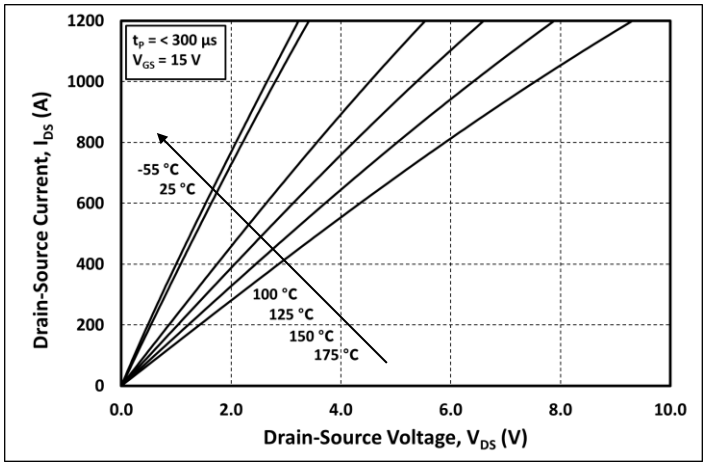


Figure 1. Output Characteristics for Various Junction Temperatures

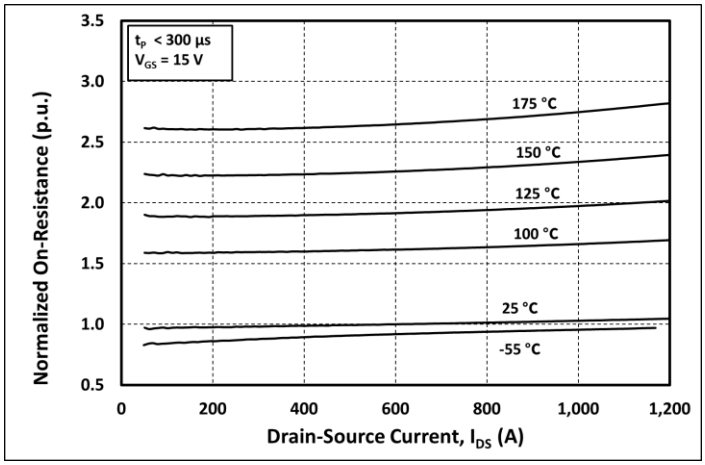


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

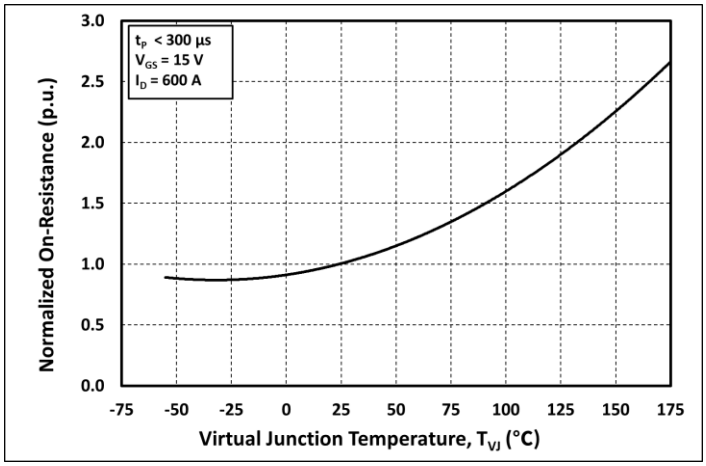


Figure 3. Normalized On-State Resistance vs. Junction Temperature

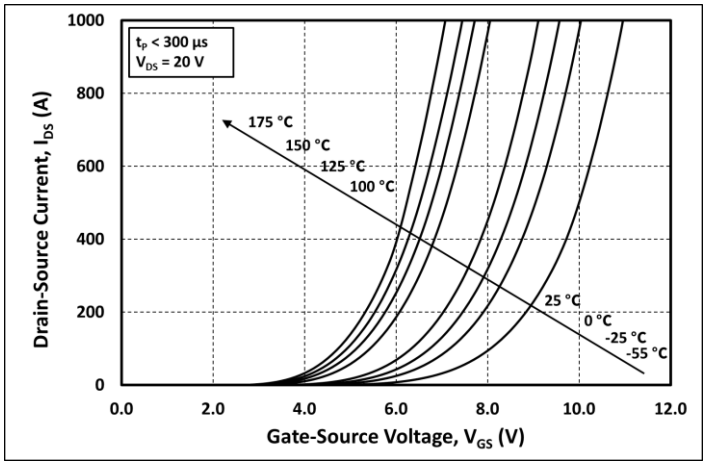


Figure 4. Transfer Characteristics for Various Junction Temperatures

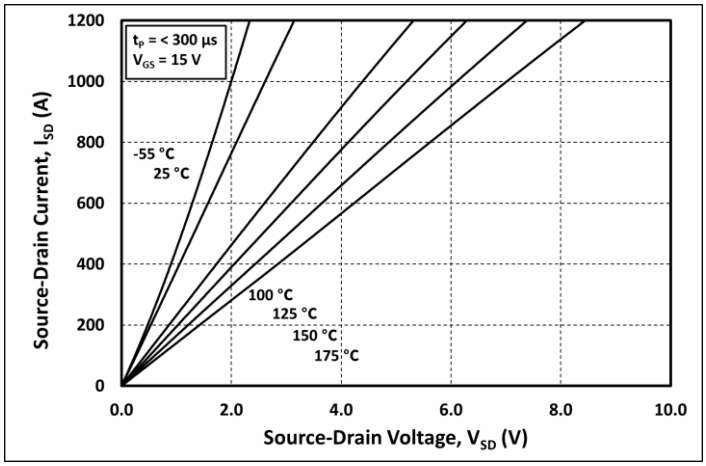


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

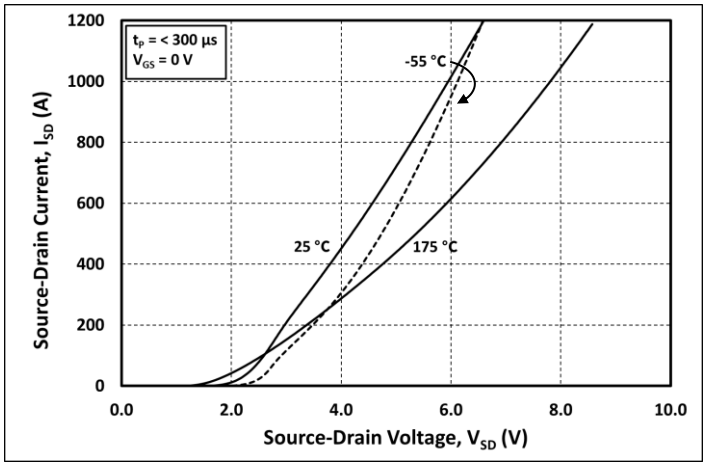


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V

Typical Performance

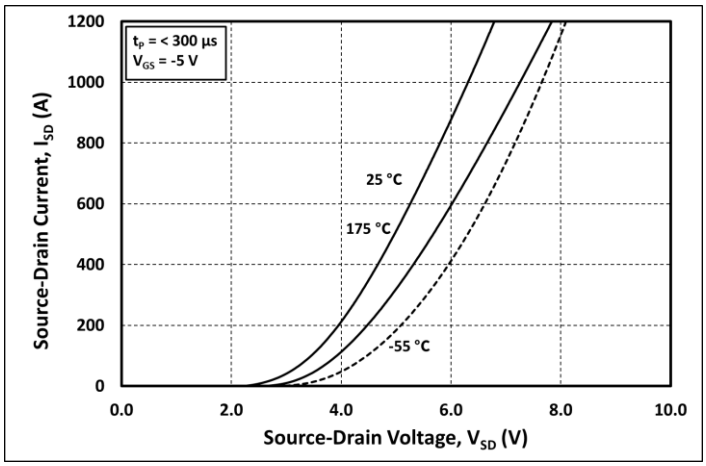


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -5 V (Body Diode)

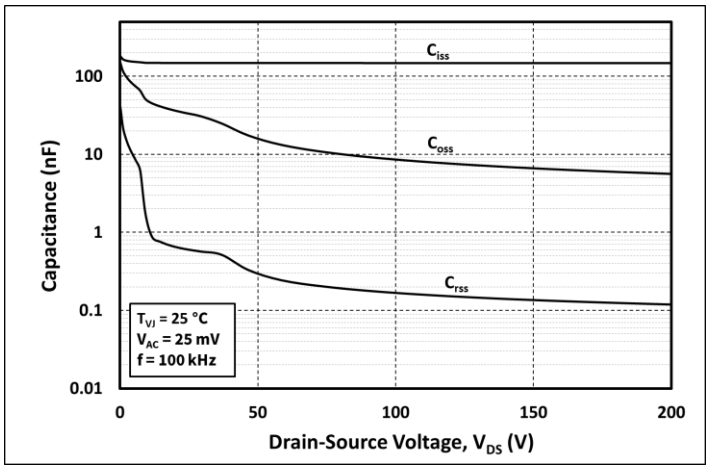


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 – 200 V)

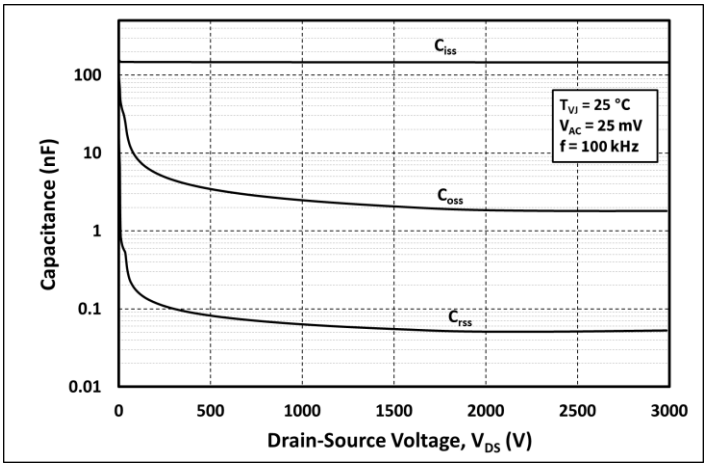


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 – 3000 V)

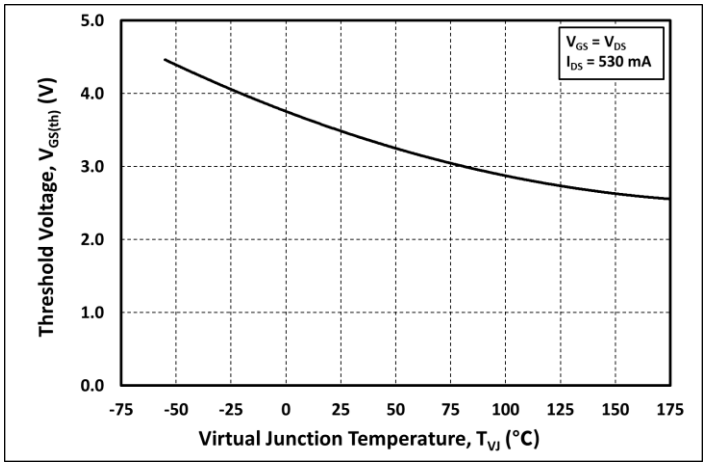


Figure 10. Threshold Voltage vs. Junction Temperature

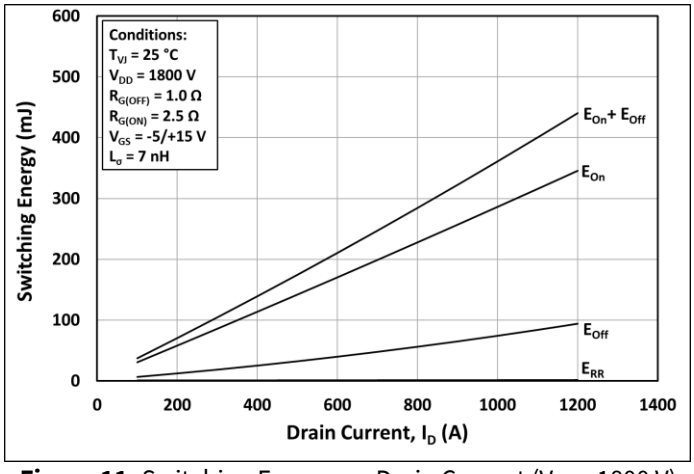


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 1800 V)

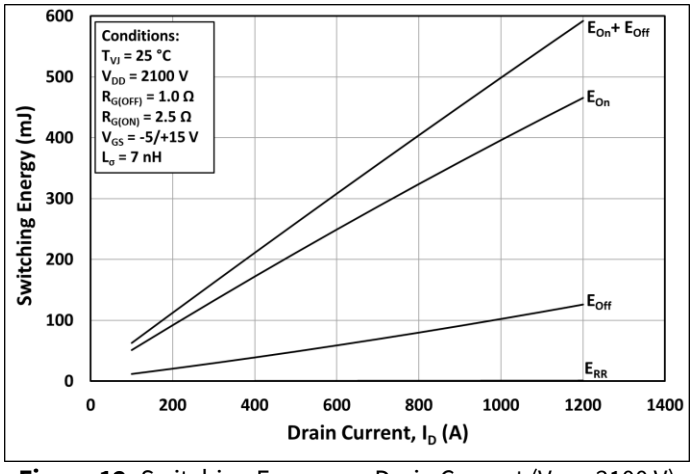


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 2100 V)

Typical Performance

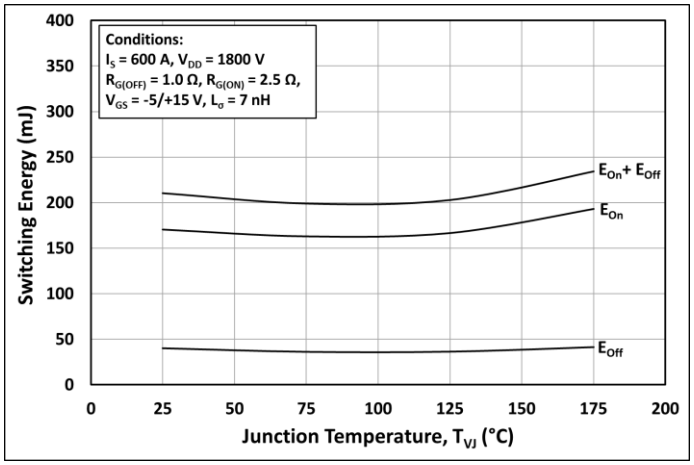


Figure 13. MOSFET Switching Energy vs. Junction Temperature

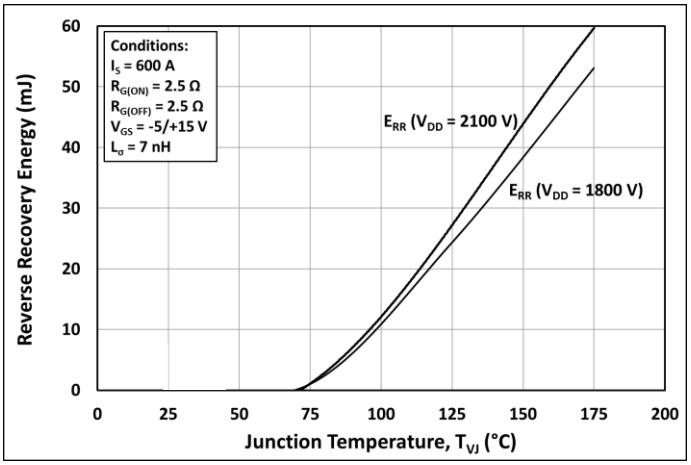


Figure 14. Reverse Recovery Energy vs. Junction Temperature

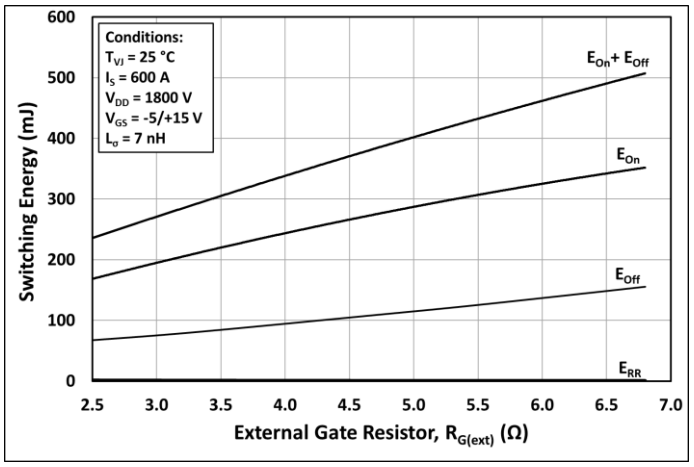


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

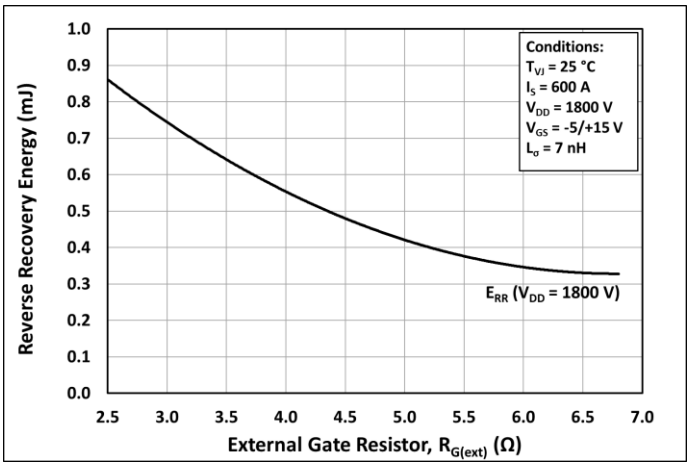


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

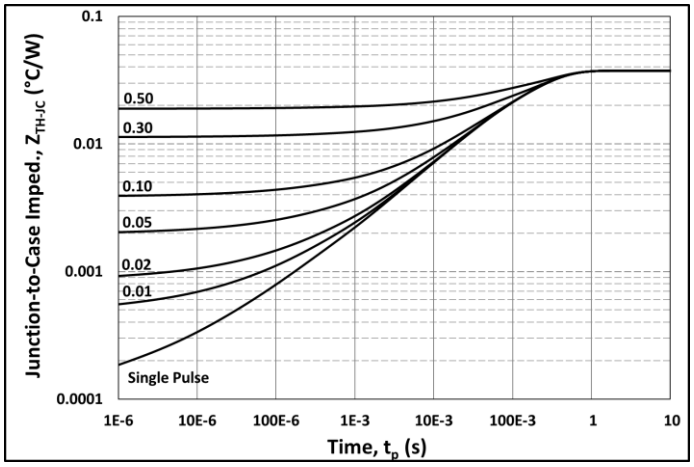


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

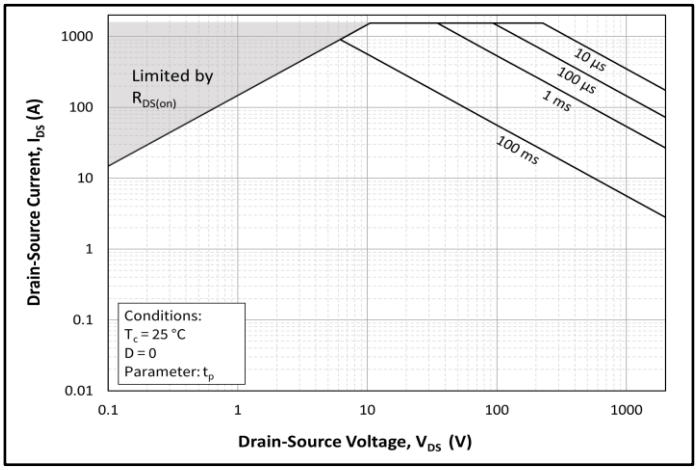


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

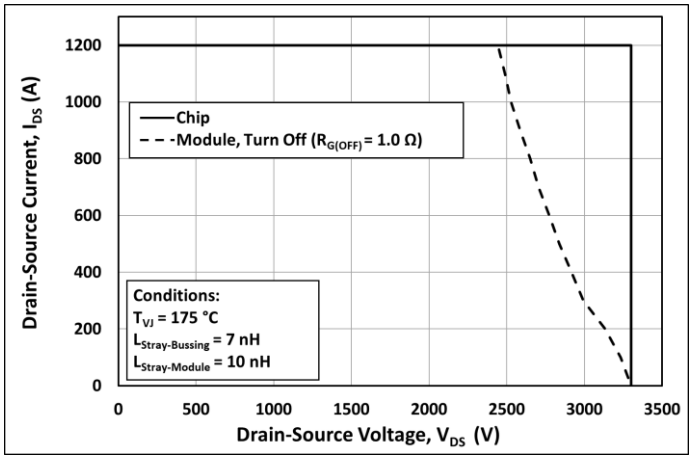


Figure 19. Switching Safe Operating Area

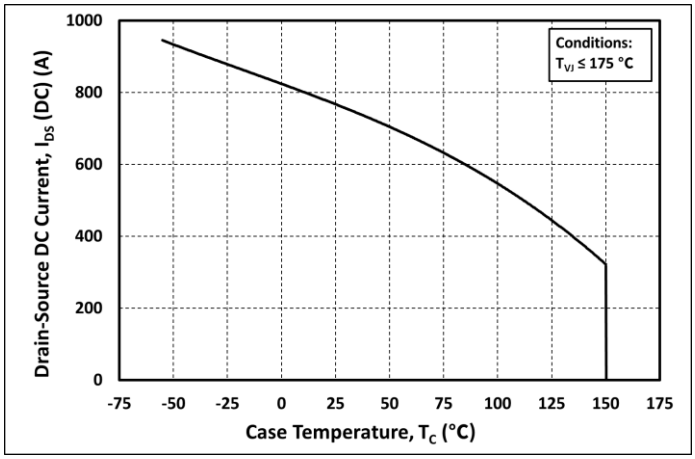


Figure 20. Continuous Drain Current Derating vs. Case Temperature

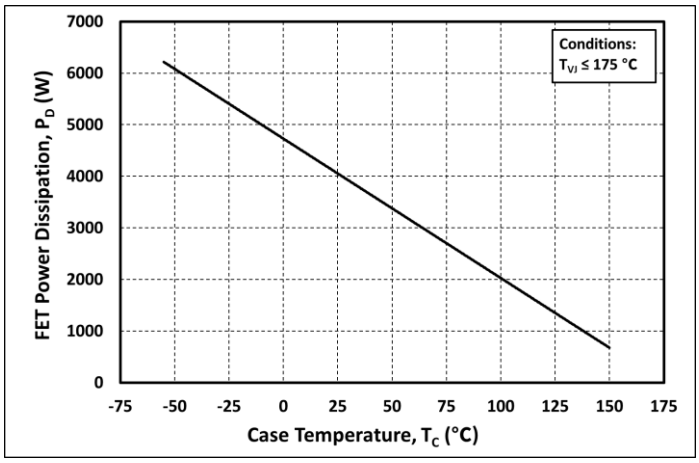


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

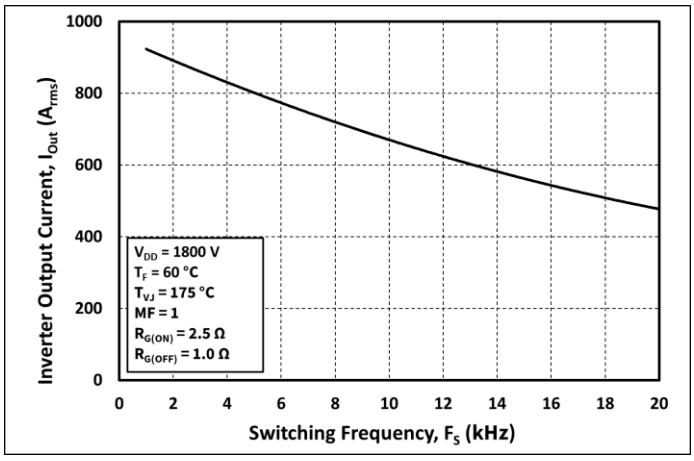


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

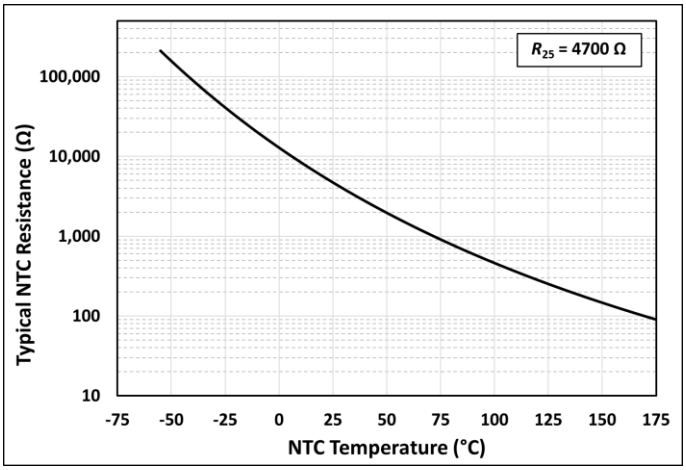


Figure 23. NTC Resistance vs. NTC Temperature

Timing Characteristics

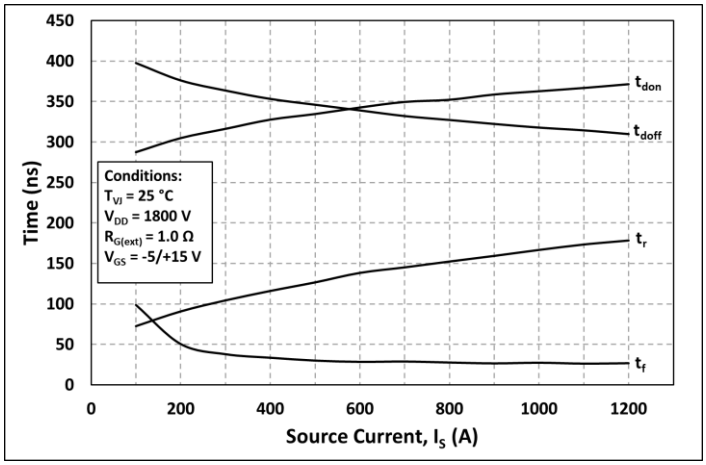


Figure 24. Timing vs. Source Current

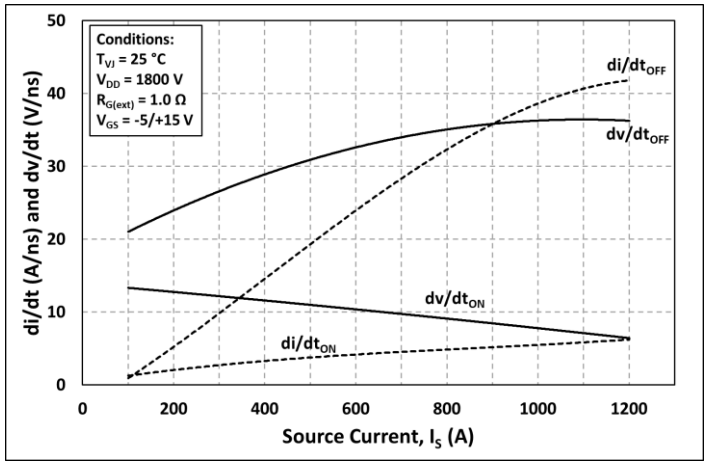


Figure 25. dv/dt and di/dt vs. Source Current

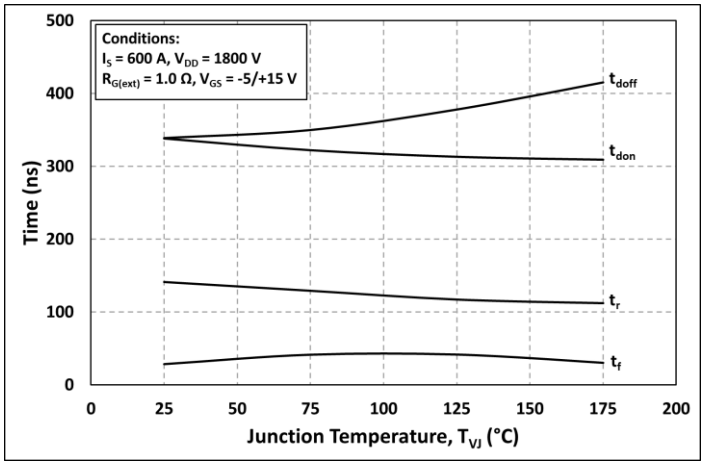


Figure 26. Timing vs. Junction Temperature

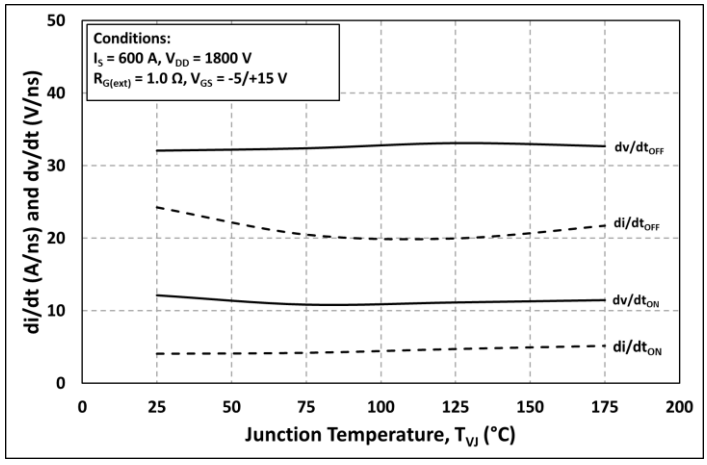


Figure 27. dv/dt and di/dt vs. Junction Temperature

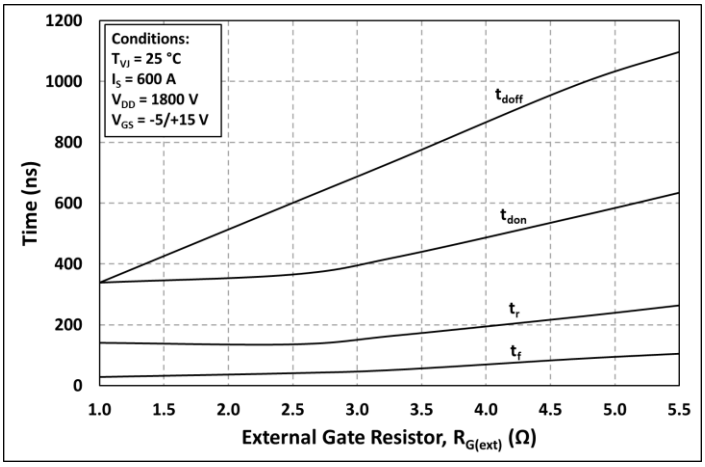


Figure 28. Timing vs. External Gate Resistance

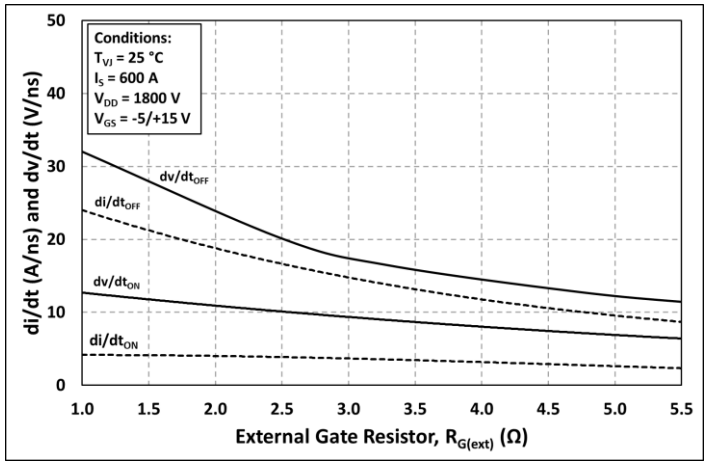


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

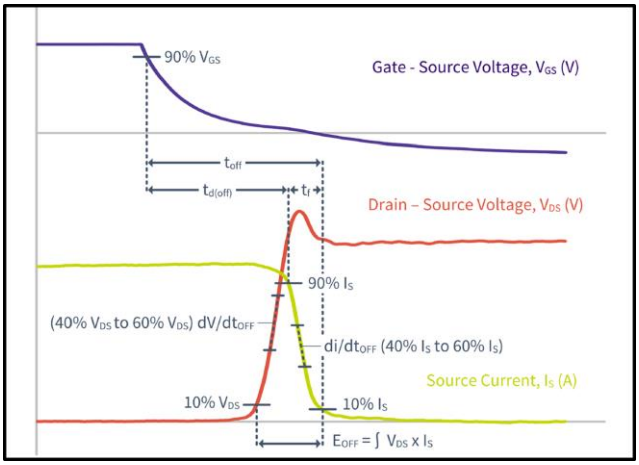


Figure 30. Turn-off Transient Definitions

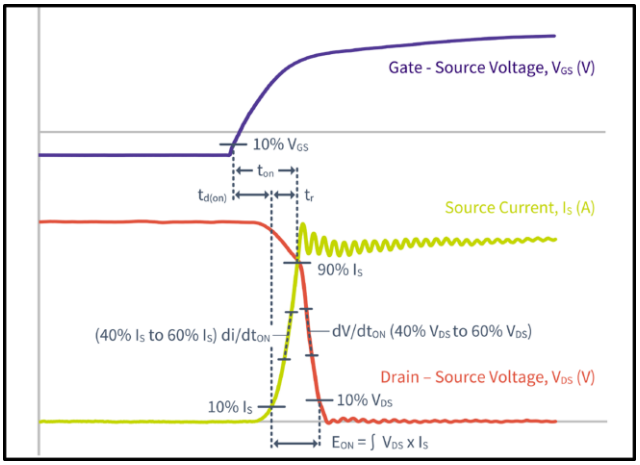


Figure 31. Turn-on Transient Definitions

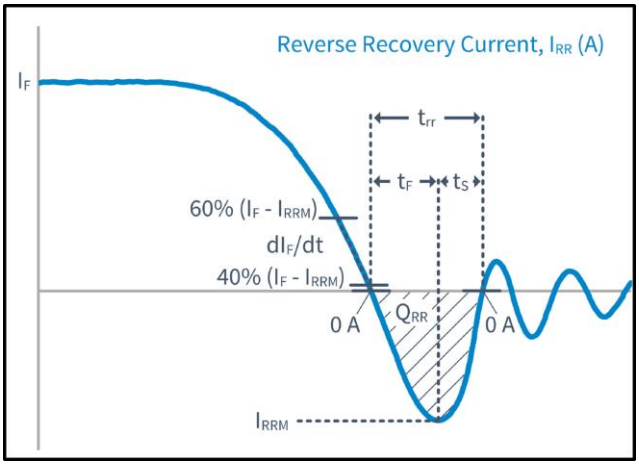


Figure 32. Reverse Recovery Definitions

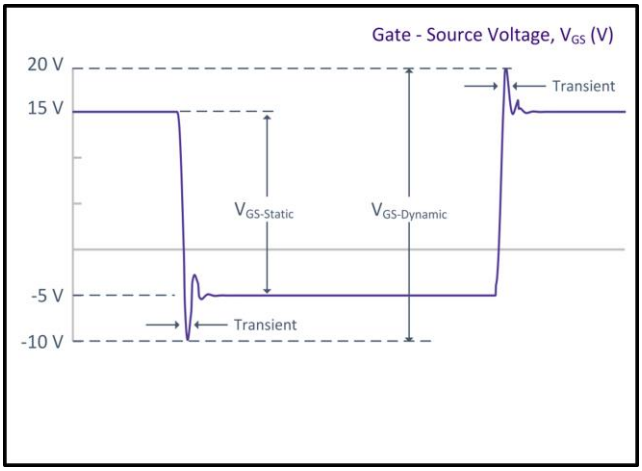
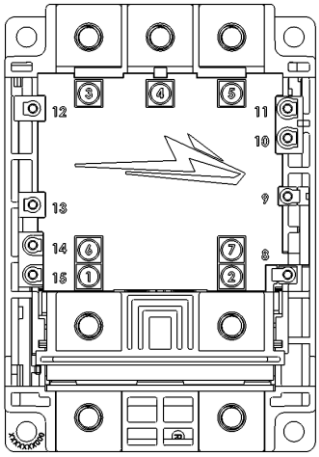
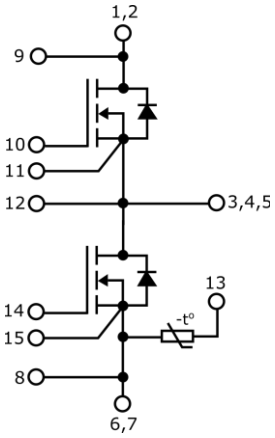
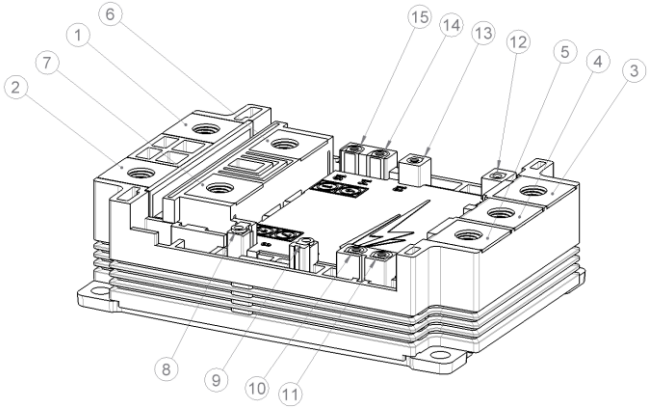


Figure 33. V_{GS} Transient Defintions

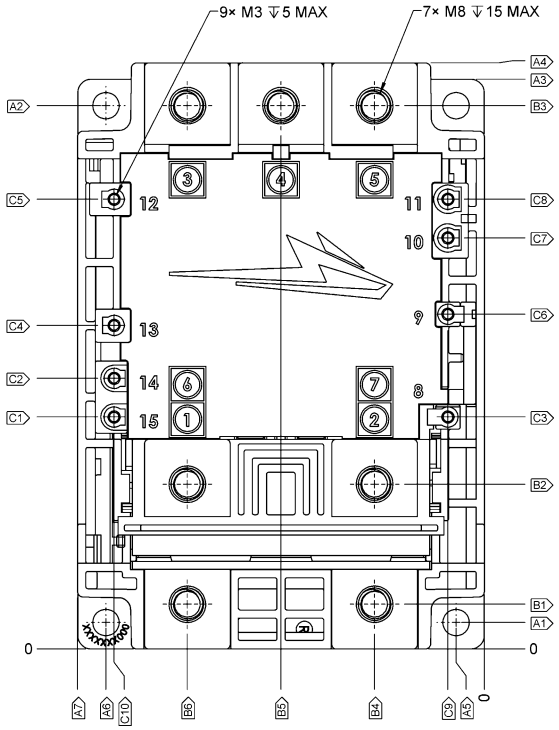
Schematic and Pinout

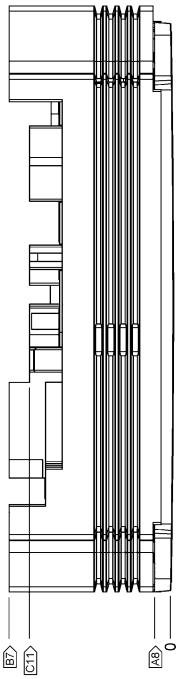






Package Dimensions (mm)





DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	2× 6.5	±1.0
A2	2× 133.5	±1.0
A3	140	±0.75
A4	144	±0.5
A5	2× 7	±0.75
A6	2× 93	±0.75
A7	99.9	±0.5
A8	3.9	±0.3
B1	2× 11	±0.5
B2	2× 40.5	±0.5
B3	3× 133.5	±0.5
B4	3× 27	±0.5
B5	50	±0.5
B6	3× 73	±0.5
B7	39.6	±0.75
C1	57	±0.4
C2	66.5	±0.4
C3	57	±0.6
C4	79.5	±0.4
C5	110.5	±0.4
C6	82.3	±0.5
C7	101	±0.4
C8	110.5	±0.4
C9	4× 9	±0.6
C10	4× 91	±0.6
C11	34.6	±0.75

Supporting Links & Tools

Evaluation Tools & Support

- LTspice and PLECS Models
- KIT-CRD-CIL33N-LM: Dynamic Performance Evaluation for the LM3 Module
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- CGD3300HB6P-LM3: Dual Channel Differential Isolated Half-Bridge Gate Driver Board

Application Notes

- LM Module Signal Pinout Clarification Guide
- LM Module Platform Mounting Guide
- LM3 Thermal Interface Material Application User Guide

Notes & Disclaimers

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