Ahsanullah University of Science and Technology
Department of computer Science and Engineering

Course no : CSE 3117

Course Title: Microprocessor and Microcontroller

Assignment : 01

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Section: B

Ans to the Q. No-1

(i) Given that DS = 0402H

In binary (0000 0100 0000 0010)B

$\therefore$ RRL = $(10)_2 = 2$

here access right = (F2)H

$= (11100010)_2$

$\therefore$ DPL = $(11)_2 = 3$ A

(ii) Ans: RPL is greater or equal to DPL value then privillege segment will allow access ~~or equal to DPL value~~

In there 10 is higher and 11 is lower in privilege level. so the segment is allowed to access.

(iii) Given that, Base = (101010)H, Limit = 00FF

Ending address = Base + limit

= 101010 + 00FF

= (10110F)H A.

Ans to the Q NO- 2

Given that, Selector = 1012 H

0000 EE 101100 FFFF H

Selector in binary: 0001000000010101

here, RPL = 10; DPL = 11

RPL >, DPL

so that the segment can be accessible according to its privilege level.

Base = 101100 H; limit = FFFF H

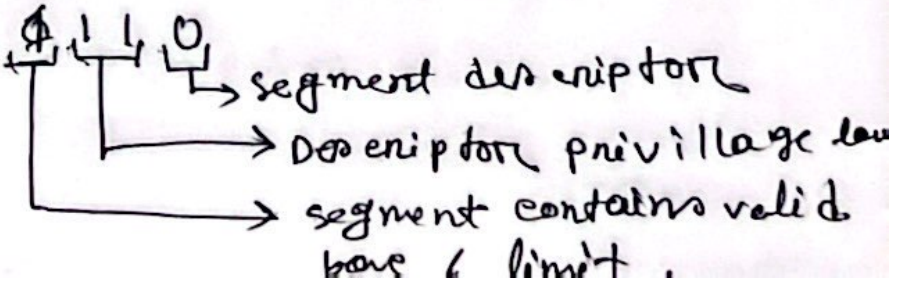
Ending Address = 101100 H
FFFF
111 0FF H.

SA = 101100 H; EA = 1110FF H..

Ans to the Q. NO-3

Access Right = (F6) H

= (1110 0110)



0 → describes data segment

1 → segment expands downwards

1 → segment read/write

0 → Segment not accessed.

Ans to the Q NO-4

→ The LDT selector is a value stored in the LDTR. The LDT selector point to the LDT descriptor without the GDT. The LDT selector is used to index into the GDT and retrive the LDT descriptor. The LDT descriptor in the GDT contains the Base address and limit of the LDT. The structure of the LDT. The structure of the LDT descriptor is similar to the other most of other segment descriptors Base address distribute across the descriptor fields. where Base address is obtained by combining Baselow, Basehigh, Base mid fields.

Ans to Q No. 5

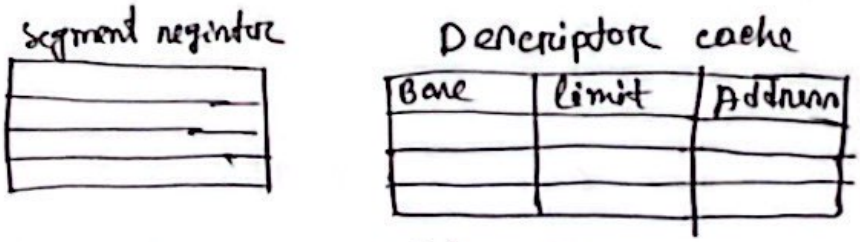
In the flat mode memory addressing the term "40 bit linear address refers to the size of the addressable memory space. The reason for having only 40 bit addressing in some system is due to the specific design and capabilities of processor memory management unit

(i) Processor Design: The width of the address bus in a processor determines the maximum range of memory it can address directly.

(ii) Memory requirement: At the time when certain processor where designed it was not anticipated that system would need to address more than 1TB of memory directly making a 40 bit address space sufficient.

(iii) Efficiency: Using small address space can lead to more effective use of memory and cache resources within the processor.

Ans to the Q: No-6



descriptor table address

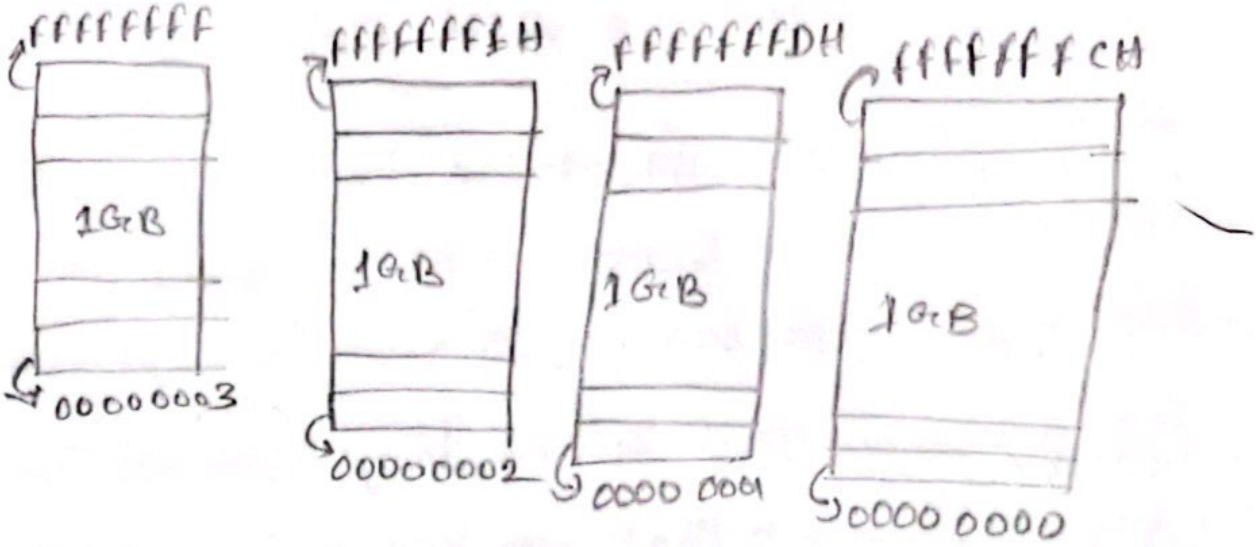
	Address	limit
GDTR	Address	limit
IDTR		

we know that the gobal descriptors contain segment definaton that apply to all programs. registers can access 16 bit. But base address's in grater then 16 bit. That why we use GDT application segments, for locating the starting address one register is used this called GDTR (Global Descriptor table register). This register ~~starting~~ storing starting. base address and limit. Then we can access any discripton for use.

Ans to Q. No. 7

Given that 32 bits data bus and 4 GB memory.

$\frac{32}{8}$ = 4 bank



A memory bank is a unit of memory that can be accessed independently. To optimize the data flow we want to arrange the memory in such a way that allow for the most efficient use of the 32-bit data bus.

Ans to Q. No-8

Given that, Base: 01000000 H

limit: 0FFFFH

when G=1

so the limit = 0FFFFFFF.

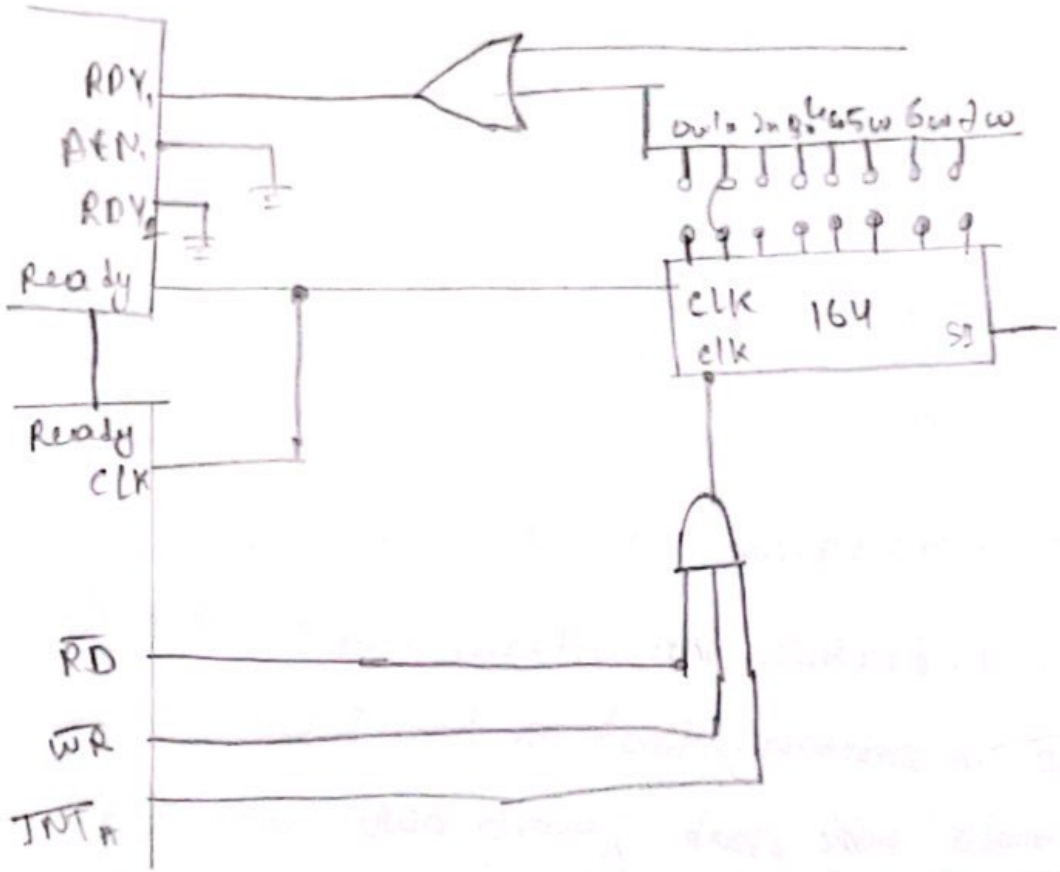
∴ Ending address: (01000000 + 0FFFFFFF) H

= 10FFFFFF A.

Ans to the Q: No-9

→ The ASYNC input selects one stage of synchronization when it is a logic 1 and two stages when it is a logic 0. If one stage is selected, then the RDY signal is kept from reaching the 8086/ 8088 READY pin until the next negative edge of the clock. If two stages are selected, the first positive edge of the clock capture RDY in the first flip-flop. The output of this flip-flop is fed to the second flip-flop. So on the next negative edge of clock, the second flip-flop captures RDY.

Ans to Q.NO 10



A circuit used to introduce almost any number of wait states for the 8086/8088 micro processor. Here an 8-bit serial shift register shift a logic 0 for one or more clock periods from one of the 8 output through to the RDY1 input of the 8284A with appropriate strapping, this circuit can provide various number of wait states.

Notice also how the shift register is cleared back to its starting point. The output of the register is forced high when the $\overline{RD}$, $\overline{WR}$ and $\overline{INTA}$ pin are logic 1. There three signals are high until state T_2. So the shift register shifts for the first time when the positive edge of the T_2 arrives. If any wait is desired, output Q_B is connected to the OR gate. If two waits are desired, output Q_C is connected and so forth. Notice in above figure that this circuit does not always generate wait states. It is enable from the memory only. For memory device that require the insertion of waits. If the selection signal from a memory device is a logic 0, the device is selected then the circuit will generate a wait state.