Ahsanullah University of Science & Technology

Department of computer Science & Engineering

Course no : CSE 3117

Course Title : Microprocessor & microcontroller

Assignment : 01

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section : B

1. Use the value of DS=0402H register and the descriptor (in Hex code) information given in Table I to answer the question

Table I: Descriptor Table

0000	E2	10
1010	00FF	

32 16 15 0

(i) Illustrate the value of Request privilege Level (RPL) and Descriptor Privilege Level (DPL)

$DS = 0402H$

$= (0000\ 0100\ 0000\ 0010)\ B$

$\therefore RRL = (10)_2 = 2$

Access right $= (E2)\ H$

$= (1110\ 0010)_2$

$\therefore DPL = (11)_2 = 3$

(ii) Is the segment allowed to access?

As RPL is greater in Privillege segment will allow access.

(iii) Calculate the starting and ending memory address in a protected mode of the 80286-microprocessor system.

=>

Starting address = Base = $(101010)_H$

ending " = Base + limit

= 101010 + 00FF

= $(10110F)_H$

(2) Find out the segment starting and Ending Address, and whether the segment can be accessible according to its privilege level.

Descriptor Information (64 bits): 0000 EE 101100 FFFF H

Selector: 1012H

=> DPL is the 6th and 5th bit of access Right.

Access right = $(EE)_{16}$

= 1110 1110

∴ DPL = 11

Selector = $(1012)_{16}$

= $(0001\ 0000\ 0001\ 0010)_2$

RPL = 10

As RPL > DPL in Privilege, the segment can be accessible.

Base is the starting Address,

$\therefore$ Starting Address $= (101100)_{16}$

given limit $= (FFFF)_{16}$

$\therefore$ Ending Address $= (101100 + FFFF)_{16}$

$= (111 0FF)_{16}$

(3) ~~Explain~~ An 80286 microprocessor has 64-bit descriptors. The information is as follows:

0000 E6 to 1000 FFFF

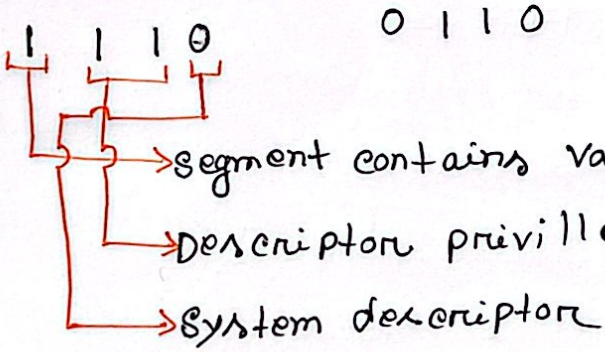
Explain the Access Right bits.

=>

Access Right = (E6) H

= (1110 0110)

0 1 1 0



0 → describes data segment

1 → segment expands downwards

1 → segment may read/write

0 → segment not accessed.

④ Explain the way to locate the starting address of the local Descriptor Table (LDT).

⇒ ~~The local~~ To locate LDT starting address ~~lets~~ we have to follow these steps:

1) Identify the LDT selector: The LDT selector is a value stored in the LDTR. The LDT selector points to the LDT descriptor within the GDT.

2) Retrive the LDT Desoriptor from the GDT: The LDT selector is used to index into the GDT and retrive the LDT descriptor.

3) Extract the base address and limit from the LDT Descriptor: The LDT descriptor in the GDT contains the Base address and limit of the LDT. The structure of the LDT. The structure of the LDT descriptor is similar to that of other segment descriptors. Base address distributed across the descriptor fields. where Base address is obtained by combining Baselow, Base mid and Base high fields. Limit is obtained by combining limit low and limit high and considering the granularity bit.

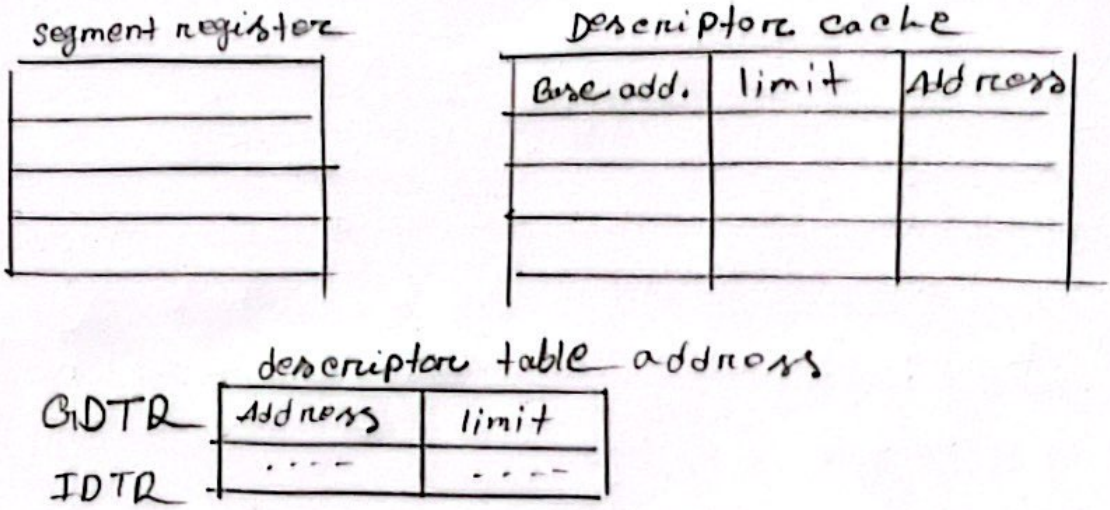
(5) Why are there only 40 bits linear address in flat mode memory addressing? Explain.

=> The memory system in a pentium-based computer that uses the 64-bit extensions uses a flat model memory system. A flat model memory system is one in which there is no segmentation. The address of the first byte in the memory is at 00 0000 0000H and the last location is at FF FFFF FFFFH (address is 40 bits). The flat model does not use a segment register to address a location in the memory. The CS segment register is used to select a descriptor from the descriptor table that defines the access rights of only a code segment.

In Summary, the 40-bit linear address in flat mode memory addressing are a result of the architectural choices made in the design. While the full 64-bit range provides a theoretical maximum, practical implementation and current technology constraints limit physical addressing to 40 bits. This provides a substantial memory space while keeping the system design feasible and efficient.

6. Explain the way to locate the starting address (base limit) of the Global Descriptor Table (GDT)

⇒ The gobal descriptors contain segment defination that apply to all programs.

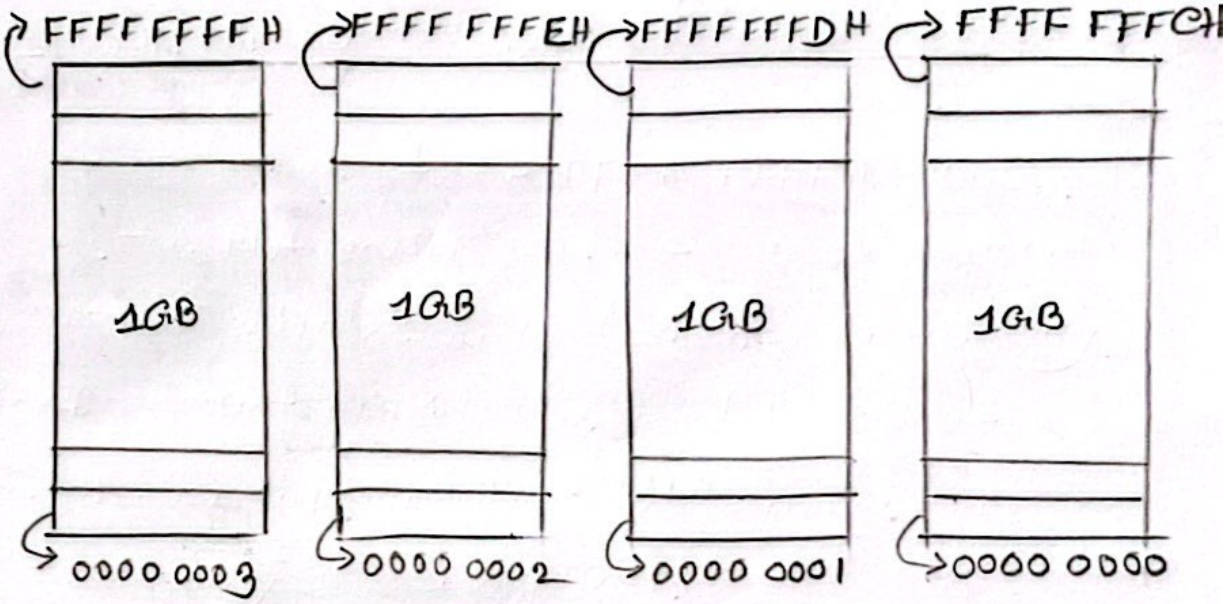


we know that our registers are 16 bit. but the base address is greter then 16 bit, so, we can not access the base address in register. So. we use GDT storing applications segment. for locating the starting address one register is used. It's called GDTR (Global Descriptor table register). This register Store base address and limit. then we can access any descriptor now for use.

(7.) 80386 DX has 32 bits data bus and 4GB memory. How many banks of memory will be optimized the data flo between microprocessor and memory system. Explain your ans

⇒

$$\frac{32}{8} = 4 \text{ bank}$$



A memory bank is a unit of memory that can be accessed independently. To optimize the data flow, we want to arrange the memory in such a way that allows for the most efficient use of the 32-bit data bus. Each bank should be able to provide 32 bits of data to match the width of the data bus.

(8) A core 2 descriptor contains a base address of 01000000, a limit of OFFFFH, and G=1, what are the starting and ending locations addressed by descriptor

=> Descriptor has:

Base: 01000000H

and limit = OFFFFH

when, G=1

append limit in descriptor by FFFH

so, actual limit = OFFFFFFFH

So, starting location address = 01000000H

and ending " " = (01000000+OFFFFFFF)H

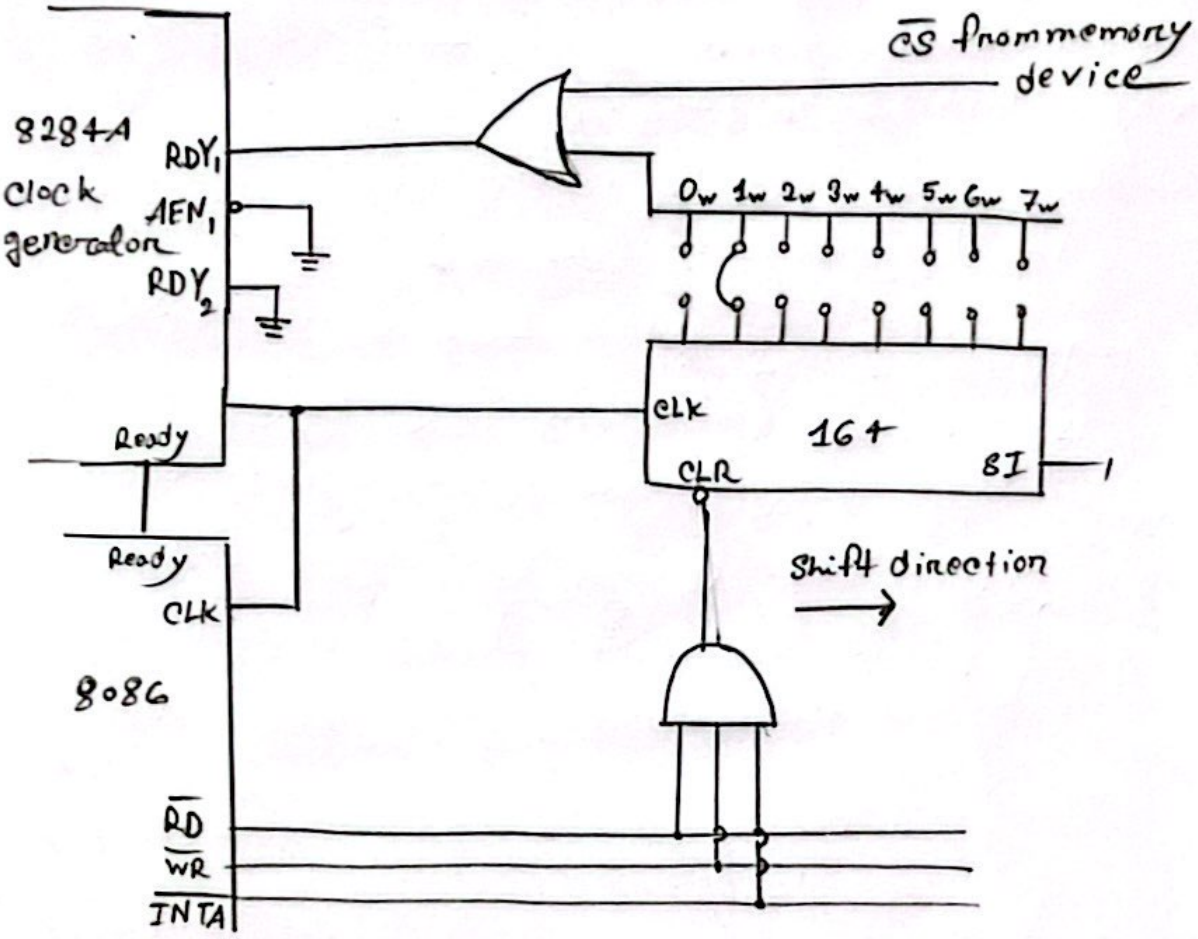
= 10FFFFFFH

(9). Explain the activity of the ASYNC signal to generate READY synchronization circuit in 8086.

=> The ASYNC input selects one stage of synchronization when it is a logic 1 and two stages when it is a logic 0. If one stage is selected, then the RDY signal is kept from reaching the 8086/8088 READY pin until the next negative edge of the clock. If two stages are selected, the first positive edge of the clock capture RDY in the first flip-flop. The output of this flip-flop is fed to the second flip-flop. So, on the next negative edge of clock, the second flip-flop captures RDY.

10. Explain the activity of the Shift Register (LS164) to generate the number of wait states.

⇒



Above figure illustrates a circuit used to introduce almost any number of wait states for the 8086/8088 micro processors. Here, an 8-bit serial shift register (74LS164) shift a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A. with appropriate strapping, this circuits can provide various numbers of wait states. Notice also how the shif register is cleared back to its starting point. The output of the register is forced high when the $\overline{RD}$, $\overline{WR}$ and $\overline{INTA}$ pins are all logic 1. These three

signals are high until state T_2, so the shift register shifts for the first time when the positive edge of the T_2 arrives. If one wait is desired, output Q_B is connected to the OR gate. If two waits are desired, output Q_C is connected and so forth.

Notice in above figure that this circuit does not always generate wait states. It is enabled from the memory only for memory device that require the insertion of waits. If the selection signal from a memory device is a logic 0, the device is selected; then the circuit will generate a wait state.