MCA SEMESTER-I
School of Computer and Systems Sciences,
Jawaharlal Nehru University,
New Delhi -110067
DIGITAL LOGIC (CS-181) Mid-I

Total Marks: 20 **Date: 11.09.2019** **Time: 2hrs**

All Compulsory

1. a) By means of a timing diagram similar to Fig. 1(a), show the signals of the outputs f and g in Fig.1(b) as functions of the inputs a, b and c.

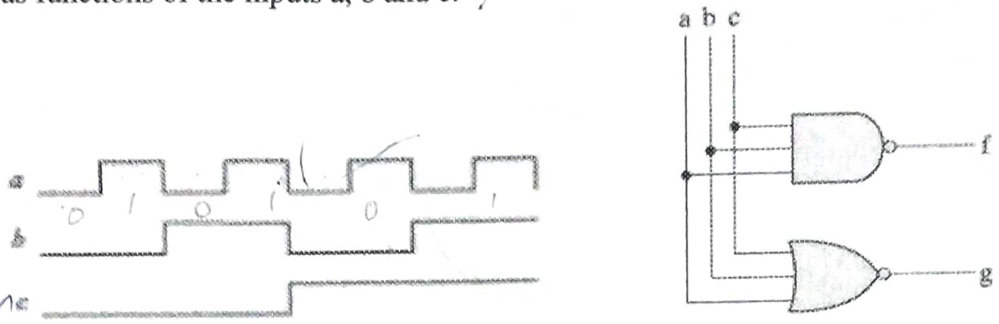

Figure 1: a) Input waveform signals b) Logic circuit

b) Convert the decimal number 431 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal and then from hexadecimal to binary. Which method is faster? 4

2. a) Write the Boolean equations and draw the logic diagram of the circuit whose outputs are defined by the following truth table:

a	*b*	*c*	f_1	f_2
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	1	1	0

b) Simplify the following Boolean function *F*, together with the don't-care conditions *d*, and then express the simplified function in sum-of-minterms form: 4

$F(A, B, C, D)=\Sigma(0,6,8,13,14)$
$d(A, B, C, D)= \Sigma(2,4,10)$

3. Design and implement even parity generator. 4
4. Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority. 4
5. Design and implement full adder. 4