

Assignment

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1. Consider the *D*-Latch shown in the figure, which is transparent when its clock input *CK* is high and has zero propagation delay. In the figure, the clock signal *CLK1* has 50% duty cycle and *CLK2* is a one fifth period delayed version of *CLK1*. The duty cycle at the output of the latch in percentage is.

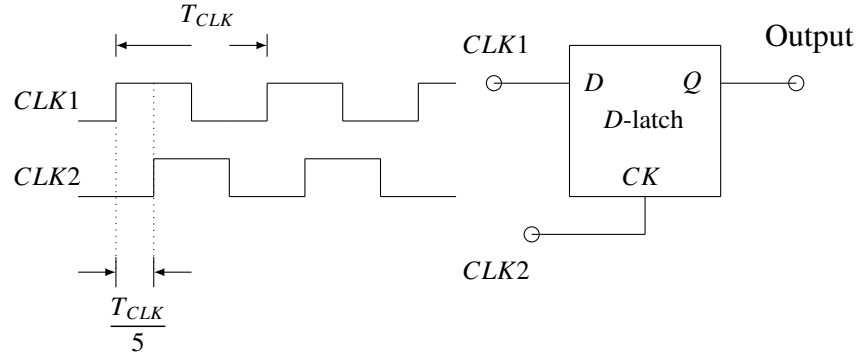


Figure 1