HELIX Master Trigger Review

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Overview

- General function
- Clocks/crystals
- Interfaces
- Power consumption
- Layout
- Physical information
- Enclosure

General functions

1. System clock generation
   - 40 MHz VCTCXO TTEAALJANF-40.000000, +/-2 ppm accurate, +/-0.28 ppm over temperature, can be steered by FPGA PWM output
   - Overall timing from PPS (IRIG?)
   - Fanout: Si5395 12-clock fanout
     - 40 MHz to 10 ToF outputs (1 spare)
     - 40 MHz to FPGA
     - 80 MHz to Si53307 2-clock fanout (system clock + MGT clock)

2. Two-level (ZLO/ZHI) master trigger formation
   - 2 inputs from each ToF readout (10 total, 1 spare)
   - 5 connectors (Mini-SAS 4i), 2 ToF readouts each
     - Bore paddle trigger can be delayed using IDELAYs up to ~20 ns (unused inputs)
     - All trigger inputs into same I/O bank
   - External trigger SMA input

3. Asynchronous trigger fanout to RICH
   - Variable output delay possible via IDELAY fabric chain (up to ~40 ns, 78 ps resolution or better)
   - Also trigger SMA output

4. Run control to mergers
   - Clock, sync, trigger, and run control on Mini-SAS HD external outputs (x6, 2 spare)
   - 2 outputs have gigabit links as well (nominally unneeded)

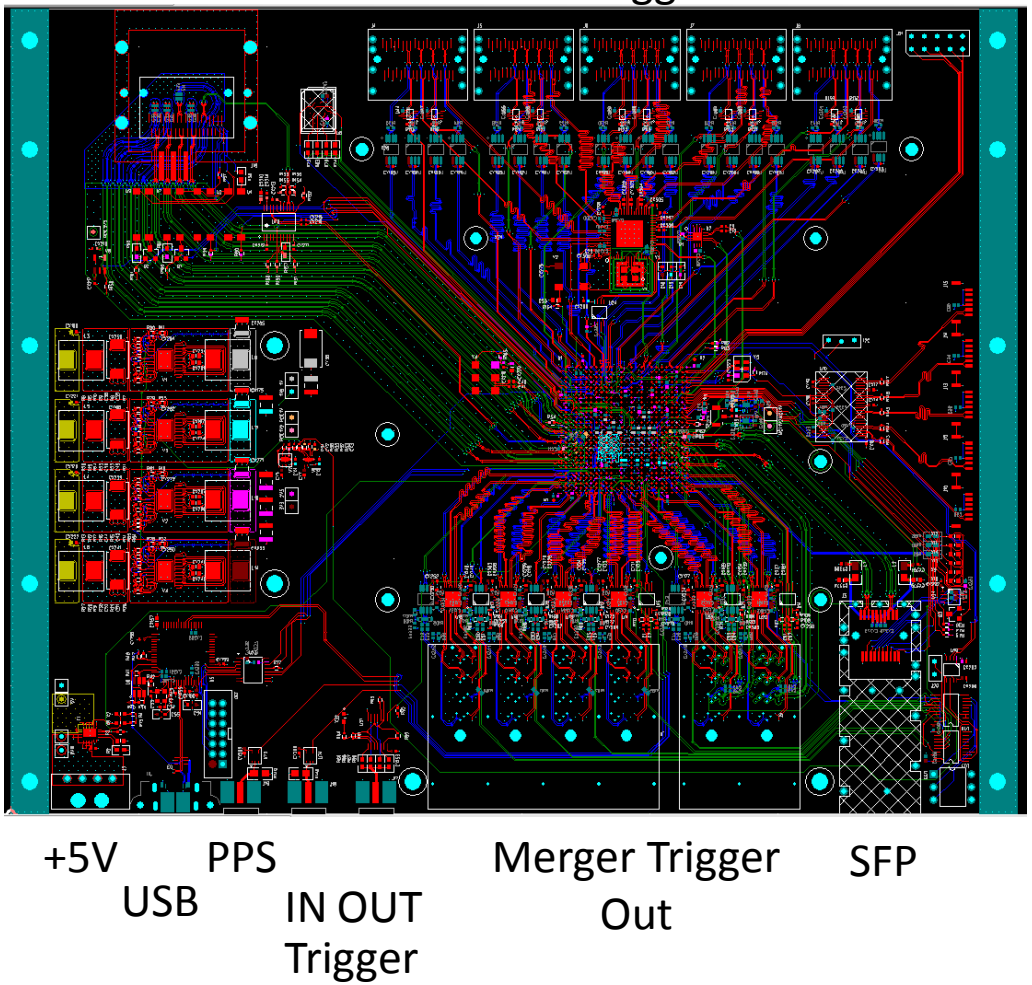
5. Event trigger information and status to flight computer via SFP link to master merger

Onboard clocks/crystals

- 40 MHz VCTCXO (turned into 40 MHz ToF and 80 MHz system)
- 48 MHz reference crystal
- 200 MHz FPGA local clock (can be disabled)
- 100 MHz PCIe auxiliary clock (can be disabled)
- 12 MHz USB crystal (will be disabled if not connected)

Interfaces

- 5x dual ToF trigger inputs (Mini-SAS 4i)
- 6x merger trigger outputs (Mini-SAS HD external)
- SFP transceiver
- ATRG outputs
- External PCIe x4 (debug)
- USB (JTAG debug)
- External trigger in/out
- PPS (IRIG?) input
- Spare GPIOs



Power consumption

- Non-FPGA primary components: ~8 W
  - FPGA should be ~2.5 W for flight (1 MGT link only), so ~10 W reasonable, ~15 W solid upper limit
  - 1W max extra if SFP is active
  - Power is pretty distributed, no serious hotspots
    - May need heatsinking on both top and bottom, though
- Debugging components power down for flight
  - When *all on*: ~3W extra expected, ~5W solid upper limit
  - Total upper limit ~ 20W
  - Input power e-fused (TPS25940) at 5A (25W)

Layout information

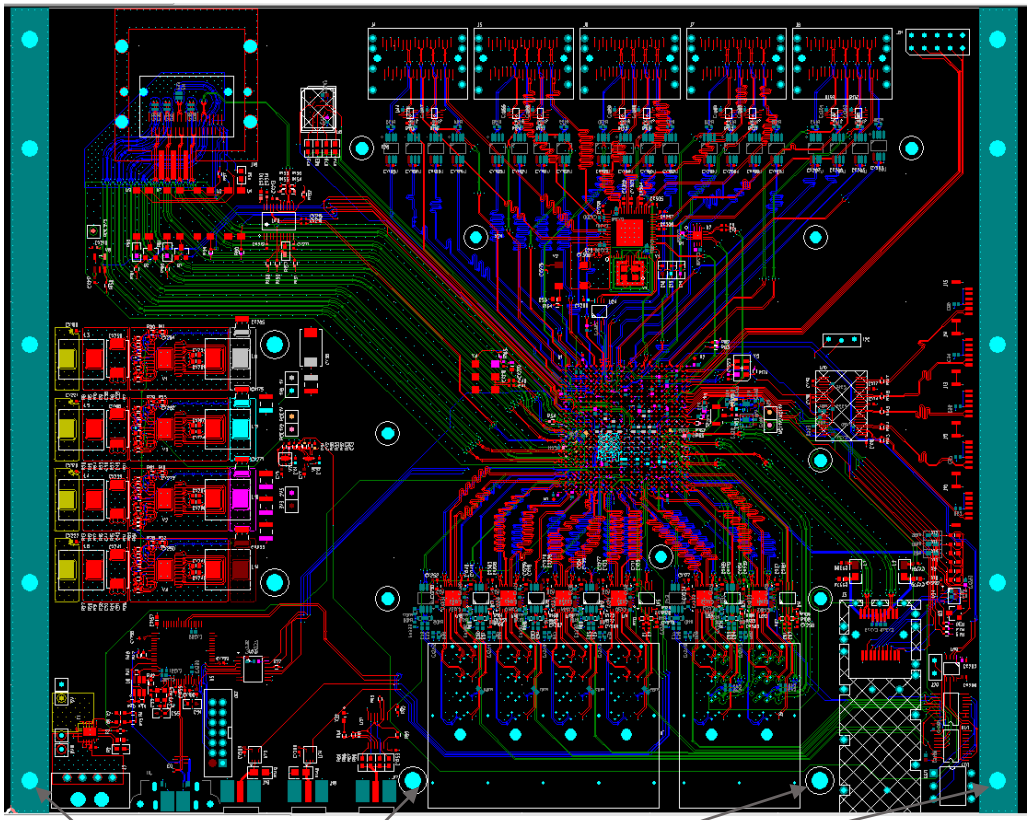
- 8-layer PCB, 3 signal layers (top/shielded stripline/bottom), 2 power layers, 3 ground layers
- MGT links (mostly) on shielded stripline
- Average (4/4) design rules, should be buildable at several fab houses
- Fiducial marks for FPGA BGA

Physical information

Screw mounts for panel mounting

Mounting holes along edges to attach board to carrier

Carrier slides into enclosure



4-40 screw mounts for front panel mounting (using angle bracket)

Physical enclosure

Heat transfer either through rails or back panel

Carrier slides into rails, board is mounted onto carrier

ATRG/trigger inputs are connected to bulkhead connector via cables