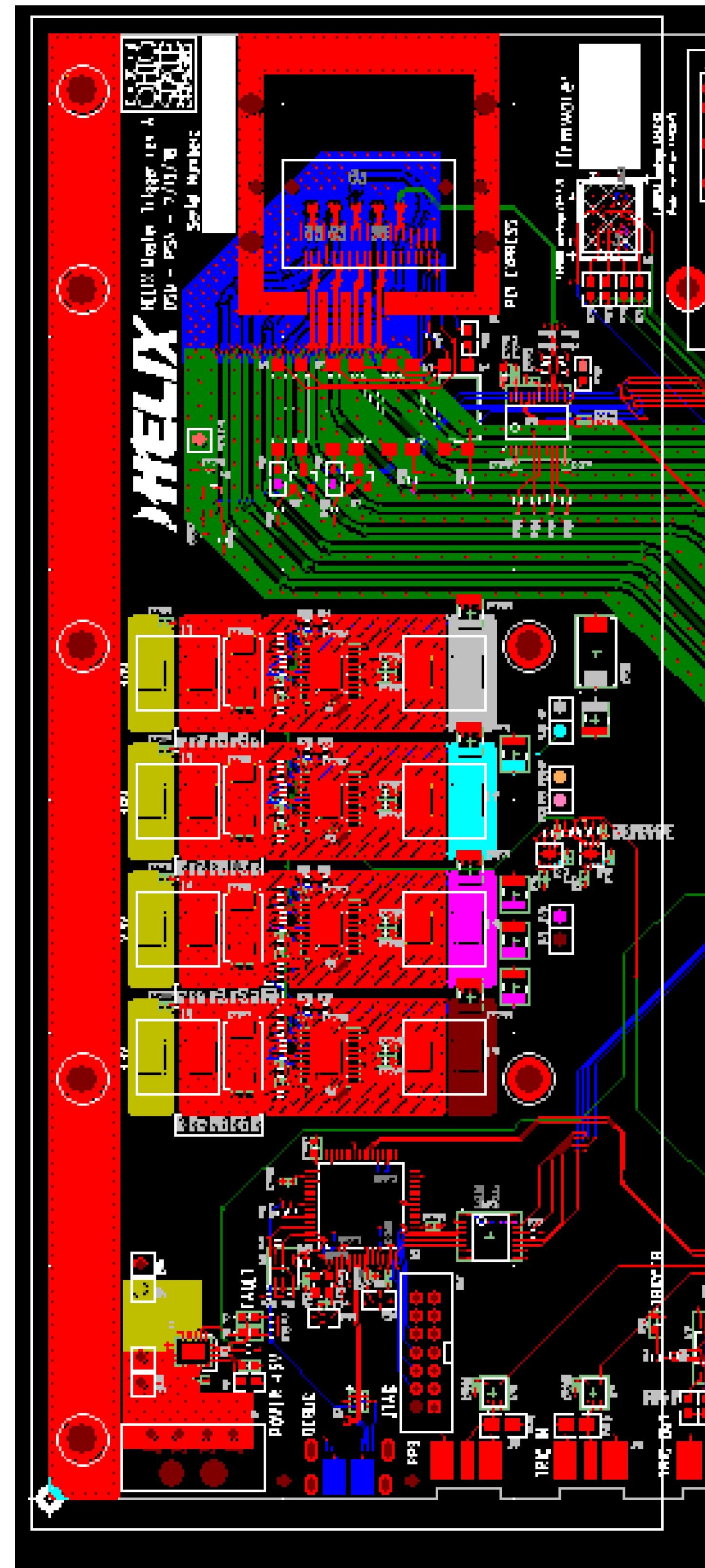
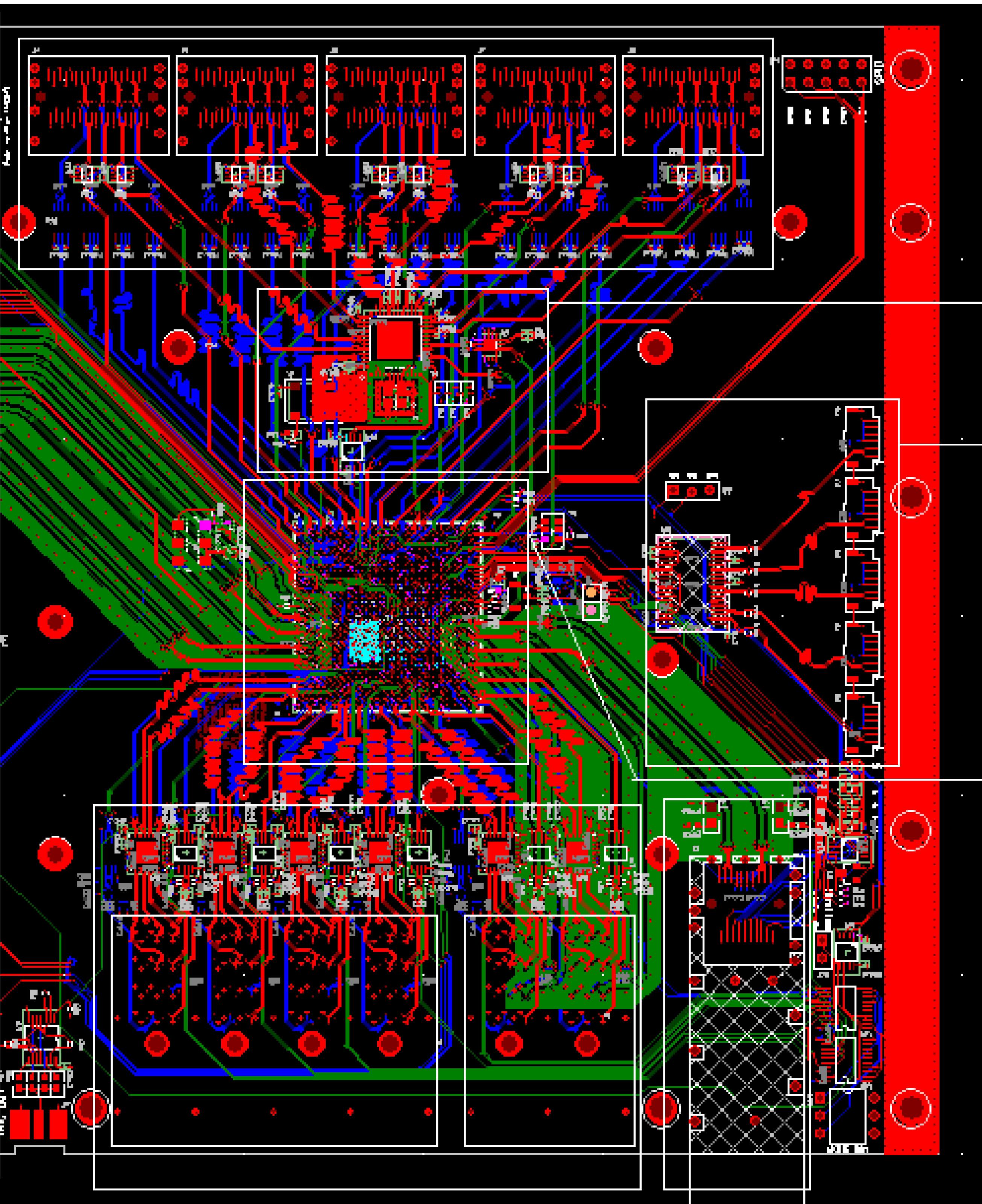


POWER_DEBUG (Sheet 8)



TRIGGER_OUT (Sheet 2) SFP (Sheet 4)

TRIGGER_IN (Sheet 7)



FPGA_IO (Sheet 6) ATRG (Sheet 5) Clock (Sheet 3)

Layer Stackup:

8 Layer Stack-up						
Layer Order	Layer Name	Material Type	Material Description	Dielectric Constant	Thickness	Copper Weight
1	Top	Copper	Signal	4.2	0.0014"	1 oz
		1080 (2 sheets)	Prepreg	4.2	0.0059"	
2	Inner 1	Copper	Plane	4.2	0.0014"	1 oz
		Core	Core	4.2	0.009"	
3	Inner 2	Copper	Plane	4.2	0.0014"	1 oz
		7628	Prepreg	4.2	0.0073"	
4	Inner 3	Copper	Plane	4.2	0.0014"	1 oz
		Core	Core	4.2	0.0051"	
5	Inner 4	Copper	Plane	4.2	0.0014"	1 oz
		7628	Prepreg	4.2	0.0073"	
6	Inner 5	Copper	Plane	4.2	0.0014"	1 oz
		Core	Core	4.2	0.009"	
7	Inner 6	Copper	Plane	4.2	0.0014"	1 oz
		1080 (2 sheets)	Prepreg	4.2	0.0059"	
8	Bottom	Copper	Signal	4.2	0.0014"	1 oz

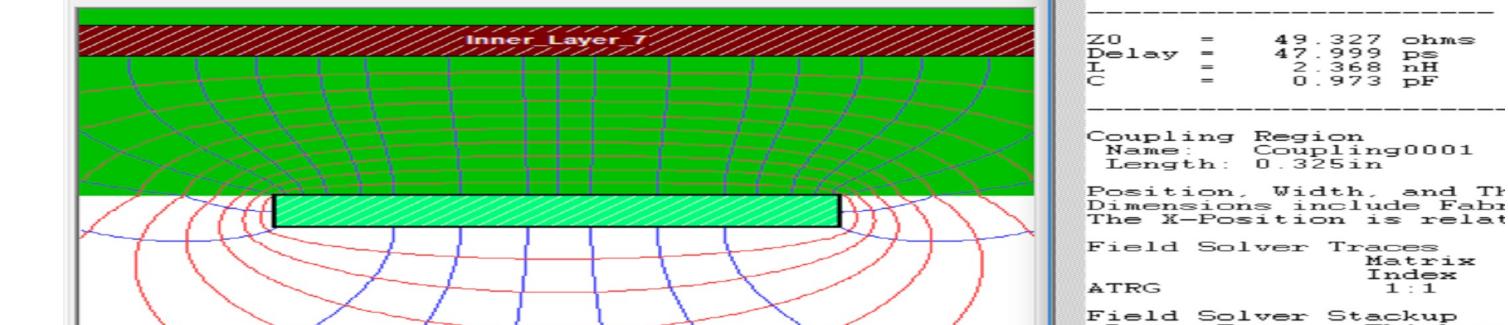
Final board thickness: 0.062" ± 10%

Top/Bottom 50 ohms: 10 mils

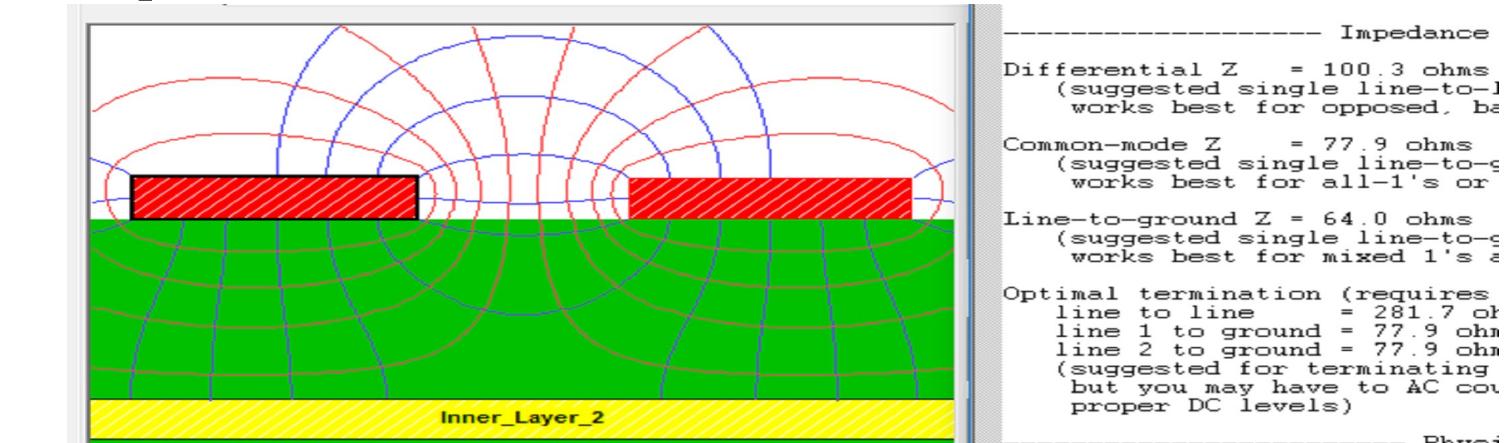
Top/Bottom 100 ohms differential: 6.3/4.7 trace/space

Layer 3 100 ohms differential: 4/7 trace/space

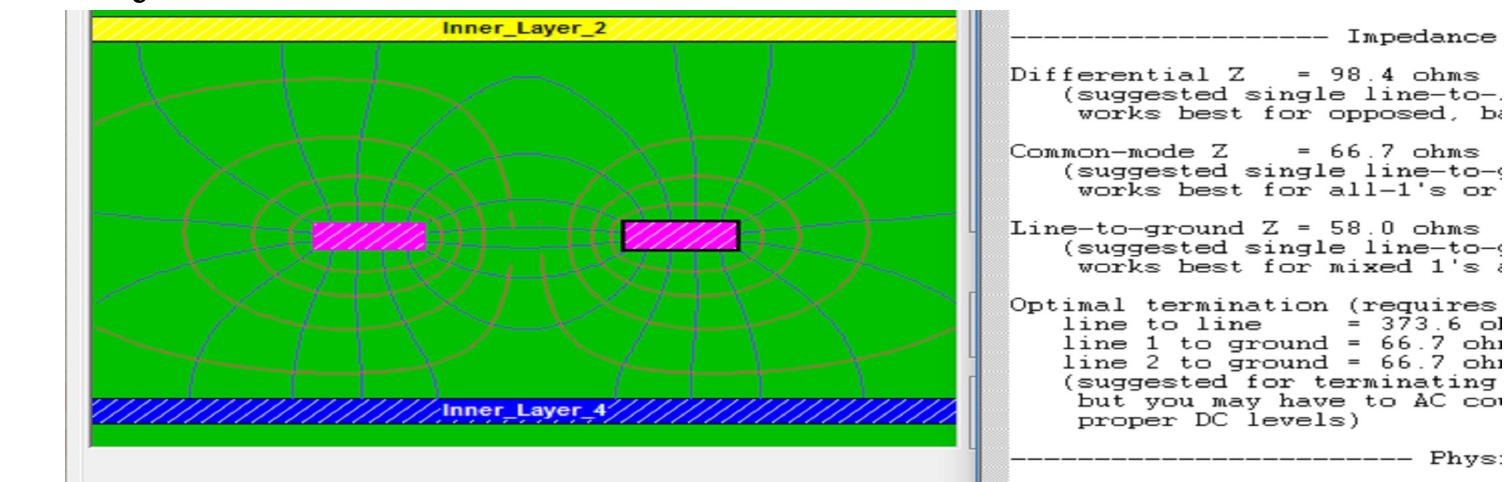
Top/Bottom single-ended 50 ohms:



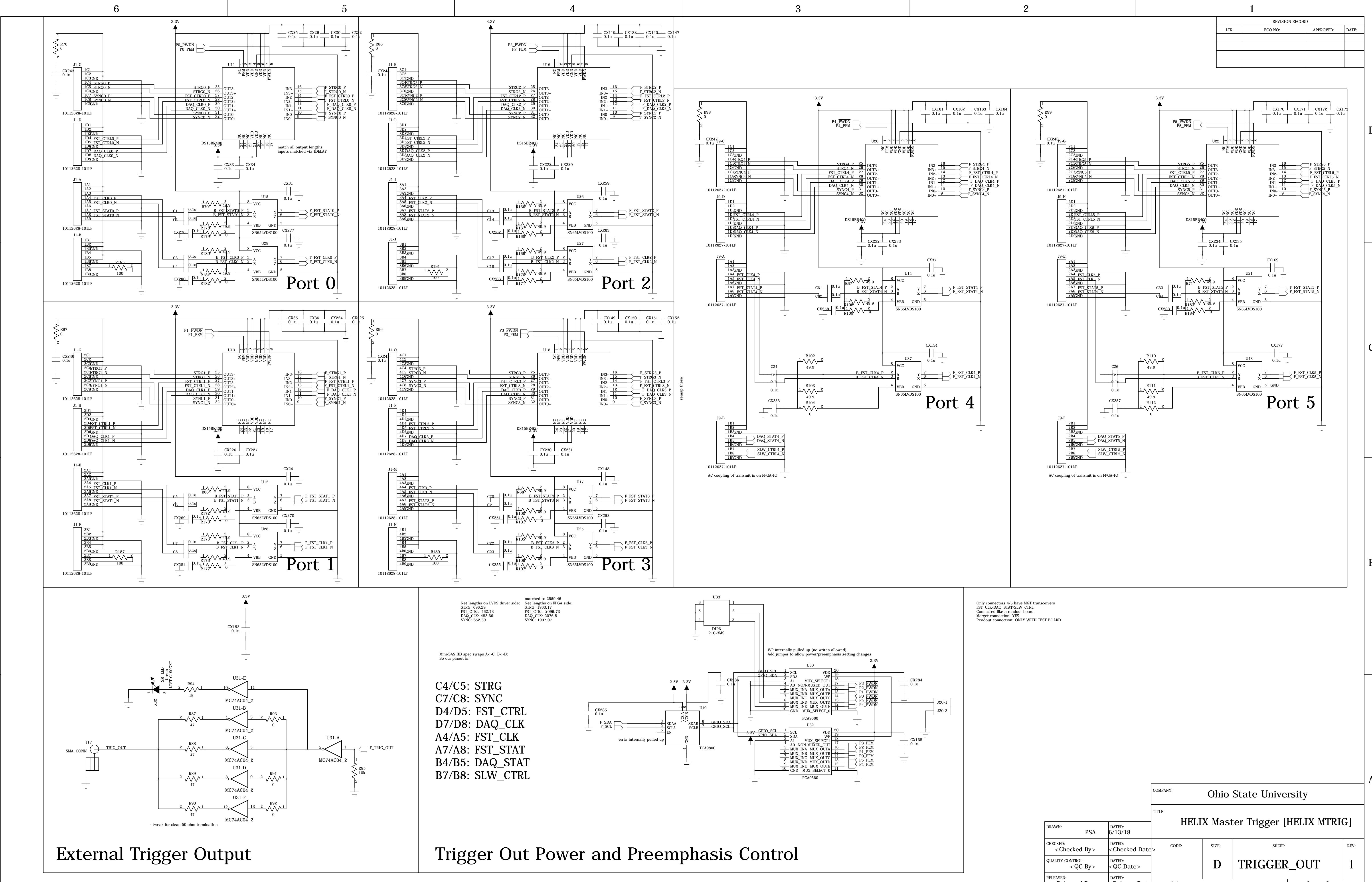
Top/Bottom differential 100 ohms:

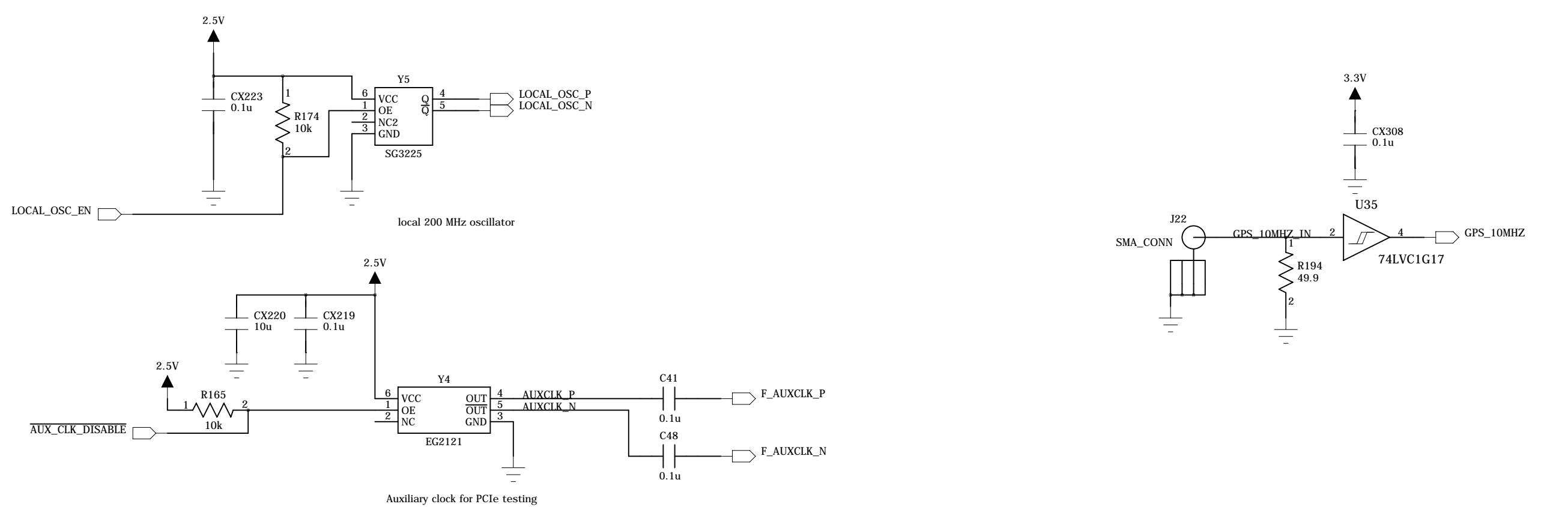


Layer 3 differential 100 ohms:

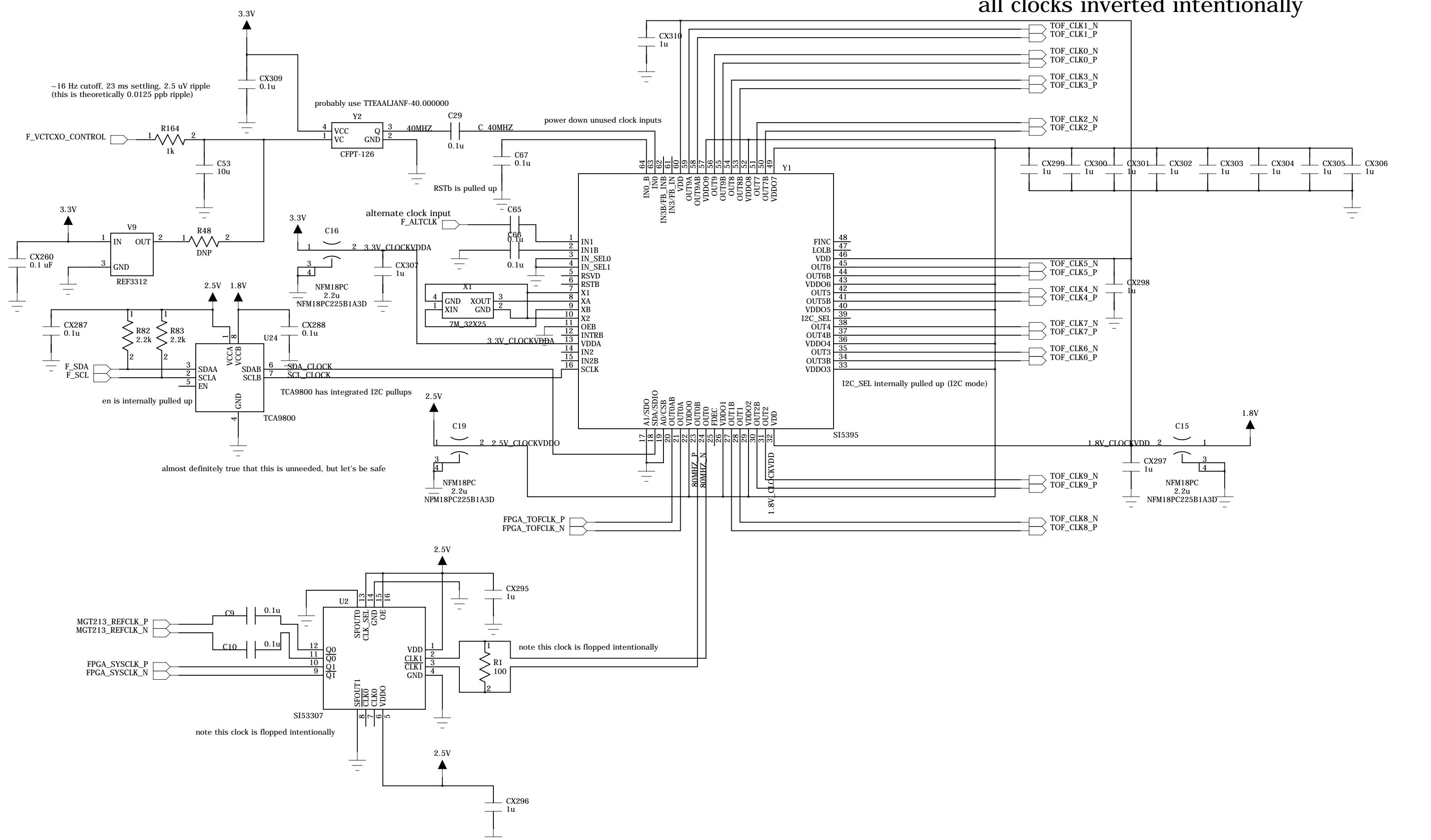


COMPANY:	Ohio State University		
TITLE:	HELIX Master Trigger [HELIX MTRIG]		
DRAWN:	PSA	DATED:	6/13/18
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>
SCALE:	1:1		
SHEET:	1 OF 8		





all clocks inverted intentionally



		COMPANY: Ohio State University			
		TITLE: HELIX Master Trigger [HELIX MTRIG]			
DRAWN: PSA	DATED: 6/13/18	CODE: D	SIZE: CLOCK	SHEET: 1	REV: 1
CHECKED: <Checked By>	DATED: <Checked Date>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>				
		SCALE: 1:1	SHEET: 3 OF 8		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

D

C

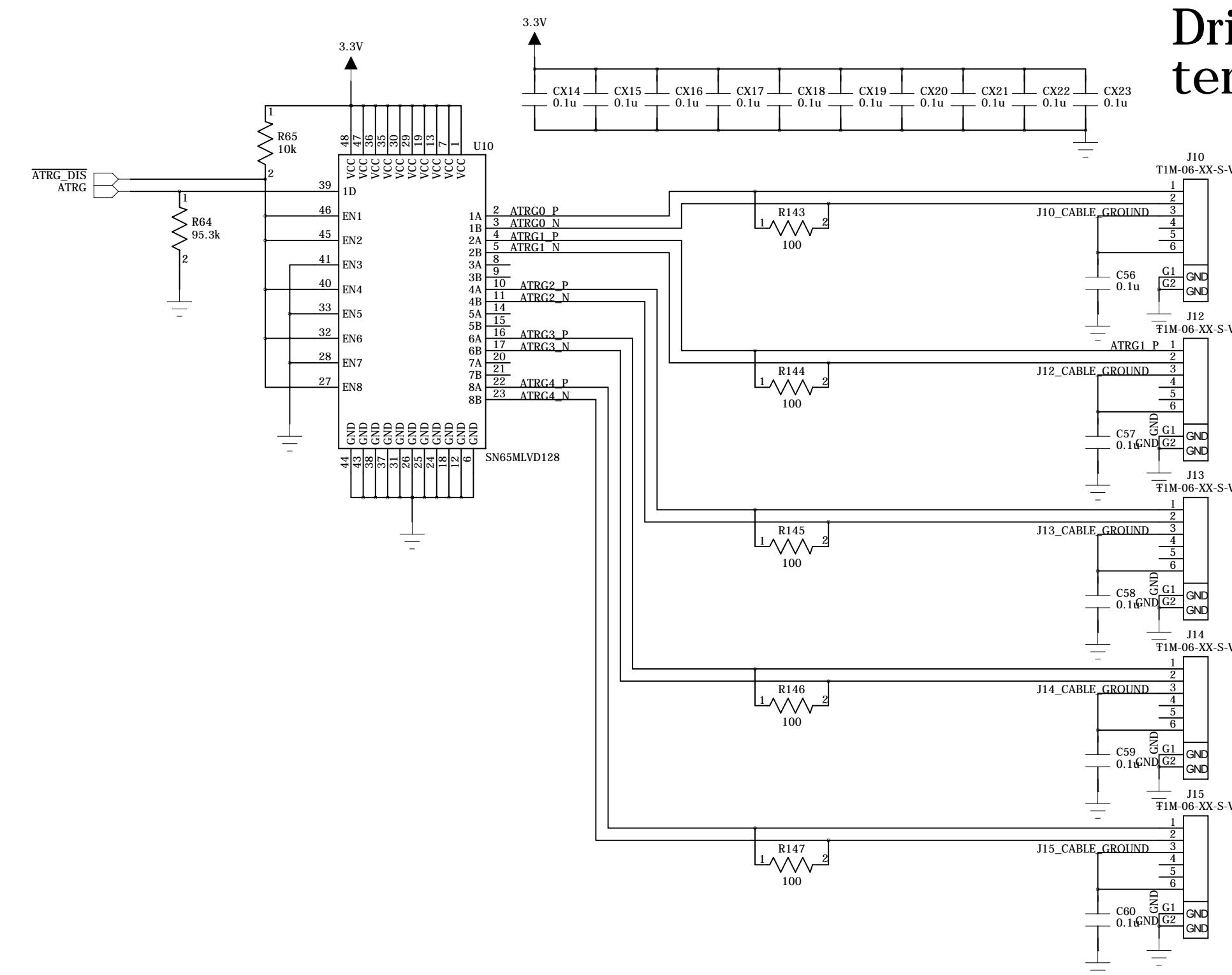
C

B

B

A

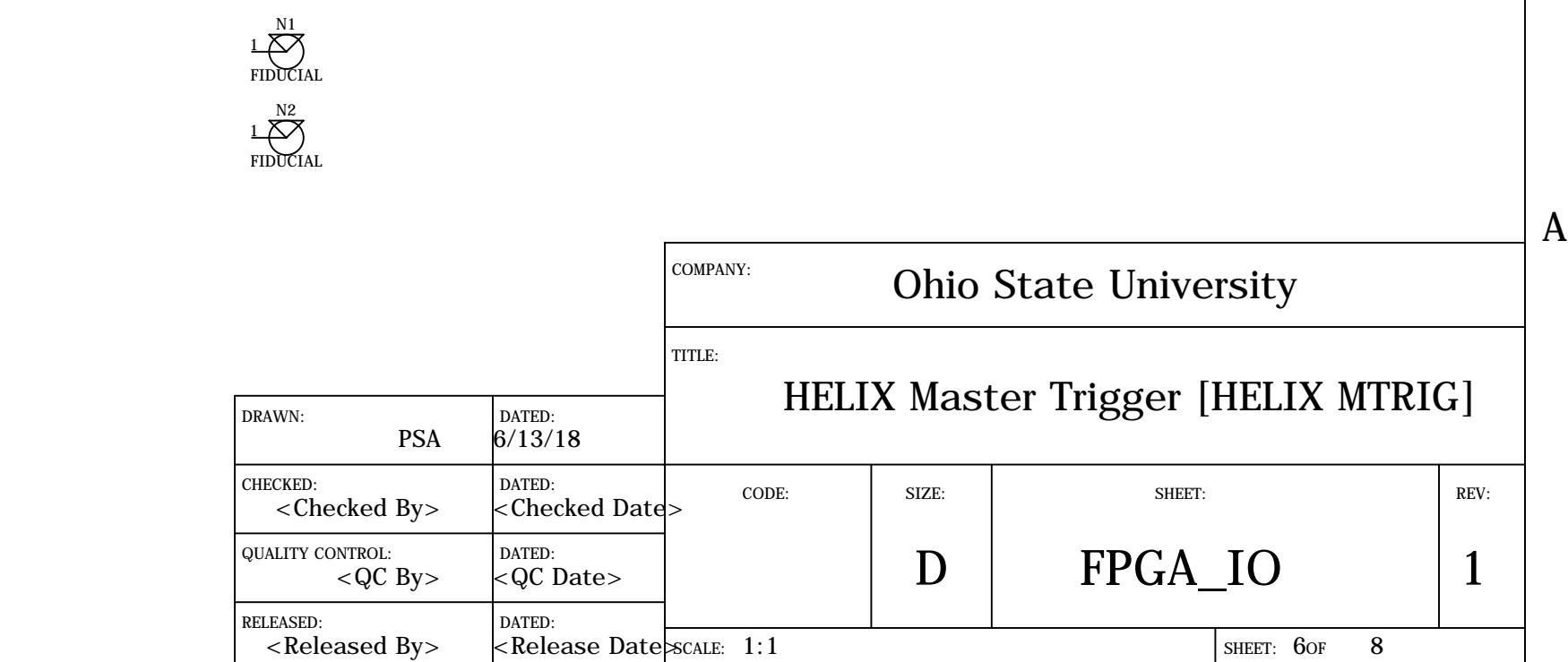
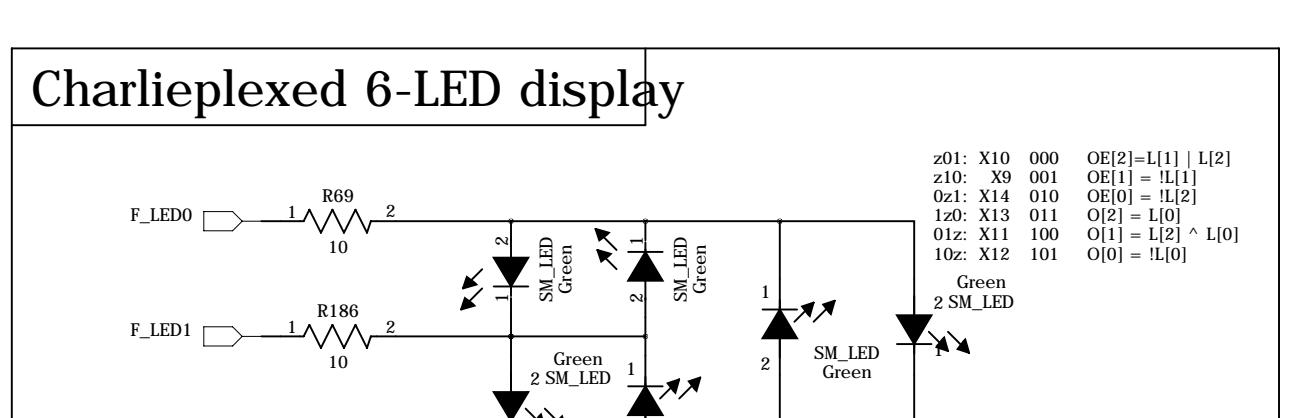
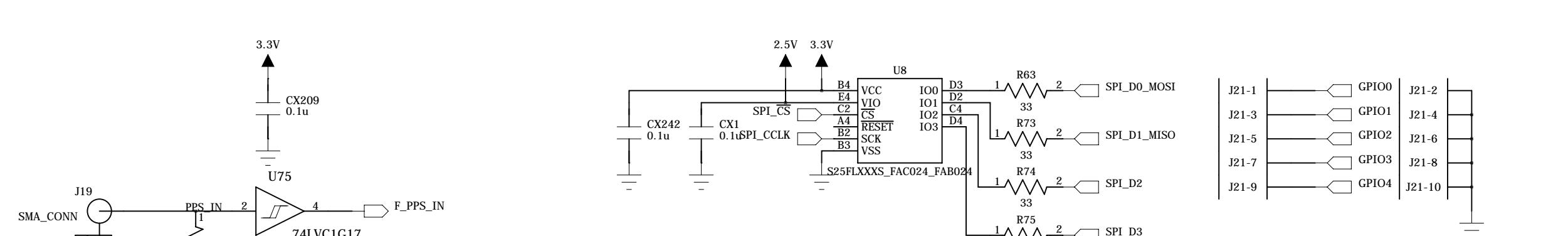
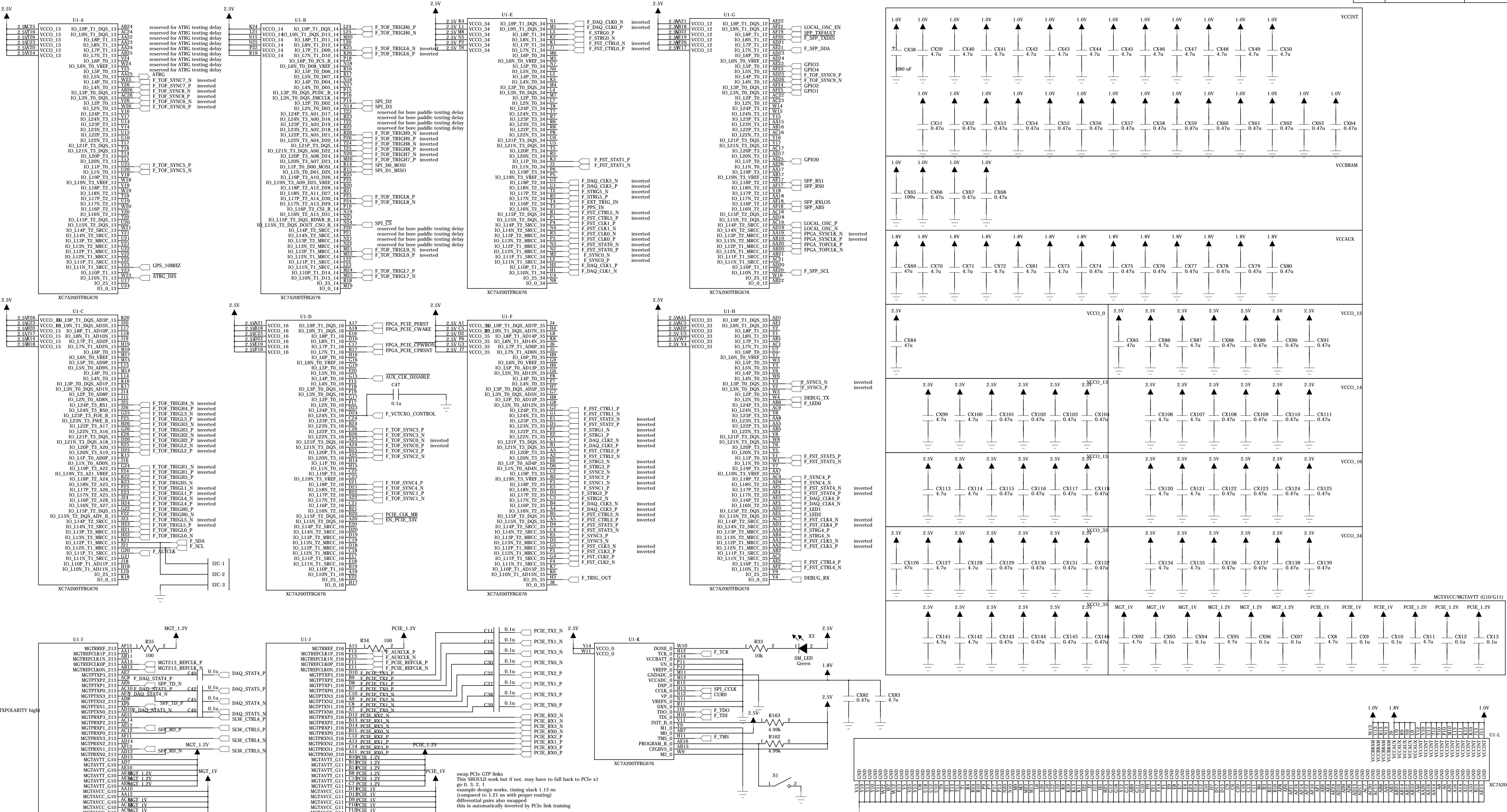
A



Drive only pins 1/2
terminate 100 ohms at beginning/end to meet LVDS spec

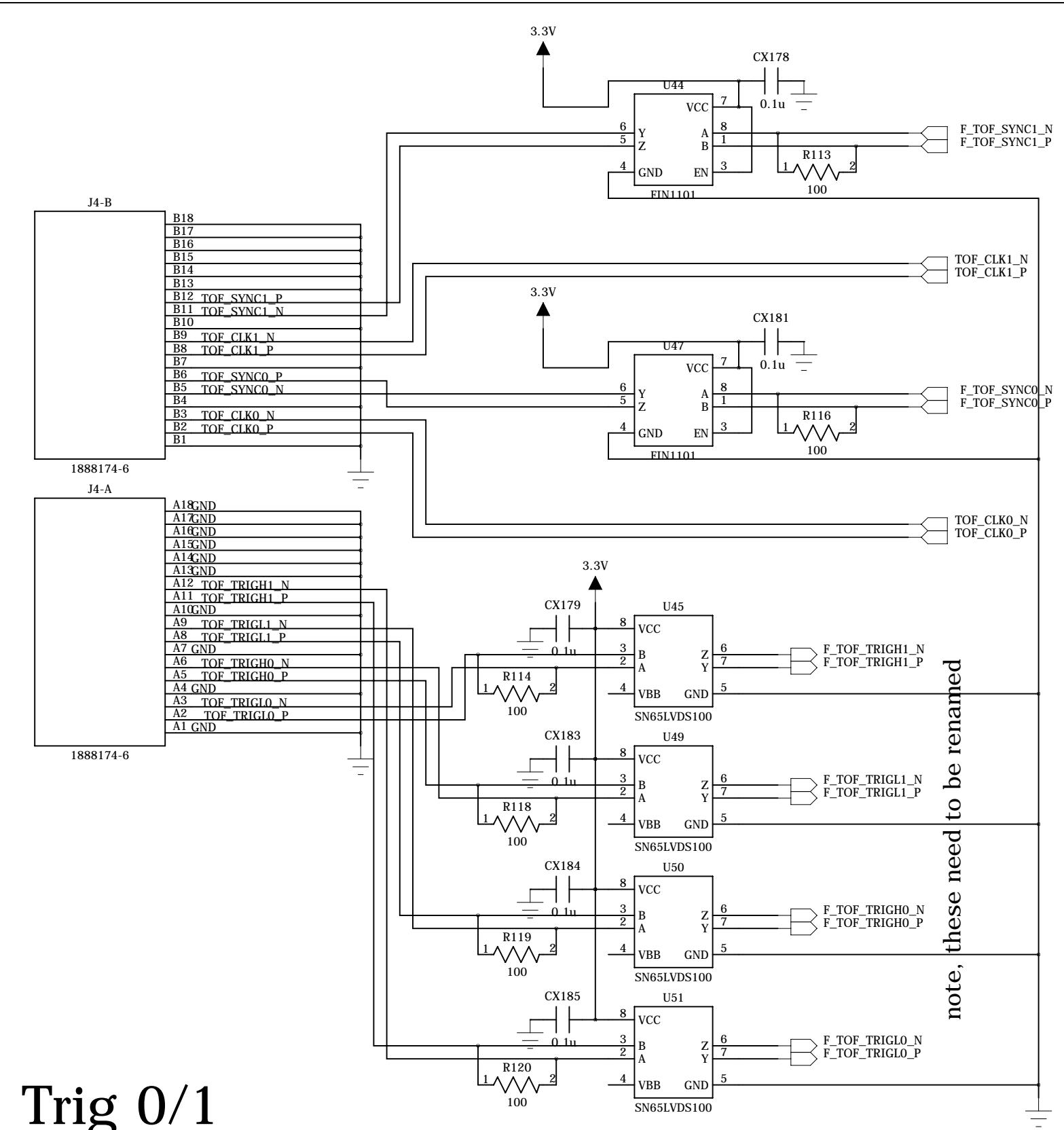
COMPANY: Ohio State University	TITLE: HELIX Master Trigger [HELIX MTRIG]		
DRAWN: PSA	DATED: 6/13/18	CODE: D	SIZE: ATRG
CHECKED: <Checked By>	DATED: <Checked Date>	SHEET: 1	REV:
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>	SCALE: 1:1	sheet: 5 of 8

REVISION RECORD		
ECO NO:	APPROVED:	DATE:

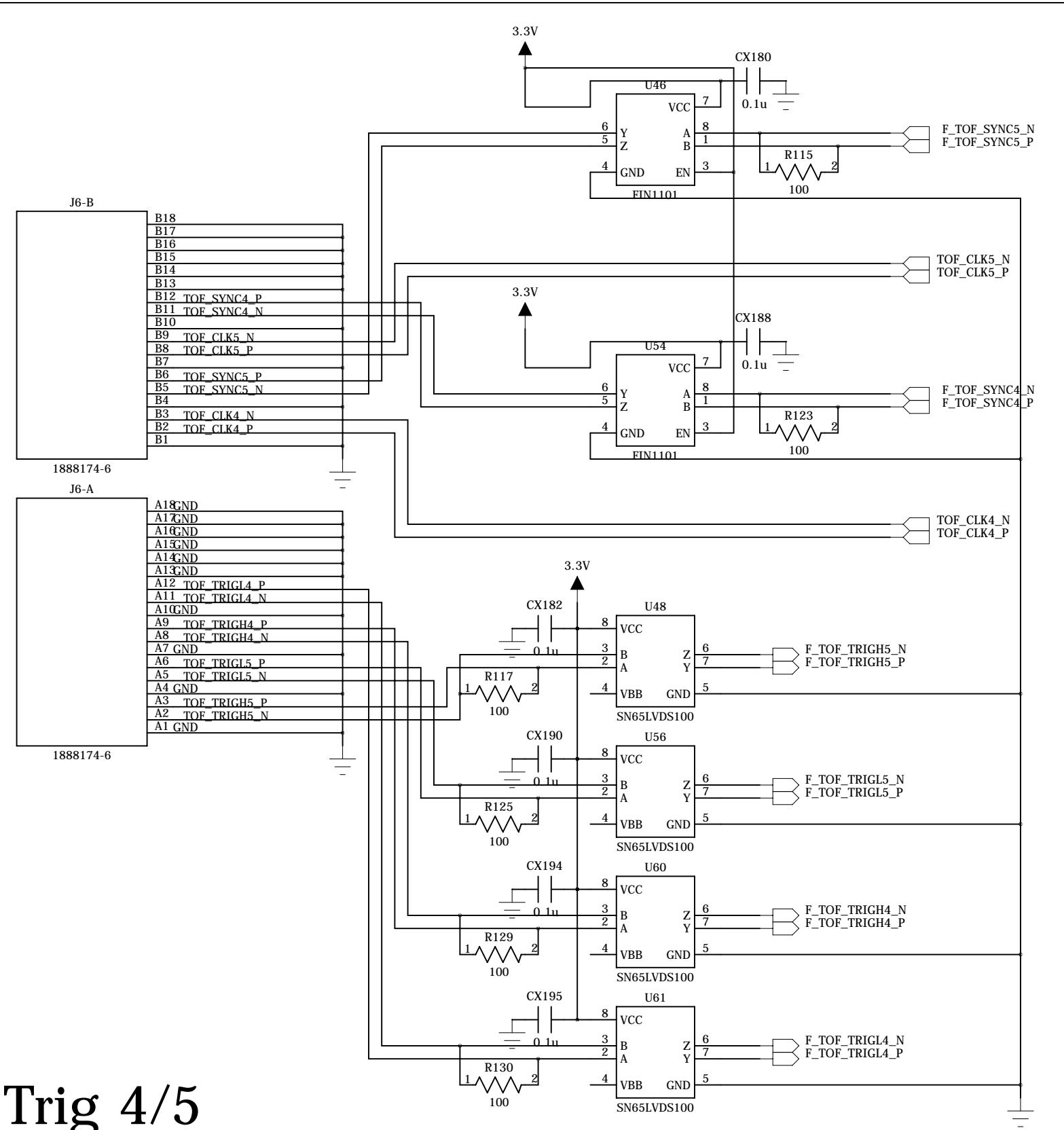


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

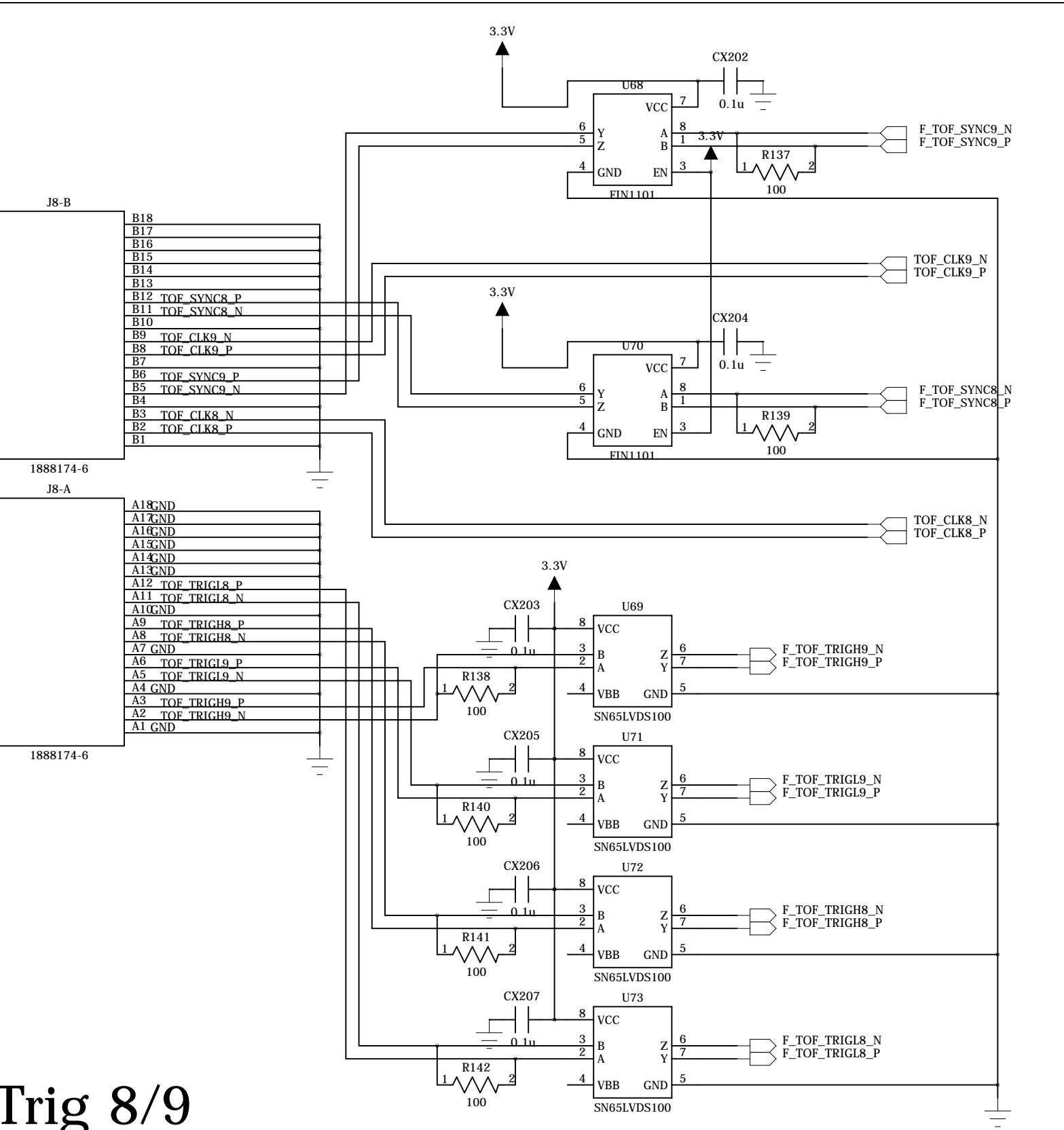
D



Trig 0/1



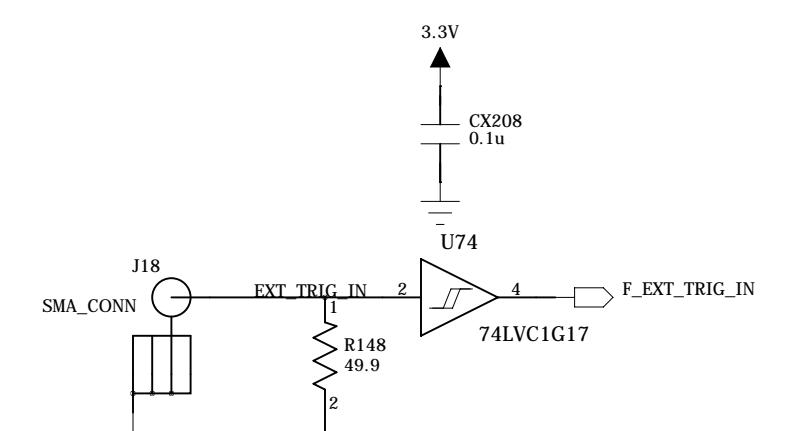
Trig 4/5



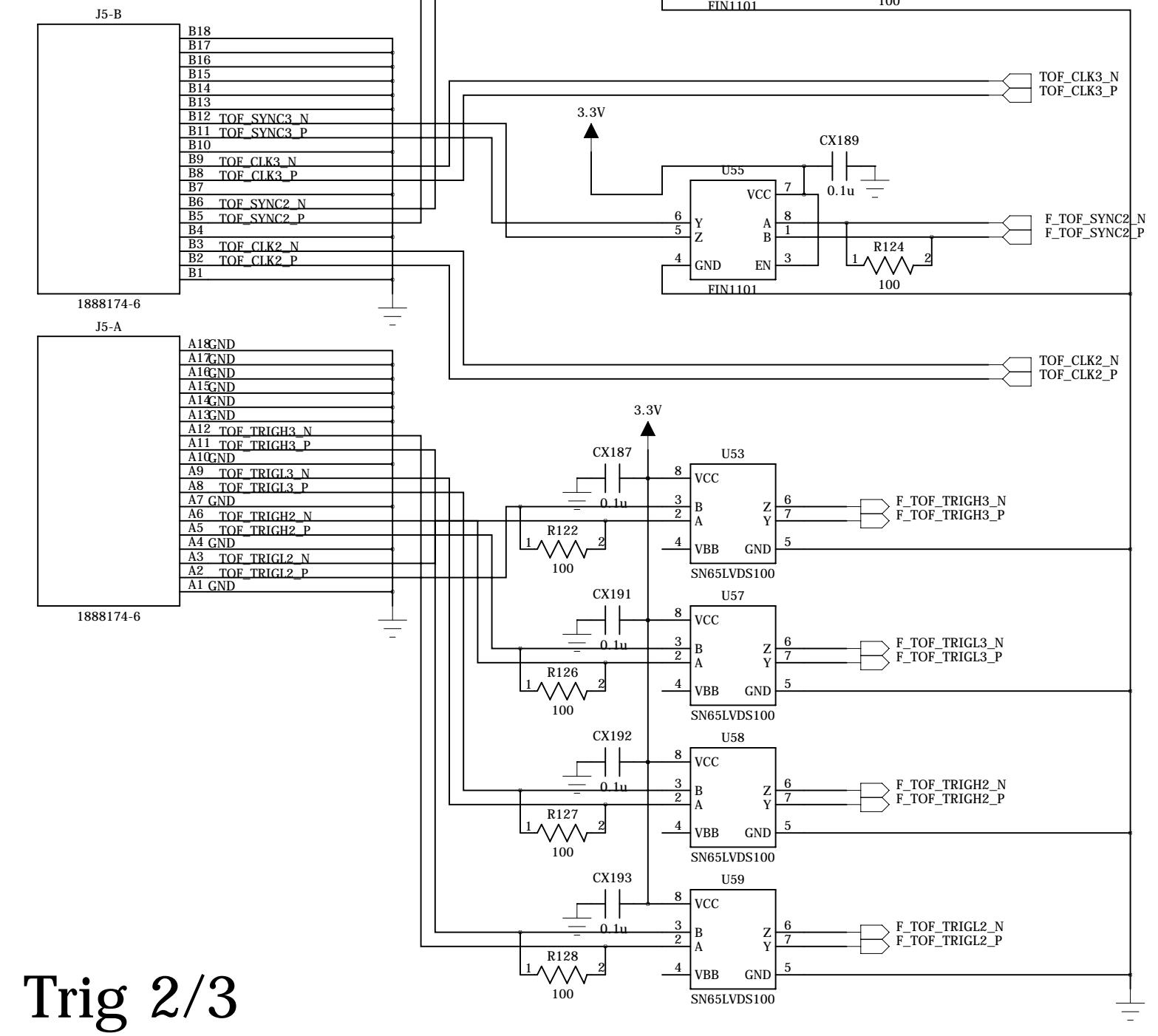
Trig 8/9

Trig 8 is nominally bore paddle
Indicated by single panel-mount (others are dual)

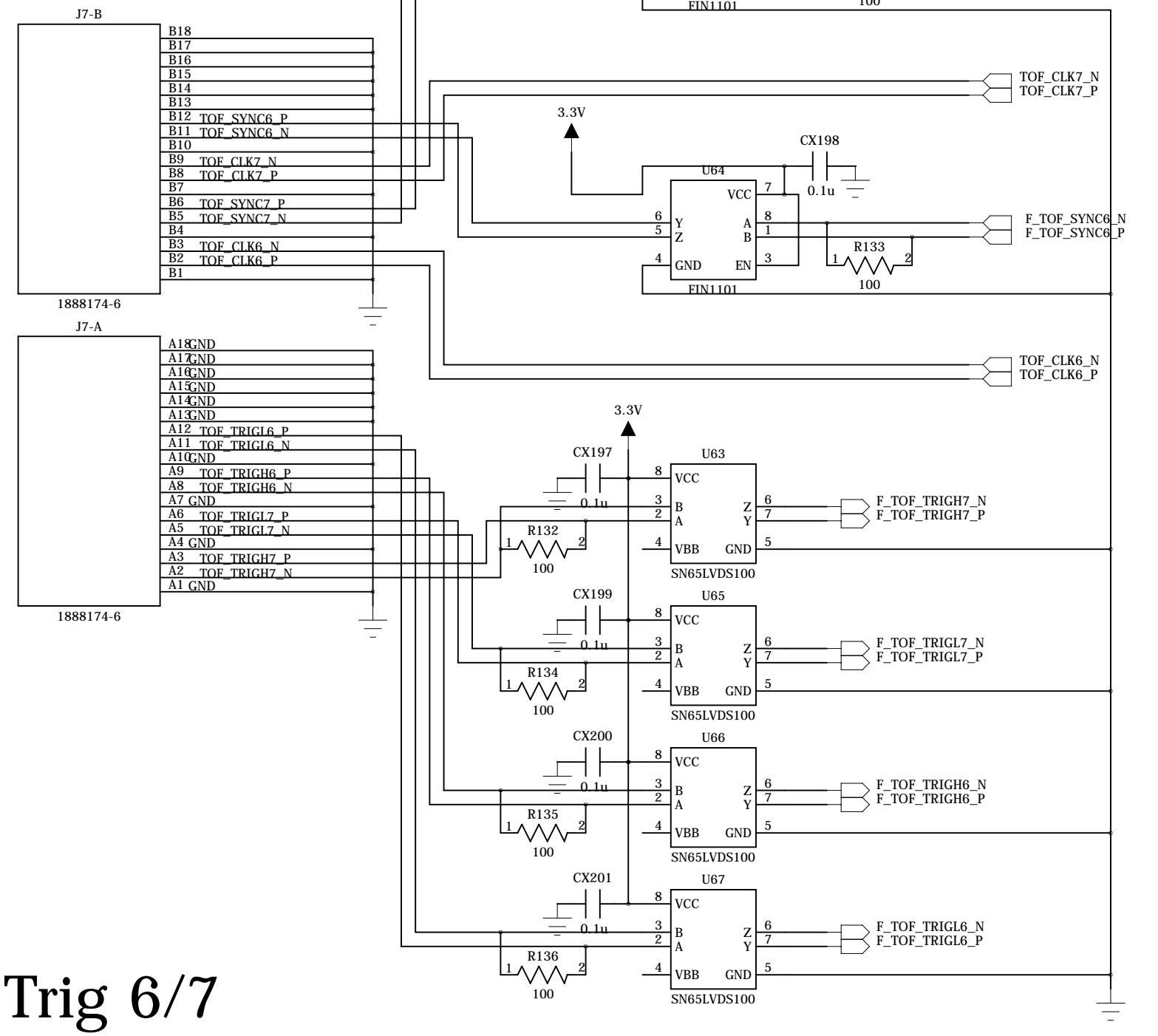
All clocks are straight from clock fanout



A



Trig 2/3



Trig 6/7

DRAWN:	PSA	DATED:	6/13/18
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>

COMPANY: Ohio State University

TITLE: HELIX Master Trigger [HELIX MTRIG]

CODE: D SIZE: SHEET: REV: 1 TRIGGER_IN

SCALE: 1:1

SHEET: 7 OF 8

