SURFv6 Design Document

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1 Introduction

This document describes the Sampling Unit for RF (SURF) version 6. The SURFv6 is designed to work with a Trenz Electronik TE0835 RFSoC board and interface in an IEEE 1101.1 rack to the Radio Array Carrying Kit (RACK). This document describes the overall design of the SURFv6.

1.1 Definitions

- SURF: Sampling Unit for RF. This document describes this board. This term will be used interchangeably for just the board itself as well as the SURF+TE0835 combined board.
- TURF: Trigger Unit for RF. This is the master trigger and clock distribution system for PUEO.
- TURFIO: Trigger Unit for RF I/O. This board provides the interface between the SURF (via the RACK) and the TURF.
- RACK: Radio Array Carrying Kit. This is the custom backplane by which the SURF units communicate with each other and with the TURFIO.
- TE0835: This is the Trenz Electronik RFSoC module. The specific module (ZU47DR, ZU25DR) is unimportant as the SURF is compatible with both.
- U: IEEE 1101.1 standard for vertical spacing. It is equal to 1.75" (44.45 mm). Common increments are 3U, 6U, 9U, etc.
- HP: IEEE 1101.1 standard for horizontal spacing. It is equal to 0.2" (5.08 mm). Common increments are 4HP, 5HP, etc.
- CompactPCI Serial: This is a computer interconnect standard. While the electrical interface is not used in the SURF design, the CompactPCI Serial Conduction Cooled physical specifications are used to provide a thermal design.

2 Physical Dimensions

The SURFv6 is designed as a standard IEEE 1101.1 3U plug-in card, with primary dimensions of 160 mm × 100 mm and a 5HP front panel area.

The connector interface extends slightly, resulting in a maximum bounding box of the SURFv6 of 163 mm × 100 mm. Overall physical dimensions are shown in Fig 1. The backplane connector is a Hirose FX23 100-pin floating connector. This connector has a nominal distance from backplane to back of daughtercard of 10.1 mm, and a connector mating length of 1.5 mm. The IEEE distance from "front attachment plane" to "backplane connector mounting plane" is $175.24 - 176.1$ mm. With the 2.54 mmfront panel gap, this places the nominal distance from front of the board to the backplane as $172.7 - 173.56$ mm. Therefore, we extend the connector portion to 163 mm, resulting in a board separation distance of $9.7 - 10.56$ mm, well within the 10.1 ± 0.75 allowable range.

In general, component clearance from the top and bottom sides of the board is 9.4 mm, however from $59.5 - 124.5$ mm, that clearance reduces to 5 mm to accomodate the TE0835, and from $124.5 - 144$ mm the clearance is 8.5 mm. This clearance extends only until 144 mm. The component clearances are shown in Fig. 2. Direct contact can be made with the board within this area only. Component clearance ends at 144 mmas no parts beyond that point are expected to have significant power consumption.

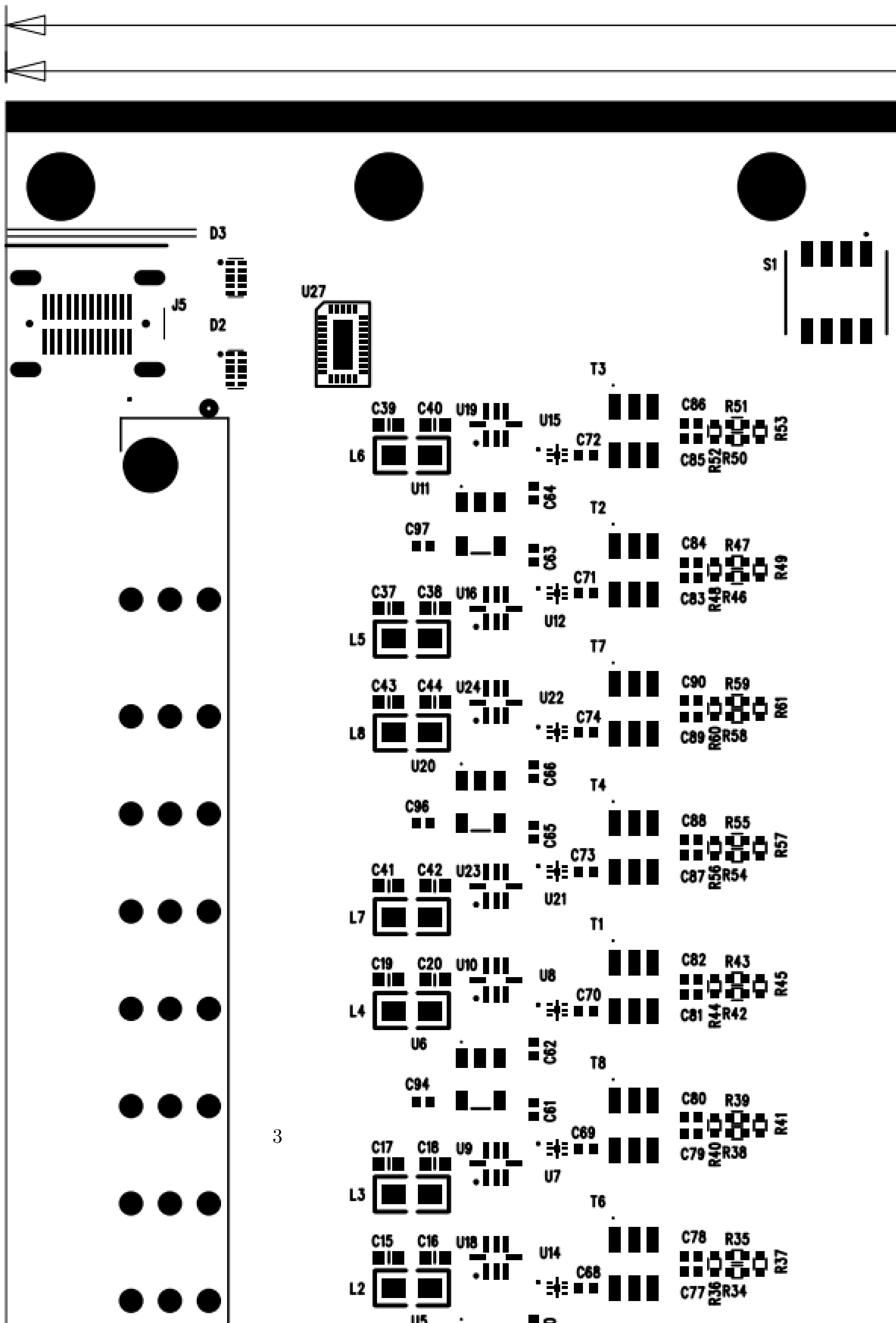
Standard IEEE 1101.1 mounting holes are located at 5.55 mm from the top and bottom and 3.57 mm and 140.07 mm from the front of the PCB. IEEE 1101.1 uses the bottom mounting hole for a convection-cooled insertion/extraction handle and the top mounting hole for a front-panel bracket.

2.1 Convection cooled assembly

The SURFv6 can be inserted into any IEEE 1101.1 3U 160 mm Eurocard convection-cooled crate by adding a standard front panel, insertion/extraction handle and front-panel bracket. An example kit would be Schroff P/N #20848-585 with a replacement front panel (e.g. Schroff P/N #30848-300) as a 5HP kit is not available. For operation in a convection cooled crate, a slim 12V DC fan+heatsink is required, powered by connector J8. Power to the fan is only provided when a convection crate is indicated by a floating connection on the \CONVECTION pin on the RACKbus.

2.2 Conduction cooled assembly

The SURFv6 is designed to be assembled into a CompactPCI Serial (CPCI-S) Conduction Cooled Assembly (CCA) for use in a conduction-cooled crate meeting these specifications. The CPCI-S conduction-cooled specification restricts the maximum height of the PCB+heatsink to 14.5 mmon the top side ("side 1"), and a maximum height of the PCB+heatsink on the rear side ("side 2") of 4 mm. The through-hole pins of the RF connector on the SURFv6 slightly exceed this


D3
J5
D2
U27
S1
T3
C39
C40
U19
U15
C72
C86
R51
R53
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R52
R50
U11
C64
T2
C97
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U10
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R43
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C62
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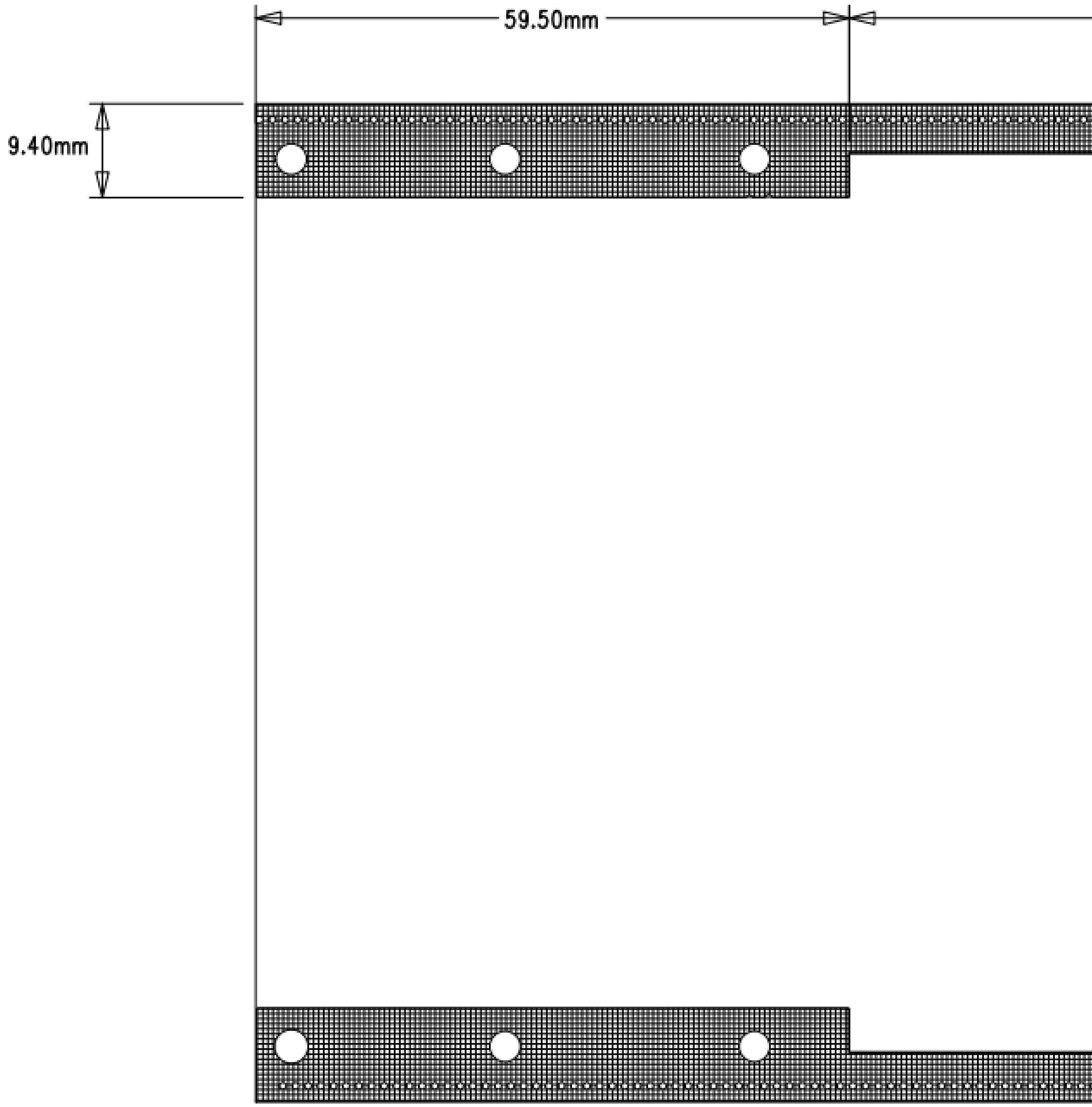

Figure 2: Component keepout area for the SURFv6. Dimensions are identical top and bottom. Direct contact with the board can be made in this area only.

distance (4.4 mm), however the heatsinks for all boards are cleared in this area preventing an interference issue.

3 Features

The SURFv6 is designed to the following features.

- 8 ADC inputs with a 3 dB bandwidth of $90 - 1400$ MHz and an insertion loss of 1.75 dB, flat to ± 0.5 dB over $100 - 1200$ MHz
- Calibration inputs available for all channels, from either an FPGA derived impulse or a backplane input
- Backplane connection to PUEO Radio Array Carrying Kit (RACK) via a Hirose FX23 100-pin floating connector, also providing power
- Fan power connector for benchtop use
- Auxiliary power connector for benchtop use
- Inter-polarization connection utilizing a USB-C connector
- $9 - 15$ V input range
- Overvoltage, undervoltage, and overcurrent protection
- 8 DAC outputs and additional Zynq MPSoC gigabit transceivers (Ethernet, DisplayPort, etc.) available on daughterboard connector
- Gigabit Ethernet available via FFC cable

4 Power Supply

The SURFv6 is designed to be powered by a nominal +12V supply, with an acceptable range of $9 - 15$ V. The SURFv6 can be powered either from the backplane (via J3) or via a dedicated connector for benchtop testing (J12). The J12 input is a 3.5 mm pitch 2-pin terminal block header, with many mating options.

4.1 Input protection

The SURFv6 has undervoltage, overvoltage, and overcurrent protection, as well as a soft-start current draw and FET temperature protection during fault conditions. The SURFv6 does **not** have reverse current protection. Therefore, **great care** should be taken when connecting the auxiliary power input! Polarity is marked on the connector.

Input protection is provided by the ADM1278 hot-swap controller chip. **Note that the SURFv6 should not be plugged in live,** although it is likely that no damage will occur. The ADM1278 has PMBus communication for voltage and current reporting as well as fault detection. Each SURFv6 has its own I2C address provided by the backplane to identify which slot it is inserted into.

Parameters for the ADM1278 were developed on the ADM1278 worksheet. The ADM1278 device is currently listed as NRND (it became NRND early 2022) but device availability is high. Design parameters are as follows.

Parameter	Value	Notes
Undervoltage lockout	9.5 – 10.17 V	corresponds to single-battery voltage as v
Overvoltage lockout	15.58 – 16.50 V	corresponds to single-battery voltage as v
Current limit	3.43 – 3.92 A	corresponds to >30W at abs. min V
Output ramp time	3.8 – 6.93 ms	
Nominal inrush current	0.23 – 0.39 A	based on 100 μF load capacitance
Current limit during inrush	1.3 – 1.71 A	~70% margin
Maximum FET power **in fault**	24.134 – 26.141 W	*Not* max load power! During fault, FET limited t
Fault time	140 – 196.84 μs	Results in 80.22% FET thermal margi

Note that the ADM1278 has two separate current limits - one that applies during startup (determined ISTART, the current limit during inrush), while the voltage is ramping, and one that applies during normal operation. Starting up into a dead short therefore produces significantly less peak current (during fault) than normal operating. Note that the high margin on the ISTART current limit is designed to allow increasing the +12 V output capacitance if needed. Up to 220 μFload capacitance can be tolerated by this design with good margins.

4.2 TE0835 supply (+5V)

The Trenz TE0835 RFSoC is supplied via a high-efficiency 12 V to 5 V regulator, an LT8648. Component values were determined and simulated using LTPowerCad with the project in design folder, with a target maximum load of 6 A. The efficiency exceeds 97.4% beyond 2 A. Note that this efficiency includes inductor and capacitor losses. Output is 4.98 V with $\pm$10 mV ripple (0.2%). Note that the LT8648S design uses the default loop compensation, rather than the "LTpowerCAD Suggested Compensation" as the "suggested" compensation is quite sensitive to the ESR of the bulk filtering capacitor. Loop parameters for the default compensation have sufficient stability and margin (80 deg phase margin, -11.27 dB gain margin). However, pads were made available for all possible loop compensation options.

The LT8648 bulk input capacitor is a high-temperature solid polymer aluminum capacitor. At operating temperatures below 65C expected lifetime is 200K hours. The low ESR of the input capacitor implies that heat generated inside the capacitor will be minimal (10 – 20 mW). Ceramic input capacitors were chosen for a total of 27 μF at 12VDC bias, reducing the ripple seen by the bulk capacitor at a 6A maximum load to 1340 mA, well below the bulk capacitor maximum of 3300 mA.

The LT8648 was chosen for its extremely high efficiency combined with the extremely low emissions.

4.3 Calibration amp supply

The calibration amplifier (an ADL5544) is provided a 4.75 V supply via a MAX8873. Input power to the MAX8873 is filtered through an NFM21PC105B1A3D, providing 30 dB of filtering at the 400 kHz DC-DC switching frequency. Along with the 30 dB PSRR of the MAX8873, this should reduce the 10 mV supply ripple to microvolt-levels.

4.4 Fan power supply

In a convection crate, the TE0835 consumes enough power that an active cooling solution is needed. This is provided via a +12V fan connector, switched by a DS4560 load-switch. The fan is deactivated when the $\overline{CONDUCTION}$ pin is pulled low by the backplane, indicating a conduction cooled crate. Note that the fan is obviously also not installed in this case, so the disabling of the supply isn't strictly necessary, but it prevents a live high-current voltage on a pin.

5 RF Inputs

The SURFv6 RF inputs pass through a high-pass section, a low-pass section, a calibration switch, and finally a wideband balun before arriving at the TE0835 inputs.

5.1 High pass filter

The high pass filter is designed as an extremely simple 3rd order tee-style (minimum inductor) Butterworth filter with a 90 MHz cutoff. This cutoff was intentionally made significantly lower than the PUEO design so that variation in the filter cutoff will have no effect on the observed band.

5.2 Low pass filter

The low pass filter used was a Mini-Circuits LFCG-1000+ with a 3 dB cutoff of 1370 MHz. The low-pass filter functionally acts primarily as an antialiasing filter, offering roughly 20 dB of rejection above Nyquist (1500 MHz).

5.3 Calibration switch

The RF switch used for the calibration switch is a SKY13323. Note that the isolation of this switch is ~ 27 dB, which while high, may still allow some signal leakage in. Therefore the calibration amplifier should be turned off when the normal signal path is in use. Signal leakage into the calibration path should be unimportant if the calibration signal is strong enough. The SKY13323 is driven with a high-range (3.3 V) output from the FPGA, giving an OP1dB point well above the amplifier compression point.

5.4 Wideband balun

The wideband balun selected was a Mini-Circuits TCM2-43X+. This part is footprint-compatible with several other baluns from Mini-Circuits as well. The TCM2-43X+ was specifically chosen because unlike the balun used on the Trenz baseboard (a TCM2-33WX+), the TCM2-43X+ has a decreasing insertion loss with frequency, allowing it to compensate for the gain slope of the filters. In addition, the return loss is constant within the band, showing fewer artifacts when combined with the filters and switch. The downside is a slightly higher insertion loss.

5.5 Full path simulation

To simulate the full RF path, an ideal balun was used to convert the differential signal back to single-ended. Note that the ~0.05 dB "kink" visible near ~380 MHz is due to the SKY13323 S-parameter data. This appears to be a measurement artifact, as no kink is visible in the datasheet and below this frequency, the return loss of the unconnected input is an unphysical positive value and phases make a rapid unphysical jump and immediately return to their previous values. Insertion loss is flat to within ± 0.5 dB over the PUEO band, and group delay is flat to within ± 0.25 ns.

6 Calibration path

A common "CAL" input comes from the RACK backplane and is sent through another SKY13323 switch, with the other input being the output of a differential signal from the FPGA (an impulse test). This CAL input is amplified via an ADL5544, then split 8 ways via an EP4RKU+ in combination with SBTC-2-20+ power splitters (resulting in a total loss of ~16 dB, or roughly equal to the input from the backplane).

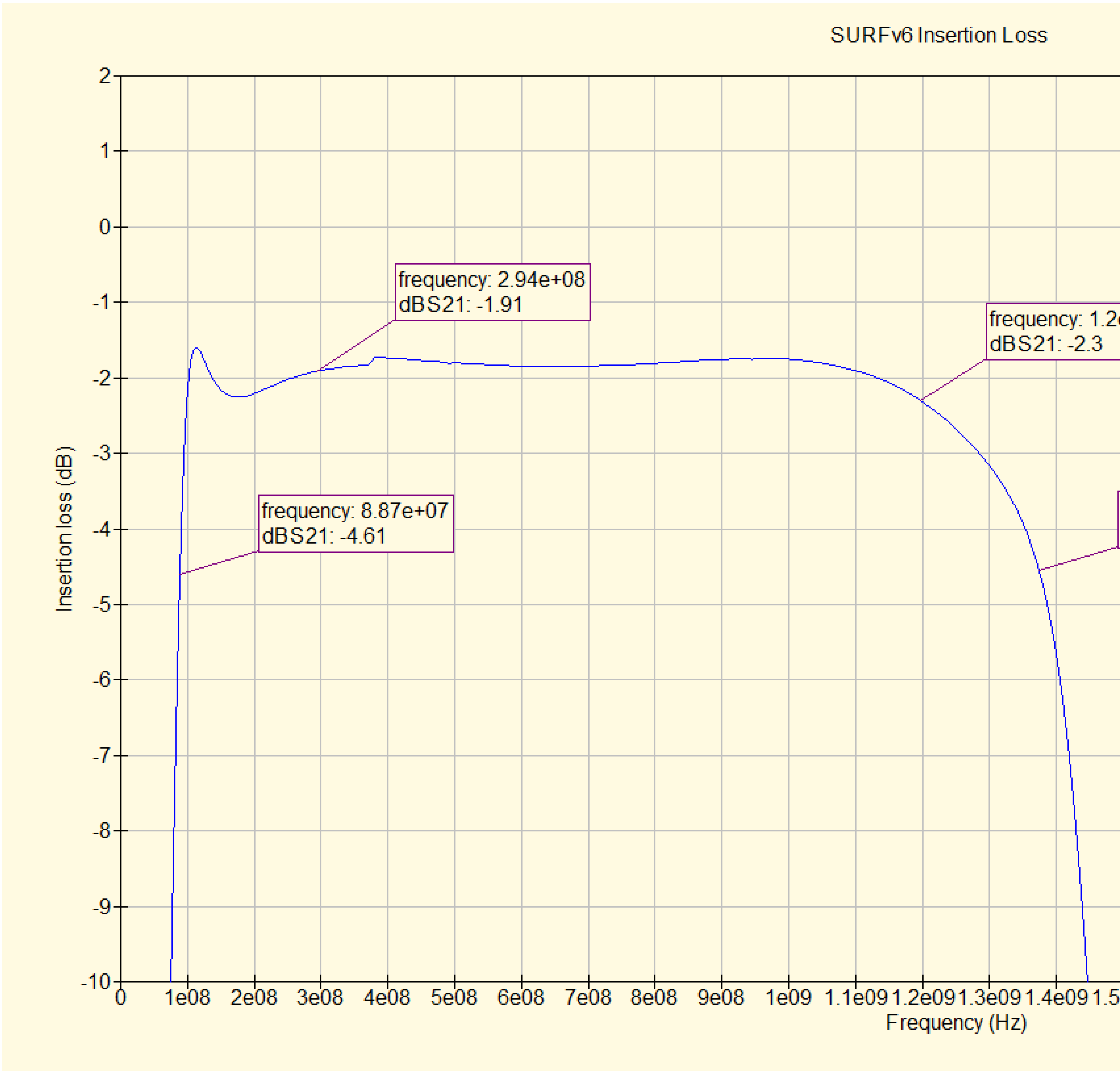

Figure 3: Simulated RF insertion loss for the SURFv6. Note that the “kink” near 380 MHz is due to the SKY13323 S-parameter data.

7 Backplane interface (RACKbus)

Left Name	Left #	Right #	Right Name
ENABLE	1	51	CAL
GND	2	52	GND
DOUT+	3	53	RX
DOUT-	4	54	TX
GND	5	55	GND
CIN+	6	56	COUT+
CIN-	7	57	COUT-
GND	8	58	GND
RXCLK+	9	59	TXCLK+
RXCLK-	10	60	TXCLK-
GND	11	61	GND
TIN+	12	62	TOUT+
TIN-	13	63	TOUT-
\CONDUCTION	14	64	\ALERT
TCK	15	65	TDO
TMS	16	66	TDI
GND	17	67	3.3VSB
PSYNC	18	68	
	19	69	
	20	70	
	21	71	
EXT_CLK_P	22	72	
EXT_CLK_N	23	73	
GND	24	74	GND
U0RX+	25	75	D0TX+
U0RX-	26	76	D0TX-
GND	27	77	GND
U0TX+	28	78	D0RX+
U0TX-	29	79	D0RX-
GND	30	80	GND
U1RX+	31	81	D1TX+
U1RX-	32	82	D1TX-
GND	33	83	GND
U1TX+	34	84	D1RX+
U1TX-	35	85	D1RX-
GND	36	86	GND
U2RX+	37	87	D2TX+
U2RX-	38	88	D2TX-
GND	39	89	GND
U2TX+	40	90	D2RX+
U2TX-	41	91	D2RX-
GND	42	92	GND
U3RX+	43	93	D3TX+
U3RX-	44	94	D3TX-
GND	45	95	GND
U3TX+	46	96	D3RX+
U3TX-	47	97	D3RX-
GND	48	98	GND
A0	49	99	SDA
A1	50	100	SCL

7.1 TURF interface

The interface to the TURF (via the TURFIO) consists of source-synchronous high speed (750 Mbps) serial links. Data is transmitted via DOUT+/-, and commands are received and responded to on CIN+/-, COUT+/- respectively. RXCLK+/- and TXCLK+/- complete the source-synchronous interfaces.

The system clock is provided on EXT_CLK_P/N.

7.2 Interphi comms

U[3:0]RX/TX+/- (increasing phi communication) and D[3:0]RX/TX+/- (decreasing phi communication) comprise the interphi communication system. Note that the "up/down" here is arbitrary, it's really just to opposite sides on the backplane.

7.3 Auxiliary trigger chain

To accomodate a secondary low-level trigger for the LF instrument, a trigger chain (TIN+/- and TOUT+/-) is formed to combine low-level trigger outputs from the TE0835s. Note that while nominally a loss of a single TE0835 breaks the chain, this problem can be mitigated since the trigger chain could be reconfigured to wrap around the ends of the crate.

7.4 Single-ended control signals

- A0/A1: Address pins to identify the slot. These address pins have 3 possible values (open, resistor to ground, or ground). Combined with the backplane identification (left/right) that gives 18 total possibilities (only 14 are needed).
- SDA/SCL/\ALERT : SMBus interface pins.
- PSYNC: Power system synchronization clock.
- ENABLE: Allows disabling power to all TE0835s
- 3.3VSB: standby low current 3.3V supply
- RX/TX: Asynchronous slow-control interface
- \CONDUCTION: Identifies type of crate.
- TCK/TMS/TDI/TDO: JTAG interface.

Clock #	TE0835 name	SURFv6 name	Frequency	Purpose
0A	unused	unused		
0	CLKC_P/N	ACLK0_P/N	187.5 MHz	ADC 0/1 clock
1	CLKB_P/N	ACLK1_P/N	187.5 MHz	ADC 2/3 clock
2	CLKA_P/N	ACLK2_P/N	187.5 MHz	ADC 4/5 clock
3	CLKD_P/N	ACLK3_P/N	187.5 MHz	ADC 6/7 clock
4	CLKE_P/N	PLCLK_P/N(*)	187.5 MHz	Logic clock
5	CLKF_P/N	unused (*)		
6	B128_CLK0_P/N	–	125 MHz	MGT clock
7	B129_CLK0_P/N	–	125 MHz	MGT clock
8	CLK8_P/N	–	7.8125 MHz	PL_SYSREF
9	PSMGT_100MHz_P/N	–	125 MHz	PS MGT clock
9A	CLK0A_100MHz_P/N	SYSREFCLK_P/N	7.8125 MHz	Analog SYSREF

Table 1: Clock outputs of the Si5395 clock generator on the TE0835. CLKE/F - marked with (*) - can also be routed as DAC clocks. Note that clocks 9 and 9A do not match their TE0835 frequency names. This is unimportant and only represents the original usage in the TE0835 base project.

8 Clocking system

The TE0835 contains a Silicon Labs 12-output clock generator which takes either an internal clock or an external reference clock. One of these clocks is unconnected. It should be sadly noted that the unused clock was not routed back to the feedback input, and therefore the Si5395 cannot be operated in zero-delay mode. There will therefore be some unknown propagation delay between the common system clock and the sampling clock of the ADCs. However, this delay can be measured (independent of the ADCs) using a similar setup to the phase scanner present in the SURFv5 and TISC firmware to sub-10 ps precision. This is because the FPGA will have both the input clock (from the TURFIO, via TXCLK_P/N) and the output clock (via PL_SYSREF). If this arrangement proves unworkable, a second revision of the SURFv6 would be necessary with its own Si5395 onboard (which would allow the onboard Si5395 to be shut down).

The outputs from the Si5395 are shown in Table 1. Note that the clocks must be configured differently between internal (10 MHz input) and external (7.8125 MHz input).

9 Inter-phi communication

Adjacent RFSoCs communicate via a 4-lane MGT link. To meet the required 20 Gbit/s throughput, the MGTs must operate at *least* up to 5 Gbit/s. MGT connections are routed on layer 3 as stripline.

10 Inter-polarization communication

Because all 8 logic MGTs are taken, any inter-polarization communication must occur using the PS MGTs, which are restricted to operate using fixed protocols. Two PS MGTs are routed to a USB-C connector on the front panel via two differential pair exchange switches to accomodate the USB-C connector reversal function. This should allow *both* a USB 3.0 connection (5 Gbps) and a separate GbE connection (1 Gbps) using a USB 3.1 cable. Note that a USB 3.0 cable will only have 1 SuperSpeed pair, therefore a USB3.1 cable is preferred.

Cable detection is done using a Type C controller, either a PI5USB30216, a TUSB320, or a FUSB303B, all of which are pin-compatible. Additionally, to accomodate the possibility of USB device connection (via the PL), a DPS1113 VBUS switch is used to drive +5V onto the USB connector when connected as a USB source.

Type C roles (source or sink) can be forced using switches 5/6 on the S1 DIP switch if autonegotiation fails.

Two PI3DBS16222 exchange switches are used instead of a single for ease of routing, especially near the USB connector. Note that due to the switch arrangement the two switches must be set *opposite* each other, so two control lines (USB_SW0/USB_SW1) are used.

USB inputs are protected via ESD8104 diode arrays.

11 Auxiliary connectors

The TE0835 has significant resources that are not nominally required for the SURFv6, however it makes sense to make them available for either testing or special purposes. This is done via 2 auxiliary connectors: first, Ethernet signals (PHY_MDIO[3:0]+/-, as well as the LED outputs) are made available on a flat-flex cable connector (J10) which can be accessed via a Molex Premo-Flex LVDS (0150121) cable. Second, an “aux” connector (J6) contains a number of auxiliary signals on an FX12B-60P board-to-board connector.

The aux connector contains:

- 8 DAC outputs
- 2 PS-MGT RX/TX pairs
- 2 general purpose differential pairs (L1_P/N and L16_P/N)
- MIO signals needed to implement DisplayPort on the PS-MGT signals (CPLD_IO2/IO3 and MIO27/MIO30)
- 3 general purpose I/Os (L6_N, L7_N, and L7_P)

The last 3 GPIOs are also available on test points.

12 SDIO interface

To facilitate booting from an SD card and matching the TEB0835, a micro-SD socket was placed on the rear of the SURFv6, interfaced to the FPGA using a TXS02612 level converter, matching the TEB0835. One difference is that we do not supply 3.3V to the micro-SD socket unless a card is detected. Cards are powered via the 3.3V CPLD voltage rail present on the TE0835, which is current-limited to 300 mA, however virtually no loads on either board exist for this rail - the main draw is a CTS626 which is used as a spare MGT clock.

13 DIP switch

The TE0835 uses a 4-pole DIP switch to configure both the JTAG access and boot settings. The SURFv6 keeps those but the order changes. Therefore the settings are listed again here.

Switch #	Signal Name	Description
1	CPLD_JTAGEN	When ON, selects CPLD JTAG
2	CPLD_IO2	\PROGRAM
3	CPLD_IO1	\BOOT1
4	CPLD_IO0	\BOOT0
5	USB_SNK	When ON=USB sink
6	USB_SRC	When ON=USB source

Note: switching both 5 and 6 on will result in undefined behavior.

13.1 Boot modes

\BOOT1 and \BOOT0 produce different booting modes for the TE0835.

Boot mode	SW#4 State	SW#3 State
JTAG	ON	ON
QSPI Flash	ON	OFF
SD Card	OFF	OFF

Once firmware is completed, the basic boot mode should be QSPI flash (SW#4 ON, SW#3 OFF).