	6	5	4	3		2			1		
D	5. remove LI/L16 connections to dau 6. use transistors to invert CAL_SEL t 7. drop optional clock rerouting and j 8. replace custom ethernet connector 9. add auxiliary eMMC/SD connector 10. add serial termination resistors te LMK04610 requires new 3.3V and 1.8 LMK04610 can be programmed from	ust directly connect DCLK0/DCLK1 with ix industrial and add magnetics + swap MIOs around both SD ports 3V regulators, plus supervisor to hold in reset PL or PS side	dd connectivity	1835) with GEN3 IN DUEO			LTR	REVISION R ECO NO:	APPROVED:	DATE:	D
С	S15395 (ON TE0835) CI CLKO: ADC2 dock (224) CLK1: unused CLK2: ADC0 dock (226) CLK3: ADC3 dock (227) CLK4: DAC1 dock (227) CLK4: DAC1 dock (228) CLK5: DAC0 dock (228) CLK6: MET B128 CLK0 CLK7: MET B128 CLK0 CLK9: TE128 CLK0 CLK9: TE129 CLK0 CLK9: TE129 CLK0 CLK9A: EXPLICATION CLK9: ADC0 (ON SURF) (CLK9A: MET - 100M CLK2: ext clk to 515395 (off) CLK3: pl syscik (375M) CLK4: aclk (375M) CLK5: feedback (15.365M, no output) CLK6: 7.8125M during MTS, off other CLK6: TE125M during MTS, off other CLK8: off CLK9: off	CLK2: 375M CLK3: 375M CLK4: 375M during MTS, off otherwise CLK5: off CLK6: off CLK7: off CLK8: off CLK9: off CLK9: off CLK9: of	CLK0: off CLK1: off CLK2: off CLK2: off CLK2: off CLK4: 375M during MTS, CLK4: 375M during MTS, CLK5: off CLK6: off CLK7: off CLK8: off CLK8: off CLK8: off CLK9: off								С
В	CLK10: off After MTS, CLK6/7 can disable output With GENI STANDALONE, input is CLI In PUEO, input is CLKINO	: and the CLK6-10 buffer can be disabled KIN1									В
Α				DRAWN: PSA CHECKED: QUALITY CONTROL: RELEASED:	DATED: 3/11/24 DATED: DATED:	COMPANY: TITLE: CODE: SCALE:	Ohio	State Univers SURFv6 DRAWING	•	REV:	- A

























