CHANGELOG:
Rev B (3/2/2024)
1. remove RX/TX MIO connection (wrong voltage) - use EMIO only
2. add LMK04610. SYS_CLK goes to LMK04610, outputs to ADC1 CLK, SYSREF, PL, PL_SYSREF, EXT_CLK_IN
3. flip LED light pipe mounting holes
4. add cheap USB UART for serial console and level translation for RX/TX
5. remove L1/L16 connections to daughterboard to open up pins, hook I2C to daughterboard for add'l connectivity
6. use transistors to invert CAL_SEL to save pin
7. drop optional clock rerouting and just directly connect DCLK0/DCLK1
8. replace custom ethernet connector with ix industrial and add magnetics
9. add auxiliary eMMC/SD connector + swap MIOs around
10. add serial termination resistors to both SD ports

LMK04610 requires new 3.3V and 1.8V regulators, plus supervisor to hold in reset
LMK04610 can be programmed from PL or PS side

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SI5395 (ON TE0835) CONFIG
CLK0: ADC2 clock (224)
CLK1: unused
CLK2: ADC0 clock (226)
CLK3: ADC3 clock (227)
CLK4: DAC1 clock (229)
CLK5: DAC0 clock (228)
CLK6: MGT B128 CLK0
CLK7: MGT B129 CLK0
CLK8: to PL
CLK9: PSMGT clock
CLK9A: ext clock out (to LMK04610)

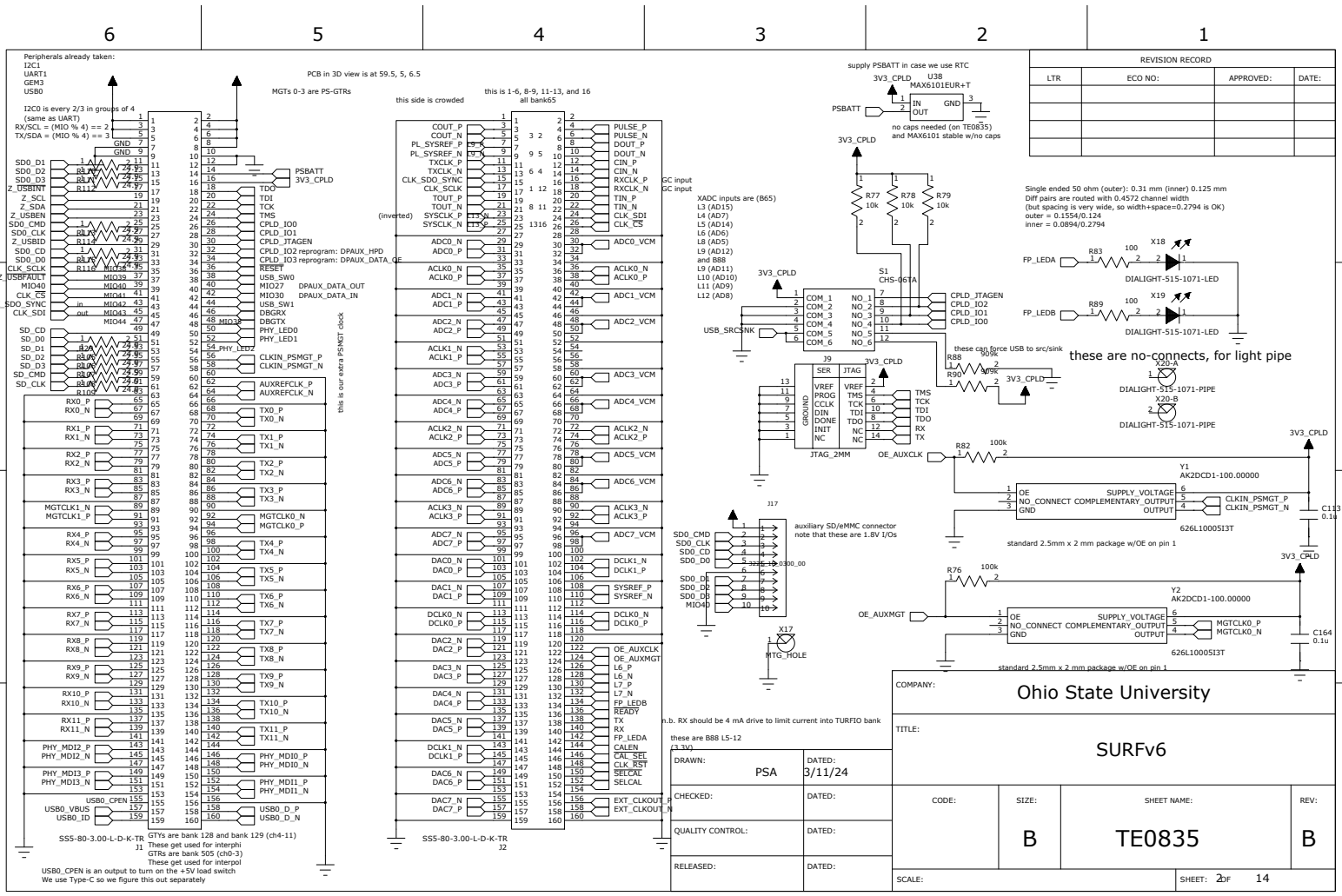
SI5395 (ON TE0835) with GEN1 STANDALONE
CLK0: 375M
CLK1: off
CLK2: 375M
CLK3: 375M
CLK4: 375M during MTS, off otherwise
CLK5: off
CLK6: off
CLK7: off
CLK8: off
CLK9: off
CLK9A: 15.365M out

SI5395 (ON TE0835) with GEN3 IN PUEO
CLK0: off
CLK1: off
CLK2: off
CLK3: off
CLK4: 375M during MTS, off otherwise
CLK5: off
CLK6: off
CLK7: off
CLK8: off
CLK9: off
CLK9A: off
POWER DOWN when out of MTS
(write 1 to 0x001E)

LMK04610 (ON SURF) CONFIG
CLK1: MGT - 100M
CLK2: ext clk to Si5395 (off)
CLK3: pl sysclk (375M)
CLK4: aclk (375M)
CLK5: feedback (15.365M, no output)
CLK6: 7.8125M during MTS, off otherwise
CLK7: 7.8125M during MTS, off otherwise
CLK8: off
CLK9: off
CLK10: off
After MTS, CLK6/7 can disable output and the CLK6-10 buffer can be disabled

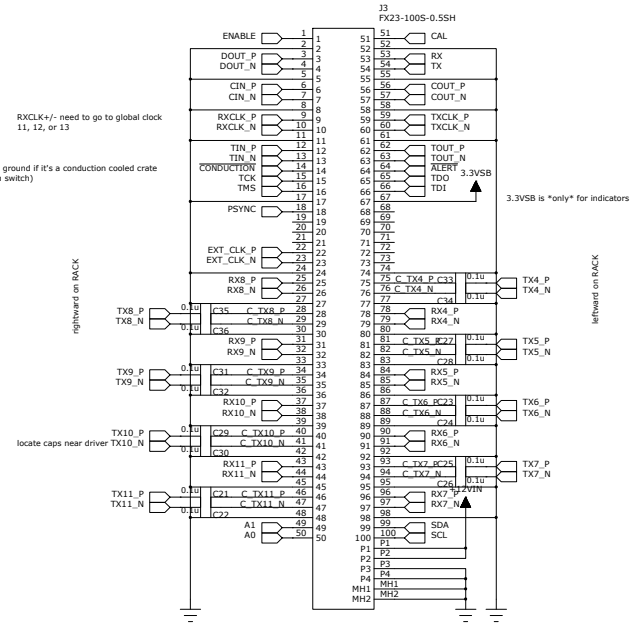
With GEN1 STANDALONE, input is CLKIN1
In PUEO, input is CLKIN0

DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University	
CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B / DRAWING NO: / REV: B
RELEASED:	DATED:	SCALE:	SHEET: 1 OF 14


Peripherals already taken:
I2C1
UART1
GEM3
USB0
I2C0 is every 2/3 in groups of 4
(same as UART)
RX/SCL = (MIO % 4) == 2
TX/SDA = (MIO % 4) == 3
PCB in 3D view is at 59.5, 5, 6.5
MGTs 0-3 are PS-GTRs
this side is crowded
this is 1-6, 8-9, 11-13, and 16
all bank65
PSBATT
3V3_CPLD
TDO
TDI
TCK
TMS
CPLD_IO0
CPLD_IO1
CPLD_JTAGEN
CPLD_IO2 reprogram: DPAUX_HPD
CPLD_IO3 reprogram: DPAUX_DATA_OE
RESET
USB_SW0
MIO27 DPAUX_DATA_OUT
MIO30 DPAUX_DATA_IN
USB_SW1
DBGRX
DBGTX
PHY_LED0
PHY_LED1
CLKIN_PSMGT_P
CLKIN_PSMGT_N
AUXREFCLK_P
AUXREFCLK_N
this is our extra PSMGT clock
TX0_P
TX0_N
TX1_P
TX1_N
TX2_P
TX2_N
TX3_P
TX3_N
MGTCLK0_N
MGTCLK0_P
TX4_P
TX4_N
TX5_P
TX5_N
TX6_P
TX6_N
TX7_P
TX7_N
TX8_P
TX8_N
TX9_P
TX9_N
TX10_P
TX10_N
TX11_P
TX11_N
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
USB0_D_P
USB0_D_N
USB0_VBUS
USB0_ID
USB0_CPEN
SSS-80-3.00-L-D-K-TR
J1
GTYs are bank 128 and bank 129 (ch4-11)
These get used for interphi
GTRs are bank 505 (ch0-3)
These get used for interpol
USB0_CPEN is an output to turn on the +5V load switch
We use Type-C so we figure this out separately
SSS-80-3.00-L-D-K-TR
J2
COUT_P
COUT_N
PL_SYSREF_P
PL_SYSREF_N
TXCLK_P
TXCLN_N
CLK_SDO_SYNC
CLK_SCLK
TOUT_P
TOUT_N
SYSCLK_P
SYSCLK_N
(inverted)
ADC0_N
ADC0_P
ACLK0_N
ACLK0_P
ADC1_N
ADC1_P
ADC2_N
ADC2_P
ACLK1_N
ACLK1_P
ADC3_N
ADC3_P
ADC4_N
ADC4_P
ACLK2_N
ACLK2_P
ADC5_N
ADC5_P
ADC6_N
ADC6_P
ACLK3_N
ACLK3_P
ADC7_N
ADC7_P
DAC0_N
DAC0_P
DAC1_N
DAC1_P
DCLK0_N
DCLK0_P
DAC2_N
DAC2_P
DAC3_N
DAC3_P
DAC4_N
DAC4_P
DAC5_N
DAC5_P
DCLK1_N
DCLK1_P
DAC6_N
DAC6_P
DAC7_N
DAC7_P
PULSE_P
PULSE_N
DOUT_P
DOUT_N
CIN_P
CIN_N
RXCLK_P
RXCLK_N
TIN_P
TIN_N
CLK_SDI
CLK_CS
ADC0_VCM
ADC1_VCM
ADC2_VCM
ADC3_VCM
ADC4_VCM
ADC5_VCM
ADC6_VCM
ADC7_VCM
DCLK1_N
DCLK1_P
SYSREF_P
SYSREF_N
DCLK0_N
DCLK0_P
OE_AUXCLK
OE_AUXMGT
L6_P
L6_N
L7_P
L7_N
FP_LEDB
READY
TX
RX
FP_LEDA
CALEN
CAL_SEL
CLK_RST
SELCAL
EXT_CLKOUT_P
EXT_CLKOUT_N
GC input
GC input
XADC inputs are (B65)
L3 (AD15)
L4 (AD7)
L5 (AD14)
L6 (AD6)
L8 (AD5)
L9 (AD12)
and B88
L9 (AD11)
L10 (AD10)
L11 (AD9)
L12 (AD8)
supply PSBATT in case we use RTC
3V3_CPLD
U38
MAX6101EUR+T
IN
OUT
GND
PSBATT
no caps needed (on TE0835)
and MAX6101 stable w/no caps
R77 10k
R78 10k
R79 10k
S1
CHS-06TA
COM_1
COM_2
COM_3
COM_4
COM_5
COM_6
NO_1
NO_2
NO_3
NO_4
NO_5
NO_6
CPLD_JTAGEN
CPLD_IO2
CPLD_IO1
CPLD_IO0
USB_SRC_SNK
these can force USB to src/sink
R88 909k
R90 909k
J9
JTAG_2MM
SER
JTAG
VREF
PROG
CCLK
DIN
DONE
INIT
NC
GROUND
TMS
TCK
TDI
TDO
RX
TX
OE_AUXCLK
R82 100k
Y1
AK2DCD1-100.00000
OE
NO_CONNECT
GND
SUPPLY_VOLTAGE
COMPLEMENTARY_OUTPUT
OUTPUT
CLKIN_PSMGT_P
CLKIN_PSMGT_N
626L10005I3T
C133 0.1u
standard 2.5mm x 2 mm package w/OE on pin 1
J17
auxiliary SD/eMMC connector
note that these are 1.8V I/Os
SD0_CMD
SD0_CLK
SD0_CD
SD0_D0
SD0_D1
SD0_D2
SD0_D3
MIO40
X17
MTG_HOLE
R76 100k
Y2
AK2DCD1-100.00000
OE_AUXMGT
MGTCLK0_P
MGTCLK0_N
C164 0.1u
standard 2.5mm x 2 mm package w/OE on pin 1
n.b. RX should be 4 mA drive to limit current into TURFIO bank
these are B88 L5-12
(3.3V)
Single ended 50 ohm (outer): 0.31 mm (inner) 0.125 mm
Diff pairs are routed with 0.4572 channel width
(but spacing is very wide, so width+space=0.2794 is OK)
outer = 0.1554/0.124
inner = 0.0894/0.2794
FP_LEDA
FP_LEDB
R83 100
R89 100
X18
X19
DIALIGHT-515-1071-LED
these are no-connects, for light pipe
X20-A
X20-B
DIALIGHT-515-1071-PIPE
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
Ohio State University
TITLE:
SURFv6
DRAWN:
PSA
DATED:
3/11/24
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
B
SHEET NAME:
TE0835
REV:
B
SCALE:
SHEET: 2 OF 14

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Horizontally this switches left/right at the RACK
(so connecting 25->75 goes right, 75->25 goes left)



RXCLK+/- need to go to global clock
11, 12, or 13

CONDUCTION is ground if it's a conduction cooled crate
(disables the fan switch)

3.3VSB is *only* for indicators

rightward on RACK

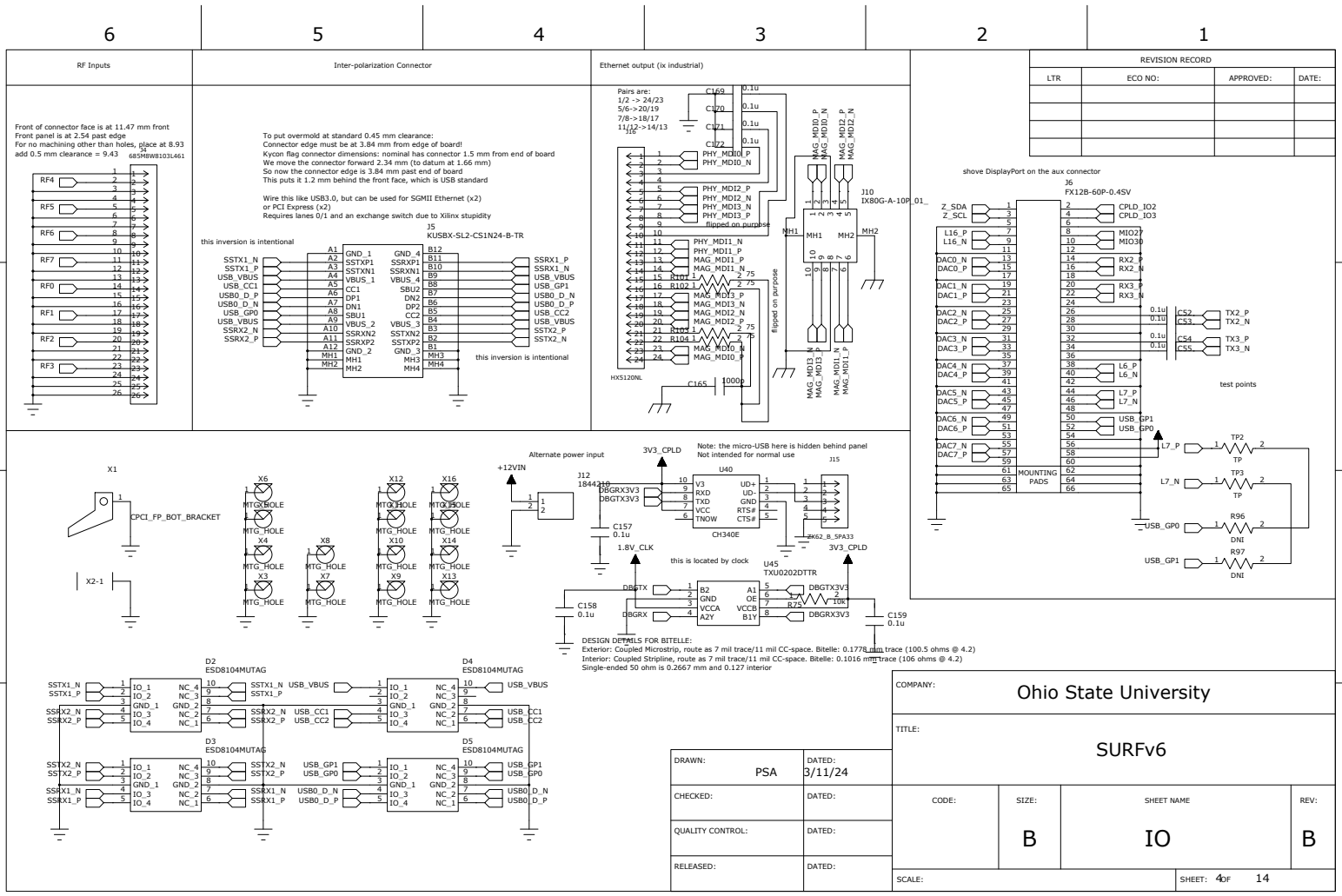
leftward on RACK

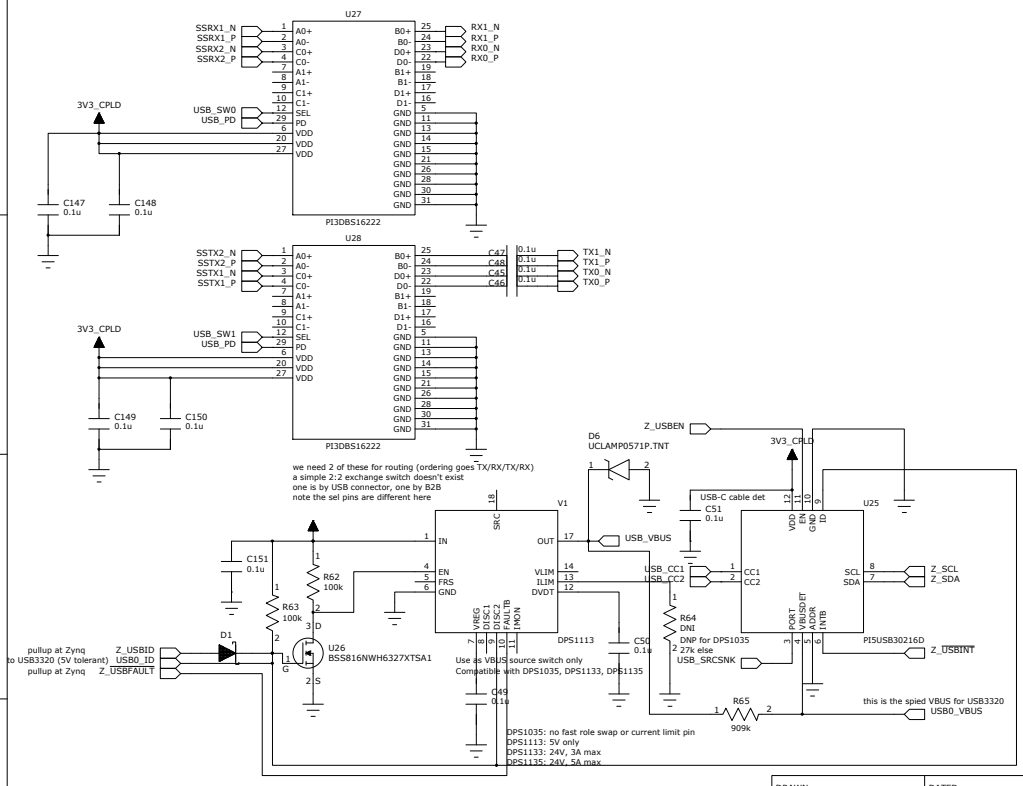
locate caps near driver

RXCLK is B65 L12_N/P (global clock): 34.1 mm
TXCLK is B65 L6_N/P: 24.5 mm
COUT is B65 L3_N/P: 21.8 mm
CIN is B65 L4_N/P: 28.5 mm
Match CIN to RXCLK (+5.6) and COUT to TXCLK (-2.7)

TXCLK = 24.5 + 105.3 = 129.98
COUT = 21.8 + 108.15 = 129.95
RXCLK = 34.1 + 104.3 = 138.4
CIN = 28.5 + 109.9 = 138.4

DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University	
CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: RACKBUS	REV: B
		SCALE:	SHEET: 3 OF 14

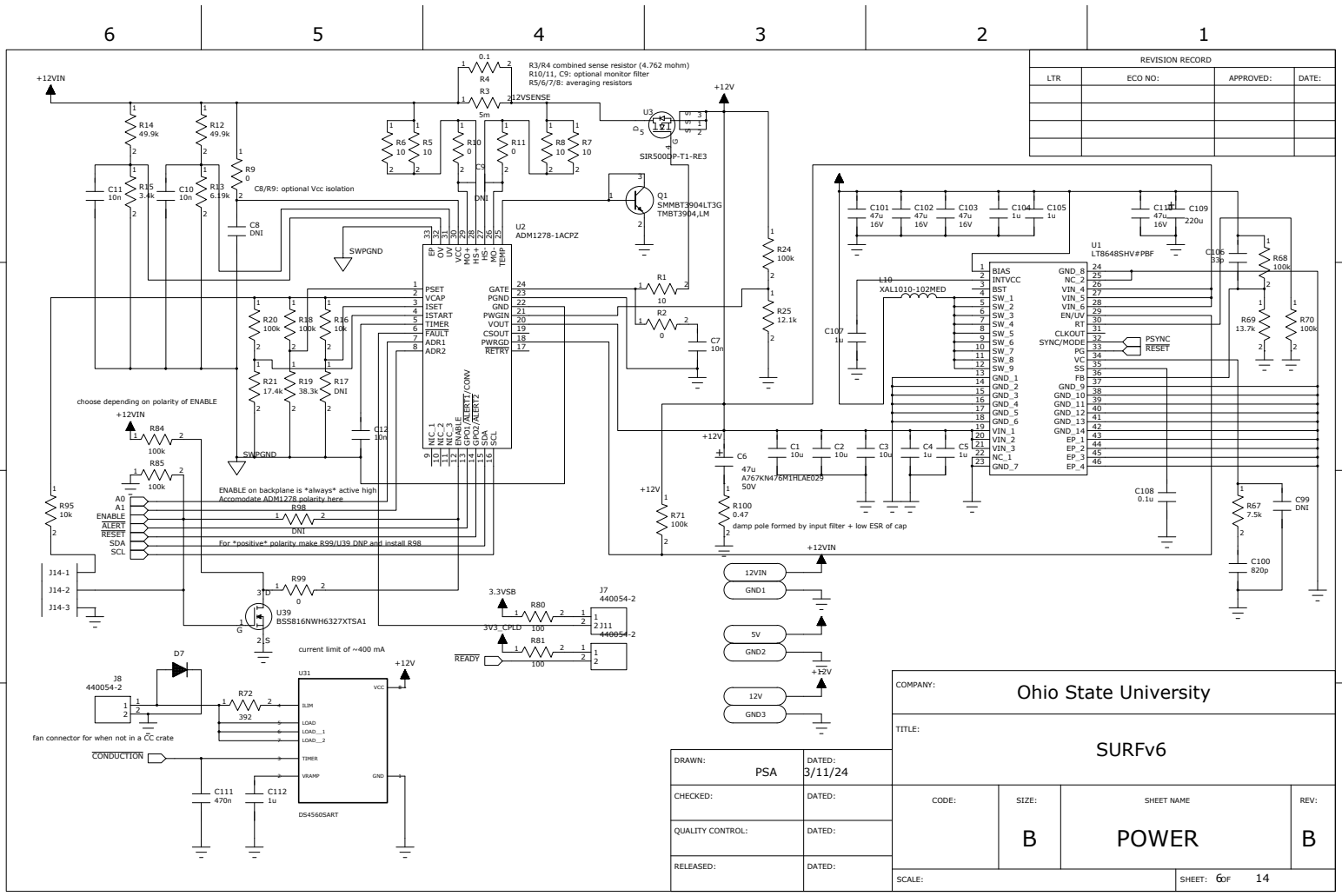

RF Inputs
Inter-polarization Connector
Ethernet output (ix industrial)
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
Front of connector face is at 11.47 mm front
Front panel is at 2.54 past edge
For no machining other than holes, place at 8.93
add 0.5 mm clearance = 9.43
J4
68SM8WB103L461
To put overmold at standard 0.45 mm clearance:
Connector edge must be at 3.84 mm from edge of board!
Kycon flag connector dimensions: nominal has connector 1.5 mm from end of board
We move the connector forward 2.34 mm (to datum at 1.66 mm)
So now the connector edge is 3.84 mm past end of board
This puts it 1.2 mm behind the front face, which is USB standard
Wire this like USB3.0, but can be used for SGMII Ethernet (x2)
or PCI Express (x2)
Requires lanes 0/1 and an exchange switch due to Xilinx stupidity
this inversion is intentional
J5
KUSBX-SL2-CS1N24-B-TR
this inversion is intentional
Pairs are:
1/2 -> 24/23
5/6->20/19
7/8->18/17
11/12->14/13
J10
IX80G-A-10P_01_
flipped on purpose
HX5120NL
shove DisplayPort on the aux connector
J6
FX12B-60P-0.4SV
test points
MOUNTING PADS
X1
CPCI_FP_BOT_BRACKET
X2-1
MTG_HOLE
Alternate power input
+12VIN
J12
1844258
3V3_CPLD
Note: the micro-USB here is hidden behind panel
Not intended for normal use
J15
U40
CH340E
ZK62_B_SPA33
1.8V_CLK
this is located by clock
U45
TXU0202DTTR
DESIGN DETAILS FOR BITELLE:
Exterior: Coupled Microstrip, route as 7 mil trace/11 mil CC-space. Bitelle: 0.1778 mm trace (100.5 ohms @ 4.2)
Interior: Coupled Stripline, route as 7 mil trace/11 mil CC-space. Bitelle: 0.1016 mm trace (106 ohms @ 4.2)
Single-ended 50 ohm is 0.2667 mm and 0.127 interior
D2
D3
D4
D5
ESD8104MUTAG
DRAWN:
PSA
DATED:
3/11/24
CHECKED:
QUALITY CONTROL:
RELEASED:
COMPANY:
Ohio State University
TITLE:
SURFv6
CODE:
SIZE:
B
SHEET NAME
IO
REV:
B
SCALE:
SHEET: 4 OF 14

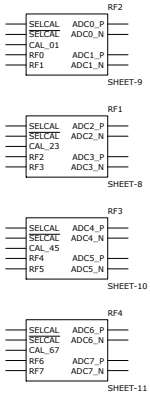


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

This is pin-compatible with:
FUSB303B
TUSB320

DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University	
CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: INTERPOL	REV: B
		SCALE:	SHEET: 5 OF 14


6
5
4
3
2
1
D
C
B
A
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+12VIN
R3/R4 combined sense resistor (4.762 mohm)
R10/11, C9: optional monitor filter
R5/6/7/8: averaging resistors
12VSENSE
SIR500DP-T1-RE3
Q1
SMMBT3904LT3G
TMBT3904,LM
C8/R9: optional Vcc isolation
U2
ADM1278-1ACPZ
SWPGND
U1
LT8648SHV#PBF
L10
XAL1010-102MED
PSYNC
RESET
choose depending on polarity of ENABLE
ENABLE on backplane is *always* active high
Accomodate ADM1278 polarity here
For *positive* polarity make R99/U39 DNP and install R98
damp pole formed by input filter + low ESR of cap
current limit of ~400 mA
fan connector for when not in a CC crate
CONDUCTION
DS4560SART
12VIN
GND1
5V
GND2
12V
GND3
3.3VSB
3V3_CPLD
READY
J7
440054-2
J8
440054-2
J14-1
J14-2
J14-3
U39
BSS816NWH6327XTSA1
D7
U31
U3
COMPANY:
Ohio State University
TITLE:
SURFv6
DRAWN:
PSA
DATED:
3/11/24
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
B
SHEET NAME
POWER
REV:
B
SCALE:
SHEET: 6 OF 14



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN: PSA	DATED: 3/11/24		
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:		

COMPANY: Ohio State University

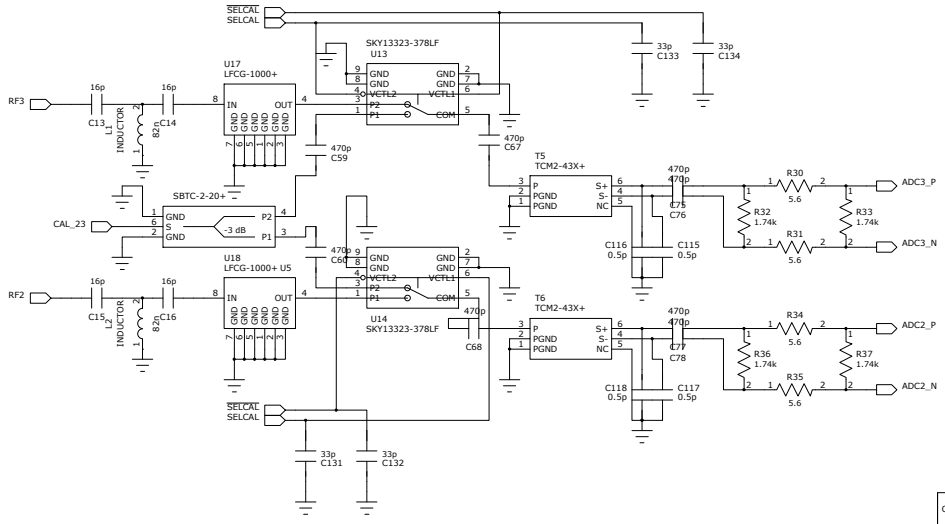
TITLE: SURFv6

CODE:	SIZE:	SHEET NAME	REV:
	B	RF_CHAIN	B

SCALE: SHEET: 7 OF 14

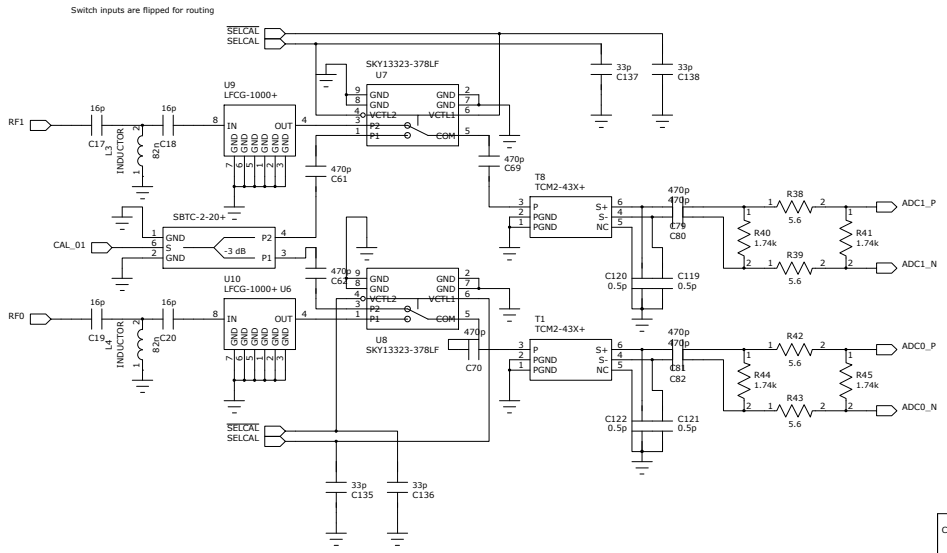
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Switch inputs are flipped for routing



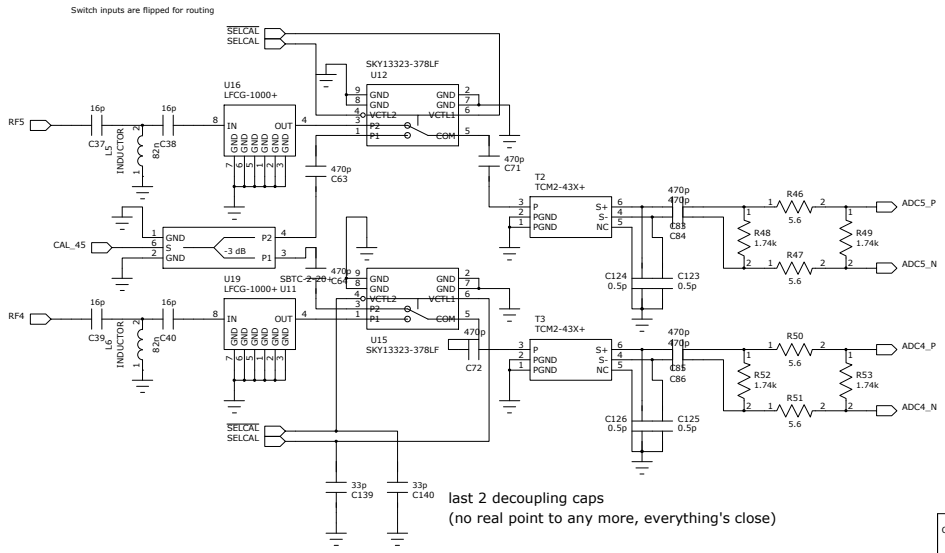
DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University	
CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: RF1	REV: B
		SCALE:	SHEET: 8 OF 14

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University			
CHECKED:	DATED:	TITLE: SURFv6			
QUALITY CONTROL:	DATED:	CODE:	SIZE: B	SHEET NAME: RF2	REV: B
RELEASED:	DATED:	SCALE:	SHEET: 9 OF 14		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



last 2 decoupling caps
(no real point to any more, everything's close)

DRAWN: PSA	DATED: 3/11/24
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: Ohio State University

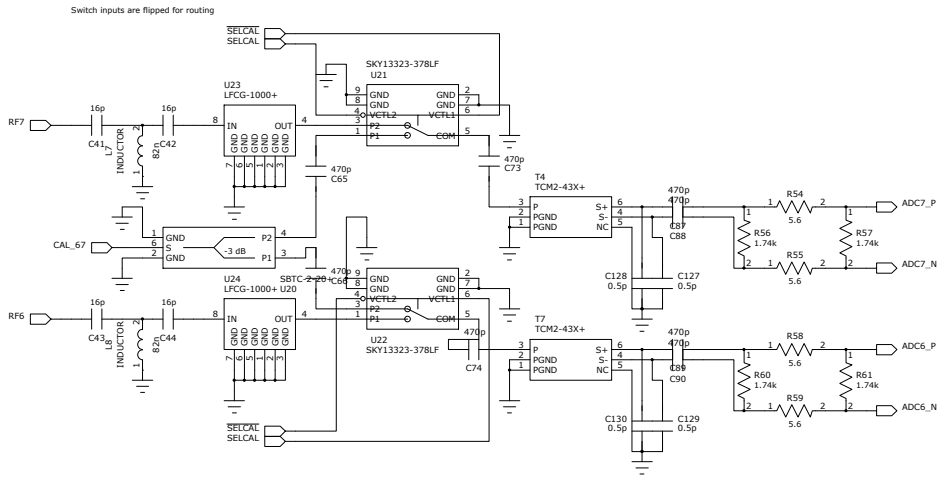
TITLE: SURFv6

CODE:	SIZE:	SHEET NAME	REV:
	B	RF3	B

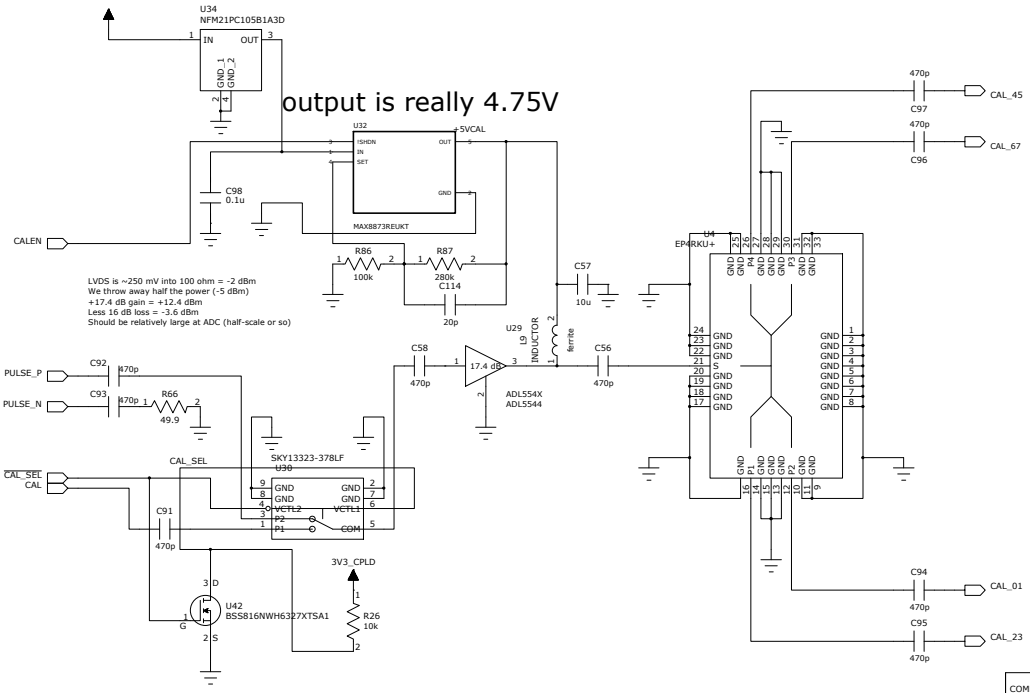
SCALE:

SHEET: 10 of 14

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



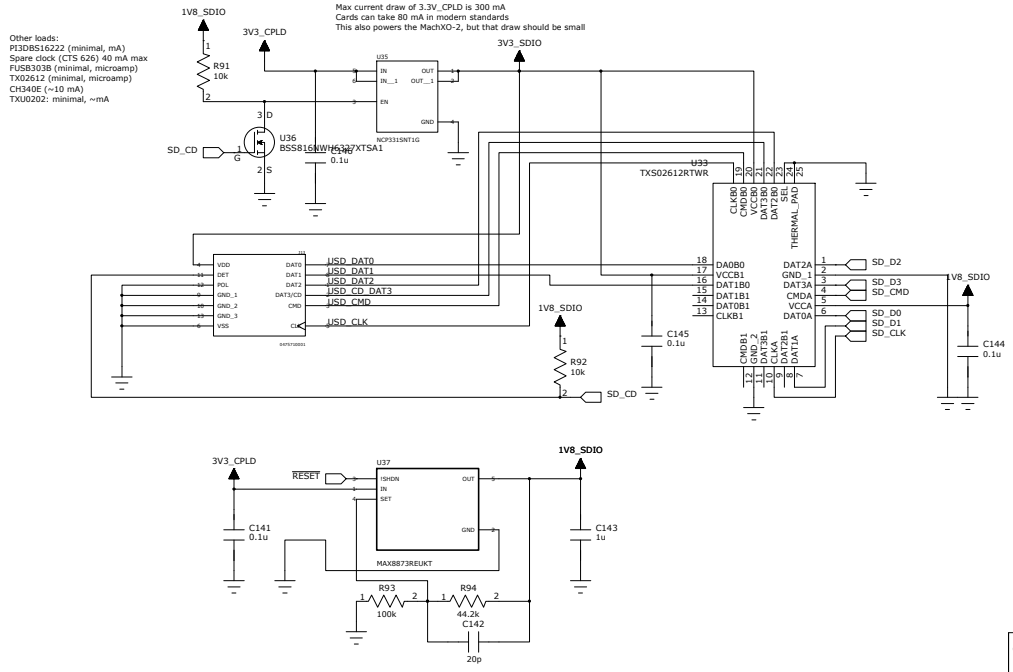
DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University			
CHECKED:	DATED:	TITLE: SURFv6			
QUALITY CONTROL:	DATED:	CODE:	SIZE: B	SHEET NAME: RF4	REV: B
RELEASED:	DATED:	SCALE:	SHEET: 14 OF 14		



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN: PSA	DATED: 3/11/24	COMPANY: Ohio State University	
CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: CAL	REV: B
		SCALE:	SHEET: 12 14

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:	Ohio State University		
TITLE:	SURFv6		
DRAWN: PSA	DATED: 3/11/24	CODE:	SIZE: B
CHECKED:	DATED:	DRAWING NO:	REV: B
QUALITY CONTROL:	DATED:	SCALE:	SHEET: 13 of 14
RELEASED:	DATED:		

6	5	4	3	2	1

REVISION RECORD

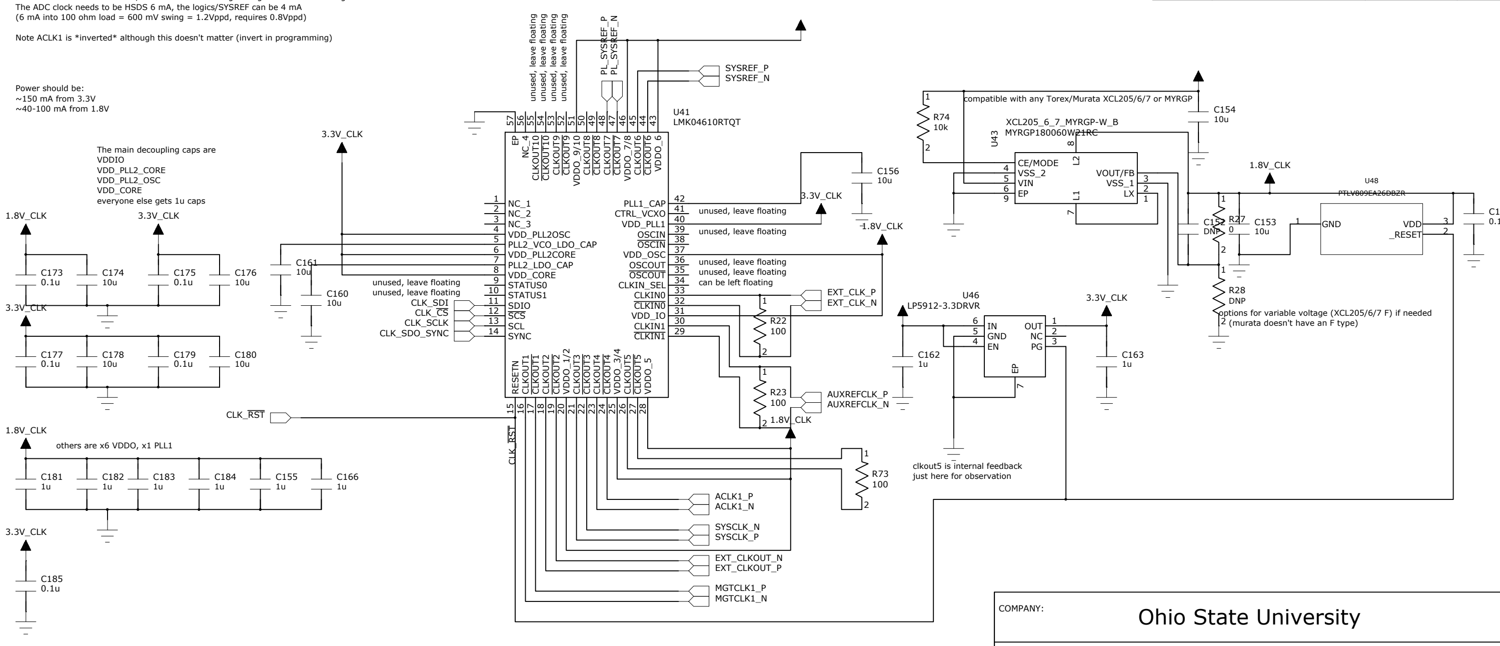
LTR	ECO NO:	APPROVED:	DATE:

RevB adds local clock gen to force phase sync
Our MINIMAL clocks are just ADC clock + PL clock (both 375 MHz)
We add analog/PL sysref and the forwarded clock as options (2 @ 7.8125M, who knows for 3rd)
We need:
ADC clock (1, using internal clock dist)
Analog SysRef
PL SysRef
PL refclk
We relocate ACLK1 to be the ADC clock here.
For the Gen1 devices we have, we clock the remaining through the onboard clockgen
The ADC clock needs to be HSDS 6 mA, the logics/SYSREF can be 4 mA
(6 mA into 100 ohm load = 600 mV swing = 1.2Vppd, requires 0.8Vppd)

Note ACLK1 is *inverted* although this doesn't matter (invert in programming)

Power should be:
~150 mA from 3.3V
~40-100 mA from 1.8V

The main decoupling caps are
VDDIO
VDD_PLL2_CORE
VDD_PLL2_OSC
VDD_CORE
everyone else gets 1u caps



COMPANY:	Ohio State University
TITLE:	SURFv6

DRAWN: PSA	DATED: 3/11/24
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

CODE:	SIZE:	DRAWING NO:	REV:
	B		B

SCALE: SHEET: 14 14