TURF Specification Document
PSA 3/1/22

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1 Overview

A simple diagram for the TURF is shown.

2 TURFIO/TURF Communication

The TURFIO/TURF communicate via a Molex iPass/PCIe x8 cable assembly. Generally any Molex cable beginning with "74546-08" will work: surplus stock may be more readily available (e.g. 74546-0840, etc.).

These cables consist of 16 primary differential pairs and 6 sidebands. The differential pairs cross over internally to the cable, therefore there is a "TURFIO" pinout side and a "TURF" pinout side.

2.1 Commanding

The TURF communicates with the SURFs via a source-synchronous LVDS serial link. Since the commanding should not be high volume, the data rate on this is not critical but would prefer to be relatively high - a target of 750 Mbps+ is reasonable (375 MHz DDR). Since the TURFIO is a 7-series device, this requires that the interface should be component-mode rather than native-mode. The commanding interface both configures the SURFs and receives/distributes triggers. This interface is synchronous and fixed-latency, hence the choice of 375 MHz (1/8th the sample clock of 3 GHz) for the data rate. TURF commands are issued common to all SURFs (on COUT+/-), but each SURF has an individual input path (CIN[6:0]+/-) to ensure that trigger inputs can be simultaneously received.

TURFIO-specific command responses are received on a separate path (CINTIO+/-), and a separate single-ended (asynchronous, UART-style) slow-control command path (RX/TX) is also available.

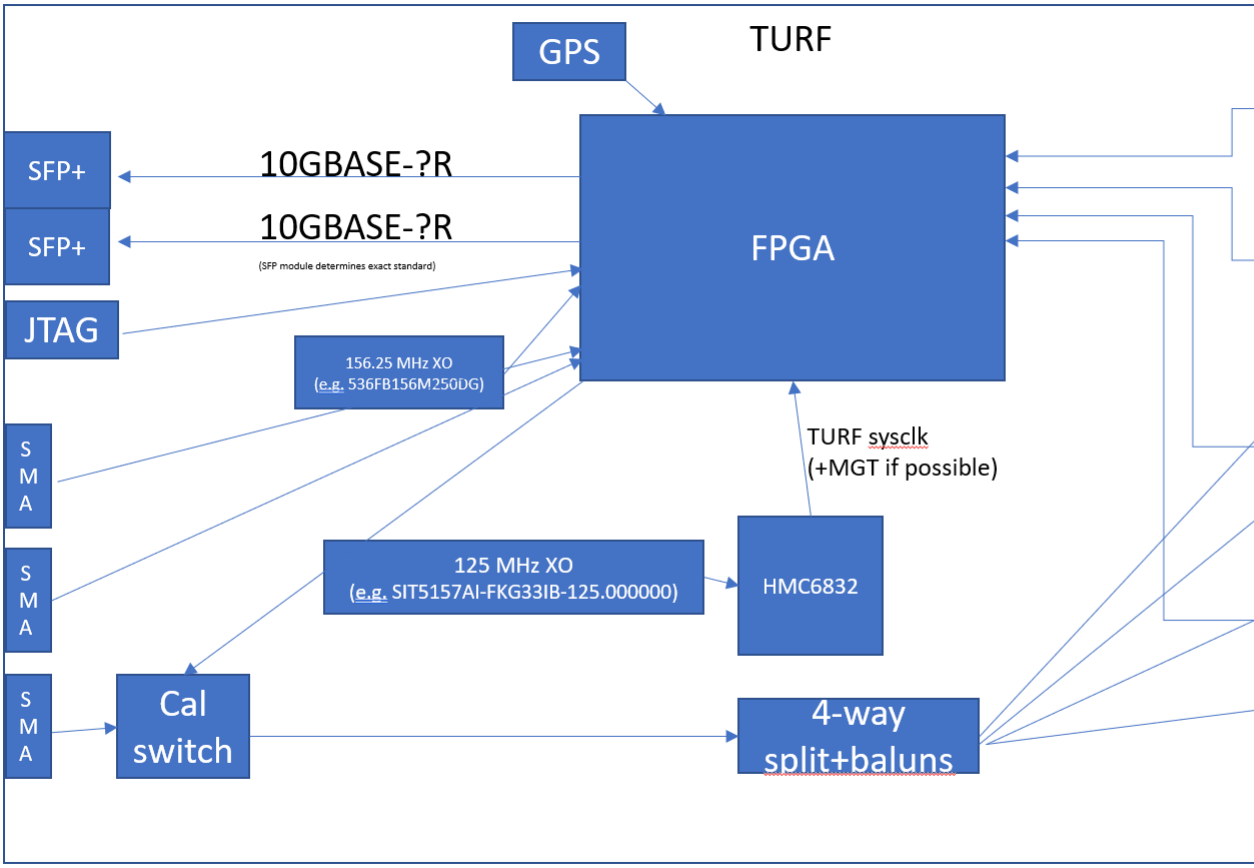

Figure 1: Simple diagram for TURF.

TURF name	TURF pin(s)	TURFIO pin(s)	TURFIO name	Function
MGTTX+/-	A2/A3	B2/B3	MGTRX+/-	Outbound TURF transceiver
MGTRX+/-	B2/B3	A2/A3	MGTTX+/-	Inbound TURF transceiver
MGTCLK+/-	A5/A6	B5/B6	MGTCLK+/-	**Reserved** (was transceiver clock)
CLK+/-	B5/B6	A5/A6	CLK+/-	System clock
TXCLK+/-	A8/A9	B8/B9	RXCLK+/-	Inbound control data clock
RXCLK+/-	B8/B9	A8/A9	TXCLK+/-	Outbound control data clock
COUT+/-	A11/A12	B11/B12	CIN+/-	Control data from TURF
CINTIO+/-	B11/B12	A11/A12	COUTTIO+/-	Control data from TURFIO
CIN0+/-	A23/A24	B23/B24	COUT0+/-	Control data from SURF0
CIN1+/-	B23/B24	A23/A24	COUT1+/-	Control data from SURF1
CIN2+/-	A26/A27	B26/B27	COUT2+/-	Control data from SURF2
CIN3+/-	B26/B27	A26/A27	COUT3+/-	Control data from SURF3
CIN4+/-	A29/A30	B29/B30	COUT4+/-	Control data from SURF4
CIN5+/-	B29/B30	A29/A30	COUT5+/-	Control data from SURF5
CIN6+/-	A32/A33	B32/B33	COUT6+/-	Control data from SURF6
SPARE+/-	B32/B33	A32/A33	SPARE+/-	Spare differential pair
CAL+/-	A14/A15	A14/A15	CAL+/-	Calibration signal
RX	A20	A20	TX	Slow control TURF inbound
TX	A21	A21	RX	Slow control TURF outbound
RSVD0	B20	B20	RSVD0	reserved (GPIO) signal
RSVD1	B21	B21	RSVD1	reserved (GPIO) signal

Table 1: Pinout of the TURFIO/TURF cable. Note that the 16 primary pairs are crossed over internal to the cable. Sidebands are not. Signals are arranged such that everything but the SURF data pairs (CIN0-6) and the CLK/MGTCLK matches the direction in the PCIe specification. This mapping was chosen to minimize possible TURF/TURFIO mapping errors.

2.2 Data path

The TURF receives data from the SURFs via a multi-gigabit transceiver link from the TURFIO (MGTTX/MGTRX) which collects and buffers all data from the SURFs. The TURFIO supports up to a 3.75 Gbps signal rate which should be more than sufficient: in aggregate this is 1.5 GB/s, corresponding to over 3 kHz total payload rate. In addition, a return transceiver path from the TURF to TURFIO supports high-rate data transfer or an alternate commanding path.

2.3 Calibration signal

The TURF also transmits an RF calibration signal which can be switched into the input ADC path. The origin of this signal is uncertain at the moment.

2.4 Clocks

The TURF outputs the system clock (CLK+/-) to each of the TURFIOs. The MGT clock originally was pushed via MGTCLK+/-, however, for simplicity, this clock was dropped. Instead, the MGT clock is located at the TURFIO (e.g. ECX2-LMV-3CN-125.000-TR) since the datapath does not have to be synchronous.

The clock fanout used is an HMC6832 2:8 clock fanout configured in LVDS mode. The source oscillator must be a multiple of 7.8125 MHz and greater than 23.4375 MHz. This is to accomodate the SYSREF frequency plan and ensure that the TURFIO input frequency (which must be divided by a minimum of 2) is above the minimum frequency for the MMCM/PLL in the FPGA. If a 125 MHz(or 156.25 MHz) clock source is used, one of the HMC6832 outputs can be used as the GTP reference provided the phase noise meets GTP specifications.

A viable option would be a SIT5157AI-FKG33IB-125.000000.

Phase noise requirements at 125 MHz for GTH transceivers are -113 dBc/Hz at 10 kHz, -132 dBc/Hz at 100 kHz, -138 dBc/Hz at 1 MHz. This covers QPLL support: CPLL support should not be needed as all GTPs in a quad should be running at equal rates. Note that the HMC6832 phase noise contribution can be neglected, as the additive phase noise is more than 20 dBc/Hz below these requirements.

3 SFC I/O

The TURF communicates with the SFC using 10GbE via an SFP+ connection. While the commercial Xilinx 10G IP is relatively expensive ($10K+) an open-source implementation exists at https://github.com/alexforencich/verilog-ethernet . Two SFP+ connections should be supported for redundancy.

3.1 10G Clock

The 10GbE clock must meet phase noise requirements above as well. This likely should be standalone from the system clock, however if a 156.25 MHz clock can be used, this will also meet 10GbE standards. It therefore may make sense to route one of the HMC6832 clocks to one MGT reference clock, and a standalone clock (e.g. 536FB156M250DG) to the other, optionally powering down the standalone clock if the system clock can meet requirements.

3.2 GPIOs

The TURF should have 2 GPIOs minimum to interface with the outside world with buffers to isolate the FPGA.

4 GPS Interface

The TURF should have an interface to the timing GPS. This allows for the TURF to directly determine system timing.

5 Cal interface

The TURF should take a calibration input on an SMA connector and fan it out to all 4 TURFIOs through baluns. In addition, a SPDT RF switch should allow switching in a high-speed calibration signal from the FPGA.

6 Debug interface

The TURF should have an external interface to allow for JTAG system debugging. Due to availability a Digilent JTAG-SMT3-NC may be the best option.

7 Total FPGA I/O

The total **minimum** FPGA I/O count requirement is therefore

- 4x MGT links to TURFIO
- 44x LVDS links to TURFIO (excluding SPARE+/-)
- 16 single-ended signals to TURFIO (including 2 reserved each)
- 2x MGT links to SURF
- Additional single-ended signals (likely 2 for I2C, 1 for GPS input, 1 for trigger in/out, and 2 for global cal pulser = 6)

This totals to 6 MGT links, 44 LVDS pairs, and 22 single-ended signals. This should fit comfortably in the iWave Systems ZU11 module I/O.