Final SURFv6C design

PSA

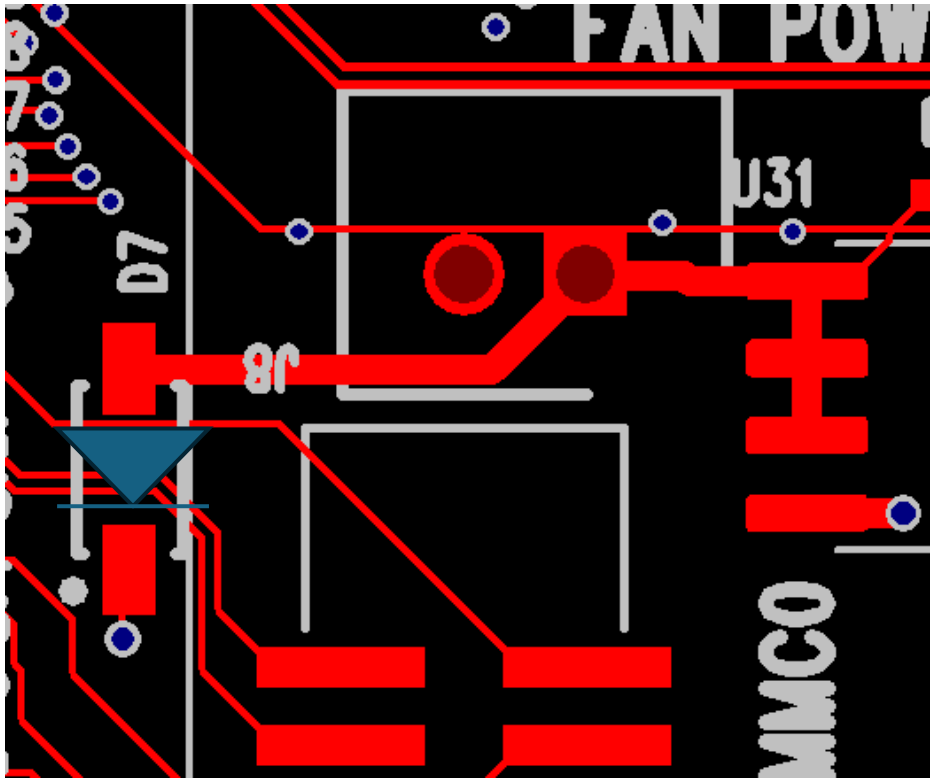
Checklist

1. ~~Freewheel diode orientation fix~~
2. ~~VCAP decoupling cap on ADM1278~~
3. ~~TXU0202 pinout fix~~
4. ~~Remove 1.8V_CLK supervisor, replace with pullup~~
5. ~~Add 74AVC4T774 buffer between TE0385<->RACK JTAG powered by 3.3VSB~~
6. ~~Add DT1446S diodes to TE0835 JTAG, remove RX/TX from connector~~
7. ~~Add MGTCLK0/1 AC coupling caps~~
8. ~~Switch Y2 626L10005I3T => SG2520VHN 156.2500M-ECHPZA6~~

https://github.com/barawn/pueo-daq-design/tree/main/SURFv6revC

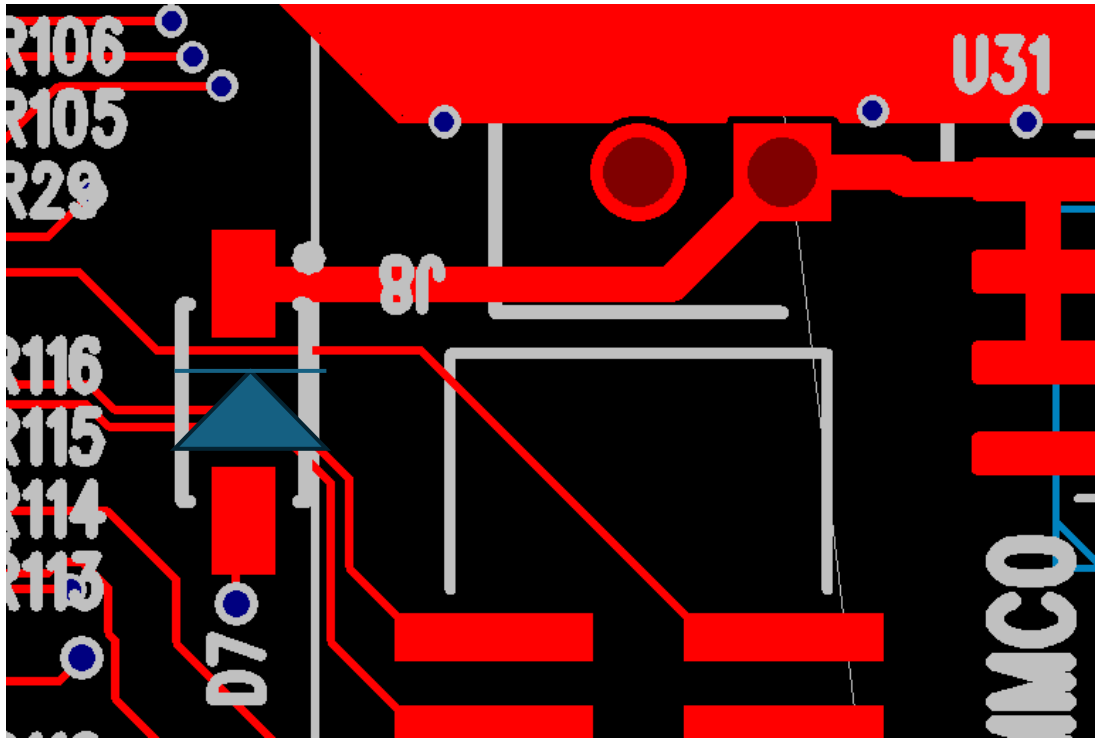
Freewheel diode (high current draw, no fan)

RevB (diode points to ground)



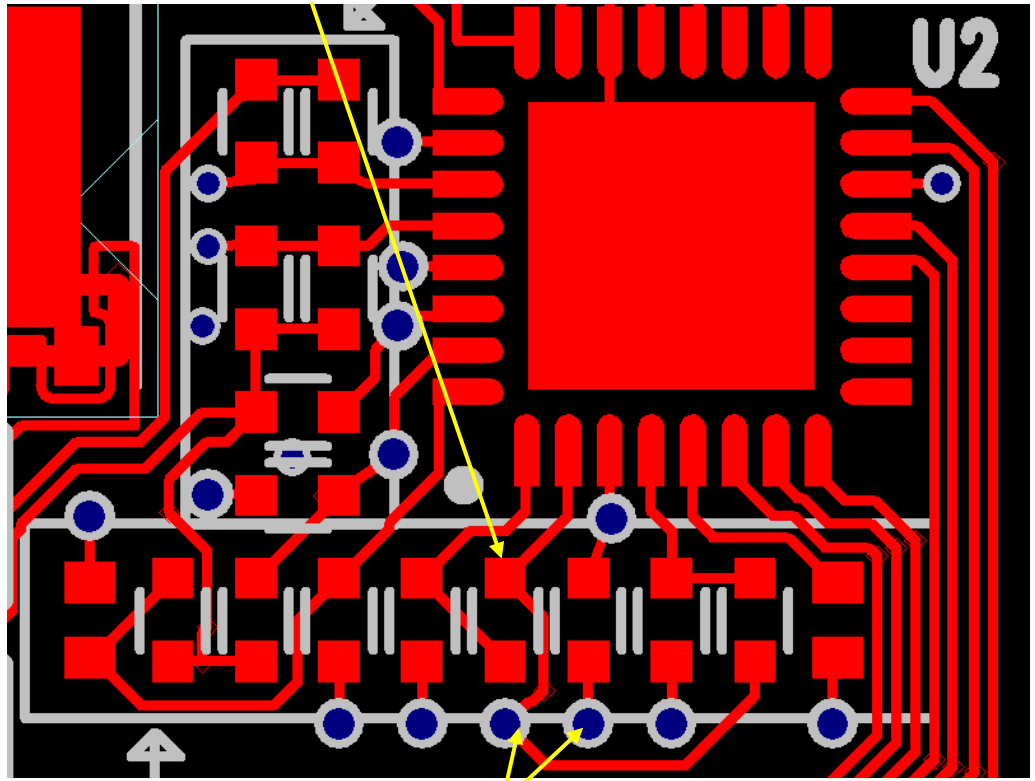
(ECO was just to flip the diode around)

RevC (diode points to power)



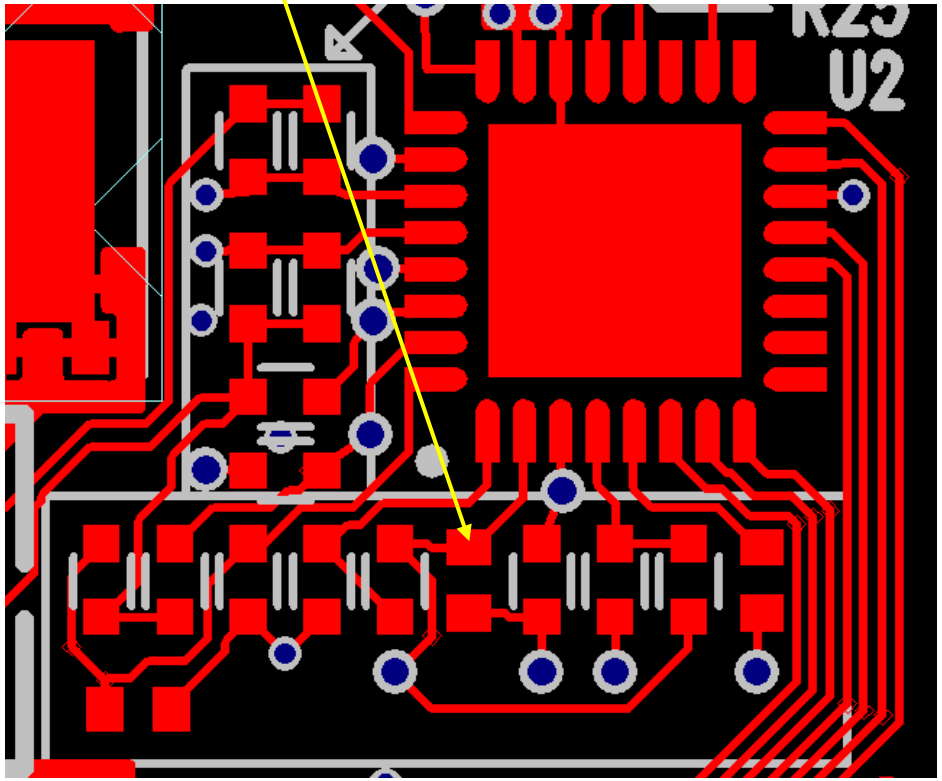
VCAP decoupling cap (unstable swap operation)

RevB: No VCAP decoupling



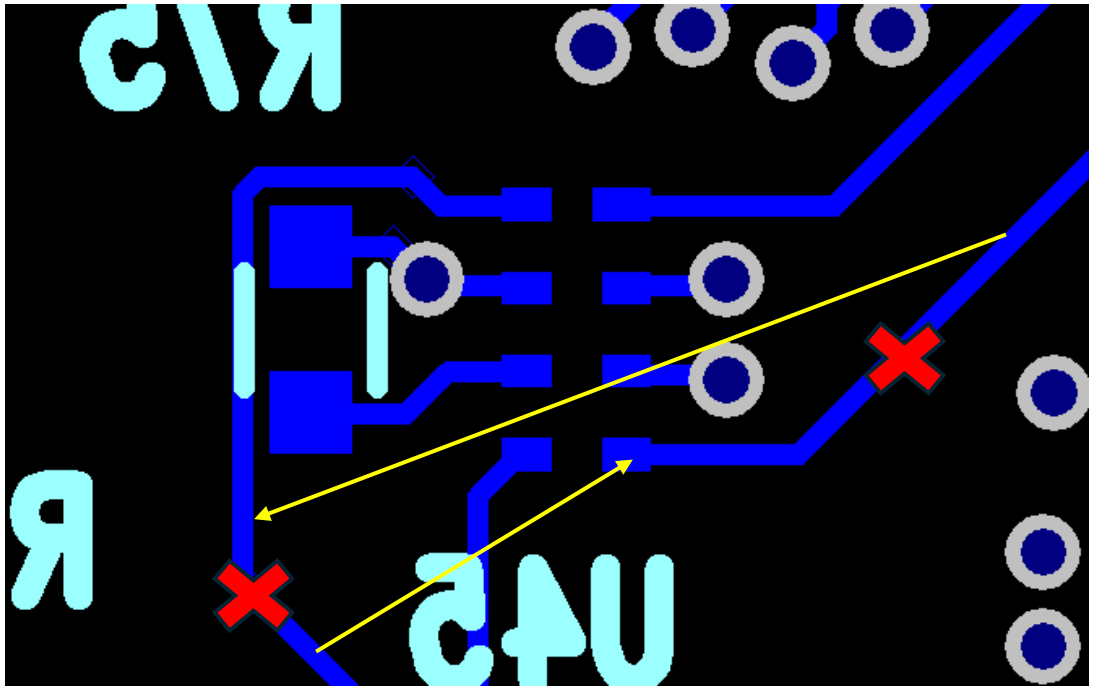
(ECO just added a cap between these vias)

RevC: VCAP decoupling

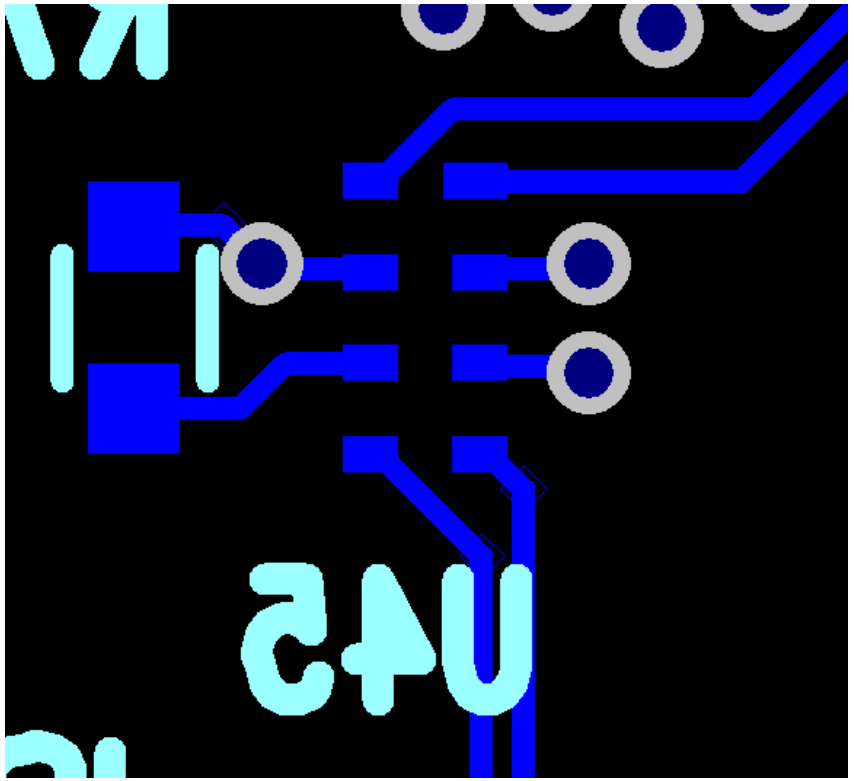


TXU0202 pinout (debug UART broken, pins swapped)

RevB: signals connected “L/R”



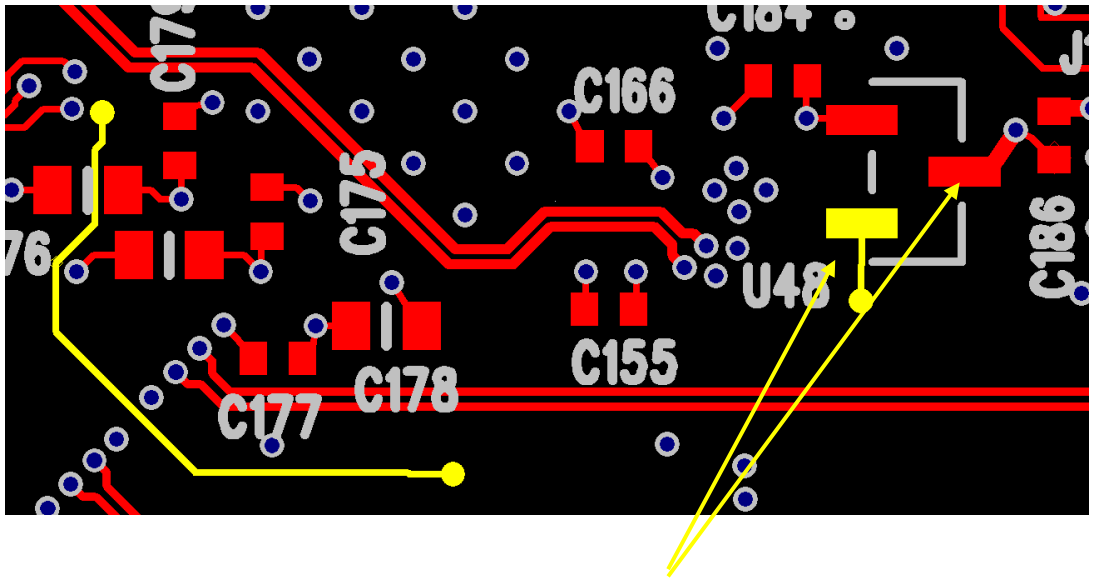
RevC: signals connected “T/B”



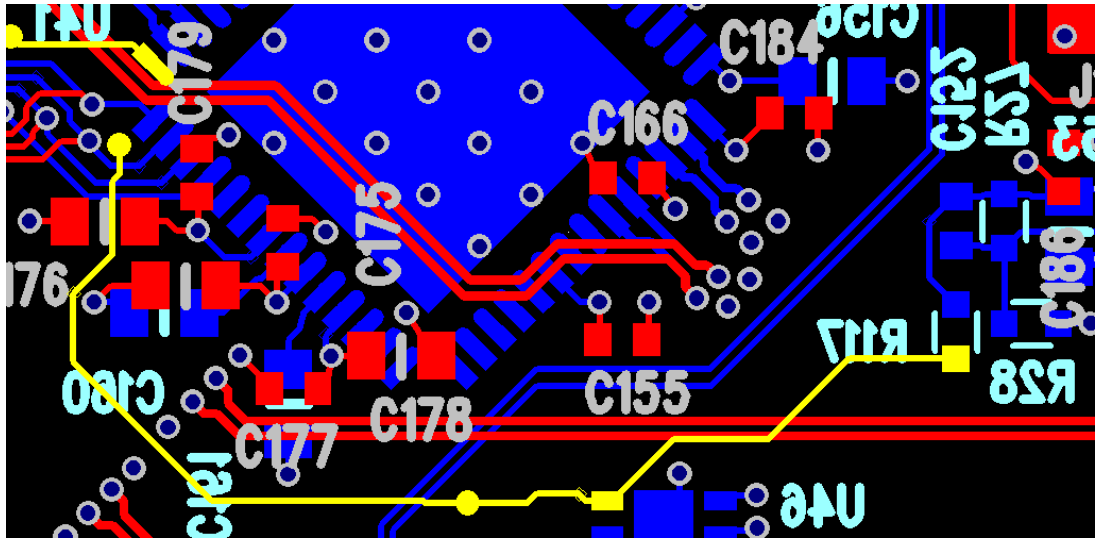
ECO is to cut and jumper

Remove 1.8V supervisor and pull up
(LMK reset held low, wrong part, correct part doesn't exist)

RevB: nonfunctional supervisor



RevC: only pullup

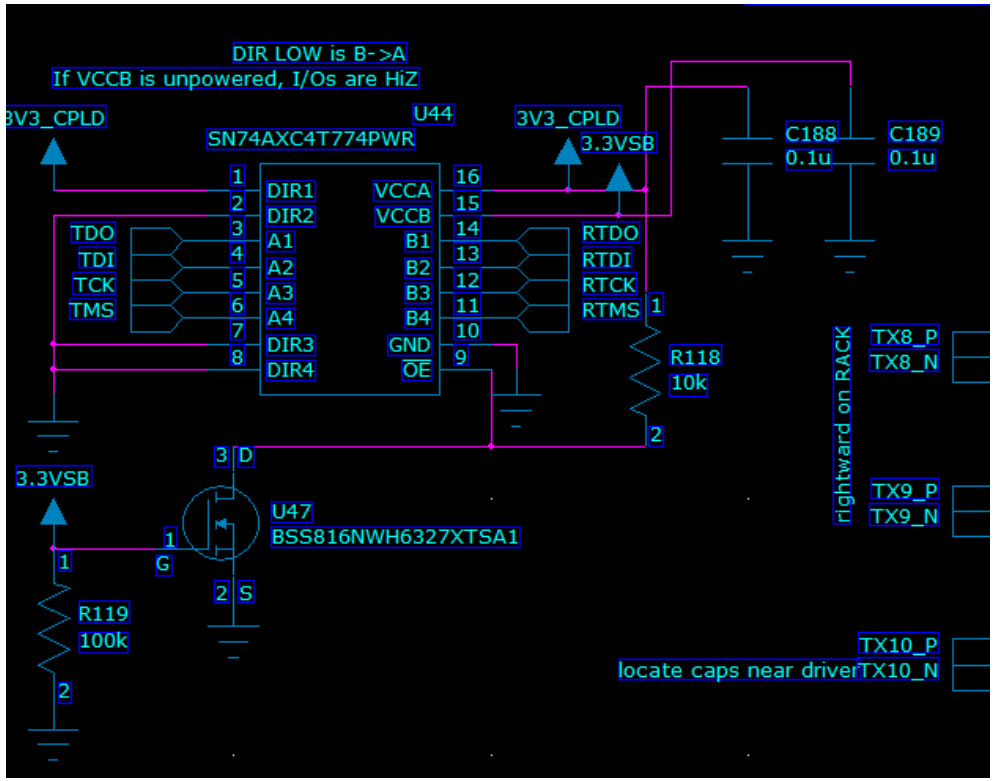


ECO is to just remove U48 and stick resistor across pads

Add 4T774 buffer to RACK JTAG

(with 3.3VSB off, TE0835 is driving into unpowered CPLD, maybe vice versa too)

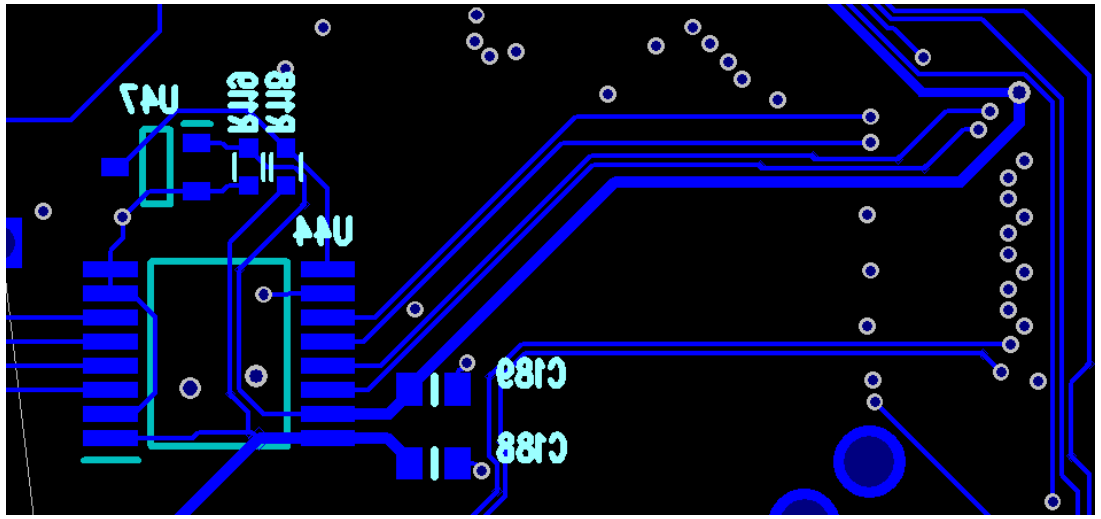
Schematic change (DIR L=B->A)



/OE transistor is needed due to inverted polarity

If need to isolate for some reason just pull U47

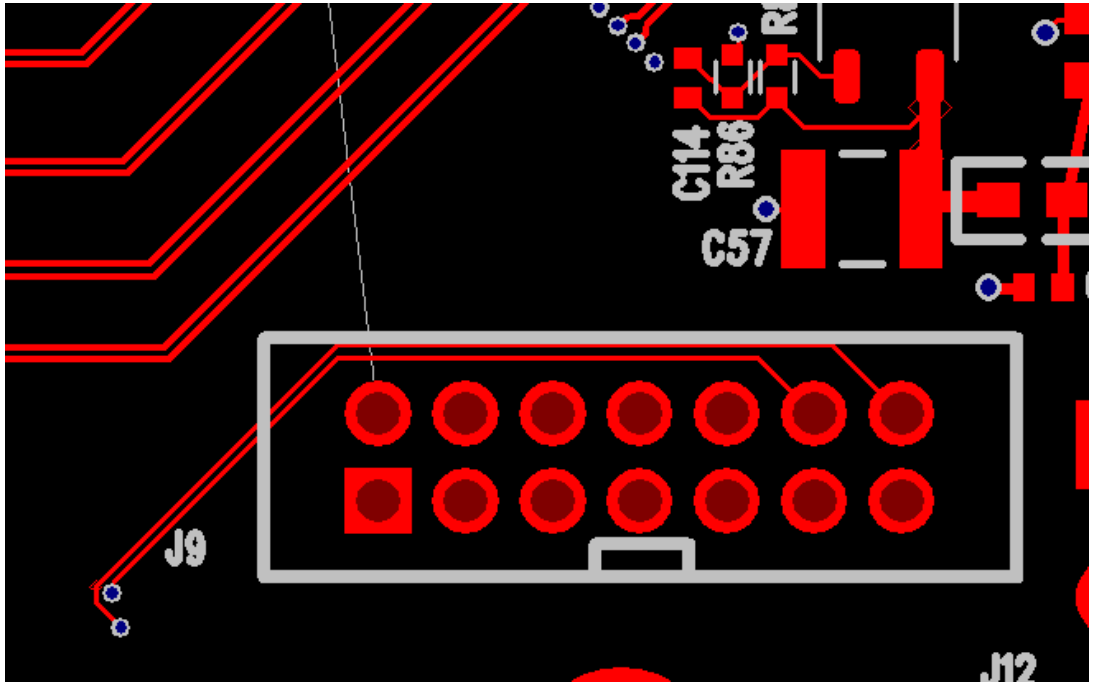
Layout



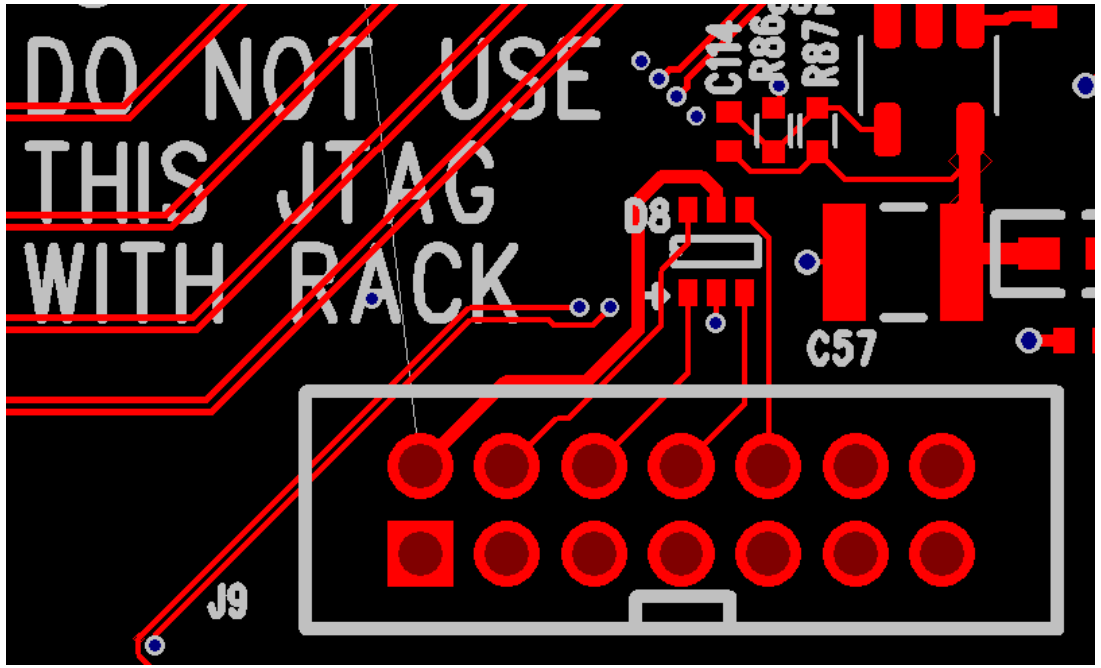
ECO for revB is probably cut-and-jumper using a patch board or something

Add DT1446 diodes to JTAG (ESD), drop RX/TX
Also added use warning. Not a risk to TE0835, only to buffer
RX/TX unneeded and risky anyway (direct MIO connection to TE0835)

RevB: no ESD protection, RX/TX



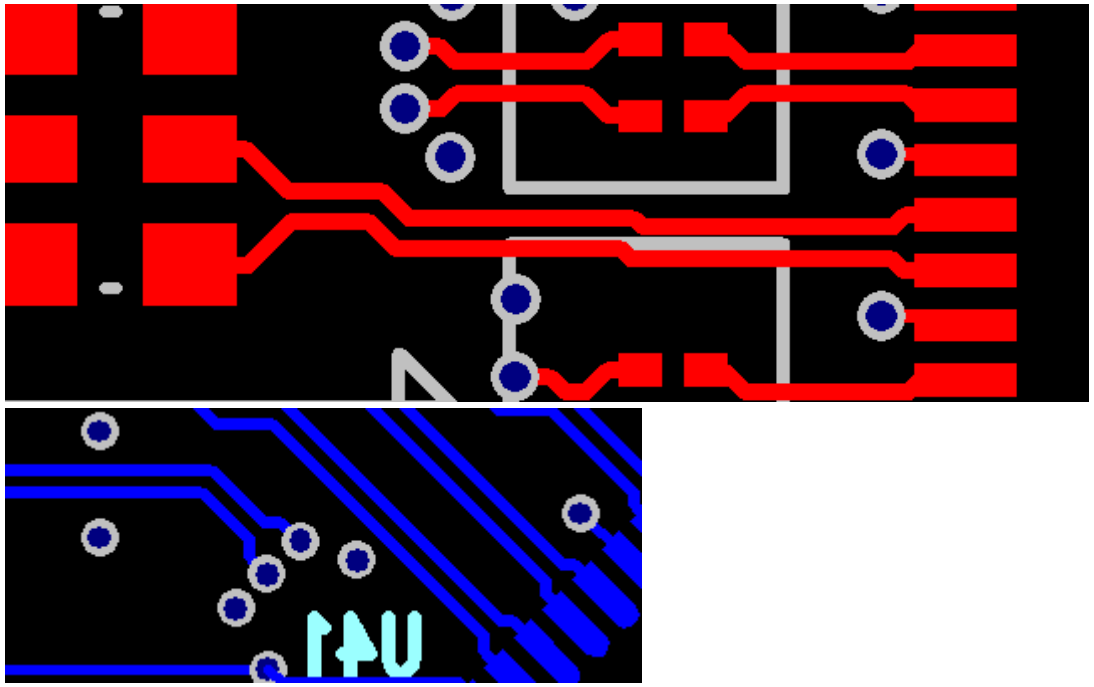
RevC: ESD diode+warning, no RX/TX



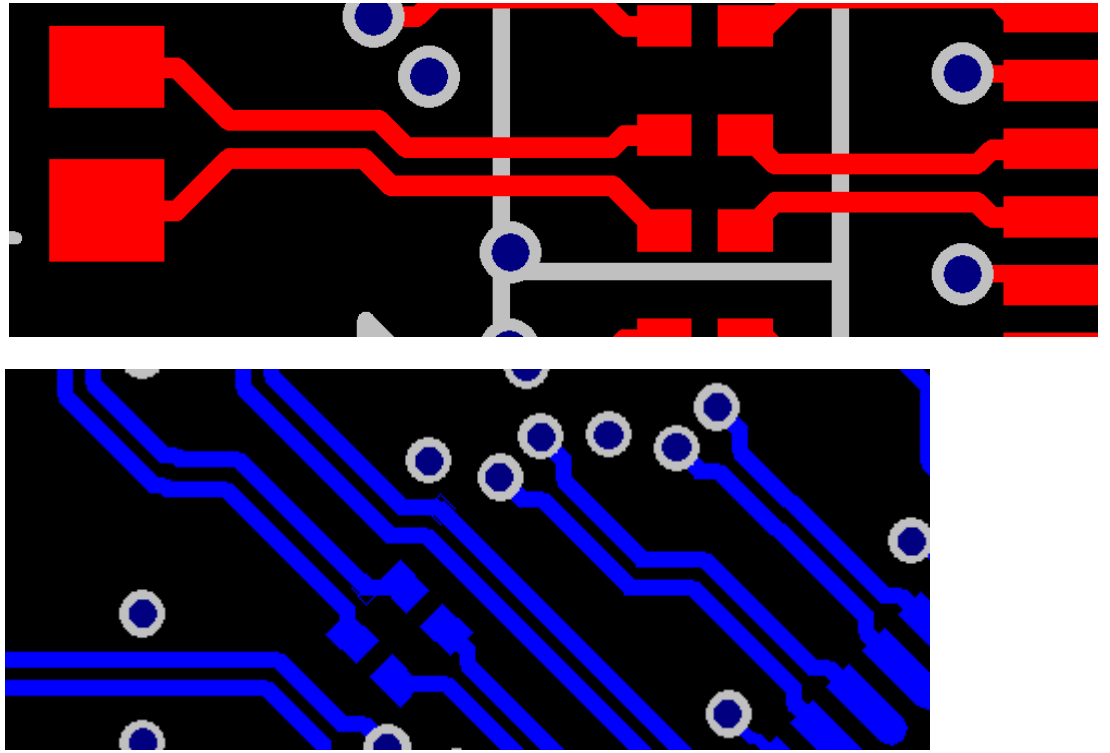
ECO adds label (+ESD diodes on patch board)

AC coupling caps for MGTCLK
(no apparent problems but bad practice)

RevB: direct connections



RevC: AC coupling caps



ECO is cut traces and insert either near vias or pads

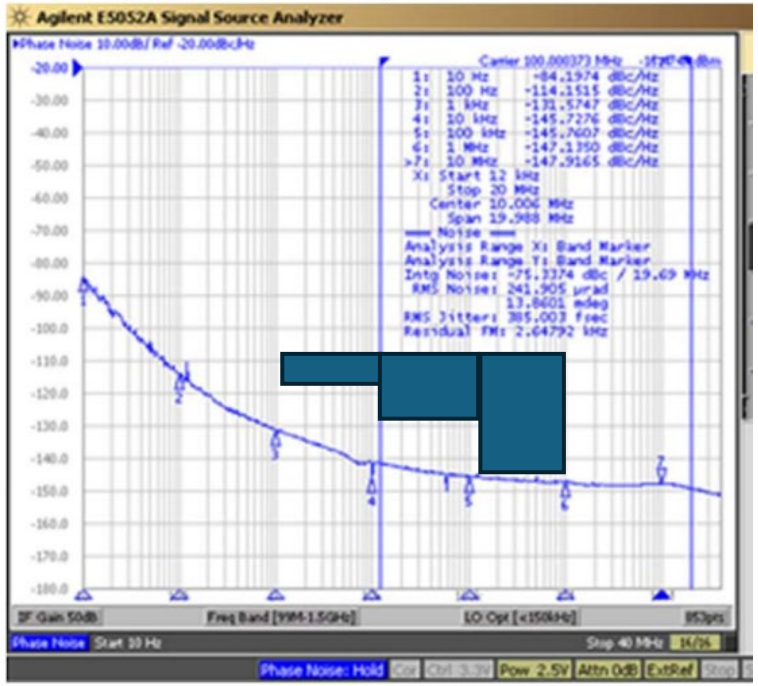
MGT onboard clock switch

(only schematic/layout change is 3.3VCPLD->1.8V_CLK)
Reduce load on 3.3V_CPLD, phase noise only slightly increases
Option to switch back to 3.3VCPLD

626L10005I3T

Phase Noise [typical]

100MHz, LVDS, V_{CC} = +2.5V, T_A = +25°C

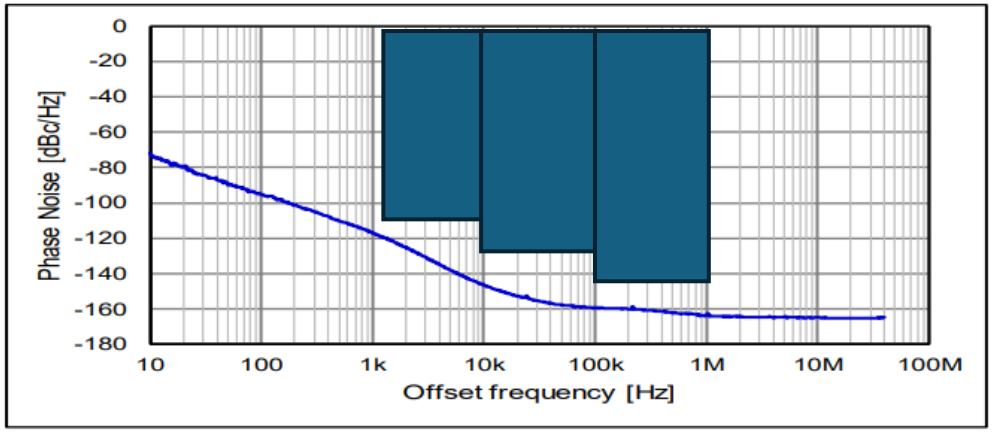


n.b. this is 100M so *significantly* worse

SG2520

Typical Performance

Phase Noise (fo = 156.25 MHz, V_{CC} = 3.3 V)

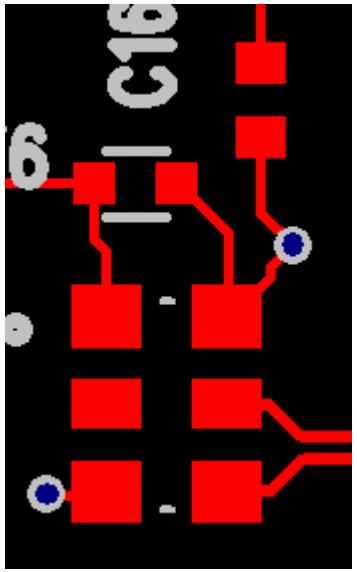


Phase Jitter (12 kHz to 20 MHz): 38 fs Typ.

Symbol	Description [1, 2]	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	

3.3V/1.8V power option

RevB: only 3.3V_CPLD



RevC: either 1.8V or 3.3V (1.8V nom)