CHANGELOG:
Rev B (3/2/2024)
1. remove RX/TX MIO connection (wrong voltage) - use EMIO only
2. add LMK04610. SYS_CLK goes to LMK04610, outputs to ADC1 CLK, SYSREF, PL, PL_SYSREF, EXT_CLK_IN
3. flip LED light pipe mounting holes
4. add cheap USB UART for serial console and level translation for RX/TX
5. remove L1/L16 connections to daughterboard to open up pins, hook I2C to daughterboard for add'l connectivity
6. use transistors to invert $\overline{\text{CAL\_SEL}}$ to save pin
7. drop optional clock rerouting and just directly connect DCLK0/DCLK1
8. replace custom ethernet connector with ix industrial and add magnetics
9. add auxiliary eMMC/SD connector + swap MIOs around
10. add serial termination resistors to both SD ports

LMK04610 requires new 3.3V and 1.8V regulators, plus supervisor to hold in reset
LMK04610 can be programmed from PL or PS side

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SI5395 (ON TE0835) CONFIG
CLK0: ADC2 clock (224)
CLK1: unused
CLK2: ADC0 clock (226)
CLK3: ADC3 clock (227)
CLK4: DAC1 clock (229)
CLK5: DAC0 clock (228)
CLK6: MGT B128 CLK0
CLK7: MGT B129 CLK0
CLK8: to PL
CLK9: PSMGT clock
CLK9A: ext clock out (to LMK04610)

SI5395 (ON TE0835) with GEN1 STANDALONE
CLK0: 375M
CLK1: off
CLK2: 375M
CLK3: 375M
CLK4: 375M during MTS, off otherwise
CLK5: off
CLK6: off
CLK7: off
CLK8: off
CLK9: off
CLK9A: 15.365M out

SI5395 (ON TE0835) with GEN3 IN PUEO
CLK0: off
CLK1: off
CLK2: off
CLK3: off
CLK4: 375M during MTS, off otherwise
CLK5: off
CLK6: off
CLK7: off
CLK8: off
CLK9: off
CLK9A: off
POWER DOWN when out of MTS
(write 1 to 0x001E)

LMK04610 (ON SURF) CONFIG
CLK1: MGT - 100M
CLK2: ext clk to Si5395 (off)
CLK3: pl sysclk (375M)
CLK4: aclk (375M)
CLK5: feedback (15.365M, no output)
CLK6: 7.8125M during MTS, off otherwise
CLK7: 7.8125M during MTS, off otherwise
CLK8: off
CLK9: off
CLK10: off
After MTS, CLK6/7 can disable output and the CLK6-10 buffer can be disabled

With GEN1 STANDALONE, input is CLKIN1
In PUEO, input is CLKIN0

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Peripherals already taken:
I2C1
UART1
GEM3
USB0

I2C0 is every 2/3 in groups of 4
(same as UART)
RX/SCL = (MIO % 4) == 2
TX/SDA = (MIO % 4) == 3

PCB in 3D view is at 59.5, 5, 6.5

MGTs 0-3 are PS-GTRs

this side is crowded

this is 1-6, 8-9, 11-13, and 16

all bank65

SS5-80-3.00-L-D-K-TR
J1

SS5-80-3.00-L-D-K-TR
J2

GTYs are bank 128 and bank 129 (ch4-11)
These get used for interphi
GTRs are bank 505 (ch0-3)
These get used for interpol

USB0_CPEN is an output to turn on the +5V load switch
We use Type-C so we figure this out separately

this is our extra PSMGT clock

(inverted)

GC input
GC input

XADC inputs are (B65)
L3 (AD15)
L4 (AD7)
L5 (AD14)
L6 (AD6)
L8 (AD5)
L9 (AD12)
and B88
L9 (AD11)
L10 (AD10)
L11 (AD9)
L12 (AD8)

supply PSBATT in case we use RTC

U38
MAX6101EUR+T

no caps needed (on TE0835)
and MAX6101 stable w/no caps

S1
CHS-06TA

revC: no RX/TX connection,
add ESD diodes

these can force USB to src/sink

these are no-connects, for light pipe

JTAG_2MM

DT1446

auxiliary SD/eMMC connector
note that these are 1.8V I/Os

n.b. RX should be 4 mA drive to limit current into TURFIO bank

these are B88 L5-12
(3.3V)

Single ended 50 ohm (outer): 0.31 mm (inner) 0.125 mm
Diff pairs are routed with 0.4572 channel width
(but spacing is very wide, so width+space=0.2794 is OK)
outer = 0.1494/0.13 (98.6 ohm)
inner = 0.1016/0.2172

DIALIGHT-515-1071-LED

DIALIGHT-515-1071-PIPE

standard 2.5mm x 2 mm package w/OE on pin 1

SG2520VHN 156.2500M-ECHPZA6

standard 2.5mm x 2 mm package w/OE on pin 1

REVISION RECORD

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TITLE: SURFv6

CODE:	SIZE:	SHEET NAME:	REV:
	B	TE0835	B

SCALE:

SHEET: 2 OF 14

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Horizontally this switches left/right at the RACK
(so connecting 25->75 goes right, 75->25 goes left)

RXCLK+/- need to go to global clock
11, 12, or 13

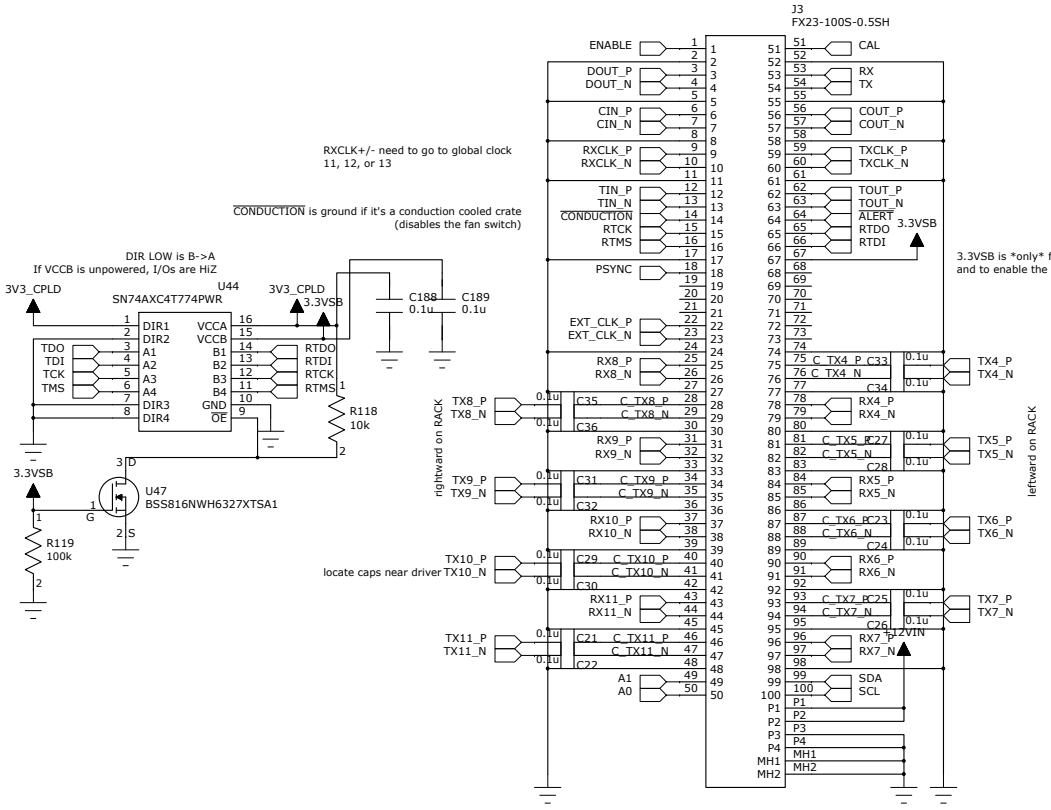
CONDUCTION is ground if it's a conduction cooled crate
(disables the fan switch)

DIR LOW is B->A
If VCCB is unpowered, I/Os are HiZ

3.3VSB is *only* for indicators
and to enable the JTAG buffer

RXCLK is B65 L12_N/P (global clock): 34.1 mm
TXCLK is B65 L6_N/P: 24.5 mm
COUT is B65 L3_N/P: 21.8 mm
CIN is B65 L4_N/P: 28.5 mm
Match CIN to RXCLK (+5.6) and COUT to TXCLK (-2.7)

TXCLK = 24.5 + 105.3 = 129.98
COUT = 21.8 + 108.15 = 129.95
RXCLK = 34.1 + 104.3 = 138.4
CIN = 28.5 + 109.9 = 138.4



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QUALITY CONTROL:	DATED:	CODE:	SIZE: B
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RF Inputs

Front of connector face is at 11.47 mm front
Front panel is at 2.54 past edge
For no machining other than holes, place at 8.93
add 0.5 mm clearance = 9.43

J4
685M8W8103L461

RF4
RF5
RF6
RF7
RF0
RF1
RF2
RF3

Inter-polarization Connector

To put overmold at standard 0.45 mm clearance:
Connector edge must be at 3.84 mm from edge of board!
Kycon flag connector dimensions: nominal has connector 1.5 mm from end of board
We move the connector forward 2.34 mm (to datum at 1.66 mm)
So now the connector edge is 3.84 mm past end of board
This puts it 1.2 mm behind the front face, which is USB standard

Wire this like USB3.0, but can be used for SGMII Ethernet (x2)
or PCI Express (x2)
Requires lanes 0/1 and an exchange switch due to Xilinx stupidity

J5
KUSBX-SL2-CS1N24-B-TR

this inversion is intentional

SSTX1_N
SSTX1_P
USB_VBUS
USB_CC1
USB0_D_P
USB0_D_N
USB_GP0
USB_VBUS
SSRX2_N
SSRX2_P

GND_1 GND_4
SSTXP1 SSRXP1
SSTXN1 SSRXN1
VBUS_1 VBUS_4
CC1 SBU2
DP1 DN2
DN1 DP2
SBU1 CC2
VBUS_2 VBUS_3
SSRXN2 SSTXN2
SSRXP2 SSTXP2
GND_2 GND_3
MH1 MH3
MH2 MH4

SSRX1_P
SSRX1_N
USB_VBUS
USB_GP1
USB0_D_N
USB0_D_P
USB_CC2
USB_VBUS
SSTX2_P
SSTX2_N

this inversion is intentional

Ethernet output (ix industrial)

Pairs are:
1/2 -> 24/23
5/6->20/19
7/8->18/17
11/12->14/13

J16
HX5120NL

PHY_MDI0_P
PHY_MDI0_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_N
PHY_MDI3_P
flipped on purpose
PHY_MDI1_N
PHY_MDI1_P
MAG_MDI1_P
MAG_MDI1_N
MAG_MDI2_N
MAG_MDI0_P

C169 0.1u
C170 0.1u
C171 0.1u
C172 0.1u
R101 75
R102 75
R103 75
R104 75
C165 1000p

MAG_MDI0_P
MAG_MDI0_N
MAG_MDI2_P
MAG_MDI2_N
MAG_MDI3_N
MAG_MDI3_P
MAG_MDI1_N
MAG_MDI1_P

J10
IX80G-A-10P_01_
MH1 MH2

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

shove DisplayPort on the aux connector

J6
FX12B-60P-0.4SV

Z_SDA
Z_SCL
L16_P
L16_N
DAC0_N
DAC0_P
DAC1_N
DAC1_P
DAC2_N
DAC2_P
DAC3_N
DAC3_P
DAC4_N
DAC4_P
DAC5_N
DAC5_P
DAC6_N
DAC6_P
DAC7_N
DAC7_P
MOUNTING PADS

CPLD_IO2
CPLD_IO3
MIO27
MIO30
RX2_P
RX2_N
RX3_P
RX3_N
TX2_P
TX2_N
TX3_P
TX3_N
L6_P
L6_N
L7_P
L7_N
USB_GP1
USB_GP0

C52 0.1u
C53 0.1u
C54 0.1u
C55 0.1u

test points
TP2 TP
TP3 TP
R96 DNI
R97 DNI

X1
CPCI_FP_BOT_BRACKET
X2-1

X6 X5 X4 X3 X8 X7 X12 X11 X10 X9 X16 X15 X14 X13
MTG_HOLE

J12
1844210
+12VIN
Alternate power input

3V3_CPLD
Note: the micro-USB here is hidden behind panel
Not intended for normal use

U40
CH340E
V3 RXD TXD VCC TNOW
UD+ UD- GND RTS# CTS#
IN DBGRX3V3
OUT DBGTX3V3

J15
ZX62_B_5PA33

C157 0.1u
1.8V_CLK
3V3_CPLD
this is located by clock

U45
TXU0202DTTR
B2 GND VCCA A2Y
A1 OE VCCB B1Y
DBGTX
DBGRX3V3
DBGTX3V3
DBGRX
R75 10k

C158 0.1u
C159 0.1u

revC: fix level-shift pinout

DESIGN DETAILS FOR BITELLE:
Exterior: Coupled Microstrip, route as 7 mil trace/11 mil CC-space. Bitelle: 0.1778 mm trace (100.5 ohms @ 4.2)
Interior: Coupled Stripline, route as 7 mil trace/11 mil CC-space. Bitelle: 0.1016 mm trace (106 ohms @ 4.2)
Single-ended 50 ohm is 0.2667 mm and 0.127 interior

D2 D3 D4 D5
ESD8104MUTAG

SSTX1_N
SSTX1_P
SSRX2_N
SSRX2_P
SSTX2_N
SSTX2_P
SSRX1_N
SSRX1_P
USB_VBUS
USB_CC1
USB_CC2
USB_GP1
USB_GP0
USB0_D_N
USB0_D_P

IO_1 IO_2 GND_1 IO_3 IO_4
NC_4 NC_3 GND_2 NC_2 NC_1

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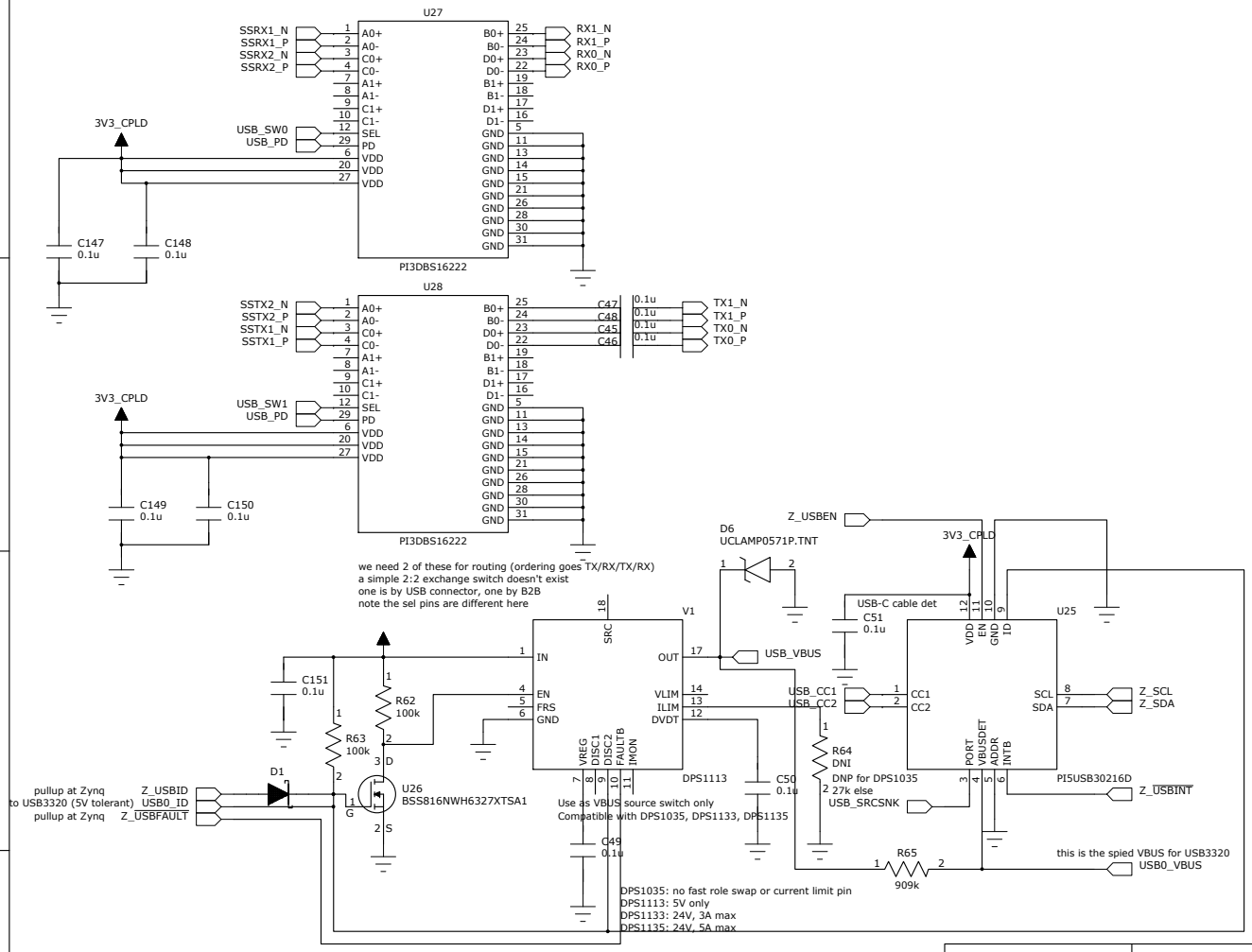
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: IO	REV: B
		SCALE:	SHEET: 4 OF 14



This is pin-compatible with:
FUSB303B
TUSB320

REVISION RECORD			
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CHECKED:	DATED:	TITLE: SURFv6	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
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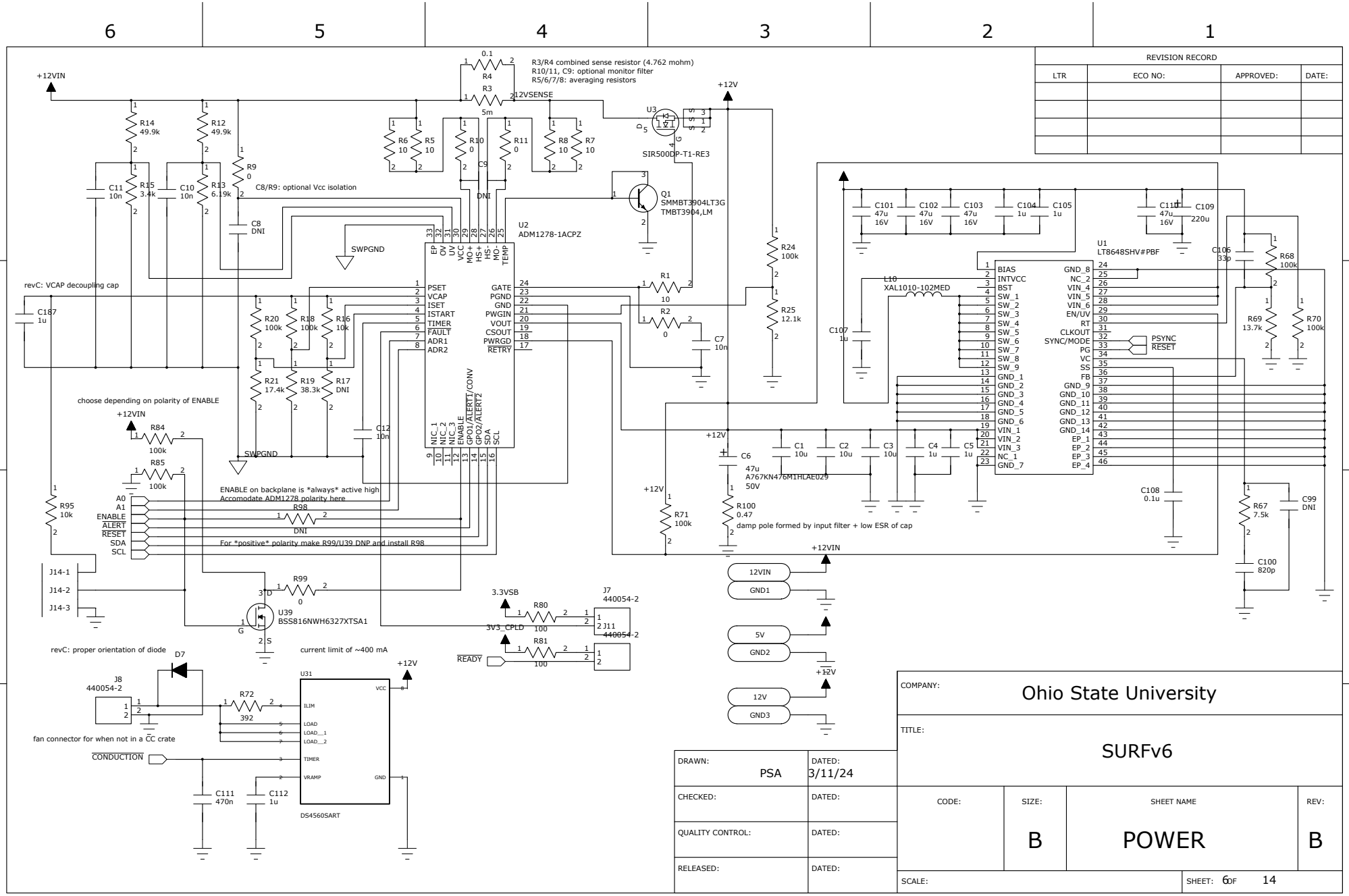
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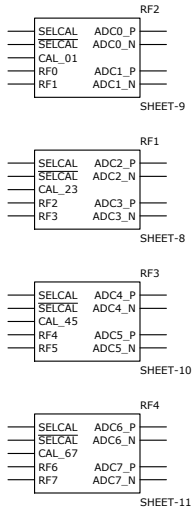
LTR | ECO NO: | APPROVED: | DATE:
R3/R4 combined sense resistor (4.762 mohm)
R10/11, C9: optional monitor filter
R5/6/7/8: averaging resistors
C8/R9: optional Vcc isolation
revC: VCAP decoupling cap
choose depending on polarity of ENABLE
ENABLE on backplane is *always* active high
Accomodate ADM1278 polarity here
For *positive* polarity make R99/U39 DNP and install R98
revC: proper orientation of diode
current limit of ~400 mA
fan connector for when not in a CC crate
damp pole formed by input filter + low ESR of cap
SIR500DP-T1-RE3
Q1 SMMBT3904LT3G TMBT3904,LM
U2 ADM1278-1ACPZ
U1 LT8648SHV#PBF
L10 XAL1010-102MED
A767KN476M1HLAE029
BSS816NWH6327XTSA1
DS4560SART
COMPANY: Ohio State University
TITLE: SURFv6
DRAWN: PSA DATED: 3/11/24
CHECKED: DATED:
QUALITY CONTROL: DATED:
RELEASED: DATED:
CODE: SIZE: B SHEET NAME: POWER REV: B
SCALE: SHEET: 6 OF 14



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN: PSA	DATED: 3/11/24		
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:		

COMPANY: Ohio State University

TITLE: SURFv6

CODE:	SIZE:	SHEET NAME	REV:
	B	RF_CHAIN	B

SCALE:

SHEET: 7 OF 14

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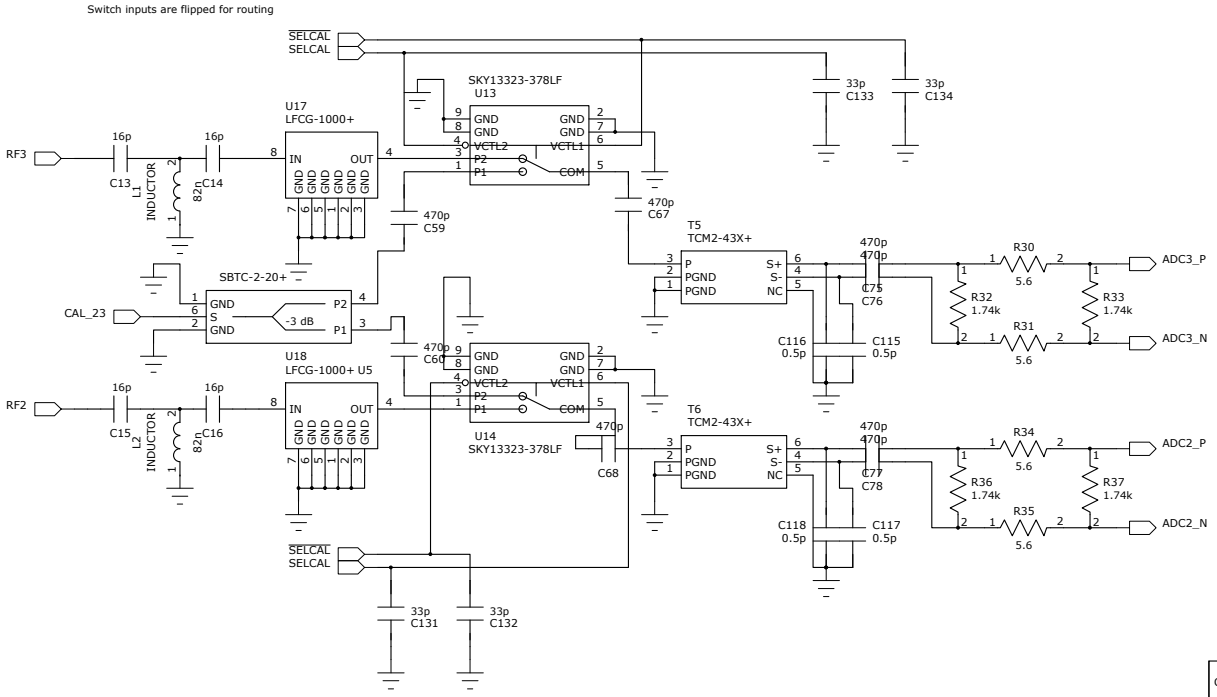

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		SCALE:	SHEET: 8 OF 14

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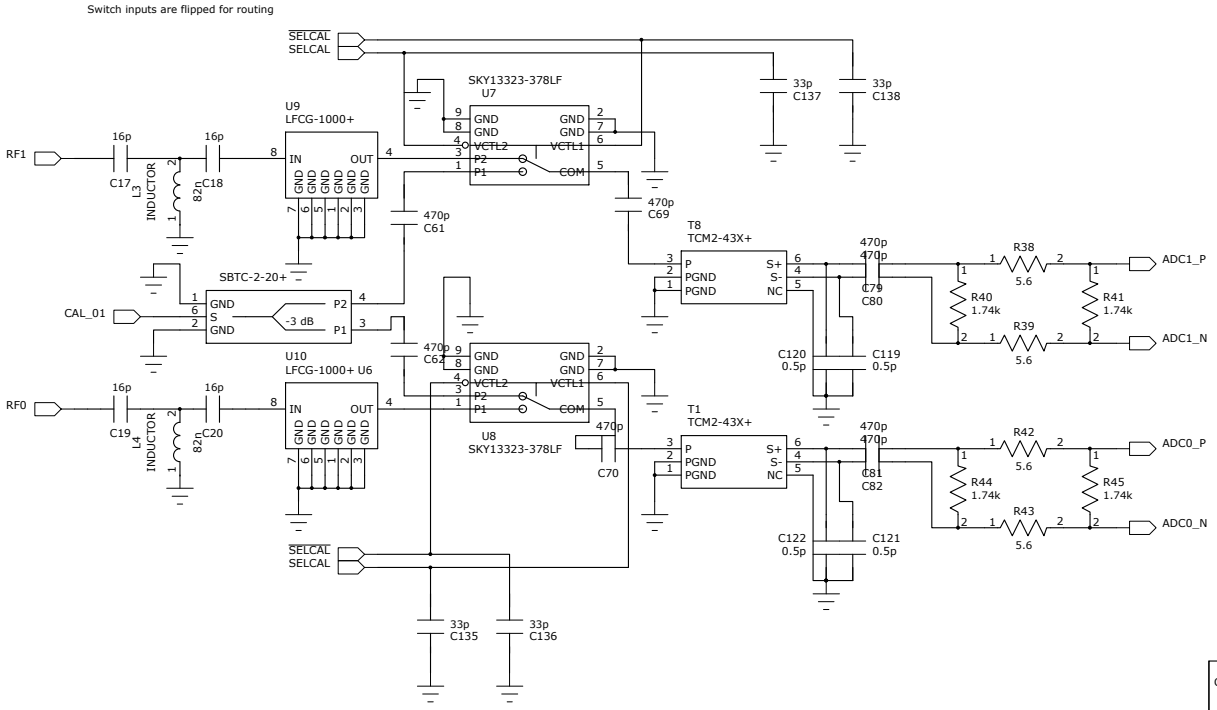

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		SCALE:	SHEET: 9 OF 14

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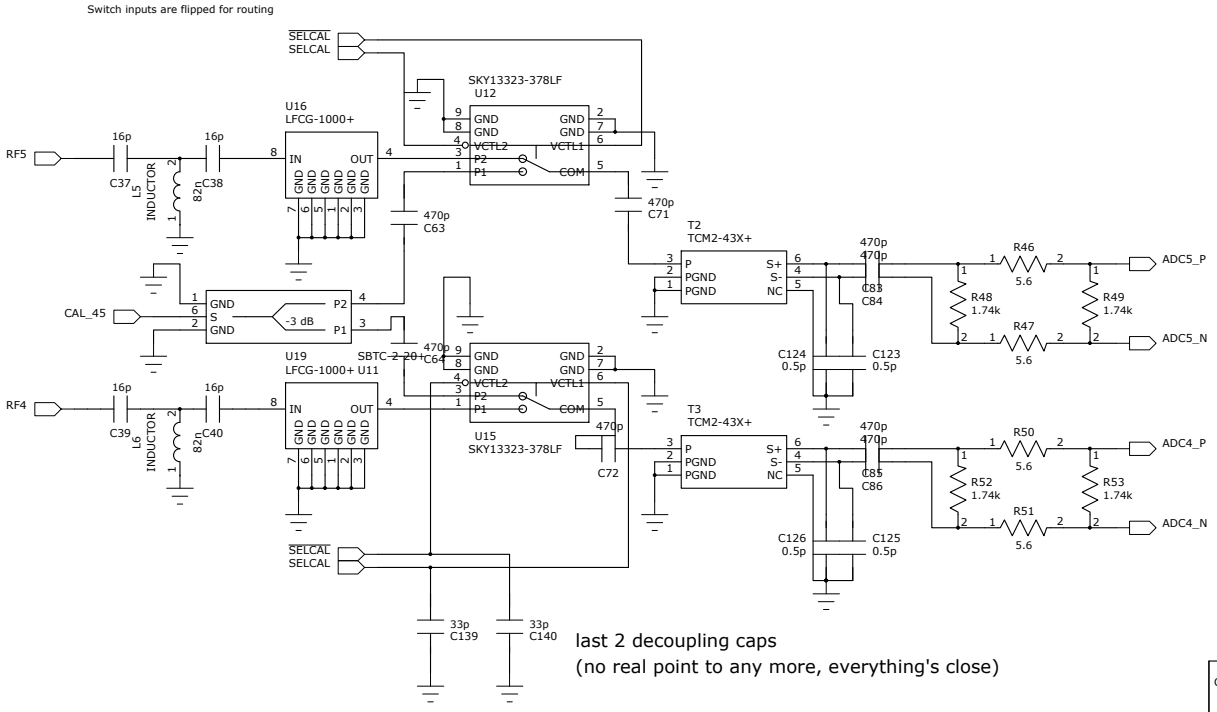

last 2 decoupling caps
(no real point to any more, everything's close)

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QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	SHEET NAME: RF3	REV: B
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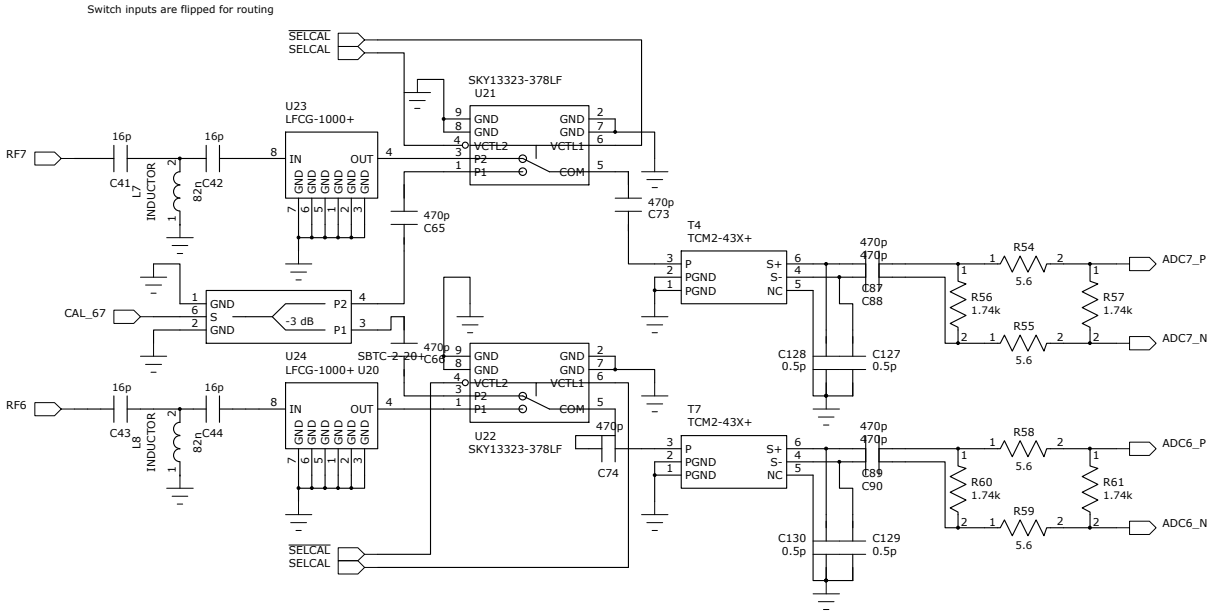

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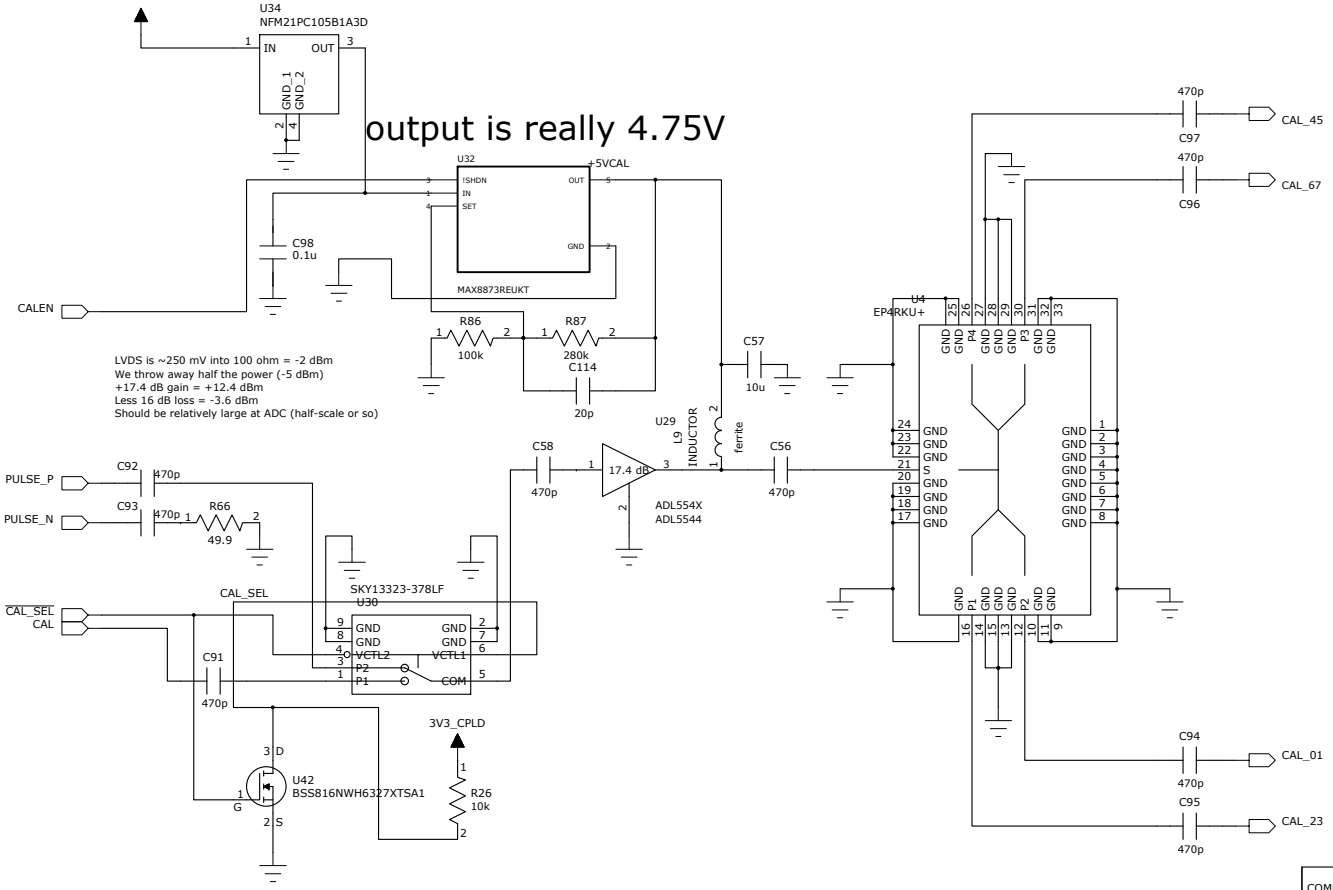
		SCALE:	SHEET: 11 of 14



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REVISION RECORD			
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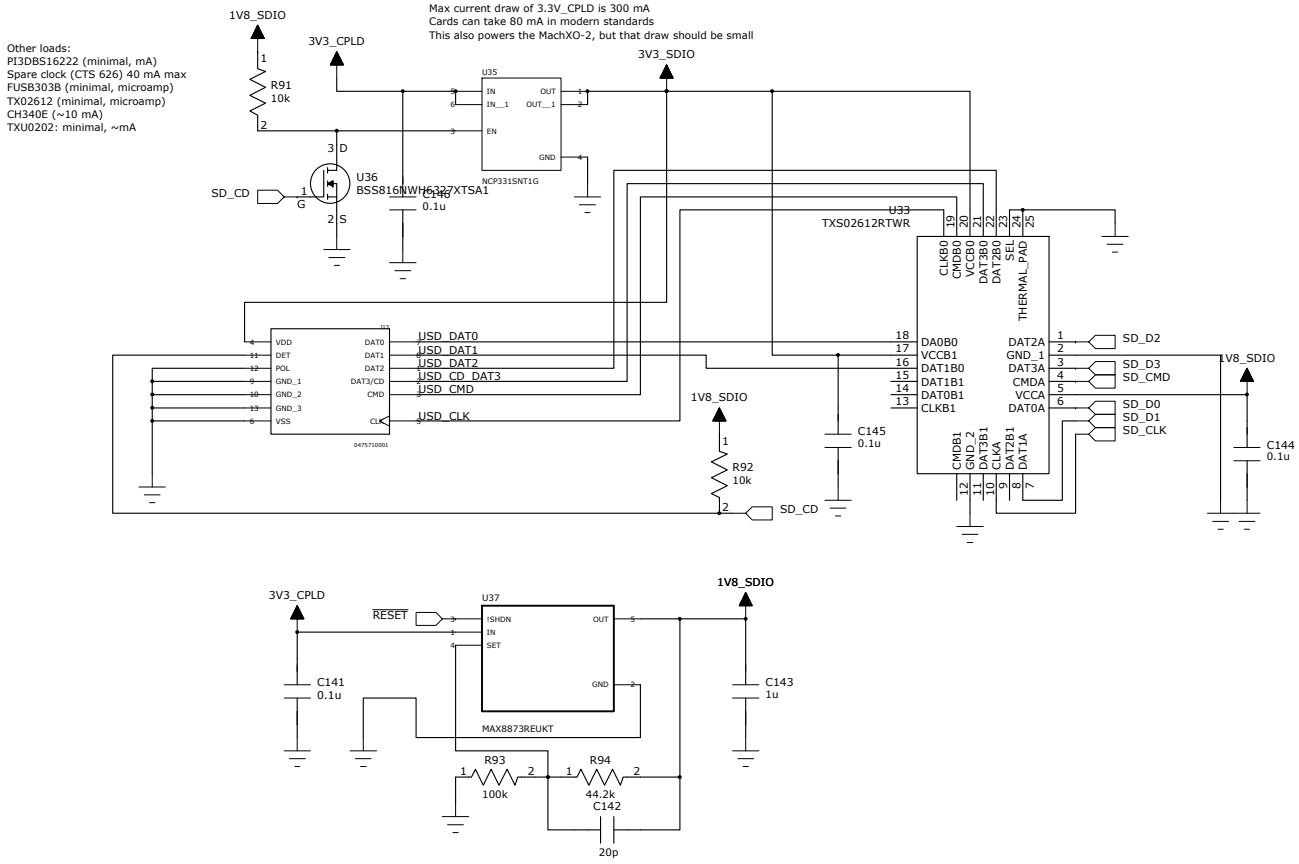

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QUALITY CONTROL:	DATED:	CODE:	SIZE: B	DRAWING NO:	REV: B
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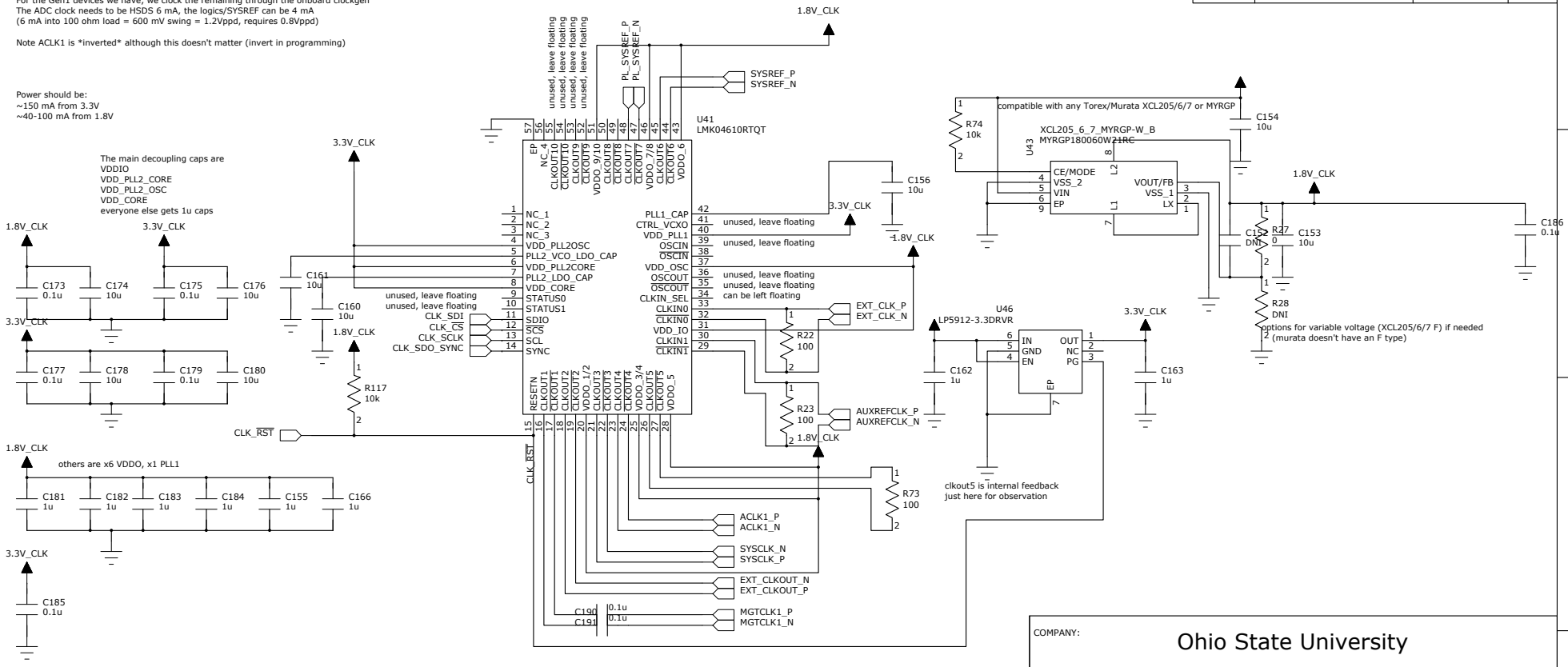
RevB adds local clock gen to force phase sync
Our MINIMAL clocks are just ADC clock + PL clock (both 375 MHz)
We add analog/PL sysref and the forwarded clock as options (2 @ 7.8125M, who knows for 3rd)
We need:
ADC clock (1, using internal clock dist)
Analog SysRef
PL SysRef
PL refclk
We relocate ACLK1 to be the ADC clock here.
For the Gen1 devices we have, we clock the remaining through the onboard clockgen
The ADC clock needs to be HSDS 6 mA, the logics/SYSREF can be 4 mA
(6 mA into 100 ohm load = 600 mV swing = 1.2Vppd, requires 0.8Vppd)

Note ACLK1 is *inverted* although this doesn't matter (invert in programming)

Power should be:
~150 mA from 3.3V
~40-100 mA from 1.8V

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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