RF Array Carrying Kit (RACK)
Design Document

March 2, 2022

1 Introduction

The RF Array Carrying Kit (RACK) is a custom backplane using FX23B 100-pin connectors designed to interconnect the SURFv6 and TURFIOv6 modules.

The RACK distributes the RACKbus signals to each of the daughterboards. It also contains 2 cabled connectors to allow two RACKs to be connected with interphi communications in a loop (skipping left slot 8 and right slot 1, where the TURFIO boards are located): as in, Left slot 1 talks to left slot 2 *and* right slot 8, and left slot 7 talks to right slot 2 over cable links.

2 Physical dimensions

The RACK physical dimensions are shown in Fig. 1. Mount hole and connector locations conform to IEEE 1101.1 standards, covering 8 total 5HP slots. The RACK mounts with its front facing the SURFv6 modules, as specified in IEEE 1101.1. This makes the mounting distance independent of board thickness.

3 Power

The RACK receives and distributes +12V to all daughterboards. Incoming power is supplied on 4x M4 screw terminals for both power and ground. These terminals are arranged in a straight line to allow for a simple bus bar to be made for connection.

3.1 3.3VSB

A separate 3.3V standby (3.3VSB) supply is provided using a MAXM15465 integrated supply. The 3.3VSB supply is only used to power the JTAG multiplexer, provide a positive voltage to force ENABLE when a TURFIO is not present, provide I2C pullups when the TURFIO is not present, and provide fault LED power for the SURFv6 boards. The 3.3VSB supply can be disabled

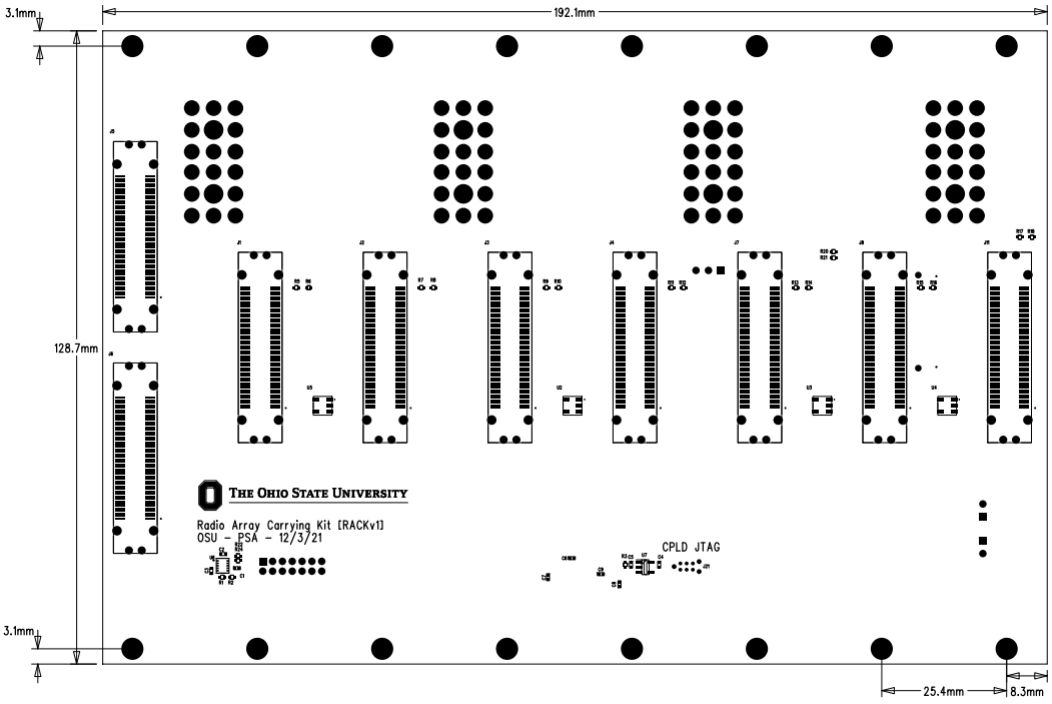

Figure 1: RACK physical dimensions. This is for a right-side RACK, however dimensions are equivalent for a left-side RACK.

by the TURFIO with no loss of flight functionality. This supply was chosen for availability and ease of integration: its efficiency is not critical.

4 Configuration switch

The S1 switch provides 4 configuration options for the RACK.

Switch #	ON function	OFF function
1	Rightside RACK	Leftside RACK
2	Vpol RACK	Hpol RACK
3	Conduction	Convection
4	I2C pullups connected	No I2C Pullups

In a flight configuration, Switch #3 should be ON and Switch #4 should be OFF. Each of the 4 total RACKs (left/right in each of the 2 crates) should have switch #1 and switch #2 set properly.

5 Cable links

As previously mentioned, the 2 RACKs located in a crate are connected via 2 cabled links to join them together into a ring. This is shown in Fig. 2. The short link (left slot 8 to right slot 2), which is 46.2 mm from connector center to center (between L7/L8 to between L1/L2), is made via Molex Premo-Flex LVDS 15021 33-pin, 0.5 mm pitch cable. Expected losses along this cable are uncertain, however these cables are rated for "5-10 Gigabits/sec," and typical FFC losses generally range around 0.5 dB/in.at > 5 GHz, meaning we would expect ~ 1 dB loss across this cable. Desired cable is Molex #0150210233.

The long link (left slot 1 to right slot 8), which is 352.4 mm connector center to center, is made via a high-performance ARC6 16-pin cable from Samtec. This cable should be requested to desired length (most likely 15"): standard lengths available include 18", which will work for testing. At 18", expected losses at ~ 5 GHz would be < 3 dB (and <4 dB at 10 GHz). The performance of this link will likely determine the overall speed of the interphi link. These losses, however, are smaller than an equivalent length FR4 link, and *should* still be able to work at least up to 10 Gbps per link (required is 5 Gbps). Desired cable is ARC6-16-18.0-LU-LU-3-1 for testing.

6 Calibration signals

The TURFIO provides 4 calibration signals for the 7 SURFv6s. The RACK contains an SBTC-2-20+ splitter to expand the 4 signals to each of the slots. The remaining unused output is routed to a U.FL socket.

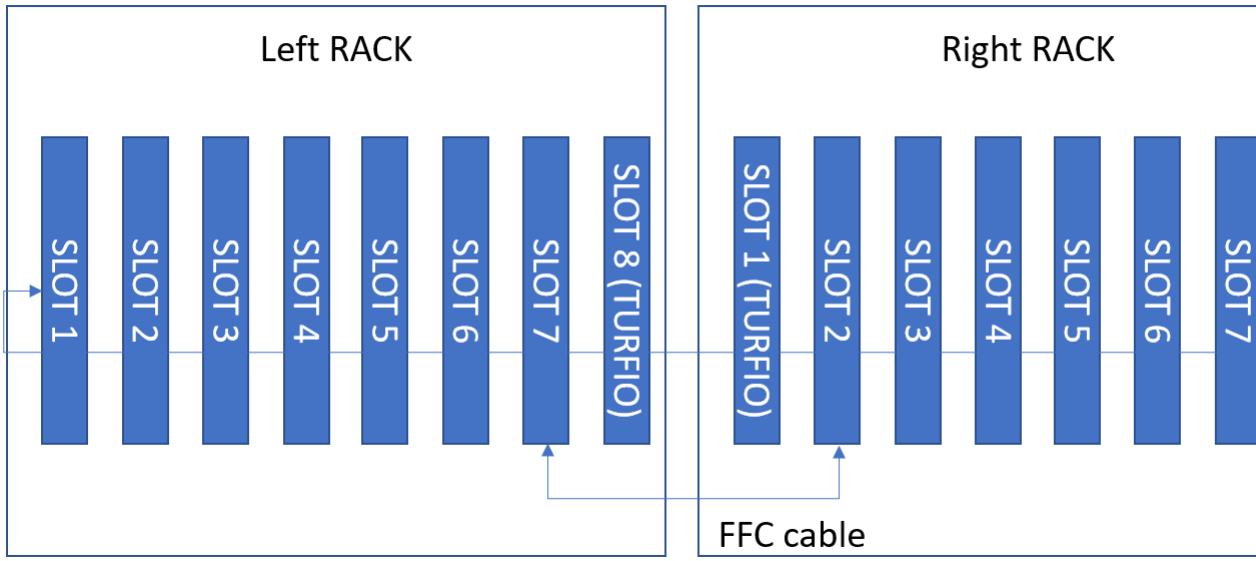

Figure 2: RACK interconnections. The two connections join the SURFv6 inter-phi communication in a ring. The short link (left slot 8 to right slot 2) is made via a controlled-impedance FFC cable, whereas the long link (left slot 1 to right slot 8) is made via a high-performance ARC6 cable from Samtec.

7 Length/impedance matching

All CLK+/- system clock traces are matched to < 5 ps, with approximately 1.29 ns of propagation delay.

All RXCLK+/- and CIN+/- traces are length matched to ± 0.1 mm, as are TXCLK+/- and COUT+/- traces.

All CAL traces are matched to < 5 ps, with approximately 1.21 ns of propagation delay, excluding propagation through the SBTC-2-20+ splitter.

The RACK stackup is designed to Bittele's standard 8 layer stackup, with 5.9 mil between L1/L2 (and L7/L8) and 9 mil between L2/L3. Interphi links, which have the highest signal quality, are routed as coupled CPWG with equivalent center-to-center spacing as the pins themselves.

8 JTAG debugging

To facilitate debugging, the JTAG links from each SURFv6 are routed to a XC2C64A CPLD where they can be programmably selected or combined. This also rearranges the JTAG chain into a star configuration, easing routing. The JTAG chain is configured using the T\CTRL signal: when this signal is low, the TTCK and TTDI pins become CTRL_CLK and CTRL_DATA, respectively, and an 8-bit JTAG configuration can be shifted in (LSB first). Note that the chain number ordering is *slot distance from the TURFIO*.

Bit #	Function
0	Connect chain 1 (R2/L7)
1	Connect chain 2 (R3/L6)
2	Connect chain 3 (R4/L5)
3	Connect chain 4 (R5/L4)
4	Connect chain 5 (R6/L3)
5	Connect chain 6 (R7/L2)
6	Connect chain 7 (R8/L3)
7	LED output

By default the CPLD will come up with chain 1 enabled (and the LED off), or an 8-bit control value of 0x01. For single-board debugging plugging a SURFv6 in the slot adjacent to the TURFIO requires no configuration.

8.1 CPLD programming

The RACK CPLD is programmed using a TAG Connect cable.