1 Envelope trigger

Each channel has an additional low-power envelope trigger based on a biased Schottky diode. An envelope detector effectively has two characteristic frequencies: the upper and lower limits of its video bandwidth. The current design uses an approximately $10 - 80\,\text{MHz}$ video bandwidth, which implies that the output is roughly the integrated power over a $\sim 12.5\,\text{ns}$ window relative to the amount of power seen in the previous 100 ns.

1.1 Diode circuit

To be aded.

1.2 Threshold generation

The output of the envelope trigger is fed into one side of an LVDS input pair on the main FPGA, to allow using the LVDS input as a comparator. The other side of the LVDS input is the trigger threshold, which is generated via pulse-width modulation (PWM) from a separate FPGA pin, coupled to a smoothing capacitor through a series resistor. The RC filter frequency ($0.1\,\mu\text{F}$ and $4.7\,\text{k}\Omega$) result in $\sim 0.1\,\text{mV}$ ripple with a 100 MHz PWM, trivially achievable in an FPGA using a DSP accumulator based design. Note that the step response for this output is $\sim 1\,\text{ms}$.

Because the PWM output is in close proximity to the threshold itself, there would be some concern regarding high-frequency switching artifacts. A HyperLynx LineSim simulation was performed to verify that the transient induced by the output switch is also sufficiently small ($< 0.1\,\text{mV}$). It is worth noting that if a faster step response is desired (at the expense of ripple), the correct solution is to reduce the size of the *capacitor*, not the size of the *resistor*. This is because the switching artifact corresponds to $O1\,(100\,\text{MHz})$ frequencies, at which point the capacitor's impedance (on the order of $0.1\,\Omega$) is dominated by both its effective series resistance and inductance, rather than the capacitance, and neither of these parasitics change as the capacitance is decreased. The switching artifact size is therefore set nearly entirely by the size of the resistor - note that simply treating this as a simple resistive divider validates the simulation in this case, as $0.1\,\Omega/4700\,\Omega \approx 2 \times 10^{-5}$, and a switching transient of 2.5 V would therefore result in $\sim 0.1\,\text{mV}$ peak-to-peak variations, as observed. This is, in fact, the reason why a resistor is needed at all - using only the effective series resistance from the output driver ($\sim 78\,\Omega$) would result in switching artifacts on the order of 15 mV, clearly too high to be acceptable. Increasing the series resistor to further reduce the ripple/switching artifacts is possible, however $4.7\,\text{k}\Omega$ was chosen to remain significantly far away from the pad leakage current (max $15\,\mu\text{A}$). Increasing the PWM frequency would actually act to increase the overall ripple as the switching transients would still be high-amplitude with periods of less than10 ns.

Ripple on the threshold pin effectively acts as an increase in the input noise: for reference, previous designs using a dedicated DAC and similar-scale input amplitudes had noise scales on the order of $\sim 20\,\text{mV}$, so the additional $0.1\,\text{mV}$ noise is a negligible increase, and comparable to reference noise levels for a typical DAC.

2 On-board calibration

2.1 Signal generator

2.2 Fast pulse

2.3 Calibration fanout

The calibration fanout was designed to provide a calibration signal of up to $\sim 10\,\text{dBm}$ ($\sim 2\,\text{V}$ peak-to-peak) to the LAB4D and trigger circuits. Providing this as a full 24-way fanout would be too difficult to route, since the calibration signals need to be fed into the inputs of each channel, and the channel inputs are at the edge of the board. Therefore a compromise solution was designed where the signal is broadcast to 4 channels (1 quad) on each side at a time, with the signal routing on each side being point-to-point through an RF switch. The output power of the ADF4351 is $-4 - 5\,\text{dBm}$ - therefore, after the switch, the input power to each quad is $-7 - 2\,\text{dBm}$. At each quad, a Mini-Circuits TSY-13LNB+ amplifier boosts the power to $8.3 - 17.3\,\text{dBm}$ (at the high side, the amplifier will be in compression at low frequencies but still well within the maximum power input specification). Following the amplifier, a Mini-Circuits SCA-4-10+ splitter distributes the signal to each input channel, with a power range of $2.3 - 11.3\,\text{dBm}$. Note that this analysis ignores insertion losses along the way, which will reduce the final power by $2 - 3\,\text{dB}$.

3 Power supply design

3.1 Input power

The RADIANT board accepts an input voltage from $4.5\,\text{V} - 5.5\,\text{V}$ for normal operation. Outside of this range (from $3.4\,\text{V} - 4.5\,\text{V}$ and $5.5\,\text{V} - 7.6\,\text{V}$) the board will power on but report input voltage out of range. For input voltages below $3.6\,\text{V}$ and above $7.6\,\text{V}$ the board will not power on, but instead indicate an input voltage fault. Input voltages must be between $-20\,\text{V}$ to $20\,\text{V}$ to prevent damage.

Voltage Range	**Minimum**	**Maximum**
Normal Operating	$4.5\,\text{V}$	$5.5\,\text{V}$
Input Voltage Out-Of-Range	$3.6\,\text{V}$	$7.6\,\text{V}$
Absolute Maximum	$-20\,\text{V}$	$20\,\text{V}$

Reverse voltage protection is provided via an Si7157DP P-channel MOSFET with $\sim 2\,\mathrm{m}\Omega$ on-resistance (with gate-source voltage clamped to 12 V). Overvoltage/undervoltage/overcurrent protection is provided via a TPS259823ONRGE (7.6 V OVP, circuit breaker overcurrent behavior) eFuse with $\sim 2.7\,\mathrm{m}\Omega$ on-resistance. Board supply current is limited to 3.5 A. This is a factor of 1.75 increase over the typical expected (~ 2 A) but should allow for all possible FPGA configurations to be used. At 2 A nominal current, the input power protection circuit consumes ~ 20 mW. The TPS259823 was chosen specifically for this point: the next-smallest eFuse on-resistance would result in a $\sim 6\times$ increase in power consumption for the protection circuit.

Protection Circuit Behavior	
Undervoltage Lockout (nom.)	3.6 V
Overvoltage Lockout (intrinsic)	7.6 V
Current Limit	3.5 A
Fast Trip Current Limit	7.35 A
Overcurrent Limit Trip Time	1 ms
Retry Delay	100 ms
Number of Retries	4

3.2 Input Voltage Out-Of-Range

The input power protection circuit guarantees that the main +5V supply is between $3.6 - 7.6$ V. All onboard DC-DC converters can accept this range. However, the calibration amplifier circuits use an MMG3H21NT1 amplifier, which is characterized from $4.5\,\mathrm{V} - 5.5\,\mathrm{V}$ (and with a rapidly increasing current past 5.5 V). The calibration amplifiers are off by default, and switched on via the board manager microcontroller. Therefore if the input voltage is outside of the $5\,\mathrm{V} \pm 10$ range, the board manager will not enable any downstream devices and responds to all commands with an Input Voltage Out-Of-Range error, along with the measured input voltage. The allowable input voltage will be programmable by the board manager to override this restriction if needed (although the calibration amplifiers are protected from turn-on past 6 V by the load switch).

The calibration amplifiers are protected from damage via an AOZ1327DI load switch with overvoltage protection beyond 6 V, thus ensuring that even if the board manager somehow enables the amplifier from $6 - 7.6$ V, the amplifier itself will not be damaged. At the maximum voltage of 6 V, the MMG3H21NT1 consumes 150 mA, resulting in a power consumption of 0.9 W and a temperature rise of 34 deg C, which will still remain comfortably inside the maximum junction temperature range for all operating temperatures. The amplifier turn-on time is set to $100\,\mu$s, which limits the input surge current to 500 mA. At the nominal voltage, the calibration amplifiers consume 90 mA.

3.3 Power rails

The main power rails for the RADIANT board are

- 5V (nominal) input
- 3.3V (logic)
- 2.5V (logic, FPGA, CPLDs, clocking)
- 1.8V (FPGA)
- 1.0V (FPGA)
- 2.6V (digitizers)
- 3.1V (trigger amps)

The 2.6V and 3.1V voltages are regulated down to 2.5V and 3.0V for the RF-sensitive sections using RippleBlocker LDO regulators.

3.4 2.6V LAB4D supply

Summary	
Nominal Voltage	$2.59 \pm 0.025\,\mathrm{V}$
Nominal Current	2.4 A(estim.)
Purpose	LAB4D Digitizer Supply
Device	TPS54824
Efficiency	95.5
Ripple	3.51 mV

The majority of the power consumption of the board comes from via the 2.6 V rail to the digitizers, which should be approximately 2.4 A, or around 5 W. However, because this rail feeds an RF-sensitive device, it makes sense to pay special attention to this converter. The converter was chosen as a TPS54824, which was a balance between total footprint size of the solution, efficiency, and output ripple. At 1.8A output, the output voltage should be $2.59 \pm 0.025\,\mathrm{V}$. The converter should be 95.5% efficient, which is equivalent to an additional power consumption of 0.21 W, and should have an output ripple of 3.51 mV. This does require a very low dropout voltage on the LDO: we therefore regulate each individual digitizer separately, which should reduce the per-regulator consumption to 75 mA, at which point the dropout voltage should be less than 30 mV using a MIC94325. The PSRR at the targeted frequency of ~500 kHz is better than 50 dB, which would reduce the output ripple to 0.02 LSBs. The total footprint size of the solution is under $200\,\mathrm{mm}^2$, or approximately 0.8×0.4". Note that the main advantage of a small footprint in this case is that it becomes practical to additionally shield the converter section if needed: higher efficiency and lower output ripple designs are both possible, but the required inductor

would be far too large to easily shield. In addition, this design can be *synchronized* to the system clock, which will allow removal of switching artifacts from coherently-added waveforms if needed.

Note that the feedback resistors for the 2.6V supply are 0.1 tolerance, which will guarantee that there exists enough headroom for the subsequent LDO.

3.5 3.1V trigger supply

Similarly, special attention was paid to the 3.1V supply. This supply is slightly less critical because although it feeds an RF sensitive device, the output bandwidth of the trigger system is below 100 MHz. A TPS54424 was used in this case, which is a 4 A version of the TPS54824. This design nominally outputs 3.074 ± 0.04 V. Again, each trigger circuit has their own LDO, a MIC94310. Total load from the trigger circuit should be 12.5 mA, at which point the dropout voltage should be less than 5 mV. Output ripple should be 3.0 mV, reduced by greater than 50 dB, resulting in a final ripple of $\sim 10\,\mu$V, which should have no impact on the trigger subsystem. Again, this design can be synchronized to the overall system clock if needed. Efficiency should be 92.8, equivalent to an added power consumption of 0.06 W.

4 Built-in self test

The RADIANT board is fully capable of evaluating all of its major subsystems systematically with no external components. This is accomplished by an onboard "board manager" which during normal operation also acts to control and program certain onboard features, and a few additional low-cost parts to allow routing normally-unused signals during built-in self test (BIST) mode.

4.1 RF quad BIST

During BIST, the power supplies and basic "alive/dead" functionality of each RF quad are determined. This requires both the auxiliary CPLD and the main FPGA to be placed into a special BIST mode as well. The quad is switched into BIST mode by setting bit 2 of the corresponding I^2C GPIO expander. BIST mode connects several signals in the quad in an alternate configuration.

- BM_MOSI is connected to $\overline{\text{LDAC}}$ for the tunnel diode bias DAC (which allows programming its I^2C address) using an N-channel MOSFET. During normal operation the N-channel MOSFET is not in conduction and thus $\overline{\text{LDAC}}$ remains high regardless of BM_MOSI.

- SHOUT is connected to SS_INCR on the LAB4D (which allows verifying the serial configuration register) through an N-channel MOSFET and a diode. This reverses the normal direction of SS_INCR, thus requiring the auxiliary CPLD pin direction (and the main FPGA pin direction) to be reversed. During normal operation the N-channel MOSFET is not in

conduction and the corresponding diode prevents conduction through the body diode of the FET.

- Analog switches are enabled, which allows for selecting analog voltages in the RF quad. The bits selected depend on the states of the WR[1:0] inputs to each LAB and bits 1 and 3 on the GPIO expander.

Note that bit 3 is multipurpose in the RF quad - it can also be forced low if the calibration amplifier is in overcurrent/overtemperature mode. See below for the proper BIST procedure to deal with this feature. The analog channels are

bit 3	bit 1	output
0	0	cascaded input
0	1	LAB4D_MON (multiplexed monitor)
1	0	+5V_SGx
1	1	5.0V, 3.1V, or 2.6V (depending on quad)

The LAB4D_MON input is a cascaded, multiplexed input, with a 4:1 analog switch near each LAB4D. The outputs are selected via WRn_S[1:0].

WRn_S[1]	WRn_S[0]	output
0	0	cascaded input
0	1	AMON_n
1	0	TRIG3.0V_n
1	1	A2.5V_n

Note that the analog switches used are actually dual 4:1 switches, but only 1 of the 2 switches are used.

4.1.1 RF quad BIST procedure

1. Beginning with quad 0, write the GPIO expander I^2C address, and look for acknowledge. If the address is acknowledged, the GPIO expander is available and working. (RF_QUADn_GPIO_PRESENT = 1).

2. Enable the pull-up on bits 3, 6, and 7 of the GPIO expander and configure as inputs. Configure bit 0, 1, 2, 4, and 5 as outputs and set to 0. Read state of bits 3, 6, and 7. Bit 3 should be high, bits 6 and 7 should match the expectations based on the configuration resistors or the DIP switch (depends on desired board configuration). (RF_QUADn_GPIO_CONFIG_OK = 1). If this step fails, end BIST.

3. Set bit 0 high. Read bit 3 and confirm that bit 3 is still high. If bit 3 is low, the +5V_SGx switch is in overcurrent/overtemp and the quad signal generator amplifier section must be debugged. If bit 3 is high, the switch is not in overcurrent. (RF_QUADn_FLG_OK = 1). Set bit 0 low. Continue if this step fails, however, RF_QUADn_5VSG_OK will likely fail later.

4. Write the DAC I^2C address, and look for acknowledge. If the address is not acknowledged, write 1 to bit 2 (BIST) and update the DAC EEPROM

with the desired address using the MCP4728 update procedure, using BM_MOSI as $\overline{\text{LDAC}}$. Repeat DAC I^2C check. (RF_QUADn_DAC_PRESENT=1). Write 0 to bit 2 (BIST).

5. Repeat from step 1 for all RF quads.
6. Beginning with quad 0, configure bit 3 as an output. Set bit 3, bit 1, and bit 2 (BIST). Read analog voltage and confirm that it meets expectation for quad number. (RF_QUADn_AUX_VOLTAGE_OK=1).
7. Set bit 3 to 1 and bit 1 to 0. Read analog voltage and confirm that it is 0. (RF_QUADn_5VSG_OFF_OK=1).
8. Set bit 0 to 1. Wait 10 ms and read analog voltage and confirm that it meets expectations for +5V. (RF_QUADn_5VSG_OK=1).
9. Set bit 3 to 0 and bit 1 to 1.
10. Beginning with LAB4D 0 + 4*quad number: configure aux CPLDs and FPGA to BIST mode, and select LAB4D for BIST in correct aux CPLD. Set WRn_S[1:0] to 11. Read analog voltage and confirm that it is 0. (RF_QUADn_LABn_OFF_OK = 1).
11. Set bit 5 to 1. Read analog voltage and confirm that it is within expectations. (RF_QUADn_LABn_2V5_OK=1).
12. Clock in a pattern via SIN/SCLK and verify that pattern is visible on SS_INCR. (RF_QUADn_LABn_SIN_OK=1).
13. Update LAB4D configuration to set AMON to a desired voltage. Set WRn_S[1:0] to 01. Read analog voltage and confirm that it meets expectations. (RF_QUADn_LABn_AMON_OK = 1).
14. Set WRn_S[1:0] to 10. Read analog voltage and confirm that it is 0. (RF_QUADn_TRIGn_OFF_OK = 1).
15. Set bit 4 to 1. Read analog voltage and confirm that it is within expectations. (RF_QUADn_TRIGn_3V0_OK=1).
16. Set bits 5 and 4 to 0. Repeat from step 10 for remaining LABs.
17. Set bits 3 and 1 to 0. Repeat from step 6 for all remaining quads.
18. Starting with quad 0, set bit 2 to 0.
19. Repeat step 18 for all remaining quads.
20. Configure aux CPLDs and FPGA for normal mode.

At this point the supplies and basic connectivity for each quad can be considered OK. Additional internal LAB4D checks can be performed at step 13 if desired, however, when in BIST mode, data can not be read out from the LAB4Ds due to the overriding of SS_INCR.