

27 December
MONDAY

Week 52

28 December
TUESDAY

① 362-3

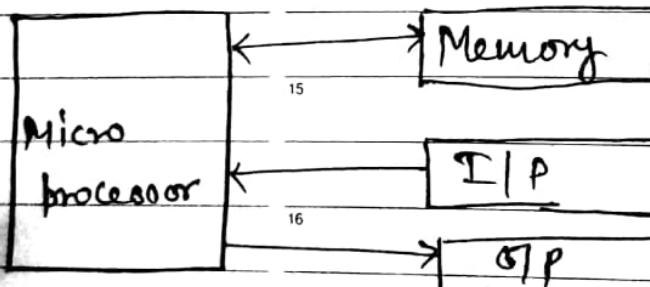
WEDNESDAY

383-2

Priorities

or
The microprocessor is a programmable Integrating device that has decision making Capability.

→ A microprocessor is a multipurpose, programmable, register based logic electronic device that reads binary instructions from memory, accept binary data as I/P process the data according to those instruction & provide results as O/P.



Programmable machine (Microprocessor system)

```
graph LR; A["Reprogrammable system"] --> B["Microprocessor Application"]; A --> C["Programmable Embedded system"]
```

Mnemonics Mnemonics

30 December

THURSDAY

31 December

364-1 FRIDAY

January

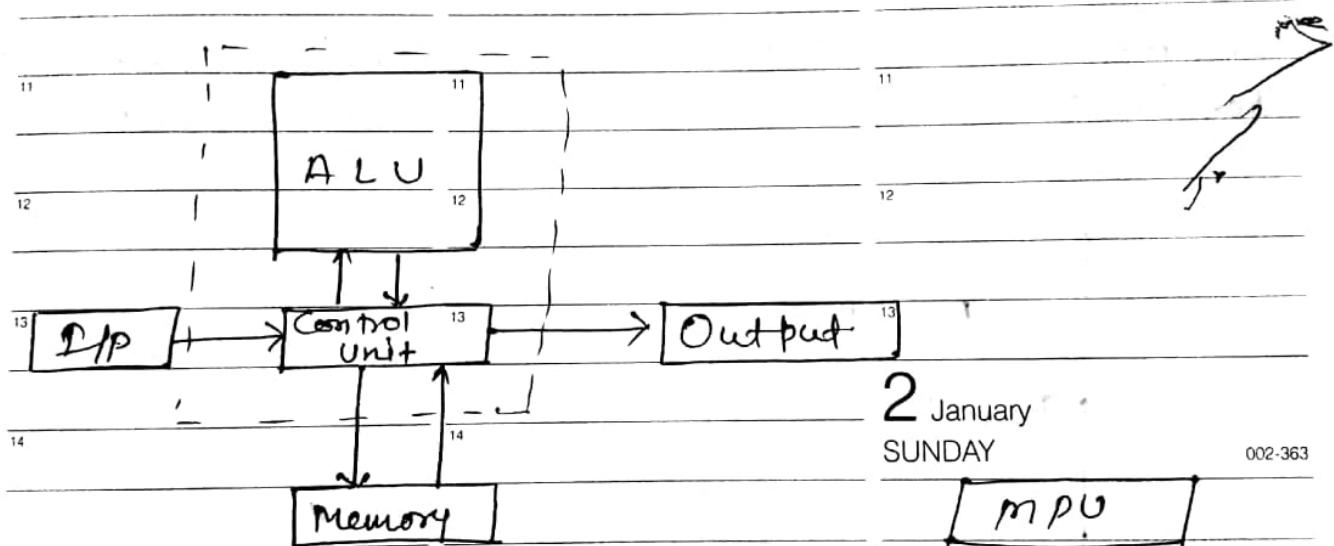
365-0 SATURDAY

001-364

Priorities Retrrogrammable system include General purpose processor Capable of handling of large data, mass storage such as ⁰⁷ CD & ⁶⁷ peripherals like printers for example ⁰⁷ PC (Personal Computer).

Micro Controllers that include all these four Components on a single chip.

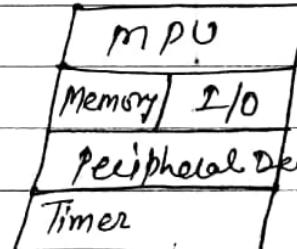
Microprocessor as CPU -



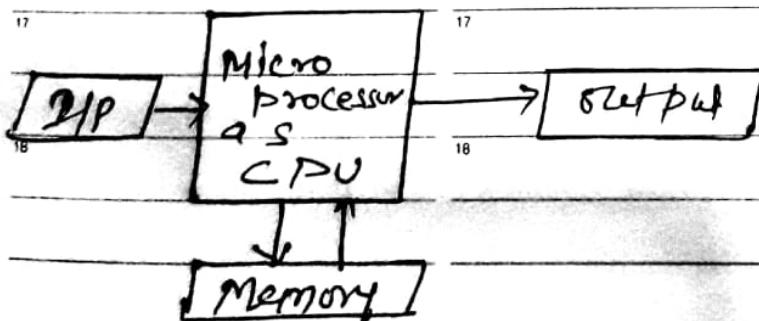
2 January

SUNDAY

002-363



Traditional Computer



Microprocessor as CPU

DECEMBER							2010		
W	M	T	W	T	F	S	S	S	
48			1	2	3	4	5		
49	6	7	8	9	10	11	12		
50	13	14	15	16	17	18	19		
51	20	21	22	23	24	25	26		
52	27	28	29	30	31				

3 January
MONDAY

Week 1
003-362

4 January
TUESDAY

004-361
J January
WEDNESDAY

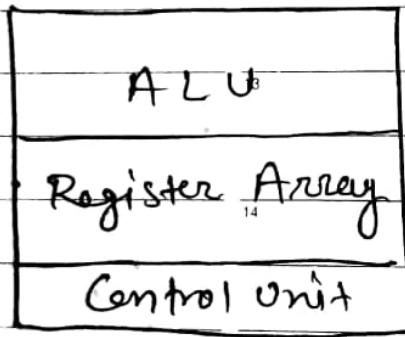
Priorities

Microprocessor - Historical perspective

NP	08	1971
4004	09	1972
8008	09	1974
8080	10	1976
8085	10	1978
8086	11	1993
pentium	11	2000
pentium 4	12	

Clock Speed

Bus	Bus
Ad.	Dat.
10 bit	4 bit
14 bit	8 bit
16 bit	8 bit
16-bit	8 bit
20 bit	16 bit
32 bit	32 bit
36 bit	64 bit



Microprocessor

EVENING

6 January
THURSDAY

7 January
006-359 FRIDAY

8 January
007-358 SATURDAY

008-357

Priorities

programming languages -

Machine language - It is the language that m/c understand. It is in binary format that is either 0 or 1 but for human being it is easy to understand this language. This language is specific to microprocessor

Advantage → (i) m/c language program execute faster than the program written in the High level langus. (ii) No Translator or converter is Required.

Disadvantage -

- (i) Difficult to learn & understand.
- (ii) programs are lengthy & complex
- (iii) programs are machine dependent

Assembly Language - Since program written in the machine language can not understand to the human being hence manufacturer of a microprocessor had devised a symbolic code for each instruction called "mnemonic"

for example - LNR A → Increments the content of accumulator by one

JANUARY							2011
W	M	T	W	T	F	S	S
52	31						1 2
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10 January
MONDAY

Week 2
010-355

11 January
TUESDAY

011-354 WEDNESDAY

Priorities
A Translator called the "Assembler" convert the
Assembly language to machine language
(source program) (Object code)

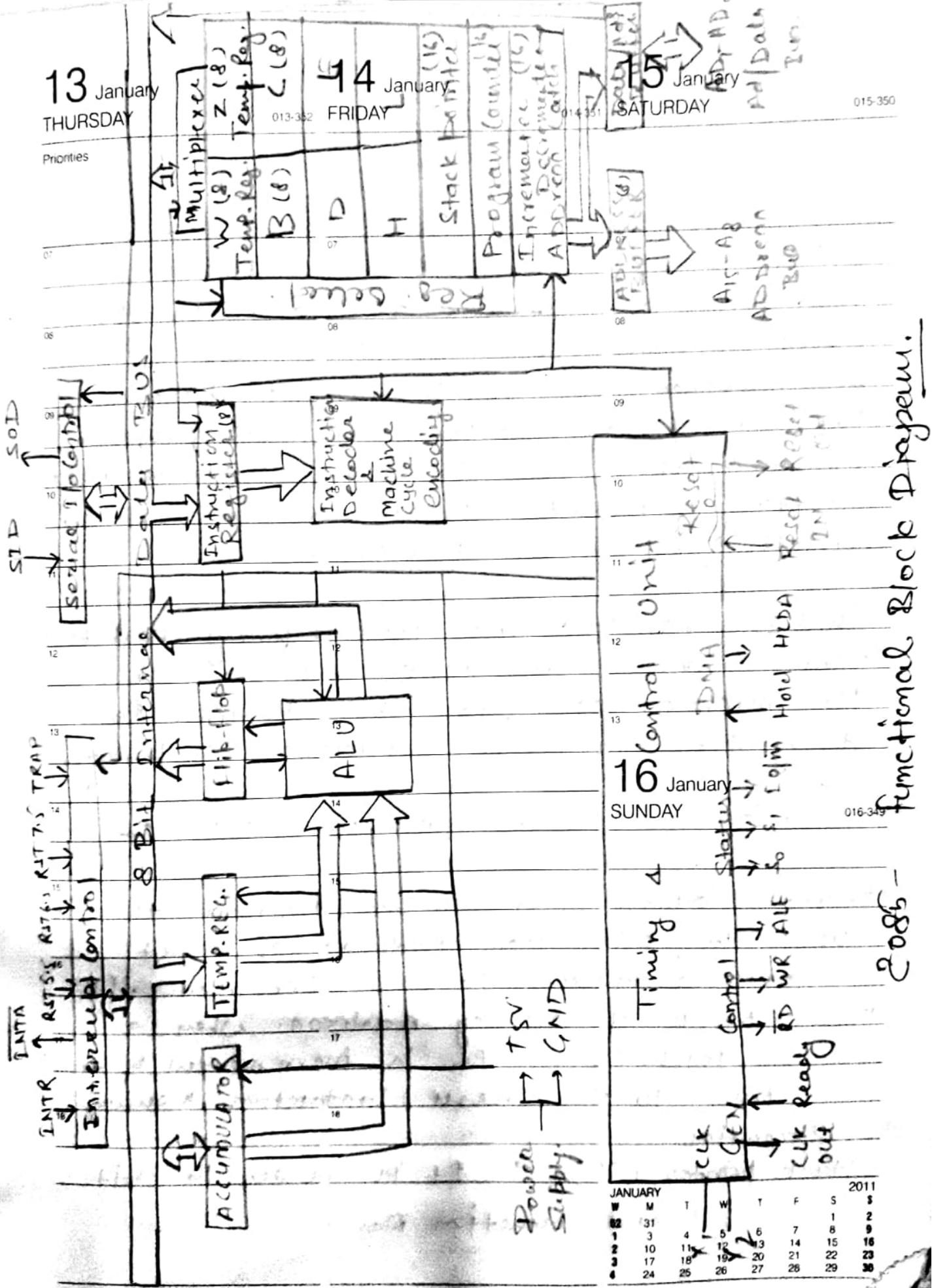
→ High Level Language :- These languages are
M/C Independent
Ex. BASIC, FORTRAN, COBOL, C, C++, FOR

8085 Microprocessor Architecture :-

8085 Microprocessor is a 8 bit General purpose
Microprocessor

It include the following blocks. →

- (1) Register Block
- (2) ALU Block
- (3) Control Unit block
- (4) Interrupt block
- (5) Serial I/O Control block



17 January
MONDAY

Priorities

Week 3
017-348

18 January
TUESDAY

018-347

19 January
WEDNESDAY

019-346

(i) Register block → 8085 microprocessor has six General-purpose registers to store data. These are B, C, D, E, H & L. They can be combined as BC, DE, HL to perform 16-bit operations. These General purpose Registers are used to store intermediate data & results. These registers are also called "Scratchpad Registers".

→ "W/Z" registers are the temporary Registers which are not accessible by the user. The microprocessor uses these Registers for storing the data or address temporary.

program Counter (PC) & Stack pointer (SP) :-

→ program Counter is a 16 bit Register that is used to point the address of next instruction to be executed. It keeps track of memory address. When a byte is fetched, the PC is incremented by one to point to the next instruction, memory location.

→ Stack pointer (SP) → It is also 16-bit special function Register.

20 January
THURSDAY

Priorities

21 January
FRIDAY

020-345

FRIDAY

22 January
344 SATURDAY

021 344

SATURDAY

022 343

Register used as memory pointer. Which "sp" always points to the top of stack. Stack is a part of memory. Stack operates on the principle of LIFO.

(ii) ALU Block -1

¹¹ Arithmetic logical unit contains the following unit —

(a) Accumulator \rightarrow It is a 13-bit Register which is used to perform a logical operation.

b) Temporary Register → It is 8-bit Register used to store temporary data in arithmetic & logical instructions. It is not accessible to user.

(c) Flag Register - ALU contains 5-flip flops, which are set or reset after an operation according to certain conditions of result in Accumulator & other register.

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27 January
THURSDAY

28 January
FRIDAY

29 January
SATURDAY

Priorities

027-338

028-337

029-336

Ex: Let content of Accumulator is 37 H &
 $B = 46H$, then ADD B operation is performed
then content of Accumulator & flag respectively
are -

sol.

00110111
01000010

Content of Accumulator 01111101

Carry flag (CY) = 0

Parity flag (P) = 1

Auxiliary carry flag (AC) = 0

Zero flag (Z) = 0

Sign flag (S) = 0

30 January
SUNDAY

030-335

Ex: Let content of Accumulator is 89 H & B = 7H
if ADD B operation is performed, then content
of Accumulator & flags respectively are -

10001001

01110111

1000000000

CY = 1

AC = 1

S = 0

Z = 1

P = 1

JANUARY							2011
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31 January
MONDAY

Week 5
031-334

1 February
TUESDAY

2 February
WEDNESDAY

033-332

Practices
(iii) Control Unit Block - I This block Controll &

Synchronize all data Transfer & Transformation
in the microprocessor system
this consist of

(i) Instruction Register (IR)

(ii) Instruction Decoder & machine cycle encoder

(iii) Timing & Control Unit

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3 February
THURSDAY

034-331

4 February
FRIDAY

5 February
SATURDAY

035-330

036-329

(v) Interrupt Block :- There are five interrupt in 8085 microprocessor

- (a) INTR (b) RST 4.5 (c) RST 5.5 (d) RST 7.5
(e) TRAP.

Except TRAP interrupt all interrupts are maskable interrupt. TRAP is a Non-maskable interrupt. i.e. if microprocessor receive TRAP request from external device, microprocessor has to respond it.

(v) Serial I/P & O/P Control block :- In 8085, there are separate pins for serial I/P & O/P operations.

These are S_{TD} & S_{OD}

6 February

SUNDAY

037-328

Serial I/P
data

Serial O/P data

FEBRUARY 2011						
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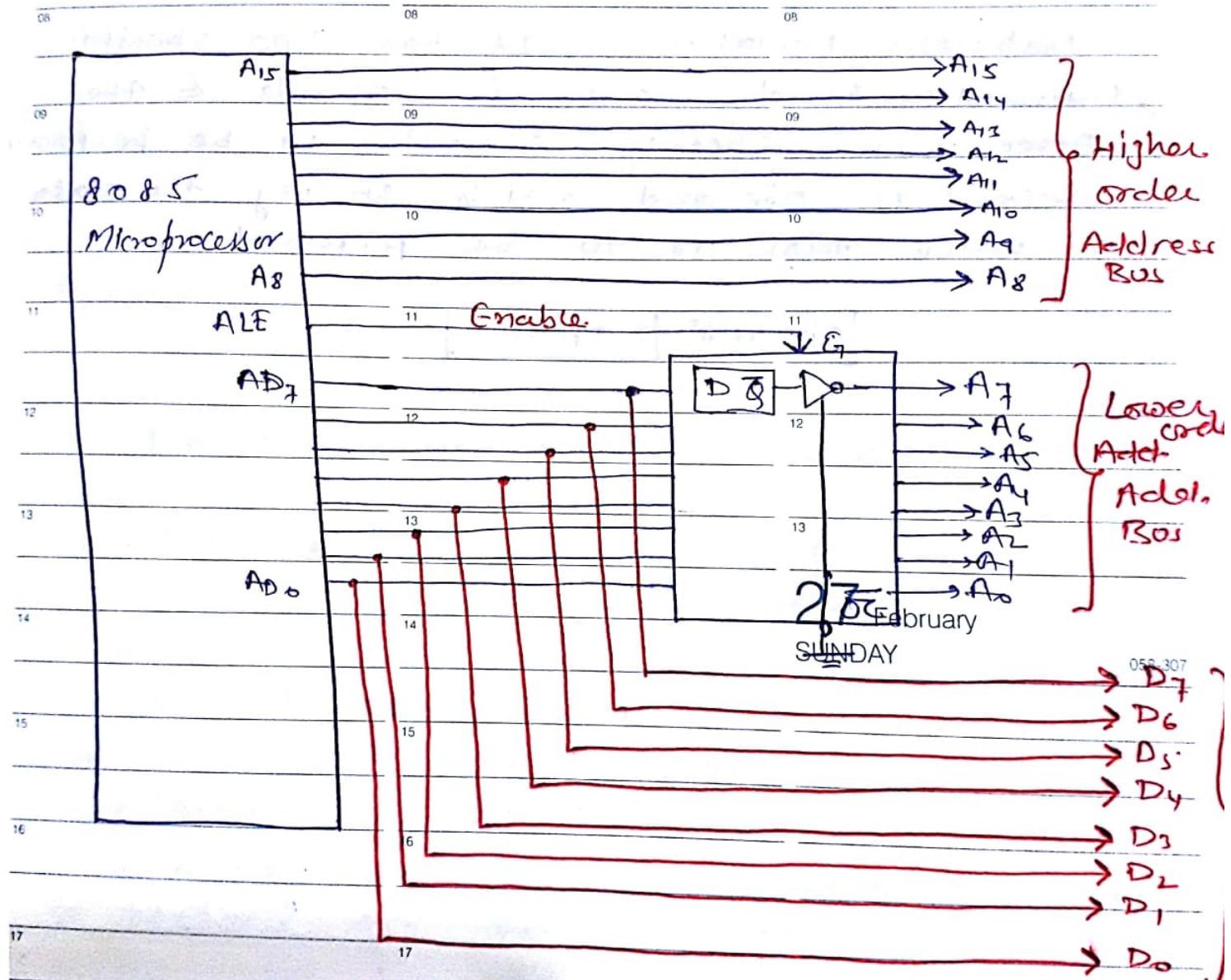
24 February
THURSDAY

25 February
055-310 FRIDAY

26 February
SATURDAY

Priorities

Demultiplexing of Address / Data Bus -



FEBRUARY							2011
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28 February
MONDAY

Week 9
059-306

1 March
TUESDAY

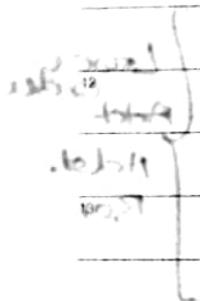
060-305
WEDNESDAY

Priorities

8085 Instruction →

Instruction format → It has two specific information field one is ⁰⁸ opcode ← the other which specify operation to be performed ⁰⁹ second is ¹⁰ operand which specify the condition in which task is to be performed

08 opcode	09 operand
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EVENING

3 March
THURSDAY

062-303

Priorities

4 March
FRIDAY

5 March
SATURDAY

064-301

→ Microprocessor organisation initiated operations & 8085 Bus

07 Mainly microprocessor performs for operations

08 (i) Memory read → Read data (Instruction) from memory

09 (ii) Memory write → write data (or Inst.) in to memory

10 (iii) I/O Read → Accepts data from I/O devices.

11 (iv) I/O write → sends data to I/O devices.

12 6 March
13 SUNDAY

065-300

14 All these operations are part of
15 communication process bet' the microprocessor
16 & peripheral devices. (Includes memory). To
17 communicate with peripheral the CPU needs
to perform the following steps.

18 (i) Identify the peripheral or the memory
19 location.

20 (ii) Transfer binary information. (data in
21 form of)

MARCH 2011						
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13	28	29	30	31	-	-

7 March
MONDAY

Priorities

Week 10
066-299

8 March
TUESDAY

9 March
WEDNESDAY

067-298

066-297

(iii) provide Timing & synchronization signals.

The 8085 perform these function using three sets of communication lines. called Buses. These are

- (i) Address Bus
- (ii) The data Bus
- (iii) The control Bus.

(i) Address Bus → The Address bus is a group of 16 lines A₁₅-A₀. The Address Bus is uni directional. Bits flow in one direction from CPU to peripheral devices. The microprocessor uses the Address Bus to perform the first function identifying a peripheral or a memory location.

Each peripheral or memory location is identified by a binary No. called an address. & The address bus Bus is used to carry 16-bit Address.

EVENING

10 March
THURSDAY

069-296

Priorities

11 March
FRIDAY

070-295

12 March
SATURDAY

071-294

07 Data Bus → The data bus is a group of eight lines used for data flow. These lines are bidirectional. Data flow from microprocessor in both the direction b/w the microprocessor & peripheral devices. The microprocessor uses the data bus to perform the second function - Transfer binary information. The eight data lines enable the microprocessor to manipulate 8 bit data ranging from 00 to FF. ($2^8 = 256$ No.) - The largest No. that can appear on the data bus is 11111111 (255).
13

14 Control Bus → The control bus is comprised of various signal lines that carry synchronizing signals. The microprocessor uses such signal lines.

MARCH							2011	
W	M	T	W	T	F	S	S	S
9		1	2	3	4	5	6	
10	7	8	9	10	11	12	13	
11	14	15	16	17	18	19	20	
12	21	22	23	24	25	26	27	
13	28	29	30	31	—	—	—	

24 March
THURSDAY

25 March
FRIDAY

26 March
SATURDAY

Priorities

085 280

07 Introduction to 8085 Assembly language →

08 Instruction format

09 Opcode | Operand

10 Op code specified operation to be performed
11 Operand specify about the data on which
12 operation is to be performed.

13 In 8085 microprocessor there are
14 274 255 instructions to perform 74
15 different instruction operations.

16 The instruction is classified on the
17 basis of three criteria. —

SUNDAY

086-279

18 (i) operation performed by the instruction.
19 (ii) length of instruction.
20 (iii) Addressing mode of instruction.

21 (ii) operation performed by the instruction

22 There are different types of instruction on the basis of their operation.

MARCH							2011
W	M	T	W	T	F	S	S
9		1	2	3	4	5	6
10	7	8	9	10	11	12	13
11	14	15	16	17	18	19	20
12	21	22	23	24	25	26	27
13	28	29	30	31	-	-	-

28 March
MONDAY

Week 13
087-278
29 March
TUESDAY

088-277
WEDNESDAY

089-276

Priorities

3
T1
P1

(a) Data Transfer Instruction.

(b) Arithmetic of instruction.

(c) Logical instruction.

(d) Branch instruction.

(e) machine or processor cycle instruction.

(i) Data Transfer (move / copy) Instruction.

In this instruction the data move from source register to destination Register with out changing the content of the source register.

In this the source can be data,

Content of register, Content of memory location or contents from the I/O devices. whereas destination can be Register, memory or I/O devices.

This operation do not effect the flag register of the micro processor.

Ex → First Operation.

MOV R, M $[R] \leftarrow [H-L]$

Comments

The content of memory location whose address is in (H-L) pair is moved to register R.

MOV M, R → $[H-L] \leftarrow R$
Move the content of register R to memory location address in (H-L) pair.

Evening

31 March
THURSDAY

1 April
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090-275
Priorities

2 April
SATURDAY

091-274
092-273

MVI R, data

$[R] \leftarrow \text{data}$

MVC M, data

$[M-L] \leftarrow \text{data}$

move immediate

data to register.
Data is moved to
memory location
where address in
in $[H-L]$ pair

Arithmetic operation.

Any 8 bit No, Content of any register,
Contents of memory location can be
added to the Accumulator & the result
is stored in the Accumulator. The content
of the two register except Accumulator
can be not be added directly. one
of two operand should be

3 April
SUNDAY

093-272

Ex' \rightarrow

ADD R

$[A] \leftarrow [A] + [R]$

, Add the contents
of register to
the content of Accumu-
lator & the sum is
placed in the
Accumulator.

ADD M

$[A] \leftarrow [A] + [H-L]$

The Content of Mem
2011
MARCH
W M C O C T A T C C W S
9 1 2 3 4 5
10 7 8 9 10 11 12 13
11 14 15 16 17 18 19
12 21 22 23 24 25 26 27
13 28 29 30 31

added to the
Accumulator

4 April
MONDAY

Priorities

Inst:

ADD data

Week 14
094 271

5 April
TUESDAY

Operation

$[A] \leftarrow [A] + \text{data}$

095-270

6 April

WEDNESDAY

Comment

096-269

7

TT
Pr

0

08

09

$[A] \leftarrow [A] - [R]$

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The content of register R is subtracted from

The content of Accumulator A The result is

stored in Accumulator

12

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Logical Group \rightarrow
perform AND, OR, EX-OR, Compare, rotate etc.

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13

The instruction of this Group

Op Inst:

Operation

Comment

14

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$[A] \leftarrow [A] \wedge [R]$

16

17

18

The content of Reg. R is Anded

with The Accumulator for & result in placed in Accumulator

AND data

$[A] \leftarrow [A] \wedge \text{data}$

Given data is Anded
with The content of
Accumulator & The
result is placed in
The Accumulator

EVENING

7 April
THURSDAY

Priorities

8 April
FRIDAY

097-268

9 April
SATURDAY

098-267

099-266

ORI data

[A] \leftarrow [A] V data

Contents of Accumulator is ORed with the data & result is placed in Accumulator

Branch Group \rightarrow

The instruction of this group.

Change the sequence of the program.

There are two types of branch

Instructions. Conditional & unconditional

The conditional branch instruction transfers

the program to the specified label when certain condition is satisfied

10 April

SUNDAY

Transfer of instruction

Transfer the program to the specified label

Unconditionally

Q1

JMP (addr)(label)

[PC] \leftarrow label

Jump to the instruction specified by the label.

The program

APRIL
13 14 15 16 17
1 2 3 4 5 6 7 8 9 10
11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30

Transfers to the first.

On Conditionally

2011

Scanned by CamScanner

11 April
MONDAY

Priorities

Week 15
101-264

12 April
TUESDAY

13 April
WEDNESDAY

103-262

SC 5010H IF CY=1

PC ← 5010H

else

PC ← PC+1

change the sequence
of the program to the
location 5010H if
Carry flag is set to 1
else follow the same
sequence

→ Machine or processor cycle Construction → this
Group include the instruction for Input / output ops,
Stack & machine control. Ex. LN, OUT, PUSH

Ex:

HLT etc

LN port address → (Input to accumulator from
R/O port)

OUT port address → (Output to from accumulator
to R/O port)

HLT → Execution of instruction HLT stops
the microprocessor

2) Length of instruction → The 8085 microprocessor
processes the 8 bit or 1 byte
Hence the word size of 8085 microprocessor
is 1 byte.

EVENING