DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
μPD78212, 78213, 78214

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78212, 78213 and 78214 are 78K/II series products. The 78K/II series is an 8-bit single chip microcomputer which can access the memory space of 1M byte with an external expansion.

Functions are described in detail the following User's Manual, which should be read when carrying out design work.

μPD78214 Series User's Manual Hardware Volume	:	**IEM-1236**
78K/II Series User's Manual Instruction Volume	:	**IEU-1311**

FEATURES

- High-speed instruction execution (at 12 MHz operation) : 333 ns (μPD78212 and 78214)
  500 ns (μPD78213)
- On-chip memory ROM : 8K bytes (μPD78212)
  16K bytes (μPD78214)
  RAM : 384 bytes (μPD78212)
  512 bytes (μPD78213, 78214)
- On-chip high-performance interrupt controller
- On-chip A/D converter (8 bits × 8 channels)
- I/O pin : 54 pins
- Real-time output port (8 × 1 or 4 × 2)
- Serial interface : 2 channels
- Timer/counter (16 × 1 and 8 × 3)

APPLICATION ★

OA equipment such as printer, typewriter, PPC, FAX, etc., electronic instrument, inverter, camera

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

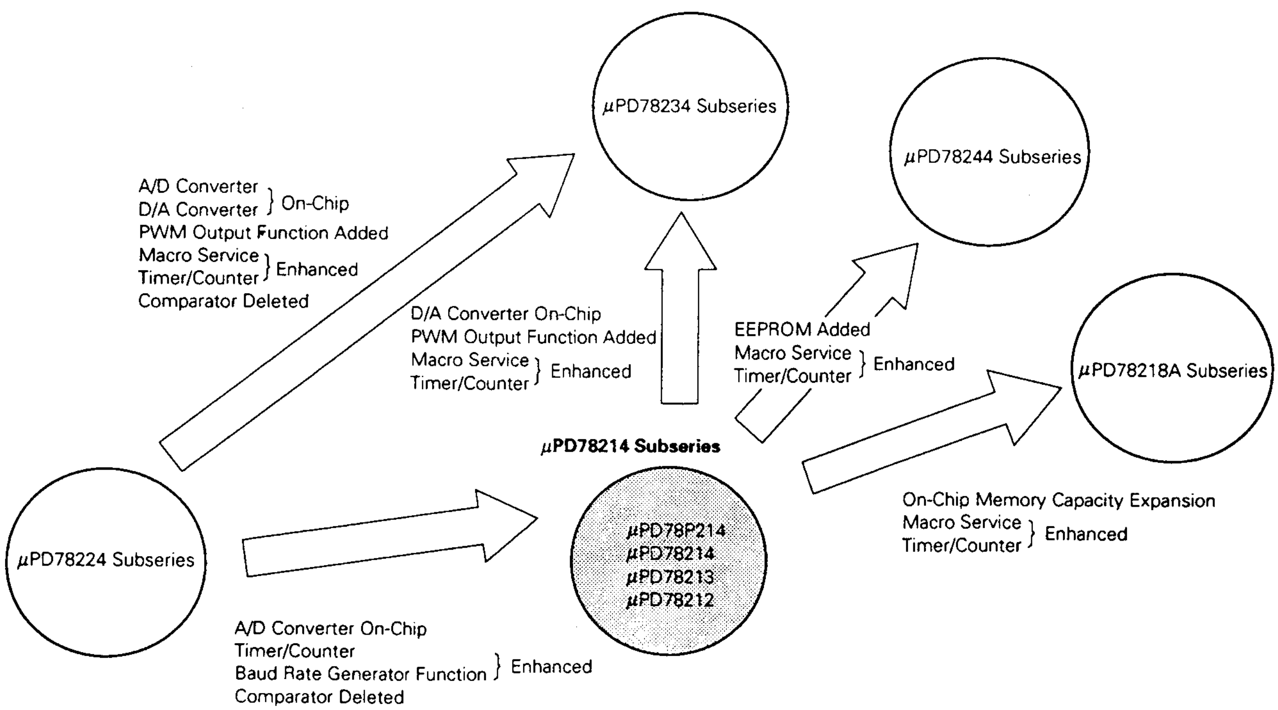
ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD78212CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78212GC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)	Standard
μPD78212GJ-xxx-5BJ	74-pin plastic QFP (20 × 20 mm)	Standard
μPD78213GC-AB8	64-pin plastic QFP (14 × 14 mm)	Standard
μPD78213GJ-5BJ	74-pin plastic QFP (20 × 20 mm)	Standard
μPD78213GQ-36	64-pin plastic QUIP	Standard
μPD78213L	68-pin plastic QFJ (□950 mil)	Standard
μPD78214CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78214GC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)	Standard
μPD78214GJ-xxx-5BJ	74-pin plastic QFP (20 × 20 mm)	Standard
μPD78214GQ-xxx-36	64-pin plastic QUIP	Standard
μPD78214L-xxx	68-pin plastic QFJ (□950 mil)	Standard

Remarks "xxx" means the specified ROM code.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/II PRODUCT LINE-UP DIAGRAM



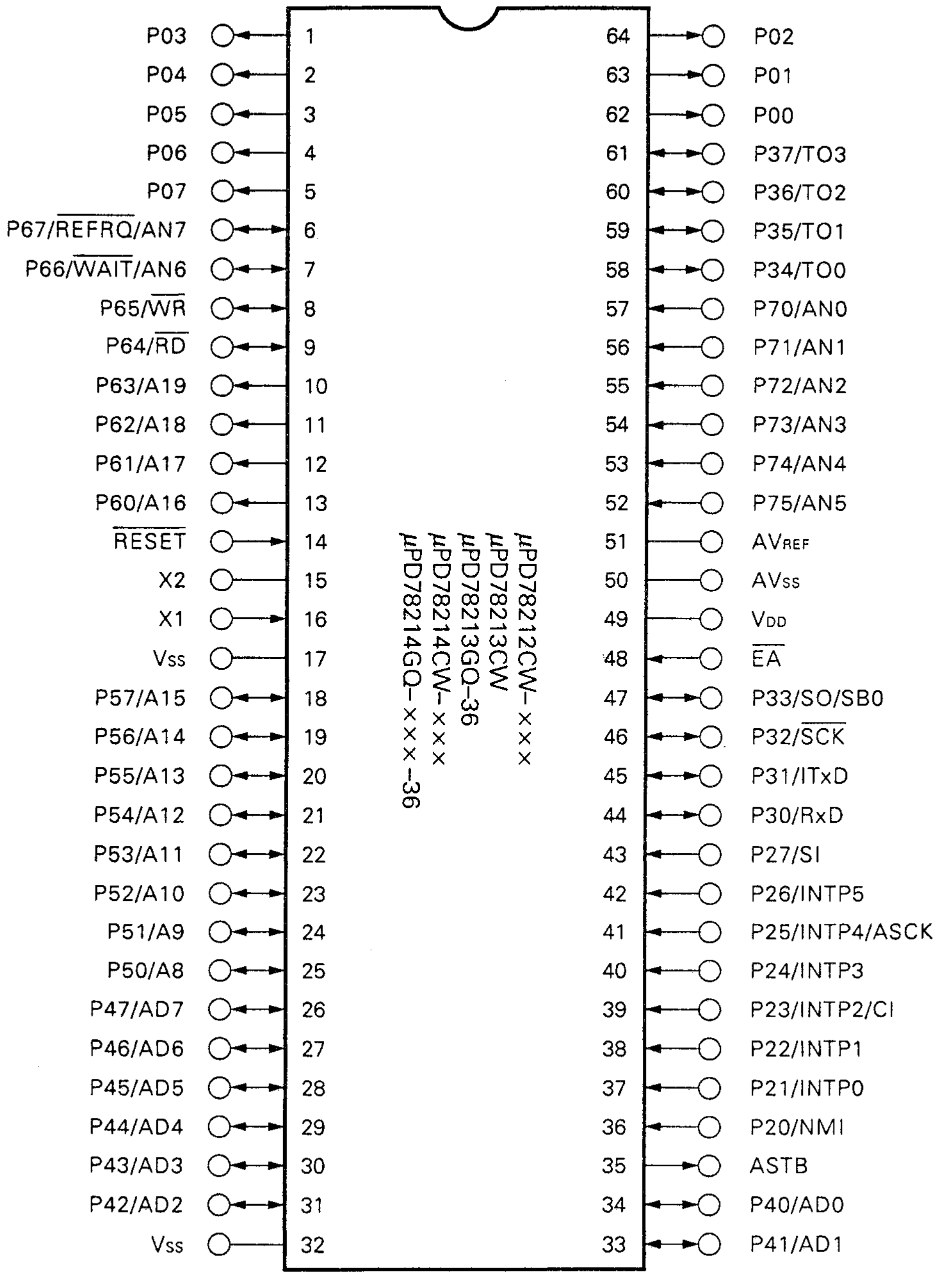
FUNCTION LIST

Item		μPD78213	μPD78212	μPD78214
Basic instruction (Mnemonic)		65		
Minimum instruction execution time (at 12 MHz operation)		500 ns	333 ns	
On-chip memory capacity	ROM	ROM-less	8K bytes	16K bytes
	RAM	512 bytes	384 bytes	512 bytes
Memory space		Program memory: 64K bytes, data memory: 1M byte		
I/O pins	Input	14		
	Output	12		
	I/O	10	28	
	Total	36	54	
Pins with additional function*	Pin with pull-up resistor	10	34	
	LED direct drive output	—	16	
	Transistor direct drive output	8		
ROM-less mode setting		ROM-less product	$\overline{EA}$ pin = High-level	
Real-time output port		4 bits × 2 or 8 bits × 1		
General register		8 bits × 8 × 4 banks (memory mapping)		
Timer/counter	16-bit timer/counter	Timer register × 1 Capture register × 1 Compare register × 2	Pulse output enable (Toggle output, PWM/PPG output)	
	8-bit timer/counter 1	Timer register × 1 Capture/compare register × 1 Compare register × 1	Pulse output enable (Real-time output: 4 bits × 2)	
	8-bit timer/counter 2	Timer register × 1 Capture register × 1 Compare register × 2	Pulse output enable (Toggle output, PWM/PPG output)	
	8-bit timer/counter 3	Timer register × 1 Compare register × 1	——	
Serial interface		UART : 1 channel (specialized baud rate generator incorporated) CSI (3-wire serial I/O, SBI) : 1 channel		
A/D converter		8-bit resolution × 8 channels		
Interrupt		19 sources (external 7, internal 12) + BRK instruction Priority order of 2 levels (programmable) 2 types of servicing (vectored interrupt, macro service)		
Instruction set		16-bit operation Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) Bit manipulation BCD adjustment, others		
Package		64-pin plastic shrink DIP (750 mil) 64-pin plastic QUIP (except μPD78212) 68-pin plastic QFJ (except □950 mil and μPD78212) 64-pin plastic QFP (14 × 14 mm) 74-pin plastic QFP (20 × 20 mm)		

* Pins with additional function included in the I/O pin.

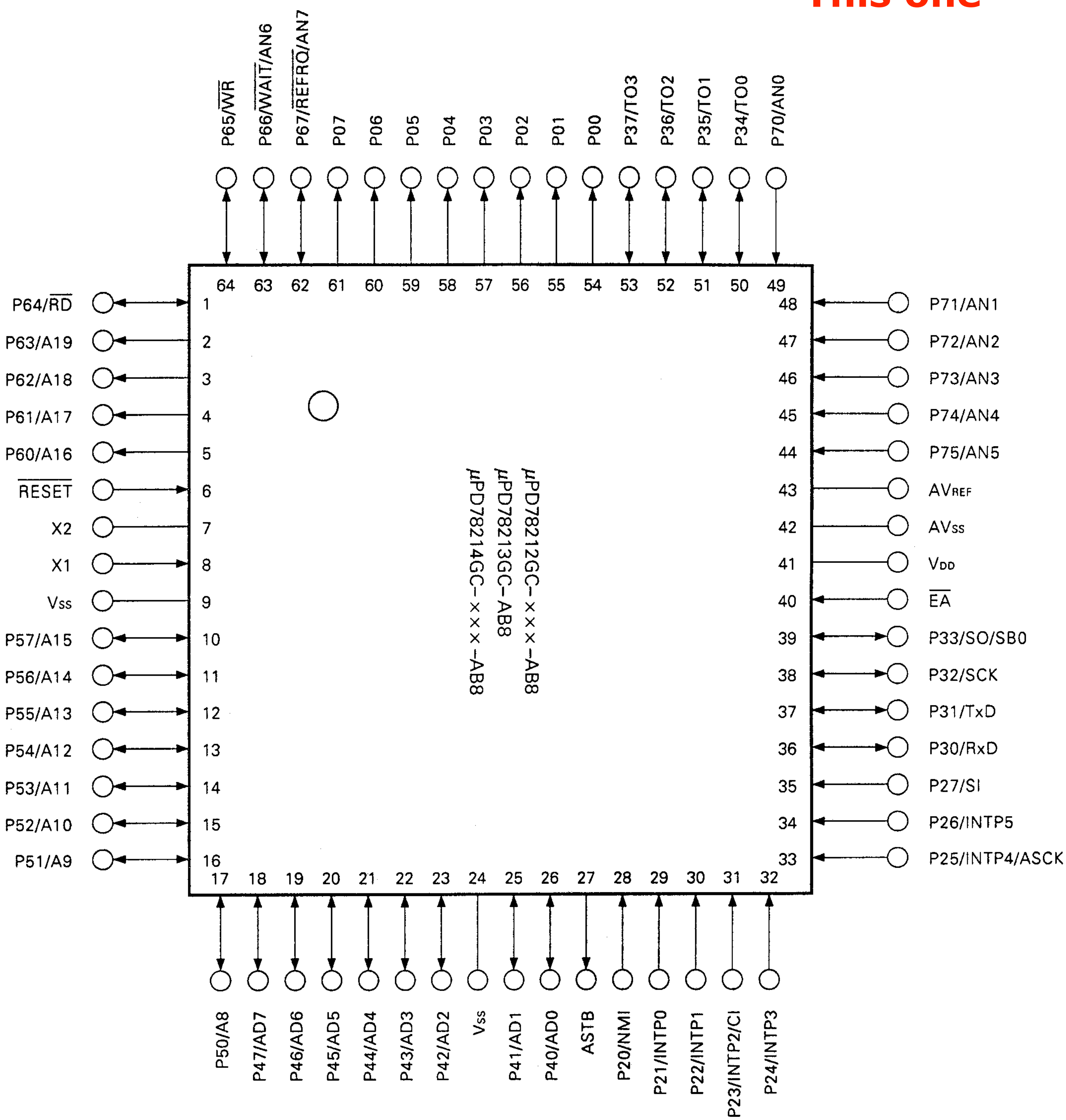
PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP, 64-pin plastic QUIP

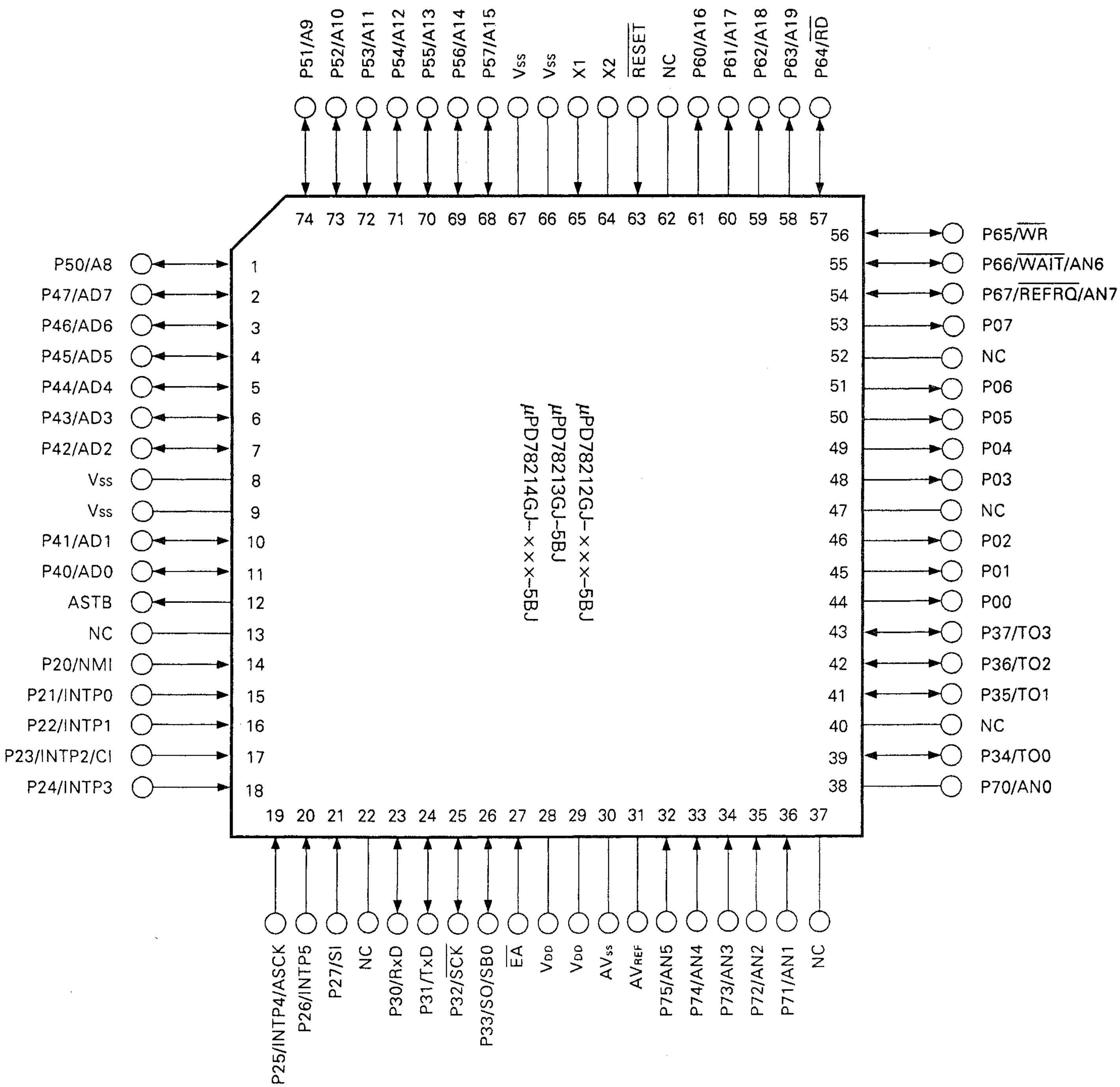


64-pin plastic QFP

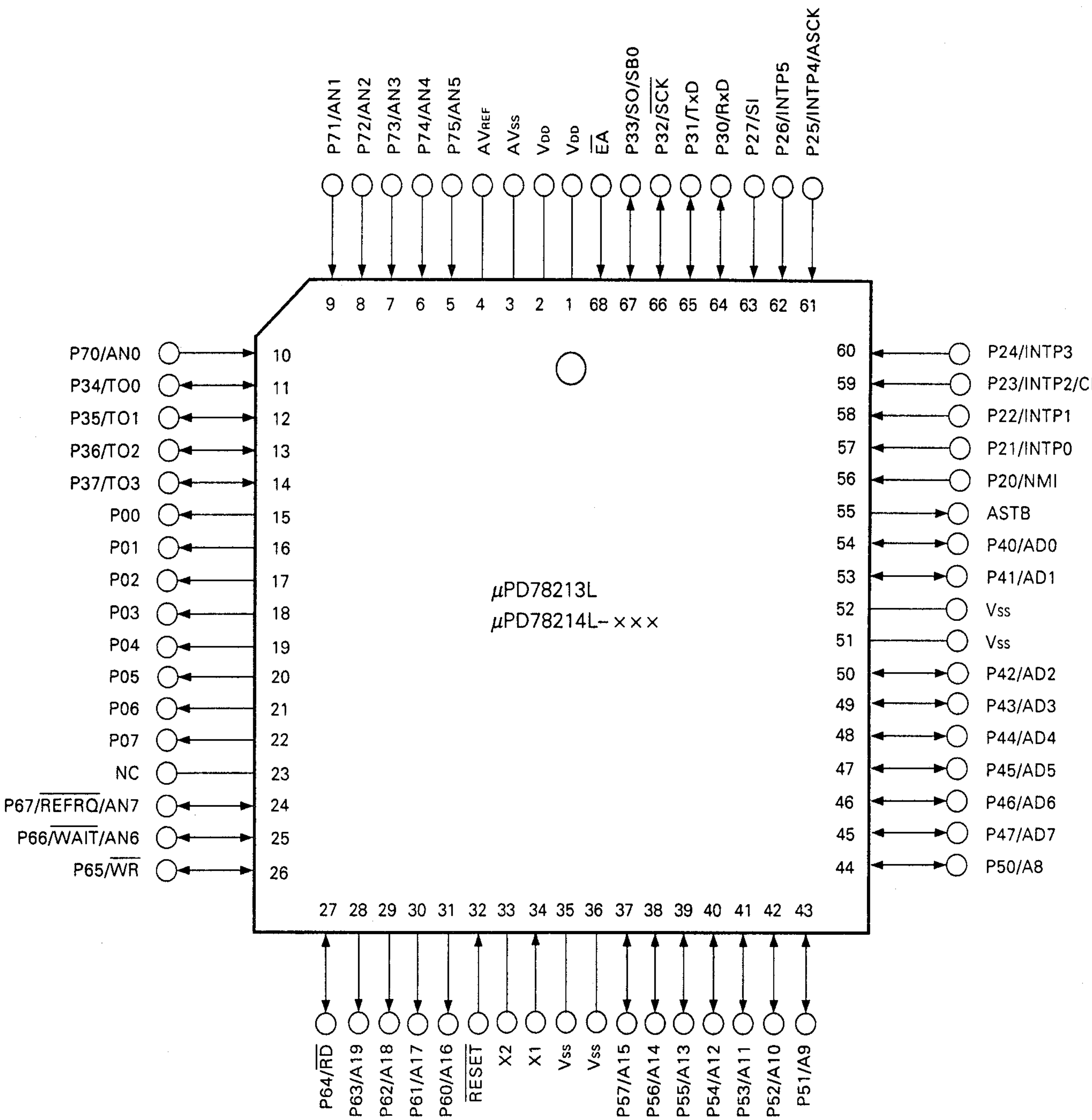
This one



74-pin plastic QFP



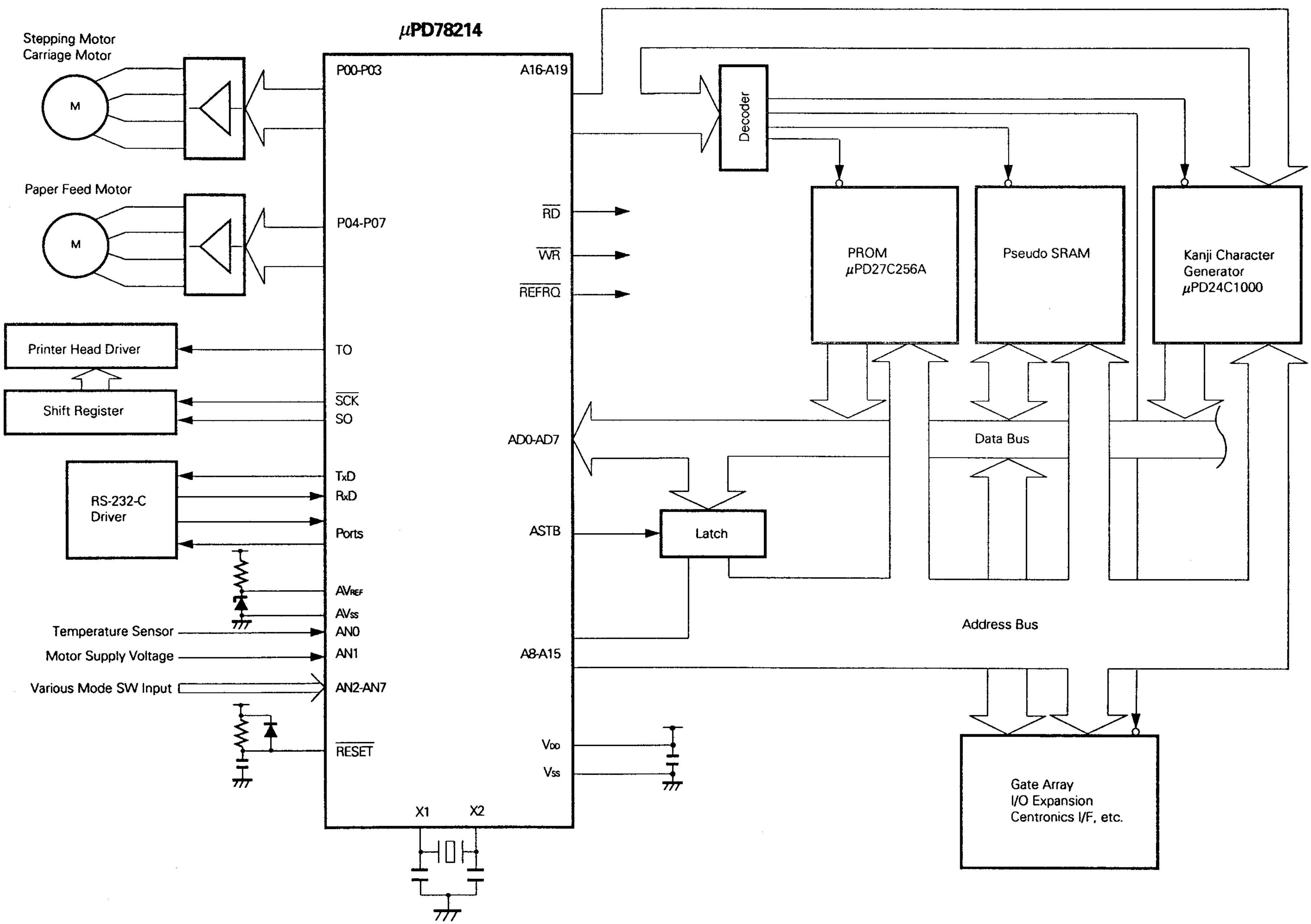
68-pin plastic QFJ



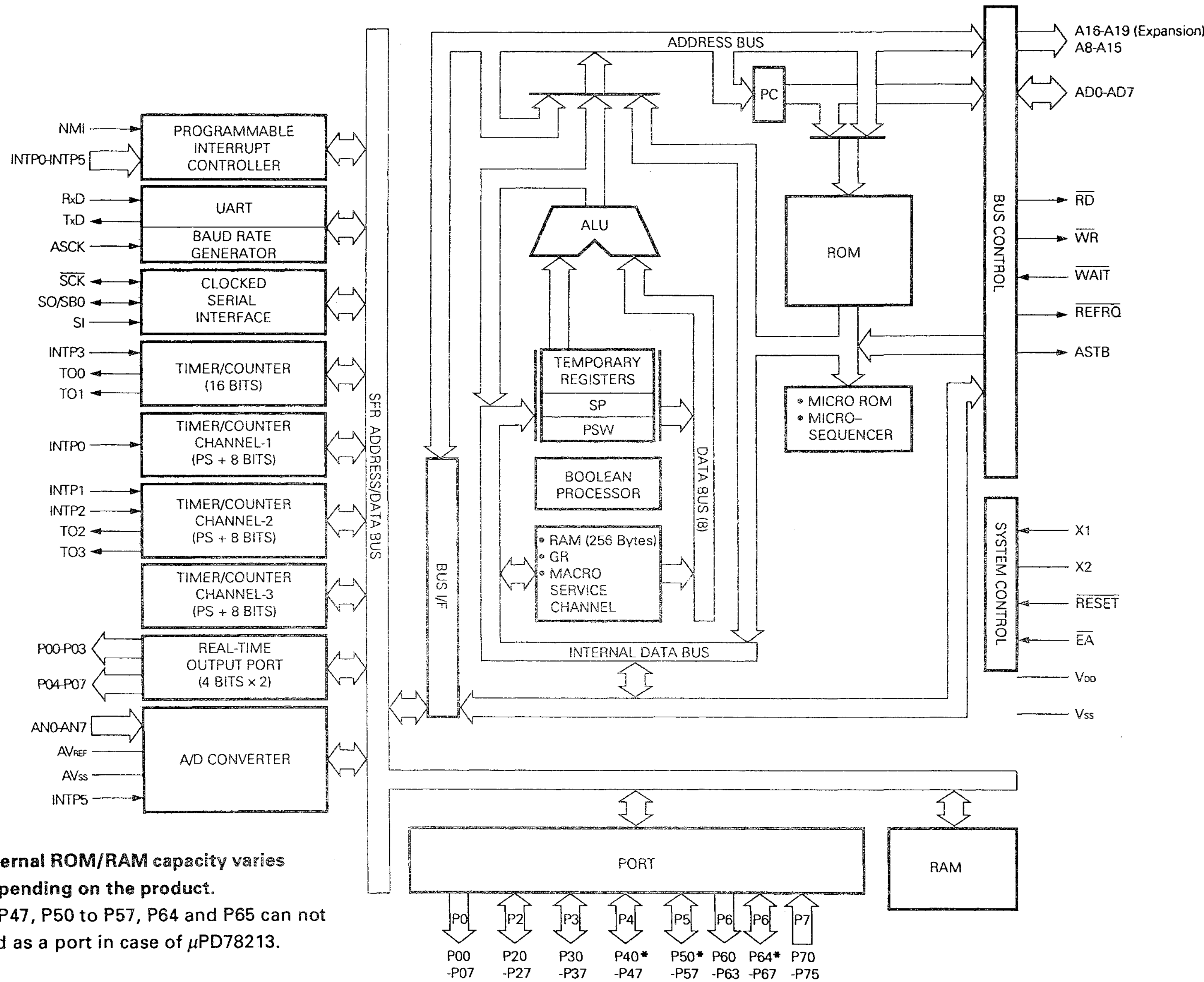
P00 to P07	: Port 0
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P70 to P75	: Port 7
TO0 to TO3	: Timer Output
CI	: Clock Input
RxD	: Receive Data
TxD	: Transmit Data
$\overline{\text{SCK}}$	: Serial Clock
ASCK	: Asynchronous Serial Clock
SB0	: Serial Bus
SI	: Serial Input
SO	: Serial Output
NMI	: Non-maskable Interrupt
INTP0 to INTP5	: Interrupt From Peripherals
AD0 to AD7	: Address/Data Bus
A8 to A19	: Address Bus

$\overline{\text{RD}}$	: Read Strobe
$\overline{\text{WR}}$	: Write Strobe
$\overline{\text{WAIT}}$	: Wait
ASTB	: Address Strobe
$\overline{\text{REFRQ}}$	: Refresh Request
$\overline{\text{RESET}}$	: Reset
X1, X2	: Crystal
$\overline{\text{EA}}$	: External Access
AN0 to AN7	: Analog Input
AV_{REF}	: Reference Voltage
AV_{SS}	: Analog Ground
V_{DD}	: Power Supply
V_{SS}	: Ground
NC	: Non-connection

SYSTEM CONFIGURATION EXAMPLE (PRINTER)



INTERNAL BLOCK DIAGRAM



Note Internal ROM/RAM capacity varies depending on the product.

* P40 to P47, P50 to P57, P64 and P65 can not be used as a port in case of μPD78213.

CONTENTS

1. PIN FUNCTIONS

1.1 PORTS

Pin Name	I/O	Dual-Function Pin	Function
P00 to P07	Output	——	Port 0 (P0): Established as a real-time output port (4 bits × 2) Direct drive of transistors capability
P20	Input	NMI	Port 2 (P2): P20 cannot be used as a general-purpose port. (Non-maskable interrupt) However, the input level can be confirmed in the interrupt routine. The connection of the on-chip pull-up resistor can be specified as a 6-bit batch for P22 to P27 by software.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK	
P26		INTP5	
P27		SI	
P30	Input/ output	RxD	Port 3 (P3): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34 to P37		TO0 to TO3	
P40 to P47*	Input/ output	AD0 to AD7	Port 4 (P4): The input/output specifiable as an 8-bit batch. The connection of the on-chip pull-up resistor specifiable as an 8-bit batch by software. LED direct drive capability.
P50 to P57*	Input/ output	A8 to A15	Port 5 (P5): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software. LED direct drive capability.
P60 to P63	Output	A16 to A19	Port 6 (P6): P64 to P67 enables to specify the input/output bit-wise. The connection of the on-chip pull-up resistor can be specified as a batch for P64 to P67 by software.
P64*	Input/ output	$\overline{RD}$	
P65*		$\overline{WR}$	
P66		$\overline{WAIT}$/AN6	
P67		$\overline{REFRQ}$/AN7	
P70 to P75	Input	AN0 to AN5	Port 7 (P7)

* Can not be used as a port in case of the μPD78213.

1.2 OTHER PORTS

Pin Name	I/O	Function	Dual-Function Pin
TO0 to TO3	Output	Timer output	P34 to P37
CI	Input	Count clock input to 8-bit timer/counter 2	P23 /INTP2
RxD	Input	Serial data input (UART)	P30
TxD	Output	Serial data output (UART)	P31
ASCK	Input	Baud rate clock input (UART)	P25/INTP4
SB0	Input /output	Serial data input/output (SBI)	P33/SO
SI	Input	Serial data input (3-wire serial I/O)	P27
SO	Output	Serial data output (3-wire serial I/O)	P33/SB0
$\overline{SCK}$	Input /output	Serial clock input/output (SBI, 3-wire serial I/O)	P32
NMI	Input	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0 to AD7	Input /output	Time multiplexing address/data bus (external memory connection)	P40 to P47*
A8 to A15	Output	Upper address bus (external memory connection)	P50 to P57*
A16 to A19	Output	Upper address when extending address (external memory connection)	P60 to P63
$\overline{RD}$	Output	Read strobe into external memory	P64*
$\overline{WR}$	Output	Write strobe into external memory	P65*
$\overline{WAIT}$	Input	Wait insertion	P66/AN6
ASTB	Output	Output Address (A0 to A7) latch timing output (at external memory accessed)	—
$\overline{REFRQ}$	Output	Refresh pulse output into external pseudo-static memory	P67/AN7
$\overline{RESET}$	Input	Chip reset	—
X1	Input	Crystal connection for system clock oscillation (capability of clock input to X1)	—
X2	—		
$\overline{EA}$	Input	ROM-less operating specification (external access of the same space as internal ROM). This is used by high level in the μPD78212 and 78214, low level in the μPD78213.	—
AN0 to AN5	Input	Analog voltage input for A/D converter	P70 to P75
AN6, AN7			P66/$\overline{WAIT}$, P67/$\overline{REFRQ}$
AV_{REF}	—	Reference voltage apply for A/D converter	—
AV_{SS}		GND for A/D converter	—
V_{DD}		Positive power supply pin	
V_{SS}		GND pin	
NC		Not connected internally	

* Can not be used as a port in case of the μPD78213.

1.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the input/output circuit configuration of each type, see Fig. 1-1.

Table 1-1 Input/Output Circuit Type of Each Pin and Recommended Connection of Unused Pins

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when not Used
P00 to P07	4	Output	Leave open.
P20/NMI	2	Input	Connected to V_{DD} or V_{SS}.
P21/INTP0			
P22/INTP1	2-A		Connected to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/SI			
P30/RxD	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P31/TxD			
P32/$\overline{\text{SCK}}$	8-A		
P33/SB0/SO	10-A		
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19	4	Output	Leave open.
P64/$\overline{\text{RD}}$	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$/AN6	11		Input : Connected to V_{DD}.* Output : Leave open.
P67/$\overline{\text{REFRQ}}$/AN7			
P70/AN0 to P75/AN5	9	Input	Connected to V_{SS}.
ASTB	4	Output	Leave open.
$\overline{\text{RESET}}$	2	Input	—
$\overline{\text{EA}}$	1		
AV_{REF}	—		Connected to V_{SS} or V_{DD}.*
AV_{SS}			Connected to V_{SS}.

★ **Note** **If the input and output are not stable on the dual-function pin as input and output, connect to V_{DD} via a resistor of tens of k . (Especially, if the reset input pin exceeds the low level input voltage at power-on or in case of change the input/output by software.)**

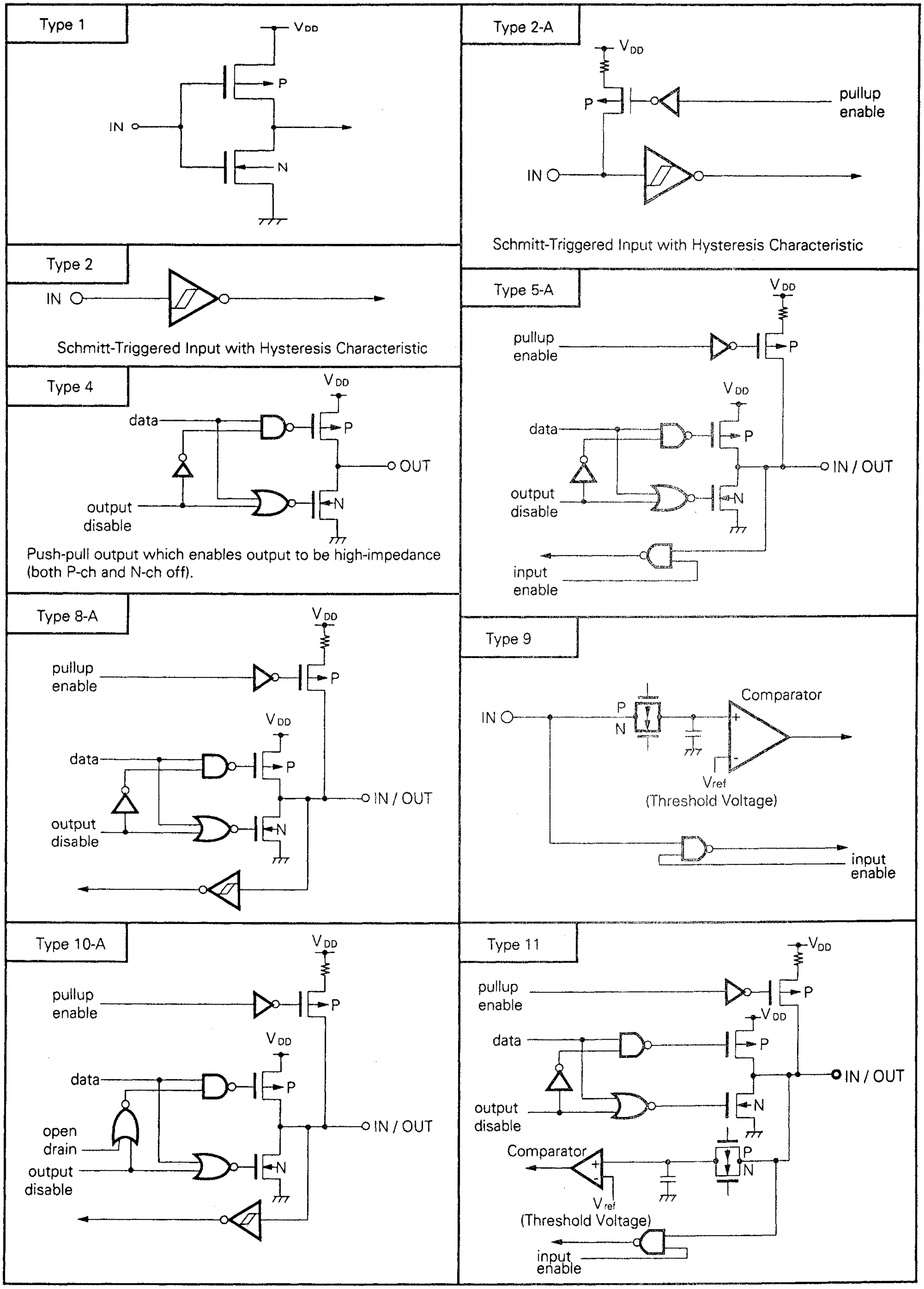
Remarks The type numbers are standardized by 78K series, therefore they are not always consecutive numbers in each product. (Some circuits are not incorporated.)

* In the following status, do not apply a voltage outside the range AV_{SS} to AV_{REF} to relevant pins, as the μPD78212, 78213 and 78214 may be damaged.

Status	Pins
A/D conversion operation	Pins for A/D conversion
A/D converter not used (or not operated)	Pins selected by the A/D converter mode register (ADM) • MS bit = 1 → Pins which are A/D converted when A/D conversion is specified • MS bit = 0 → AN0 pin

When the A/D converter is not used, if the AV_{REF} pin is fixed at the V_{SS} level, the AN0 (P70) pin is automatically selected after $\overline{RESET}$ input. Fix the AN0 pin at the V_{SS} level, or set the AV_{REF} pin to the V_{DD} level,and set the AN0 pin level to the AV_{REF} level or below.

Fig. 1-1 Pin Input/Output Circuits



2. INTERNAL BLOCK FUNCTION

2.1 MEMORY SPACE

The μPD78212, 78213 and 78214 can access a 1M-byte memory space. The Fig. 2-1 and 2-2 show that memory space. The program memory mapping depends on the $\overline{EA}$ pin status.

(1) In case of the μPD78212

The program memory is mapped into the internal ROM (8K bytes: 00000H to 01FFFH) and the external memory (56704 bytes: 02000H to 0FD7FH). The external memory is accessed by the external memory expansion mode. The mapping area into the external memory is shareable with the data memory.

The data memory is mapped into the internal RAM (384 bytes: 0FD80H to 0FEFFH). In the 1M byte extended mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as the expansion data memory.

(2) In case of the μPD78213

The program memory is mapped into the external memory (64768 bytes: 00000H to 0FCFFH). This area is shareable with a data memory.

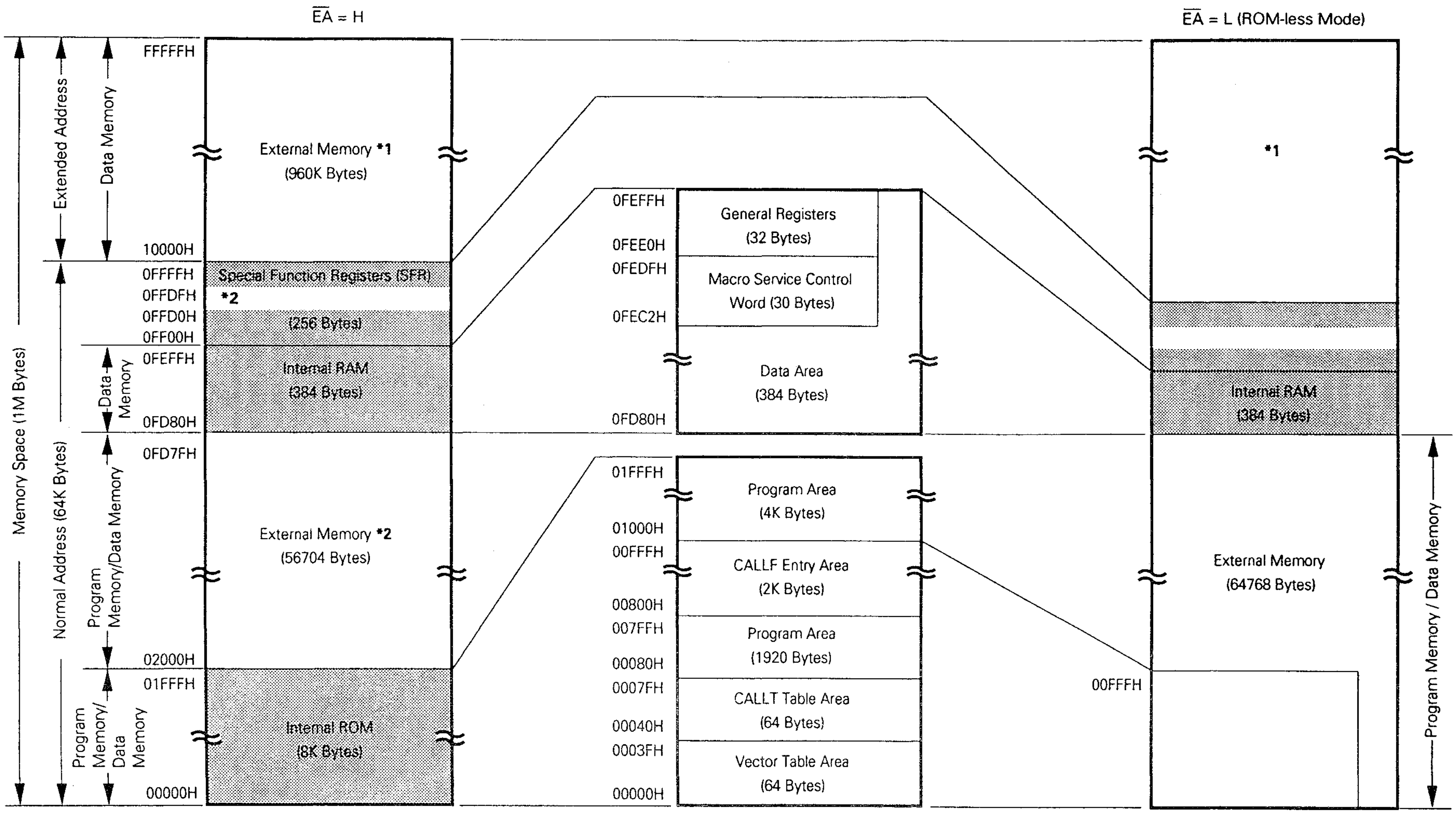
The data memory has been mapped into the internal RAM (512 bytes: 0FD00H to 0FEFFH). In the 1M byte expansion mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as a expansion data memory.

(3) In case of the μPD78214

The program memory is mapped into the internal ROM (16K bytes: 00000H to 03FFFH) and the external memory (48384 bytes: 04000H to 0FCFFH). The external memory is accessed by the external memory expansion mode. The mapping area into the external memory is shareable with the data memory.

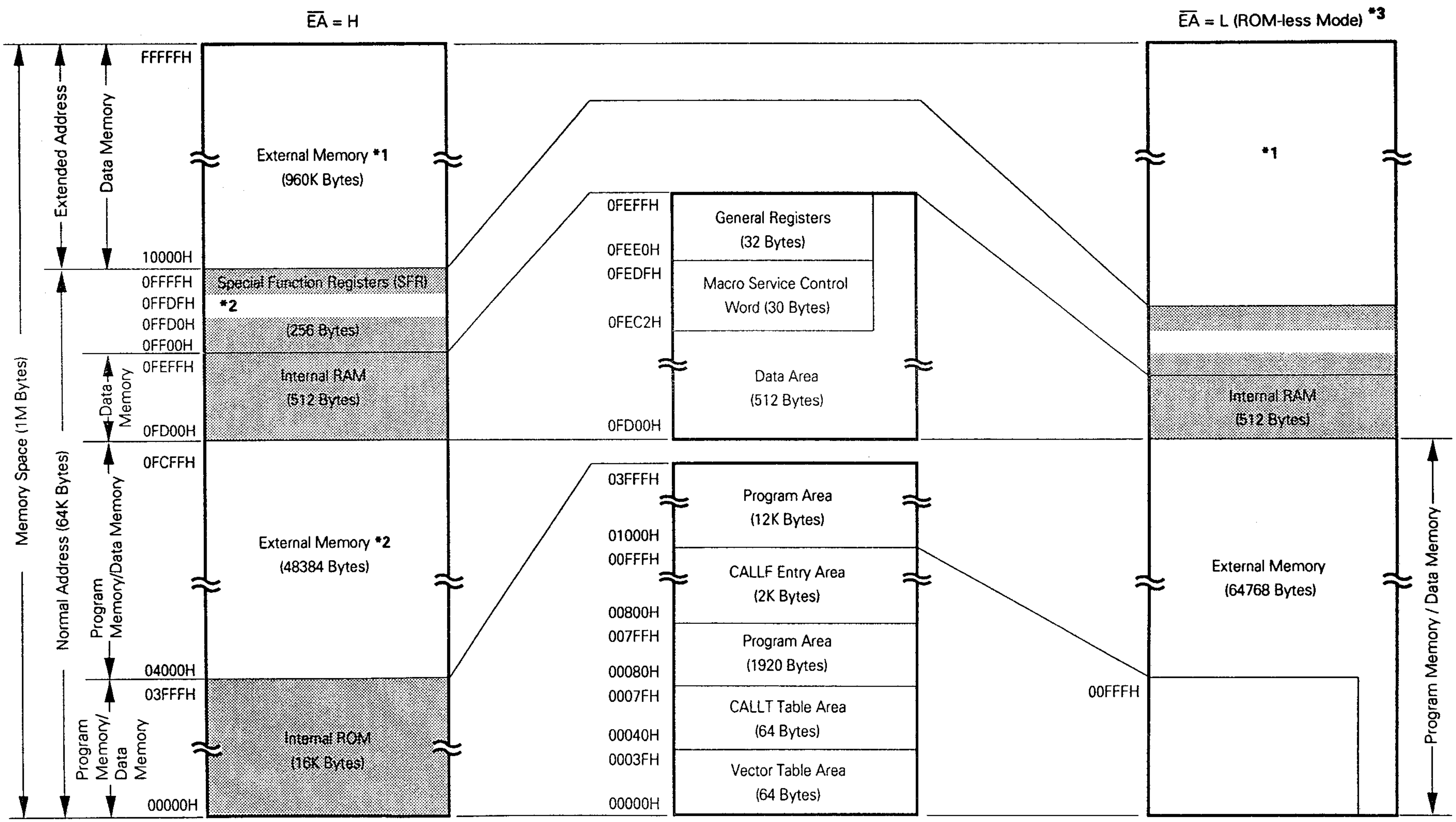
The data memory has been mapped into the internal memory (512 bytes: 0FD00H to 0FEFFH). In the 1M byte extended mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as the expansion data memory.

Fig. 2-1 μPD78212 Memory Map



* 1. Accessed by 1M-byte expansion mode. Shaded area denotes internal memory.
2. Accessed by external memory expansion mode.

Fig. 2-2 μPD78213/78214 Memory Map

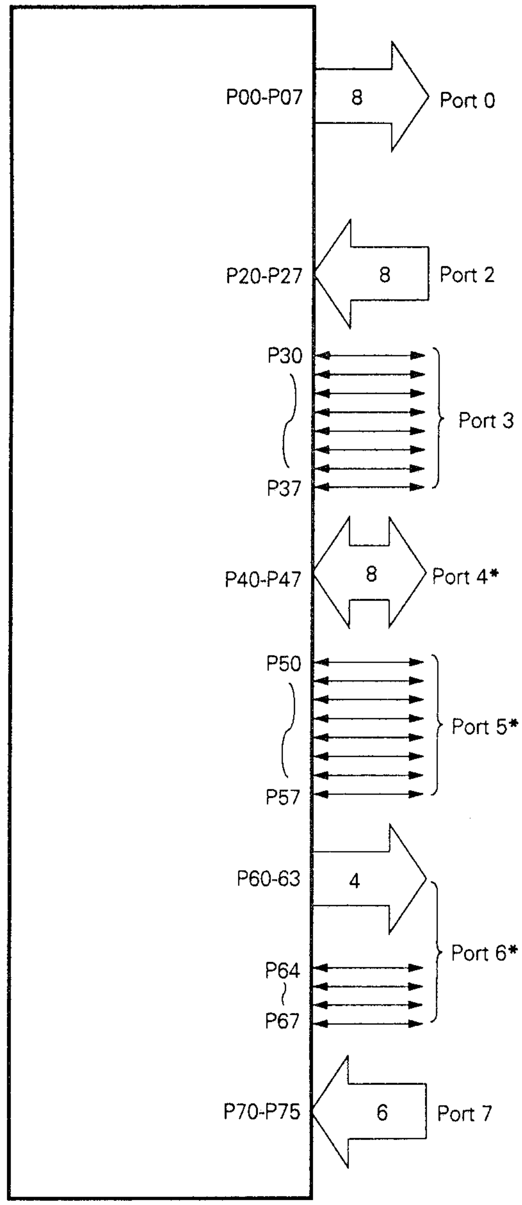


* 1. Accessed by 1M-byte expansion mode. ▒ Shaded area denotes internal memory.
2. Accessed by external memory expansion mode.
3. μPD78213 only when $\overline{EA}$ = L

2.2 PORT

The μPD78212, 78213 and 78214 are equipped with ports as Fig. 2-3, operable for various controls. The function of each port describes Table 2-1. The port 2 to port 6 can be specified to use the on-chip pull-up resistor by software at power-on.

Fig. 2-3 Port Configuration



* P40 to P47, P50 to P57, P64 and P65 can not be used as a port in case of the μPD78213.

Table 2-1 Port Function

Name	Pin Name	Function	Designation of Software Pull-Up
Port 0	P00 to P07	Outputs or high-impedance specifiable as an 8-bit batch. Operable as 4-bit real-time output (P00 to P03, P04 to P07). Transistor direct drive capability.	—
Port 2	P20 to P27	Input port	6-bit batch (P22 to P27)
Port 3	P30 to P37	Input or output specifiable bit-wise	Input mode pins specifiable as a batch.
Port 4*	P40 to P47	Input or output specifiable as an 8-bit batch. LED direct drive capability.	8-bit batch
Port 5*	P50 to P57	Input or output specifiable bit-wise. LED direct drive capability.	Input mode pins specifiable as a batch.
Port 6*	P60 to P63	Output port	—
	P64 to P67	Input or output specifiable bit-wise	Input mode pins specifiable as a batch.
Port 7	P70 to P75	Input port	—

* P40 to P47, P50 to P57, P64 and P65 can not be used as a port in case of the μPD78213.

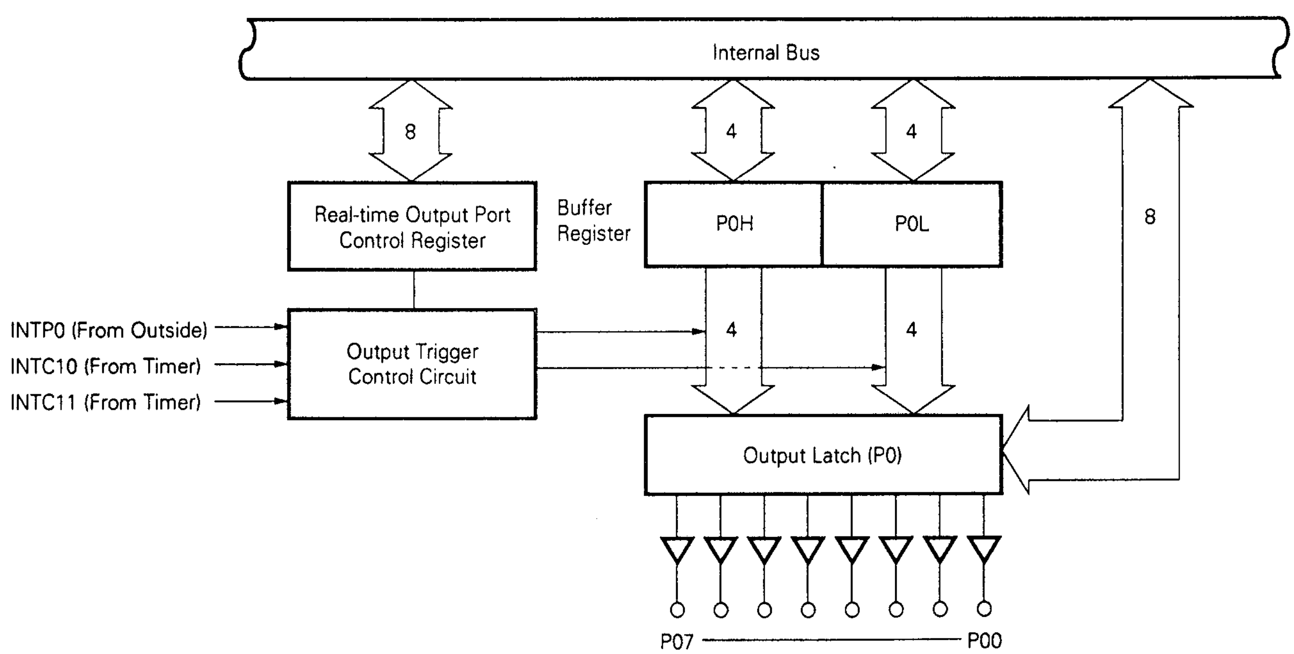
2.3 REAL-TIME OUTPUT PORT

The real-time output port outputs the data stored in the buffer in synchronization with a timer match interrupt or external interrupt. Therefore, a pulse output without jitter can be acquired.

Accordingly, this is suitable for the application (open loop control of a stepping motor, etc.) which outputs any pattern at any interval.

As Fig. 2-4, the port 0 and buffer register are the core of the configuration.

Fig. 2-4 Real-Time Output Port Block Diagram



2.4 TIMER/COUNTER UNIT

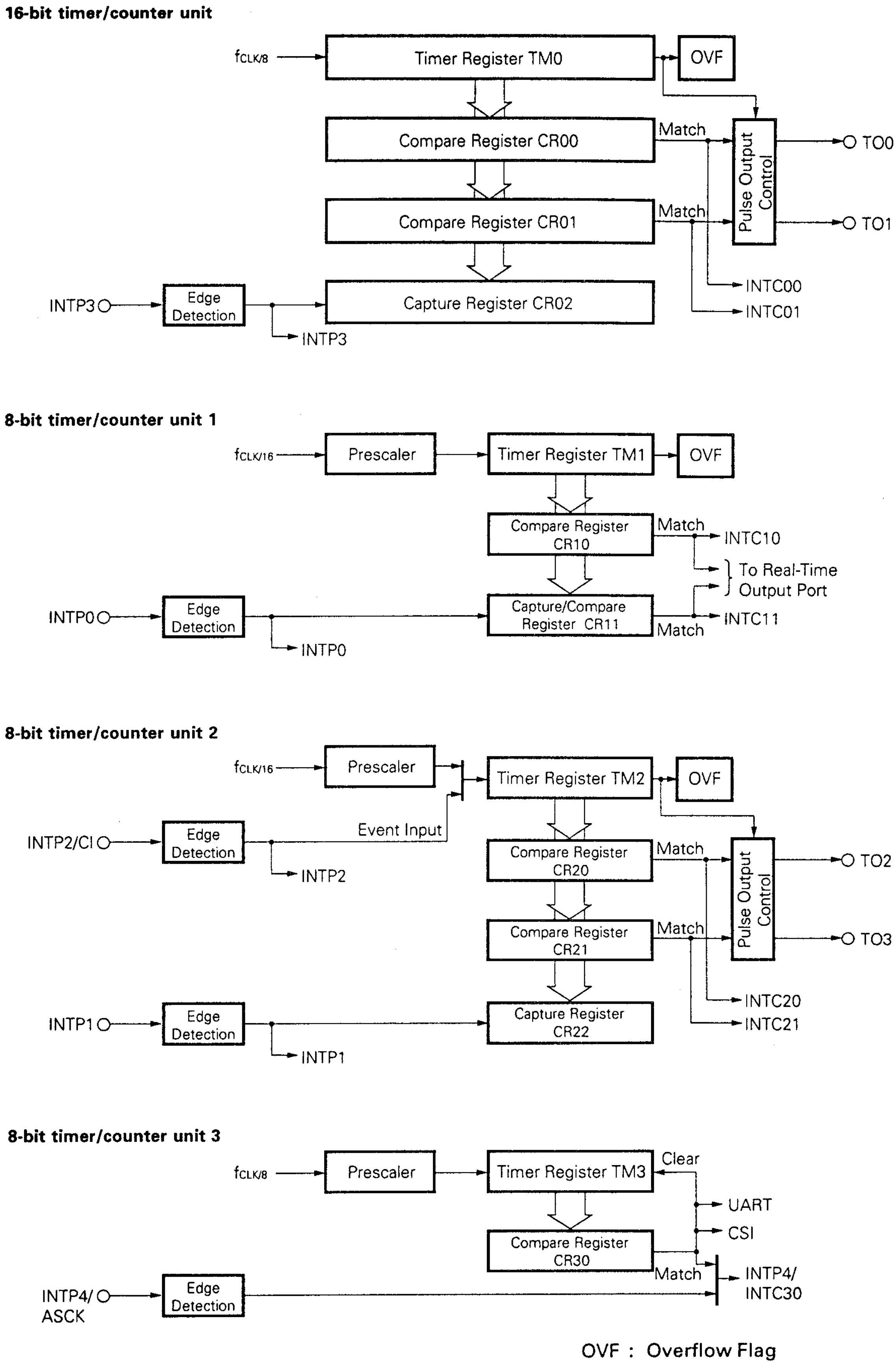
The μPD78212, 78213 and 78214 incorporate one channel of a 16-bit timer/ counter unit and 3 channels of an 8-bit timer/counter unit.

Table 2-2 Types and Functions for Timer/Counter

Type & Function \ Unit		16-Bit Timer/ Counter	8-Bit Timer/ Counter 1	8-Bit Timer/ Counter 2	8-Bit Timer/ Counter 3
Type	Interval timer	2ch	2ch	2ch	1ch
	External event counter	—	—	○	—
	One shot timer	—	—	○	—
Function	Timer output	2ch	—	2ch	—
	Toggle output	○	—	○	—
	PWM/PPG output	○	—	○	—
	Real-time output	—	○	—	—
	Pulse amplitude measurement	○	○	○	—
	Number of interrupt requests	2	2	2	1
	Clock source of serial interface	—	—	—	○

As 7 interrupt requests are supported in total, this functions as the timer of the 7 channels.

Fig. 2-5 Timer/Counter Unit Block Diagram



2.5 A/D CONVERTER

The μPD78212, 78213 and 78214 incorporate an analog/digital (A/D) converter with 8 multiplexed analog inputs (AN0 to AN7).

The conversion is a successive approximation and the conversion result is stored in the 8-bit A/D conversion result register (ADCR). Therefore, the conversion can be executed at high speed and accuracy (converting time 30 μs approximately: At 12 MHz operation).

This prepares the following modes to start the A/D converting operation.

- ○ Hardware start: Starts the conversion with a trigger input (INTP5).
- ○ Software start: Starts the conversion by setting a bit of A/D converter mode register (ADM).

Also, the following modes are prepared for the operation after started.

- ○ Scan mode : Selects analog inputs one after another and acquires the converted data from all pins.
- ○ Select mode : Fixes analog inputs to one pin and acquires the continuous conversion value.

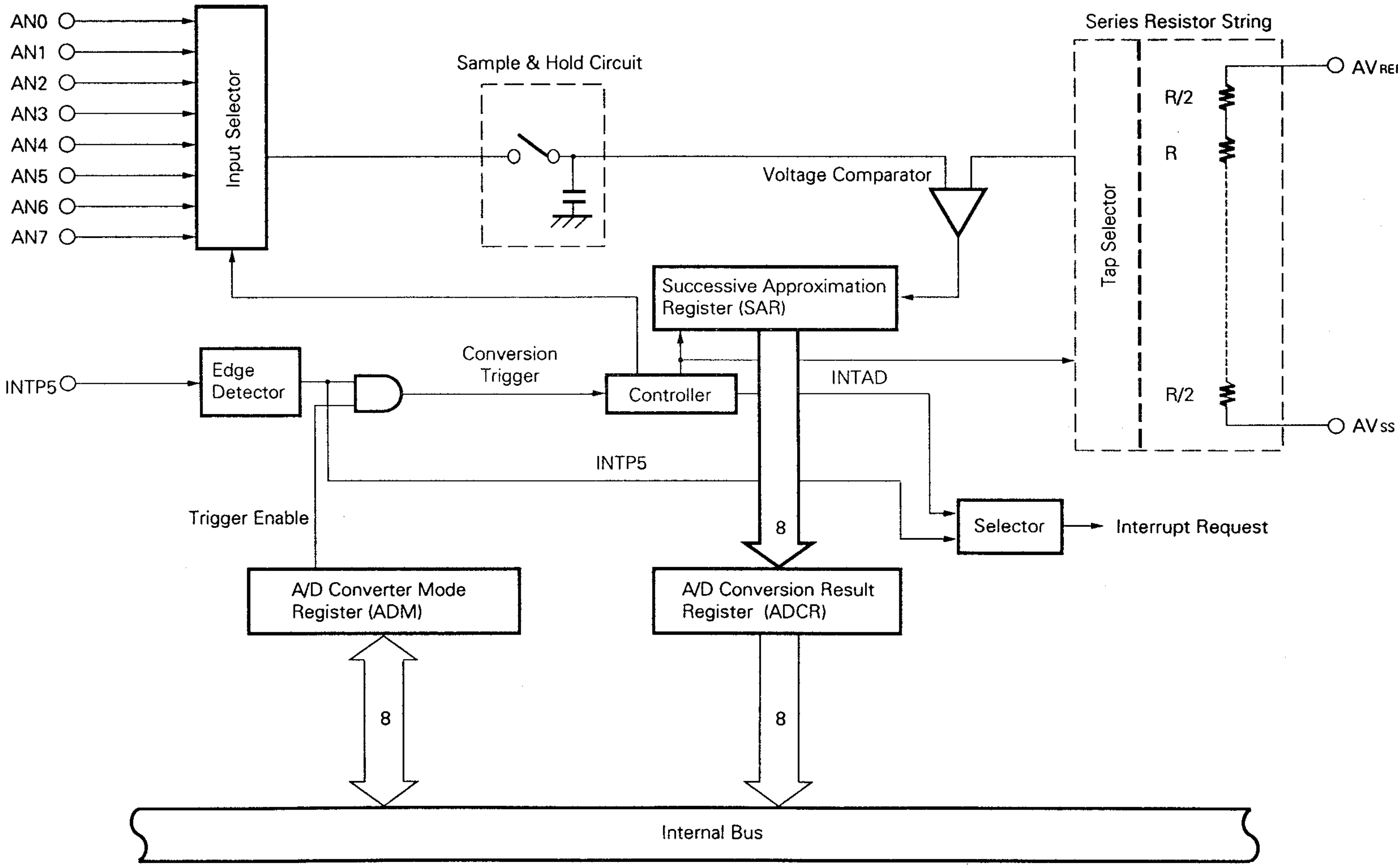
When stopping the above modes and the converting operation, all of them are specified by ADM.

The interrupt request (INTAD) occurs when the converted result is sent to ADCR, the interrupt request INTAD is generated (except the software start select mode). Therefore, by means of the macro service, the converted values can be sent into the memory continuously.

Table 2-3 INTAD Generation Mode

	Scan Mode	Select Mode
Hardware start	○	○
Software start	○	—

Fig. 2-6 A/D Converter Block Diagram



2.6 SERIAL INTERFACE

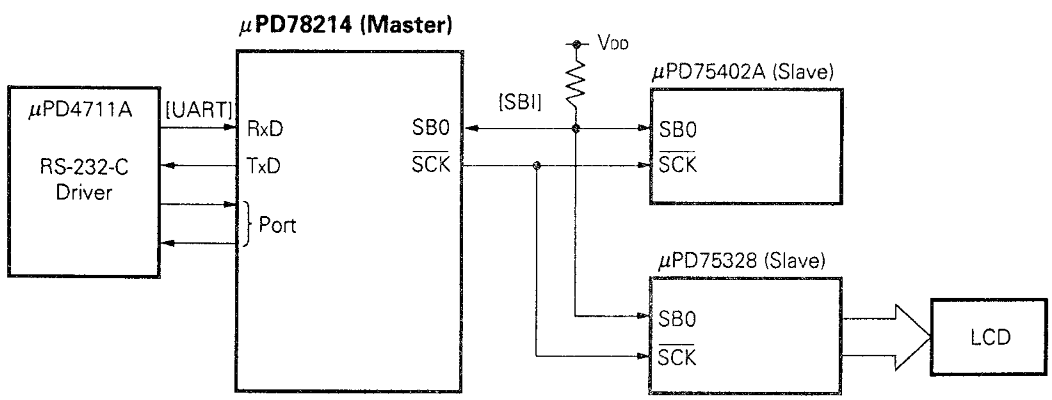
The μPD78212, 78213 and 78214 are equipped with 2 independent channels for serial interfaces.

- Asynchronous serial interface (UART)
- Clocked serial interface (CSI)
  - 3-wire serial I/O
  - Serial bus interface (SBI)

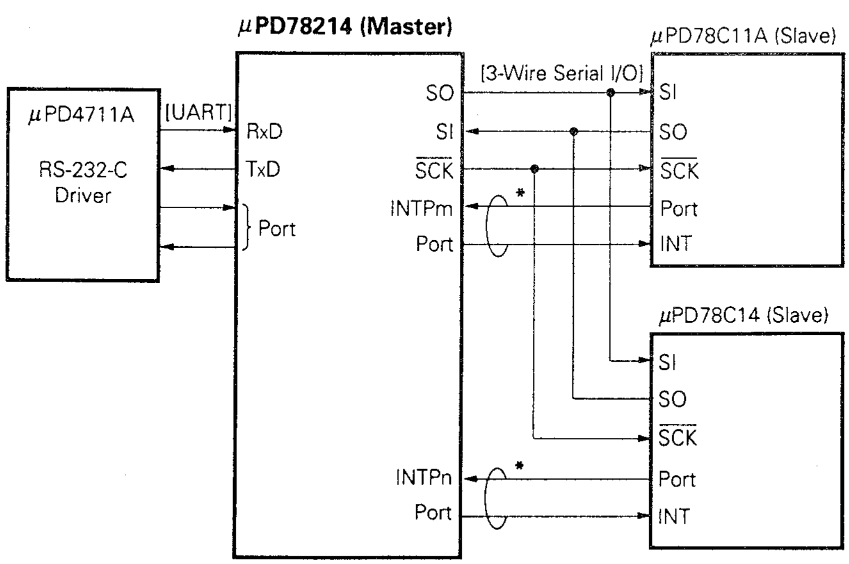
This enables both a communication with the external system and a local communication in the system simultaneously (see **Fig. 2-7**).

Fig. 2-7 Example of Serial Interface

(a) UART + SBI



(b) UART + 3-wire serial I/O



* Handshake line

2.6.1 Asynchronous Serial Interface

A UART (Universal Asynchronous Receiver Transmitter) has been incorporated as an asynchronous serial interface. This is the method to transmit the one byte data following the start bit.

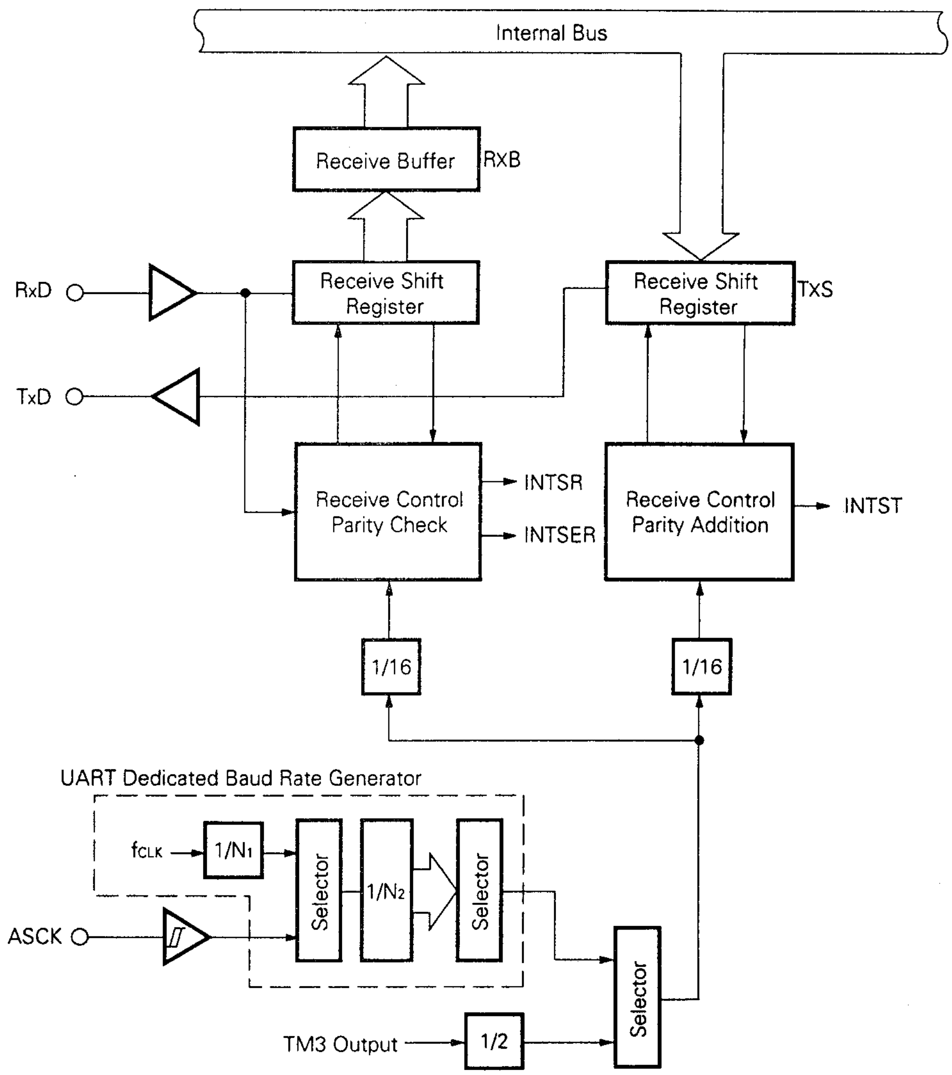
As UART dedicated baud rate generator is incorporated, communications are possible with a wide range of any baud rate.

Also, the baud rate can be defined by dividing the input clock for the ASCK pin.

Moreover, a baud rate can be generated with 8-bit timer/ counter 3.

If the UART dedicated baud rate generator is used, the baud rate (31.25 kbps) of the MIDI specification can be acquired.

Fig. 2-8 Asynchronous Serial Interface Block Diagram

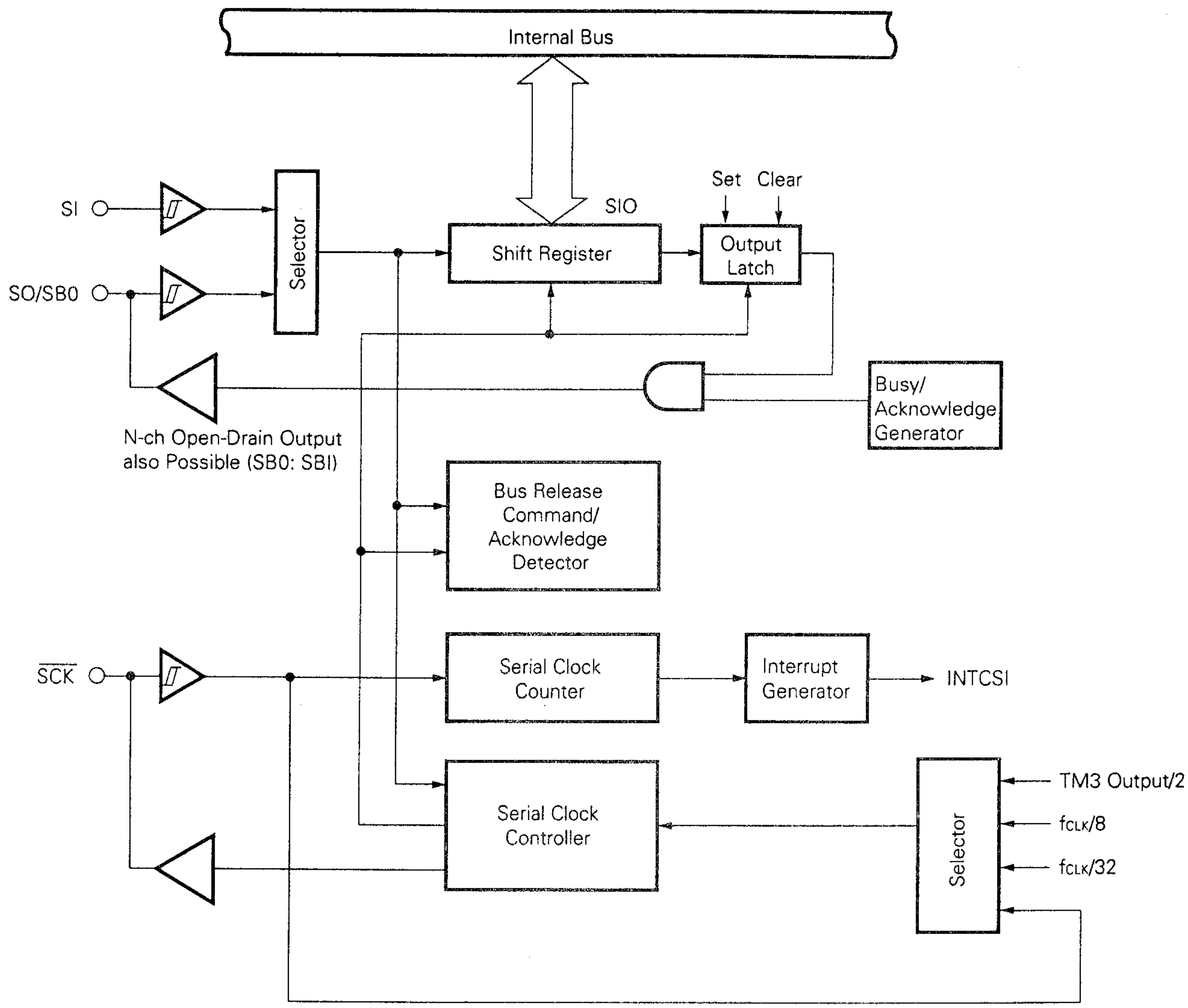


f_{CLK} : Internal system clock frequency (system clock frequency / 2)

2.6.2 Clocked Serial Interface

This is a method to communicate one byte data in synchronization with the serial clock which is activated by master device and starts to transmit.

Fig. 2-9 Clocked Serial Interface Block Diagram



f_{CLK} : Internal system clock frequency (system clock frequency / 2)

(1) 3-wire serial I/O

This is a interface to communicate with a device which incorporates a conventional clocked serial interface.

Basically, the communication is made through 3 wires of serial clock ($\overline{SCK}$) and serial data (SI, SO). In case of connecting with multiple devices, the handshake line is required.

(2) SBI

This can communicate with multiple devices through 2 wires of serial clock ($\overline{SCK}$) and serial bus (SB0) and this is a NEC standard serial interface.

The master device outputs "address" from the SB0 pin and selects the communicated slave device. Then, "command" and "data" are transmitted and received between the master and slave.

3. INTERNAL/EXTERNAL CONTROL FUNCTION

3.1 INTERRUPT

The interrupt request servicing can be selected from 2 modes in the following table.

Table 3-1 Interrupt Request Servicing

Servicing Mode	Servicing Subject	Servicing	PC, PSW Contents
Vectored interrupt	Software	Branches to service routine, and executes (any servicing contents)	With save and return
Macro service	Firmware	Data transmission, etc. between memory and I/O (fixed servicing contents)	Hold

3.1.1 Interrupt Source

The interrupt source includes the 19 types and a BRK instruction execution as shown in Table 3-2.

The priority of the interrupt servicing can be set to 2 levels (high and low priority levels). Therefore, it can separate the levels of the nest control which the interrupt is in progress and the interrupt request which occurs simultaneously (see **Fig. 3-1**, **Fig. 3-2**). But the nesting advances certainly in the macro service (not held).

The default priority is the priority level (fixed) to service the interrupt requests which occur at the same level simultaneously (see **Fig. 3-2**).

Table 3-2 Interrupt Source

<table>
<tr><th rowspan="2">Type</th><th rowspan="2">Default Priority</th><th colspan="2">Source</th><th rowspan="2">Internal/ External</th><th rowspan="2">Macro Service</th></tr>
<tr><th>Name</th><th>Trigger</th></tr>
<tr><td>Software</td><td rowspan="2">—</td><td>BRK</td><td>Instruction execution</td><td>—</td><td rowspan="2">—</td></tr>
<tr><td>Non-Maskable</td><td>NMI</td><td>Pin input edge detection</td><td rowspan="5">External</td></tr>
<tr><td rowspan="19">Maskable</td><td>0 (highest)</td><td>INTP0</td><td>Pin input edge detection (TM1 capture trigger)</td><td rowspan="15">○</td></tr>
<tr><td>1</td><td>INTP1</td><td>Pin input edge detection (TM2 capture trigger)</td></tr>
<tr><td>2</td><td>INTP2</td><td>Pin input edge detection (TM2 event counter input)</td></tr>
<tr><td>3</td><td>INTP3</td><td>Pin input edge detection (TM0 capture trigger)</td></tr>
<tr><td>4</td><td>INTC00</td><td>TM0 to CR00 match signal generation</td><td rowspan="5">Internal</td></tr>
<tr><td>5</td><td>INTC01</td><td>TM0 to CR01 match signal generation</td></tr>
<tr><td>6</td><td>INTC10</td><td>TM1 to CR10 match signal generation</td></tr>
<tr><td>7</td><td>INTC11</td><td>TM1 to CR11 match signal generation</td></tr>
<tr><td>8</td><td>INTC21</td><td>TM2 to CR21 match signal generation</td></tr>
<tr><td rowspan="2">9</td><td>INTP4</td><td>Pin input edge detection</td><td>External</td></tr>
<tr><td>INTC30</td><td>TM3 to CR30 match signal generation</td><td>Internal</td></tr>
<tr><td rowspan="2">10</td><td>INTP5</td><td>Pin input edge detection</td><td>External</td></tr>
<tr><td>INTAD</td><td>A/D converter conversion termination (transfer to ADCR)</td><td rowspan="6">Internal</td></tr>
<tr><td>11</td><td>INTC20</td><td>TM2 to CR20 match signal generation</td></tr>
<tr><td>12</td><td>INTSER</td><td>ASI receive error generation</td><td>—</td></tr>
<tr><td>13</td><td>INTSR</td><td>ASI receive termination</td><td rowspan="3">○</td></tr>
<tr><td>14</td><td>INTST</td><td>ASI transmit termination</td></tr>
<tr><td>15 (lowest)</td><td>INTCSI</td><td>CSI transfer termination</td></tr>
</table>

TM0 : 16-bit timer
TM1 to TM3 : 8-bit timer
ASI : Asynchronous serial interface
CSI : Clocked serial interface

Fig. 3-1 Servicing Example for Another Interrupt Request Occurrence while an Interrupt Servicing

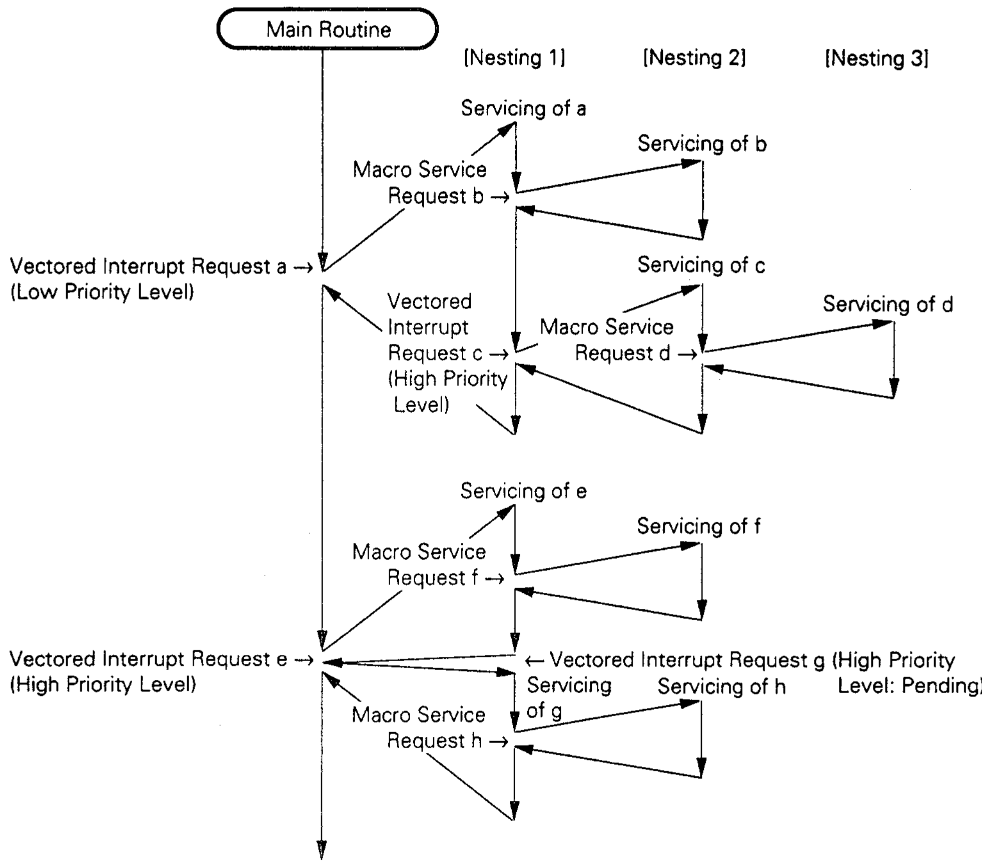
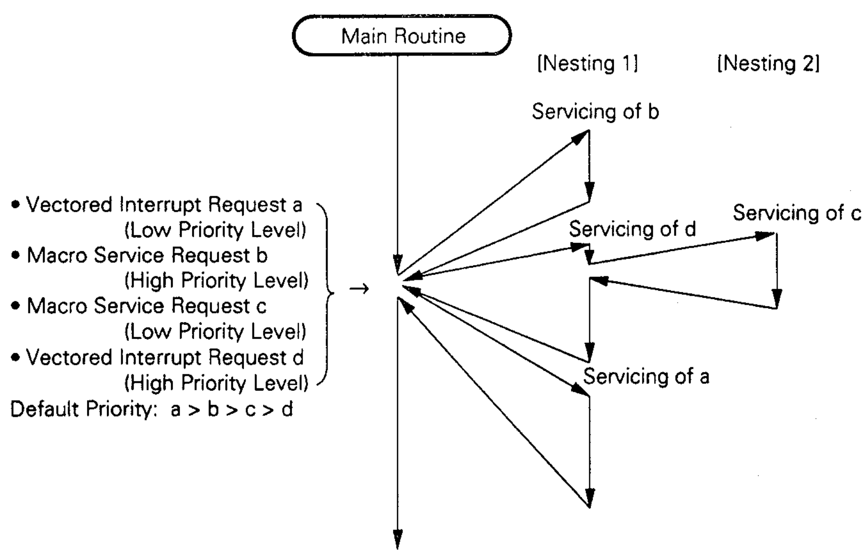


Fig. 3-2 Servicing Example for Simultaneous Occurred Interrupt Request



3.1.2 Vectored Interrupt

The memory contents of the vector table address, which corresponds to the interrupt source, is branched into the processing routine as a destination address.

As the CPU executes the interrupt servicing, the following operations occur.

- O When branch: Saving the CPU status (PC, PSW contents) to the stack.
- O When return: Returning the CPU status (PC, PSW contents) from the stack.

The RETI instruction executes returning to the main routine from the processing routine.

Table 3-3 Vector Table Address

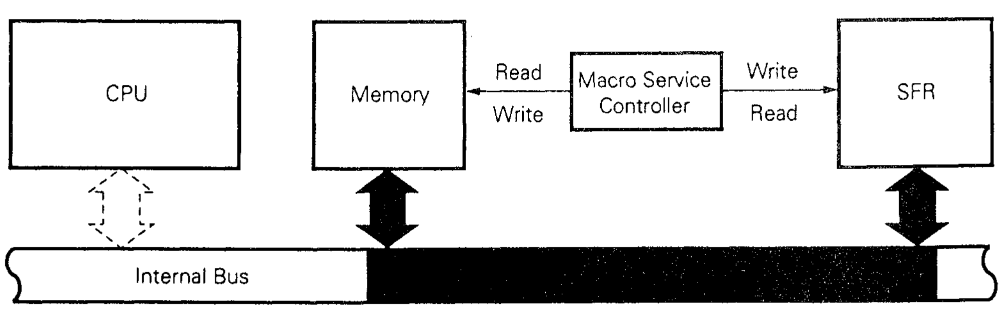
Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK	003EH	INTC21	001CH
NMI	0002H	INTP4	000EH
INTP0	0006H	INTC30	
INTP1	0008H	INTP5	0010H
INTP2	000AH	INTAD	
INTP3	000CH	INTC20	0012H
INTC00	0014H	INTSER	0020H
INTC01	0016H	INTSR	0022H
INTC10	0018H	INTST	0024H
INTC11	001AH	INTCSI	0026H

3.1.3 Macro Service

This is a function to transfer the data between the memory and special function registers (SFR) not through the CPU. The macro service controller accesses the memory and SFR, and transfers directly without fetching data.

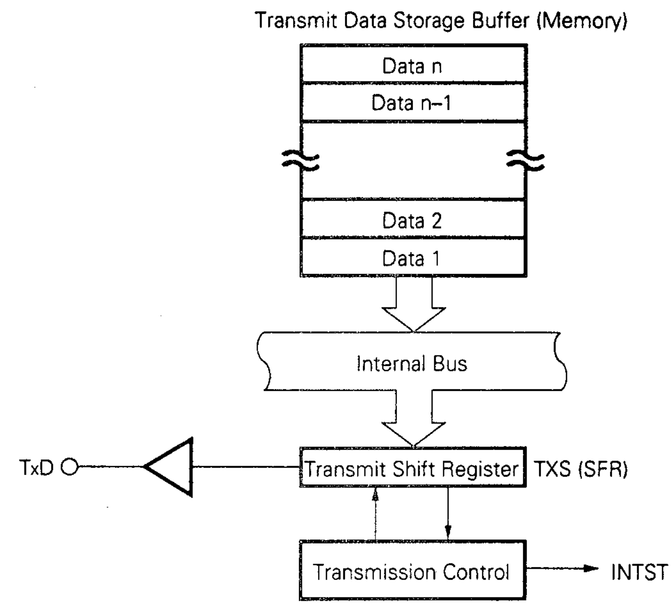
The high-speed data transfer is enabled because the CPU status is not saved/restored and no data is fetched.

Fig. 3-3 Macro Service



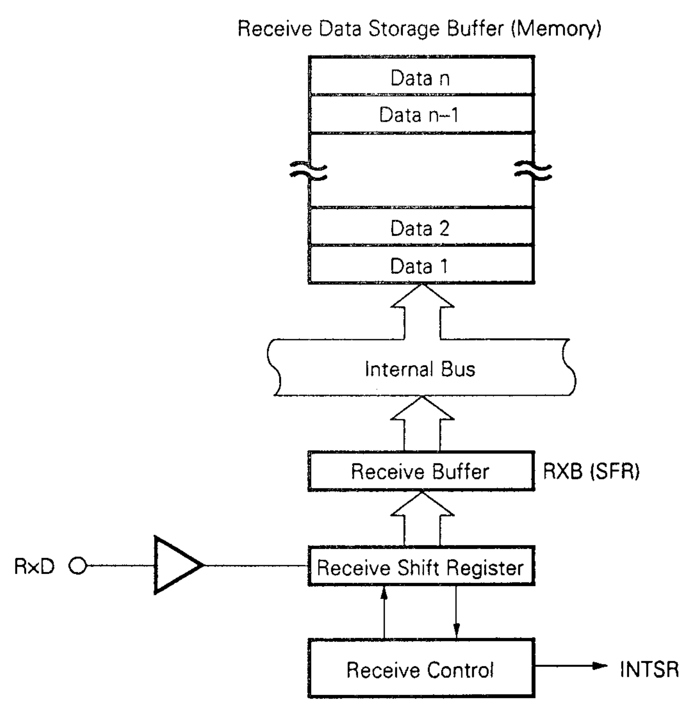
3.1.4 Macro Service Application Example

(1) Transmit operation of serial interface



Whenever the macro service request INTST is generated, the next send data is transferred to TXS from the memory. When the data n (last byte) is transferred to TXS (The send data storage buffer becomes empty.), a vectored interrupt request INTST is generated.

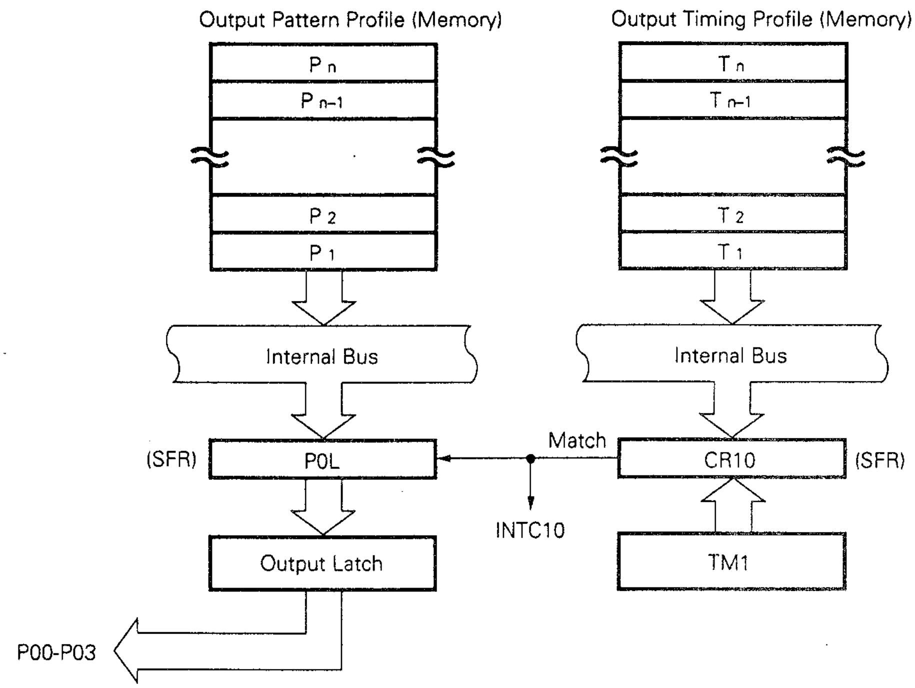
(2) Receive operation of serial interface



Whenever the macro service request INTSR is generated, the receive data is transferred to the memory from RXB. When the data n (last byte) is transferred to the memory (There will not be enough space in the receive data storage buffer.), the vectored interrupt request INTSR is generated.

(3) Real-time output port

The INTC10 and INTC11 become output triggers of the real-time output port. In the macro service to them, the next output pattern and interval can be set simultaneously. Therefore, the INTC10 and INTC11 can control 2-system stepping motor independently. Also, it can be applied to control a PWM or DC motor, etc.



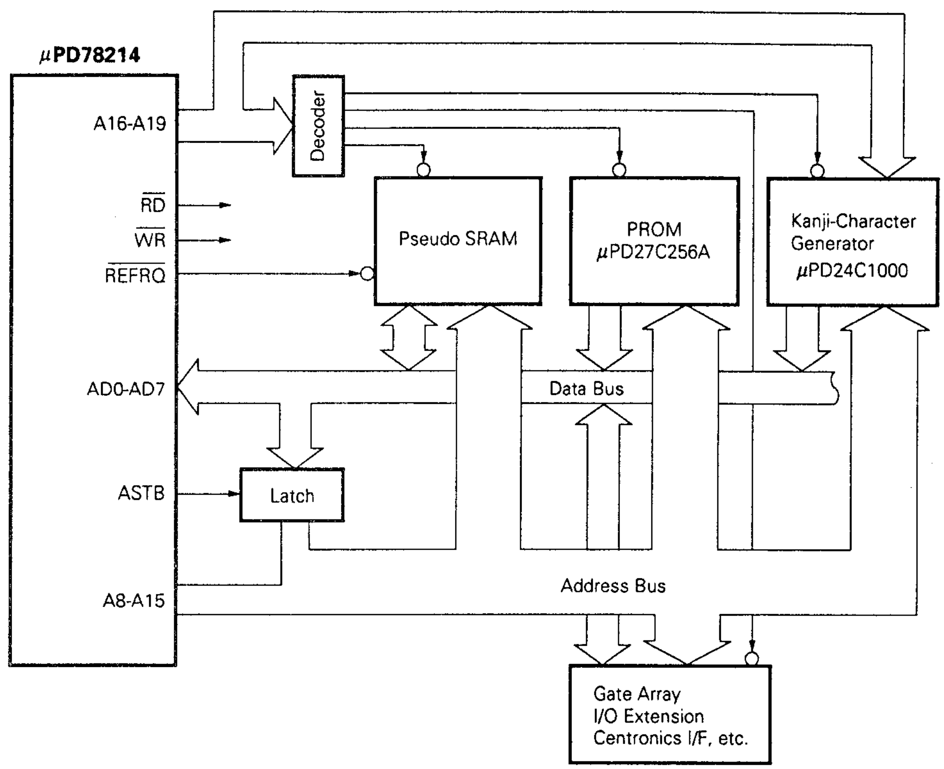
Whenever the macro service request INTC10 is generated, the pattern and timing are transferred to P0L and CR10 respectively. When the contents of the TM1 match with the contents of the CR10, the next INTC10 is generated and the contents of the P0L is sent to the output latch. If T_n (last byte) is sent to CR10, a vectored interrupt request INTC10 is generated.

The same operation is available for INTC11 (different point: CR10 → CR11, P0L → P0H, P00 to P03 → P04 to P07).

3.2 LOCAL BUS INTERFACE

The μPD78212, 78213 and 78214 can be connected a memory and an I/O (memory mapped I/O) externally and supports the 1M-byte memory space (see **Fig. 2-1** and **Fig. 2-2**).

Fig. 3-4 Local Bus Interface Example



3.2.1 Memory Expansion

The following modes have been prepared as a memory expansion function.

- External memory expansion mode:
  Expands the program memory and data memory to 48384 bytes (56704 bytes in case of the μPD78212) externally. But this area can be used unconditionally under the ROM-less mode ($\overline{EA}$ = L).
- 1M-byte expansion mode:
  Expands the data memory by 960K bytes and become a 1M-byte memory space.

3.2.2 Programmable Wait

A wait can be independently inserted to the memory mapped on both a normal address (00000H to 0FFFFH) and an extended address (10000H to FFFFFH). Therefore, the efficiency of the entire system is not decreased even if a memory with different access time is connected.

3.2.3 Pseudo-Static RAM Refresh Function

The refresh operations are as follows.

- Pulse refresh:
  Outputs the refresh pulse to $\overline{REFRQ}$ pin in synchronization with a bus cycle.
- Power-down self refresh:
  Outputs a low-level to the $\overline{REFRQ}$ pin in the standby mode and holds the contents of the pseudo-static RAM.

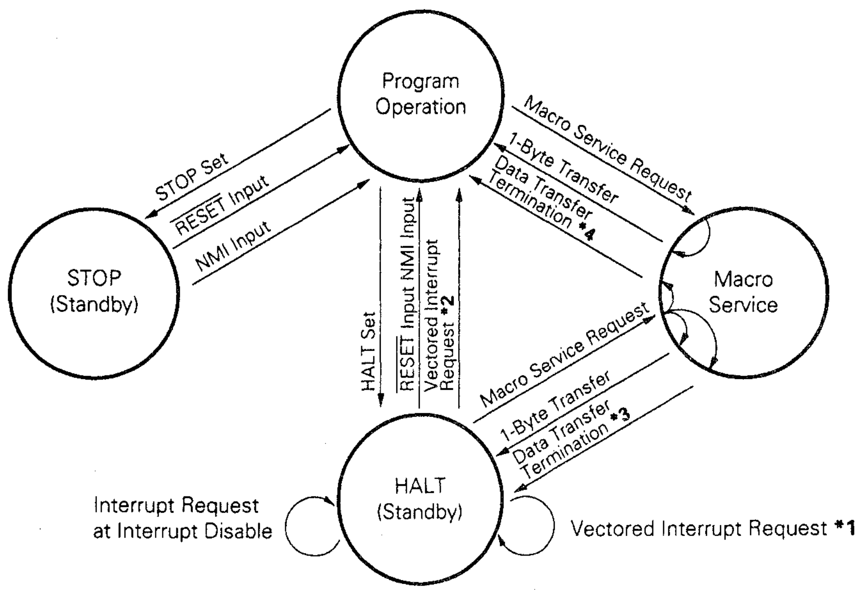
3.3 STANDBY

This is a function to reduce the power consumption of the chip. The following modes have been prepared.

- HALT mode: Stops the operation clock of the CPU. The average power consumption is reduced by the normal operation and the intermittent operation during normal operations.
- STOP mode: Stops the oscillator. This stops all operation in the chip and makes the minute power consumption status only with leakage current.

These modes are programmable.
Also, the macro service is started from the HALT mode.

Fig. 3-5 Standby Status Flow



* 1. In case a vectored interrupt request is a low priority level (status to disable interrupt of a low priority sequence under the HALT setting).
2. In case a vectored interrupt request is a high priority level or the status to enable interrupt of a low priority sequence under the HALT setting.
3. In case a macro service is a low priority level (status to disable interrupt of a low priority sequence under the HALT setting).
4. In case a macro service is a high priority level or the status to enable interrupt of a low priority sequence under the HALT setting.

3.4 RESET

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset state).

When the $\overline{\text{RESET}}$ input becomes from a low level to a high level, the following data is set in the program counter (PC).

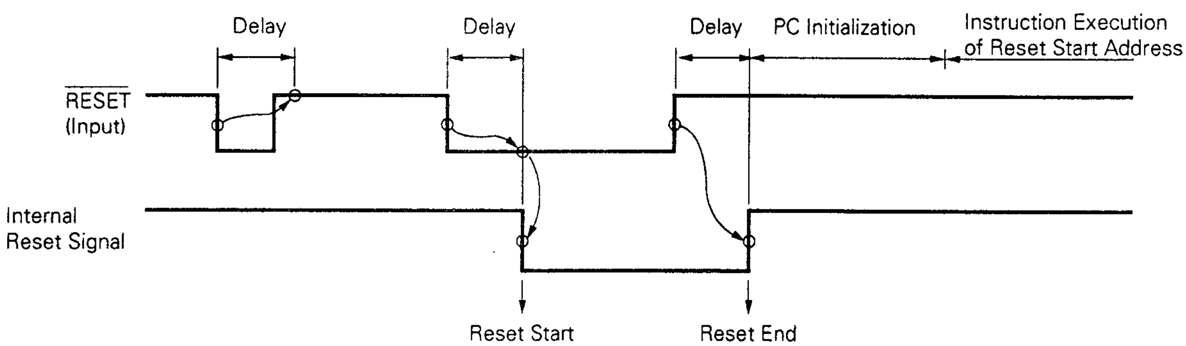
- Lower 8 bits of PC: Contents of 0000H address
- Upper 8 bits of PC: Contents of 0001H address

The contents of the PC set the destination address and the program starts to be executed from the address. Therefore, it can start from any address by reset start.

Please set the program for the contents of each register as required.

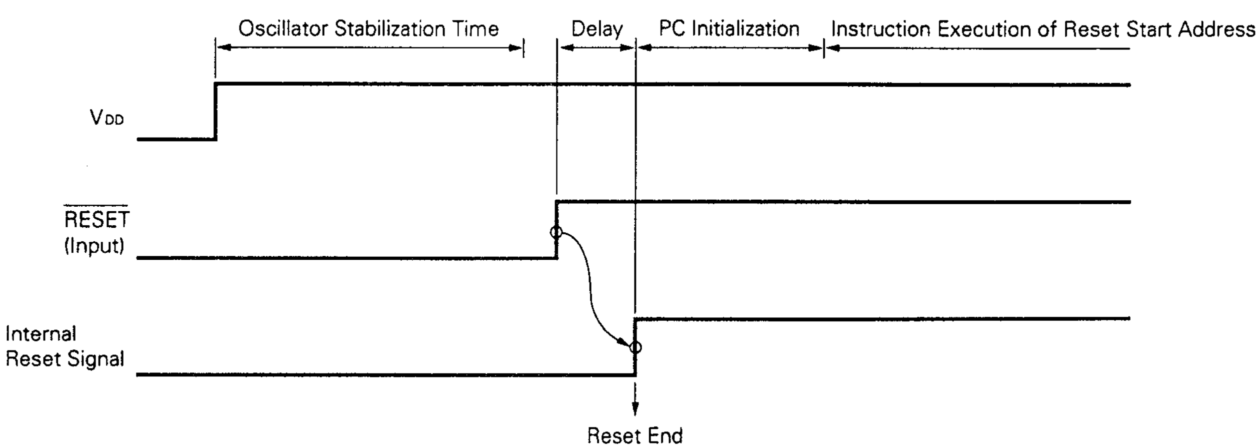
A noise eliminator has been incorporated in the $\overline{\text{RESET}}$ input circuit to prevent any error from noise. This noise eliminator circuit is a sampling circuit based on analog delay.

Fig. 3-6 Reset Acknowledge



Set the $\overline{\text{RESET}}$ signal active in the reset operation at power-on until oscillator stabilization time (approx. 40 ms) elapses.

Fig. 3-7 Reset Operation at Power-On



★ # 4. INSTRUCTION SET

(1) 8-Bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP

Table 4-1 8-Bit Instructions Classified by Addressing

2nd operand / 1st operand	# byte	A	r r'	saddr saddr'	sfr	mem	& mem	!addr16	&!addr16	PSW	n	None*2
A	ADD*1		MOV XCH	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV	MOV	MOV		
r	MOV		MOV XCH ADD*1								ROL ROLC ROR RORC SHR SHL	MULU DIVUW INC DEC
rl												DBNZ
saddr	MOV ADD*1	MOV		MOV XCH ADD*1								INC DBNZ DEC
sfr	MOV ADD*1	MOV										PUSH POP
mem & mem		MOV										
mem1 & mem1												ROR4 ROL4
!addr16		MOV										
&!addr16		MOV										
PSW	MOV	MOV										PUSH POP
STBC	MOV											

* 1. ADDC, SUB, SUBC, AND, OR, XOR and CMP are same as ADD.
2. There is no 2nd operand, or the 2nd operand is not an operand address.

(2) 16-Bit Instructions

MOVW, ADDW, SUBW, CMPW, INCW, DECW, SHRW, SHLW, PUSH, POP

Table 4-2 16-Bit Instructions Classified by Addressing

1st operand \ 2nd operand	# word	AX	rp rp'	saddrp	sfrp	mem1	& mem1	SP	n	None
AX	ADDW SUBW CMPW		ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW	MOVW	MOVW		
rp	MOVW		MOVW						SHLW SHRW	INCW DECW PUSH POP
saddrp	MOVW	MOVW								
sfrp	MOVW	MOVW								
mem1 & mem1		MOVW								
SP	MOVW	MOVW								INCW DECW

(3) Bit Instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 4-3 Bit Manipulation Instructions Classified by Addressing

1st operand \ 2nd operand	CY	A.bit	/A.bit	X.bit	/X.bit	saddr.bit	/saddr.bit	sfr.bit	/sfr.bit	PSW.bit	/PSW.bit	None*
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	SET1 CLR1 NOT1
A.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
X.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
saddr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
sfr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
PSW.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR

* There is no 2nd operand, or the 2nd operand is not an operand address.

(4) Call/Branch Instructions

CALL, CALLF, CALLT, BR, BC, BT, BF, BTCLR, DBNZ, BL, BNC, BNL, BZ, BE, BNZ, BNE

Table 4-4 Call/Branch Instructions Classified by Addressing

Operand of Instruction Address	$addr16	!addr16	rp	!addr11	[addr5]
Basic Instructions	BR BC*	CALL BR	CALL BR	CALLF	CALLT
Compound Instructions	BT BF BTCLR DBNZ				

* BL, BNC, BNL, BZ, BE, BNZ and BNE are same as BC.

(5) Other Instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, NOP, EI, DI, SEL

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{REF}		−0.5 to V_{DD} +0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input voltage	V_{I1}		−0.5 to V_{DD} +0.5	V
	V_{I2}	*	−0.5 to AV_{REF} +0.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Output current low	I_{OL}	1 pin	15	mA
		All output pins total	100	mA
Output current high	I_{OH}	1 pin	−10	mA
		All output pins total	−50	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

* Pins which are used as input pins of the A/D converter and which are selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not operated in P70/AN0 to P75/AN5, P66/$\overline{WAIT}$/AN6, P67/$\overline{REFRQ}$/AN7 pins. However, V_{I1} absolute maximum ratings should also be satisfied.

★ **Note** **Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are note exceeded.**

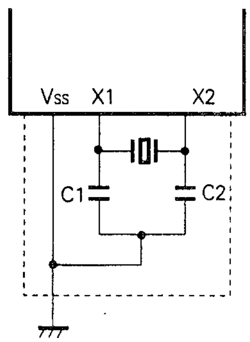
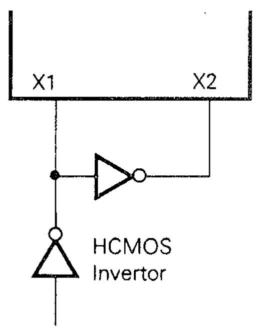
Operating Conditions

Clock Frequency	Operating Temperature (T_{opt})	Supply Voltage (V_{DD})
4 MHz f_{XX} 12 MHz	−40 to +85 °C	+5 V ± 10 %

Capacitance (Ta = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz unmeasured pins returned to 0 V.			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

Oscillator Characteristics (Ta = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	12	MHz
External clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Note **When using the clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.** ★

- **Wiring should be as short as possible.**
- **Wring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as Vss. Do not ground it to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

Recommended Oscillation Circuit Constants

Ceramic Resonator

Manufacturer	Frequency [MHz]	Product Name	Recommended Constants	
			C1 [pF]	C2 [pF]
Murata Mfg.	12	CSA12.0MT	30	30
		CST12.0MT*, CST12.0MTW	Capacitor on-chip type	
	4	CSA4.00MG040	100	100
		CST4.00MG040	Capacitor on-chip type	
Kyocera Corporation	12	KBR12.0M	33	33

* Production discontinued

Crystal Resonator

Manufacturer	Frequency [MHz]	Product Name	Recommended Constants	
			C1 [pF]	C2 [pF]
Kinseki	12	HC-49/U	18	18

DC Characteristics (Ta = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Pins except for *1 and *2	2.2		V_{DD}	V
	V_{IH2}	Pin of *1	2.2		AV_{REF}	V
	V_{IH3}	Pin of *2	$0.8V_{DD}$		V_{DD}	V
Output voltage low	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA *3			1.0	V
Output voltage high	V_{OH1}	I_{OH} = −1.0 mA	V_{DD}−1.0			V
	V_{OH2}	I_{OH} = −100 μA	V_{DD}−0.5			V
	V_{OH3}	I_{OH} = −5.0 mA *4	2.0			V
X1 input current low	I_{IL}	$0 V \leq V_I \leq V_{IL}$			−100	μA
X1 input current high	I_{IH}	$V_{IH3} \leq V_I \leq V_{DD}$			100	μA
Input leakage current	I_{LI}	$0 V \leq V_I \leq V_{DD}$			±10	μA
Output leakage current	I_{LO}	$0 V \leq V_O \leq V_{DD}$			±10	μA
AV_{REF} current	AI_{REF}	Operating mode f_{XX} = 12 MHz		1.5	5.0	mA
V_{DD} supply current	I_{DD1}	Operating mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT mode f_{XX} = 12 MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode V_{DDDR} = 2.5 V		2	20	μA
		STOP mode V_{DDDR} = 5 V ±10 %		5	50	μA
Pull-up resistor	R_L	V_I = 0 V	15	40	80	kΩ

* 1. Pins which are used as input pins of the A/D converter and which are selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not operated in P70/AN0 to P75/AN5, P66/$\overline{\text{WAIT}}$/AN6, P67/$\overline{\text{REFRQ}}$/AN7 pins.
2. X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, $\overline{\text{EA}}$ pins
3. P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins
4. P00 to P07 pins

AC Characteristics (Ta = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Read/Write Operation (1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
X1 input clock cycle time	t_{CYX}		82	250	ns
Address set-up time (to ASTB↓)	t_{SAST}*		52		ns
Address hold time (from ASTB↓)•	t_{HSTA}		25		ns
Address hold time (from $\overline{\text{RD}}$↑)	t_{HRA}		30		ns
Address hold time (from $\overline{\text{WR}}$↑)	t_{HWA}		30		ns
$\overline{\text{RD}}$↓ delay time from address	t_{DAR}*		129		ns
Address float time (from $\overline{\text{RD}}$↓)	t_{FAR}*		11		ns
Data input time from address	t_{DAID}*	No. of waits = 0		228	ns
Data input time from ASTB↓	t_{DSTID}*	No. of waits = 0		181	ns
Data input time from $\overline{\text{RD}}$↓	t_{DRID}*	No. of waits = 0		100	ns
$\overline{\text{RD}}$↓ delay time from ASTB↓	t_{DSTR}*		52		ns
Data hold time (from $\overline{\text{RD}}$↑)	t_{HRID}		0		ns
Address active time from $\overline{\text{RD}}$↑	t_{DRA}*		124		ns
ASTB↑ delay time from $\overline{\text{RD}}$↑	t_{DRST}*		124		ns
$\overline{\text{RD}}$ low-level width	t_{WRL}*	No. of waits = 0	124		ns
ASTB high-level width	t_{WSTH}*		52		ns
$\overline{\text{WR}}$↓ delay time from address	t_{DAW}*		129		ns
Data output time from ASTB↓	t_{DSTOD}*			142	ns
Data output time from $\overline{\text{WR}}$↓	t_{DWOD}			60	ns
$\overline{\text{WR}}$↓ delay time from ASTB↓ ★	t_{DSTW1}*	With refreshing disabled	52		ns
	t_{DSTW2}*	With refreshing enabled	129		ns
Data set-up time (to $\overline{\text{WR}}$↑)	t_{SODWR}*	No. of waits = 0	146		ns
Data set-up time (to $\overline{\text{WR}}$↓)	t_{SODWF}*	In refresh mode	22		ns
Data hold time (from $\overline{\text{WR}}$↑)•	t_{HWOD}		20		ns
ASTB↑ delay time from $\overline{\text{WR}}$↑	t_{DWST}*		42		ns
$\overline{\text{WR}}$ low-level width ★	t_{WWL1}*	With refreshing disabled No. of waits = 0	196		ns ns
	t_{WWL2}*	With refreshing enabled No. of waits = 0	144		ns
$\overline{\text{WAIT}}$↓ input time from address	t_{DAWT}*			146	ns
$\overline{\text{WAIT}}$↓ input time from ASTB↓	t_{DSTWT}*			84	ns

• The hold time includes the time to hold the V_{OH} and V_{OL} under the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks **1.** The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

2. For a parameter with an asterisk in the SYMBOL column, refer to "**t_{CYX} Dependent Bus Timing Definition**" as well.

Read/Write Operation (2/2)

Parameter		Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ hold time from ASTB↓		t_{HSTWT}*	No. of external waits = 1	174		ns
$\overline{\text{WAIT}}$↑ delay time from ASTB↓		t_{DSTWTH}*	No. of external waits = 1		273	ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓		t_{DRWTL}*			22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}$↓		t_{HRWT}*	No. of external waits = 1	87		ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{RD}}$↓		t_{DRWTH}*	No. of external waits = 1		186	ns
Data input time from $\overline{\text{WAIT}}$↑		t_{DWTID}*			62	ns
$\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTW}*		154		ns
$\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTR}*		72		ns
$\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}$↓ (At refresh disabled)		t_{DWWTL}*			22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}$↓	Refresh disabled	t_{HWWT1}*	No. of external waits = 1	87		ns
	Refresh enabled	t_{HWWT2}*	No. of external waits = 1	5		ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{WR}}$↓	Refresh disabled	t_{DWWTH1}*	No. of external waits = 1		186	ns
	Refresh enabled	t_{DWWTH2}*	No. of external waits = 1		104	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{RD}}$↑		t_{DRRFQ}*		154		ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{WR}}$↑		t_{DWRFQ}*		72		ns
$\overline{\text{REFRQ}}$ low-level width		t_{WRFQL}*		120		ns
ASTB↑ delay time from $\overline{\text{REFRQ}}$↑		t_{DRFQST}*		280		ns

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

2. For a parameter with an asterisk in the SYMBOL column, refer to "**t_{CYX} Dependent Bus Timing Definition**" as well.

SERIAL OPERATION

Parameter	Symbol	Test Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal divided by 16	1.3		μs
			Internal divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
SI, SB0 set-up time (to $\overline{SCK}\uparrow$)	t_{SSSK}			150		ns
SI, SB0 hold time (from $\overline{SCK}\uparrow$)	t_{HSSK}			400		ns
SO/SB0 output delay time (from $\overline{SCK}\downarrow$)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 k		0	800	ns
SB0 high hold time (from $\overline{SCK}\uparrow$)	t_{HSBSK}	SBI mode		4		t_{CYX}
SB0 low set-up time (to $\overline{SCK}\downarrow$)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remarks The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

Other operations

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 to INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0 to INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low-level width	t_{WRSL}		10		μs
$\overline{RESET}$ high-level width	t_{WRSH}		10		μs

External Clock Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D Converter (T_a = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Overall error *		4.0 V AV_{REF} V_{DD} Ta = –10 to +70°C			0.4	%
		3.4 V AV_{REF} V_{DD} Ta = –10 to +70°C			0.8	%
		4.0 V AV_{REF} V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	82 ns t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	360			t_{CYX}
		125 ns t_{CYX} 250 ns (The FR bit of ADM is to be "1")	240			t_{CYX}
Sampling time	t_{SAMP}	82 ns t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	72			t_{CYX}
		125 ns t_{CYX} 250 ns (The FR bit of ADM is to be "1")	48			t_{CYX}
Analog input voltage	V_{IAN}		–0.3		AV_{REF} +0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} current	AI_{REF}	f_{XX} = 12 MHz		1.5	5.0	mA
		STOP mode		0.2	1.5	mA

* Quantization error is not included. Represented by the ratio to full-scale value.

t_{CYX} Dependent Bus Timing Definition (1/2)

Parameter	Symbol	Expressions	MIN./MAX.	12 MHz	Unit	
X1 input clock cycle time	t_{CYX}		MIN.	82	ns	
Address set-up time (to ASTB↓)	t_{SAST}	t_{CYX} – 30	MIN.	52	ns	
$\overline{\text{RD}}$↓ delay time from address	t_{DAR}	2t_{CYX} – 35	MIN.	129	ns	
Address float time (from $\overline{\text{RD}}$↓)	t_{FAR}	t_{CYX}/2 – 30	MIN.	11	ns	
Data input time from address	t_{DAID}	(4 + 2n) t_{CYX} – 100	MAX.	228 *	ns	
Data input time from ASTB↓	t_{DSTID}	(3 + 2n) t_{CYX} – 65	MAX.	181 *	ns	
Data input time from $\overline{\text{RD}}$↓	t_{DRID}	(2 + 2n) t_{CYX} – 64	MAX.	100 *	ns	
$\overline{\text{RD}}$↓ delay time from ASTB↓	t_{DSTR}	t_{CYX} – 30	MIN.	52	ns	
Address active time from $\overline{\text{RD}}$↑	t_{DRA}	2t_{CYX} – 40	MIN.	124	ns	
ASTB↑ delay time from $\overline{\text{RD}}$↑	t_{DRST}	2t_{CYX} – 40	MIN.	124	ns	
$\overline{\text{RD}}$ low-level width	t_{WRL}	(2 + 2n) t_{CYX} – 40	MIN.	124 *	ns	
ASTB high-level width	t_{WSTH}	t_{CYX} – 30	MIN.	52	ns	
$\overline{\text{WR}}$↓ delay time from address	t_{DAW}	2t_{CYX} – 35	MIN.	129	ns	
Data output time from ASTB↓	t_{DSTOD}	t_{CYX} + 60	MAX.	142	ns	
$\overline{\text{WR}}$↓ delay time from ASTB↓	t_{DSTW1}	t_{CYX} – 30 (With refreshing disabled)	MIN.	52	ns	★
	t_{DSTW2}	2t_{CYX} – 35 (With refreshing enabled)	MIN.	129	ns	
Data set-up time (to $\overline{\text{WR}}$↑)	t_{SODWR}	(3 + 2n) t_{CYX} – 100	MIN.	146 *	ns	
Data set-up time (to $\overline{\text{WR}}$↓)	t_{SODWF}	t_{CYX} – 60 (With refreshing enabled)	MIN.	22	ns	
ASTB↑ delay time from $\overline{\text{WR}}$↑	t_{DWST}	t_{CYX} – 40	MIN.	42	ns	
$\overline{\text{WR}}$ low-level width	t_{WWL1}	(3 + 2n) t_{CYX} – 50 (With refreshing disabled)	MIN.	196 *	ns	★
	t_{WWL2}	(3 + 2n) t_{CYX} – 50 (With refreshing enabled)	MIN.	114 *	ns	
$\overline{\text{WAIT}}$↓ input time from address	t_{DAWT}	3t_{CYX} – 100	MAX.	146	ns	
$\overline{\text{WAIT}}$↓ input time from ASTB↓	t_{DSTWT}	2t_{CYX} – 80	MAX.	84	ns	

Remarks "n" indicates the number of waits.

* When n = 0

t_{CYX} Dependent Bus Timing Definition (2/2)

Parameter		Symbol	Expressions	MIN./MAX.	12 MHz	Unit
$\overline{\text{WAIT}}$ hold time from ASTB↓		t_{HSTWT}	2Xt_{CYX} + 10	MIN.	174*	ns
$\overline{\text{WAIT}}$↑ delay time from ASTB↓		t_{DSTWTH}	2(1 + X)t_{CYX} – 55	MAX.	273*	ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓		t_{DRWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}$↓		t_{HRWT}	(2X – 1)t_{CYX} + 5	MIN.	87*	ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{RD}}$↓		t_{DRWTH}	(2X + 1)t_{CYX} – 60	MAX.	186*	ns
Data input time from $\overline{\text{WAIT}}$↑		t_{DWTID}	t_{CYX} – 20	MAX.	62	ns
$\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTW}	2t_{CYX} – 10	MIN.	154	ns
$\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTR}	t_{CYX} – 10	MIN.	72	ns
$\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}$↓ (At refresh disabled)		t_{DWWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}$↓	Refresh disabled	t_{HWWT1}	(2X – 1)t_{CYX} + 5	MIN.	87*	ns
	Refresh enabled	t_{HWWT2}	2(X – 1)t_{CYX} + 5	MIN.	5*	ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{WR}}$↓	Refresh disabled	t_{DWWTH1}	(2X + 1)t_{CYX} – 60	MAX.	186*	ns
	Refresh enabled	t_{DWWTH2}	2Xt_{CYX} – 60	MAX.	104*	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{RD}}$↑		t_{DRRFQ}	2t_{CYX} – 10	MIN.	154	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{WR}}$↑		t_{DWRFQ}	t_{CYX} – 10	MIN.	72	ns
$\overline{\text{REFRQ}}$ low-level width		t_{WRFQL}	2t_{CYX} – 44	MIN.	120	ns
ASTB↑ delay time from $\overline{\text{REFRQ}}$↑		t_{DRFQST}	4t_{CYX} – 48	MIN.	280	ns

Remarks
1. X: The number of the external wait. (1, 2, ...)
2. $t_{CYX} \cong$ 82 ns (f_{XX} = 12 MHz)
3. "n" indicates the number of waits.

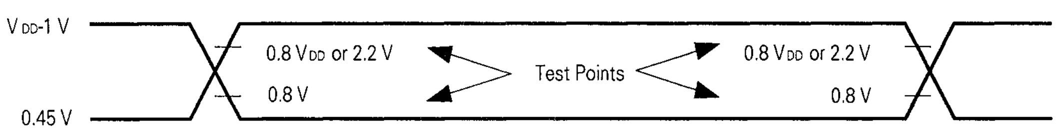
* When X = 1

Data Retention Characteristics (Ta = −40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode2.5	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V	2	2	20	μA
		V_{DDDR} = 5 V ±10 %		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pin*	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

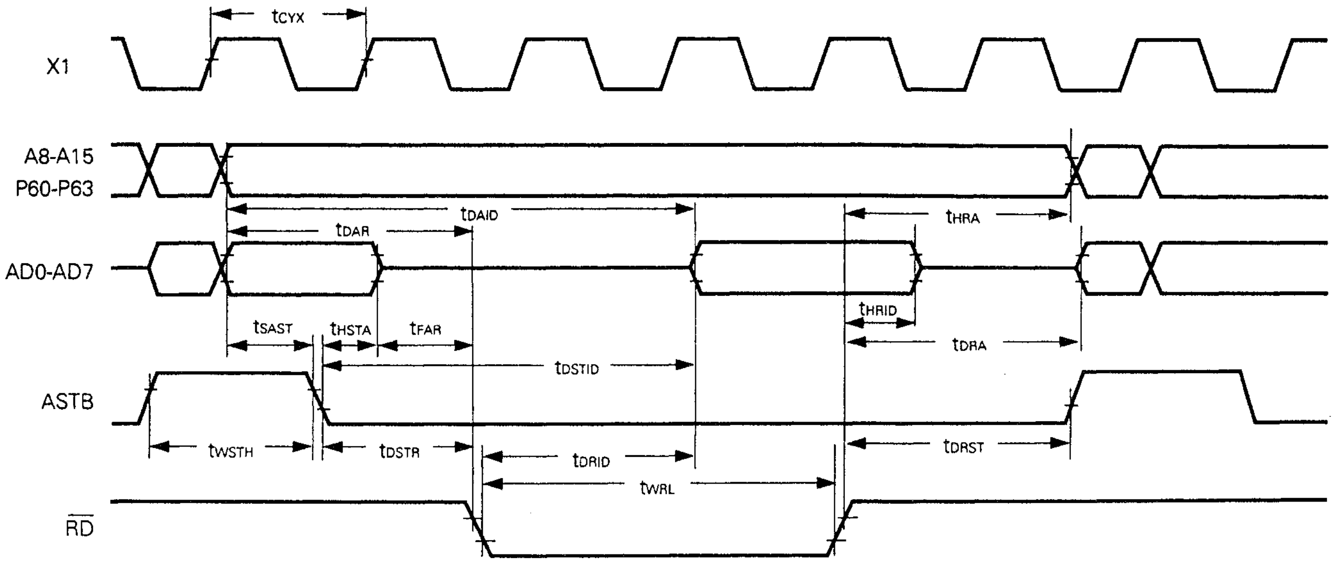
* $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0 and $\overline{\text{EA}}$ pins

AC Timing Test Point

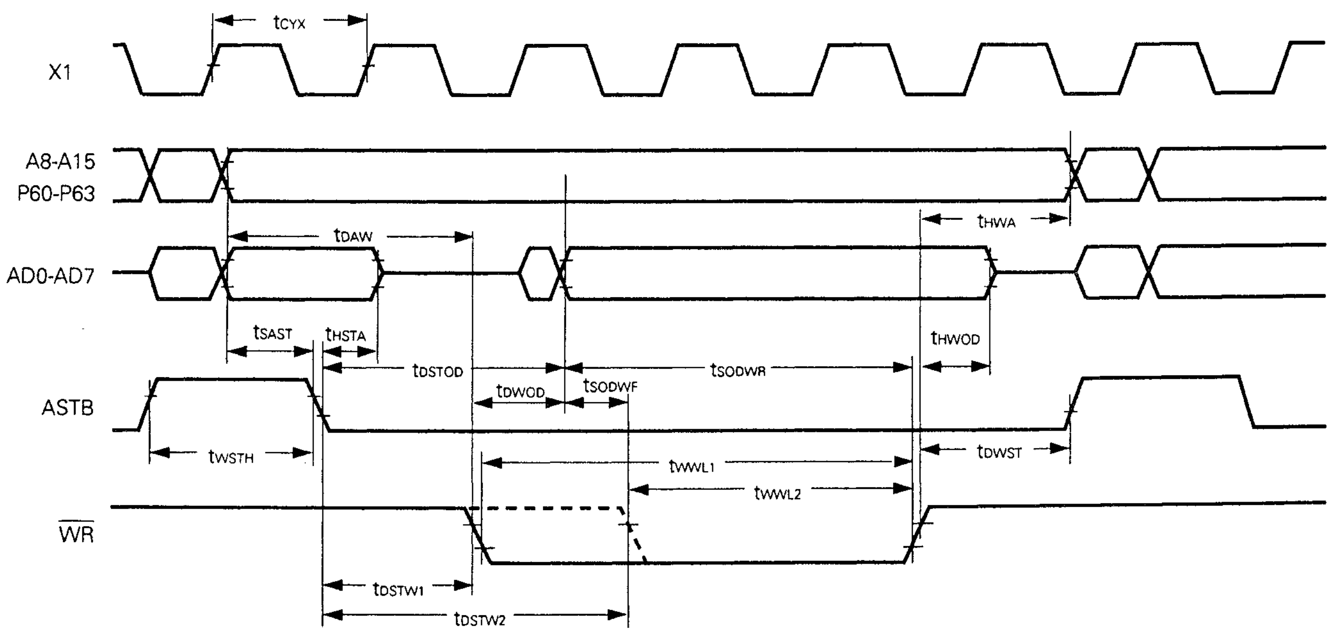


Timing Waveform

Read operation

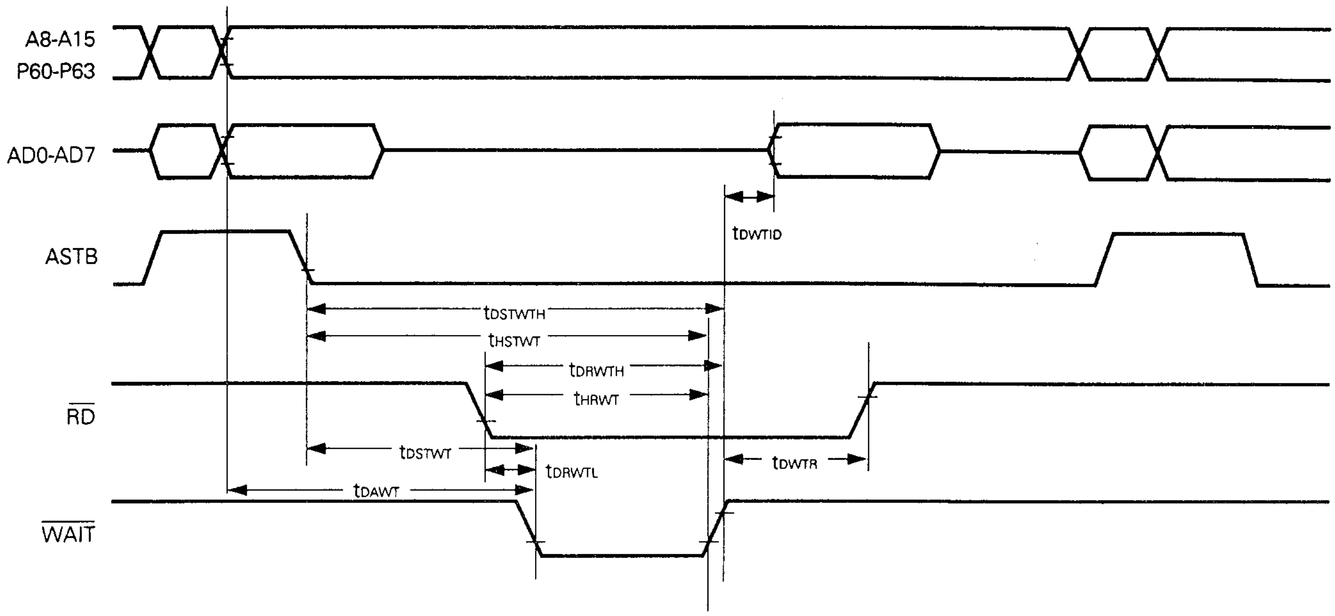


Write operation

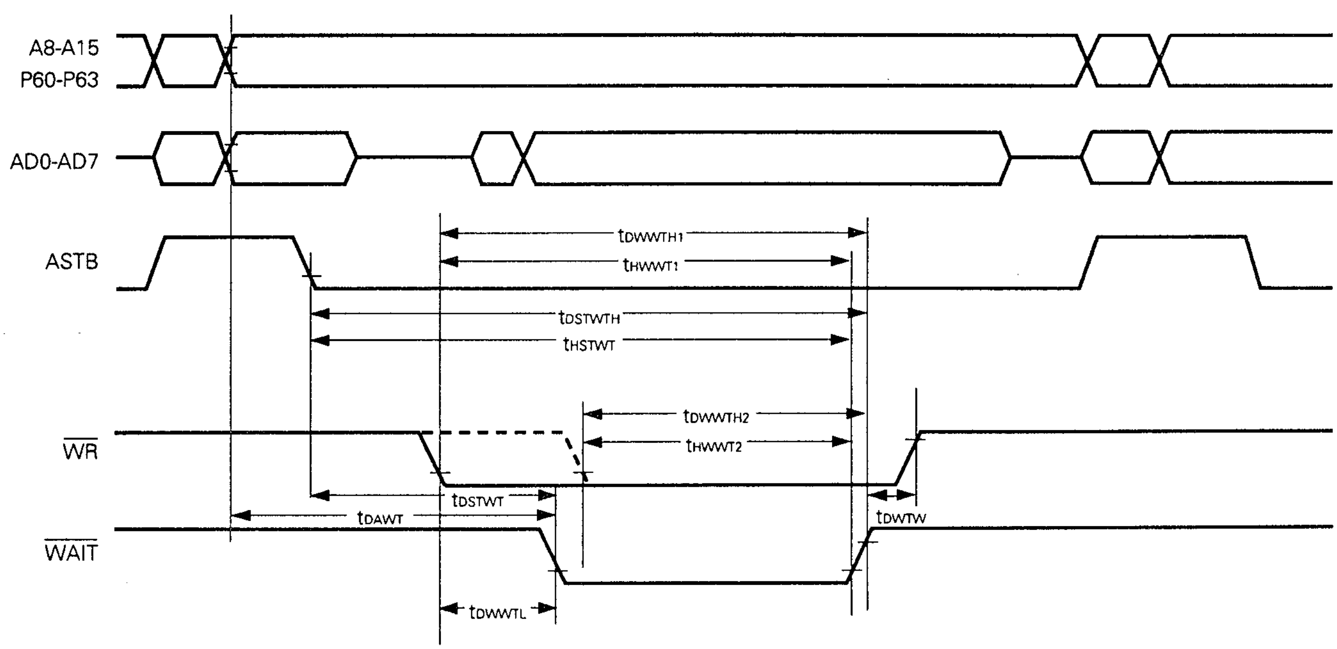


External WAIT Signal Input Timing

Read operation

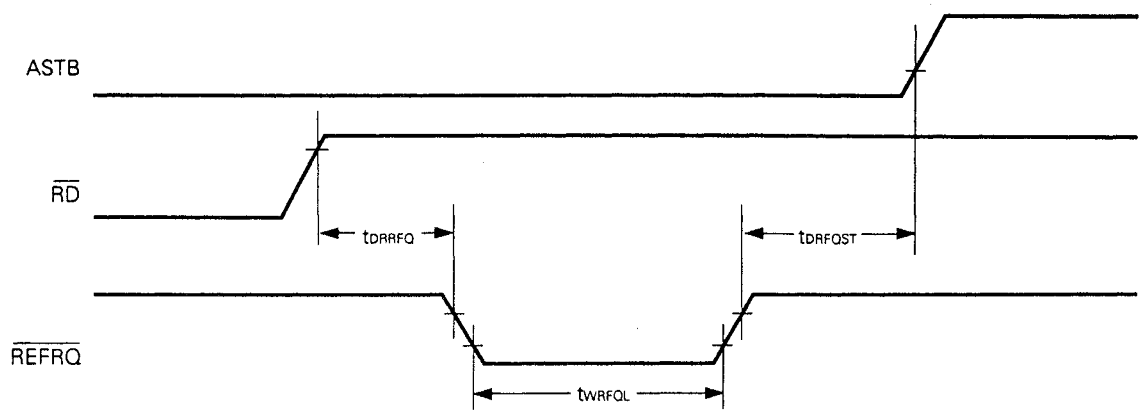


Write operation

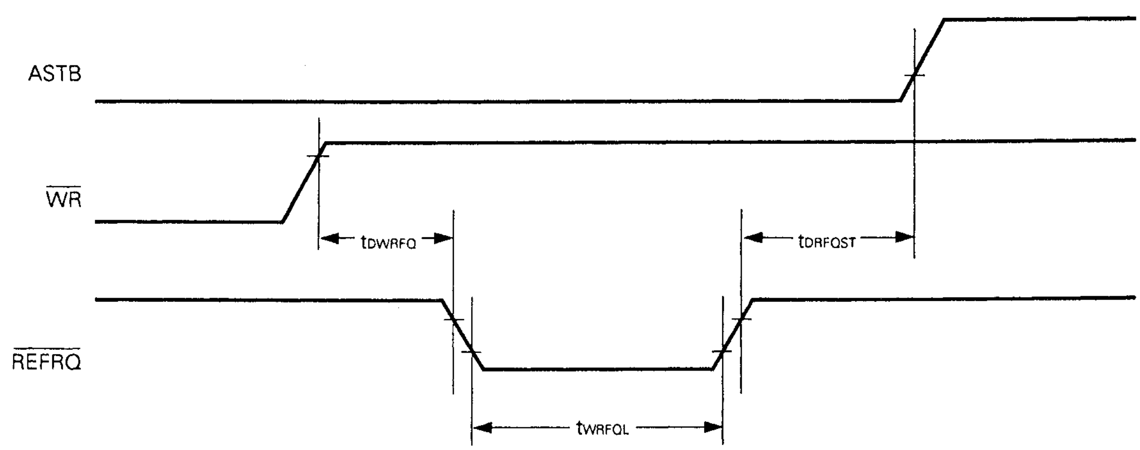


Refresh Timing Waveform

Refresh after read

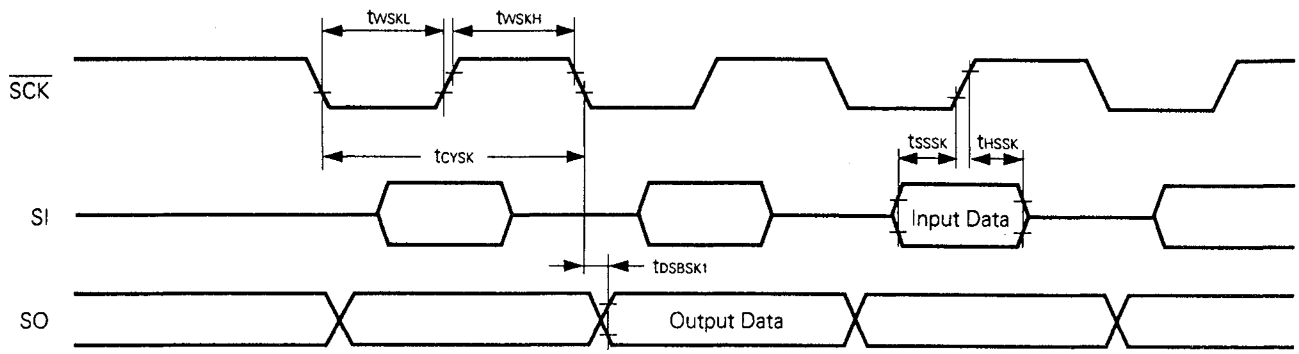


Refresh after write



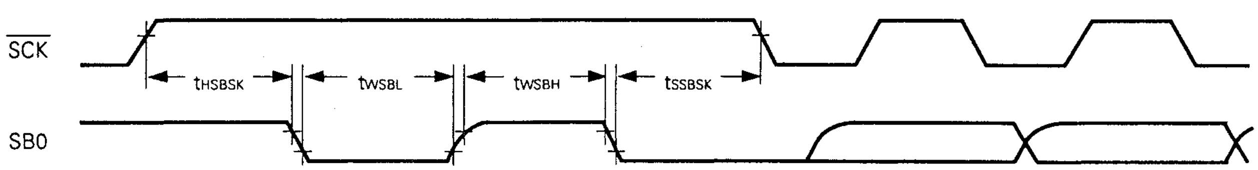
Serial Operation

3-wire serial I/O mode

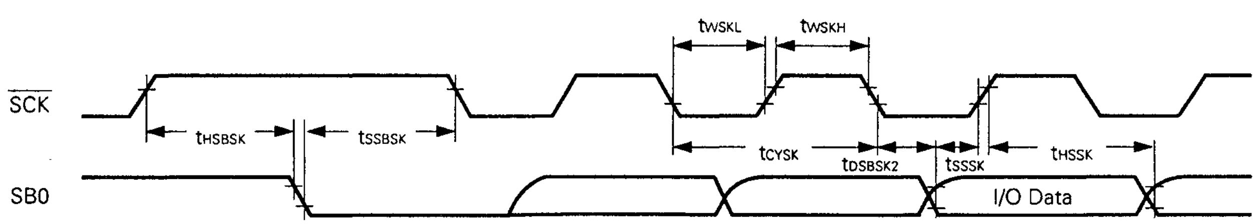


SBI Mode

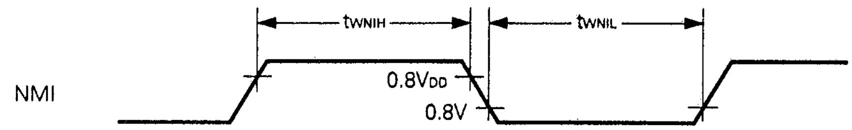
Bus release signal transfer

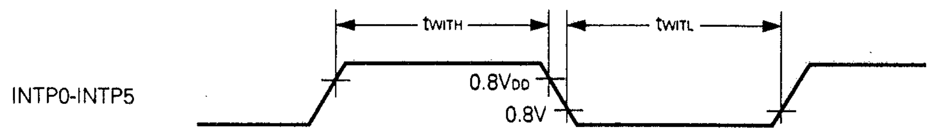


Command signal transfer

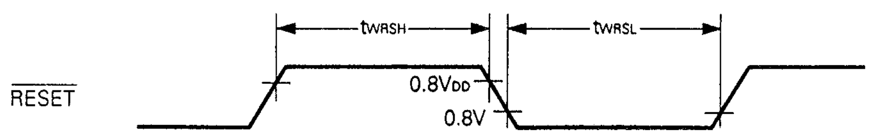


Interrupt Input Timing

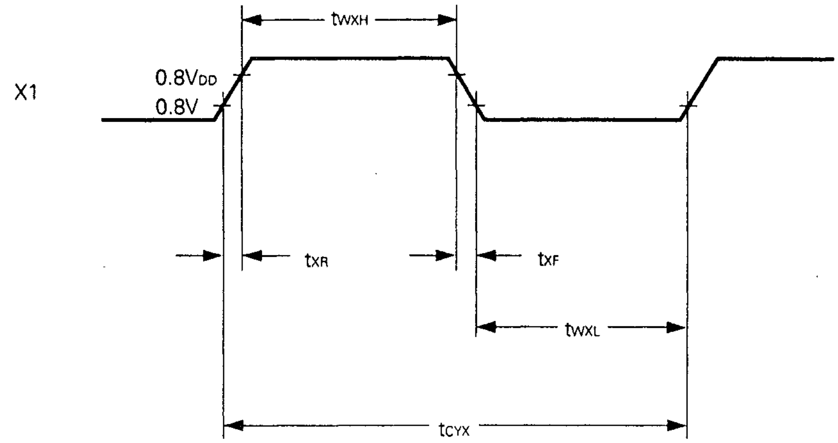




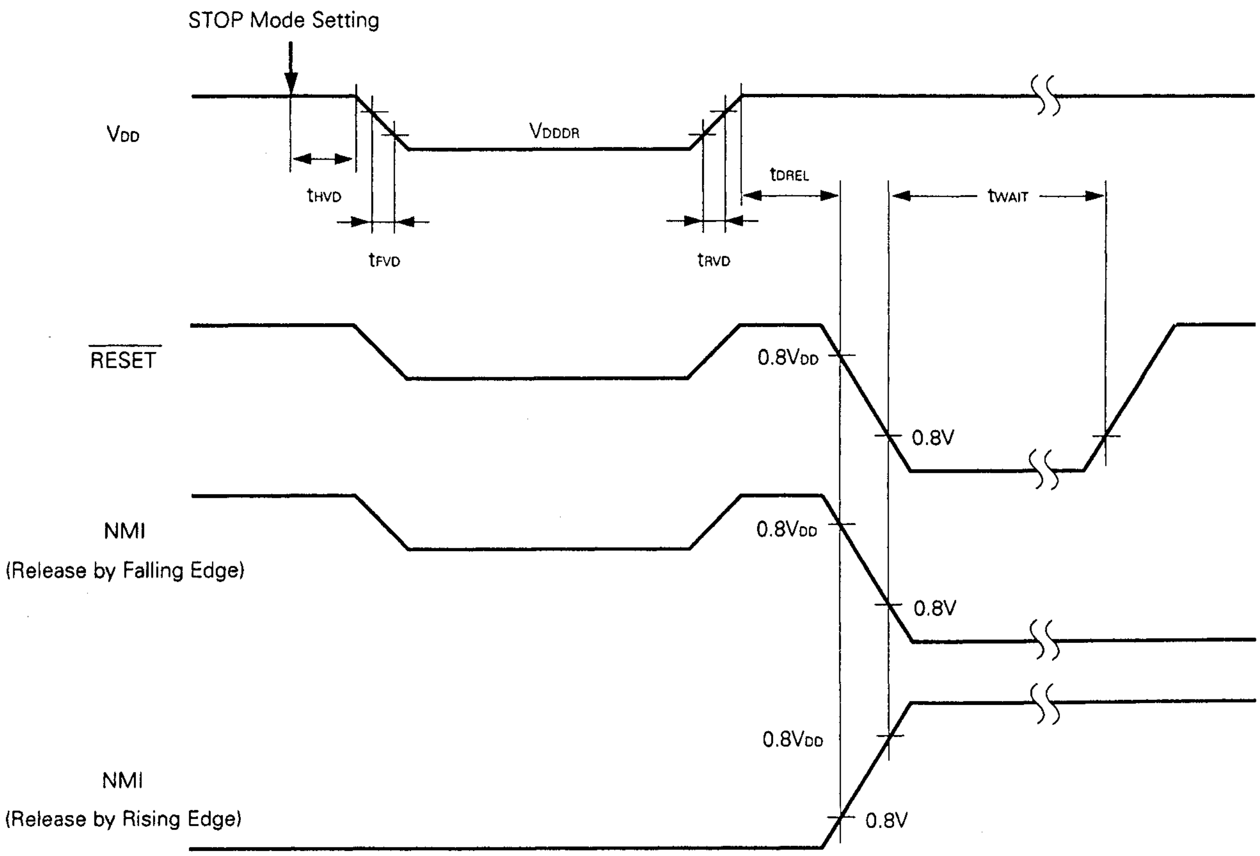
Reset Input Timing



External Clock Timing

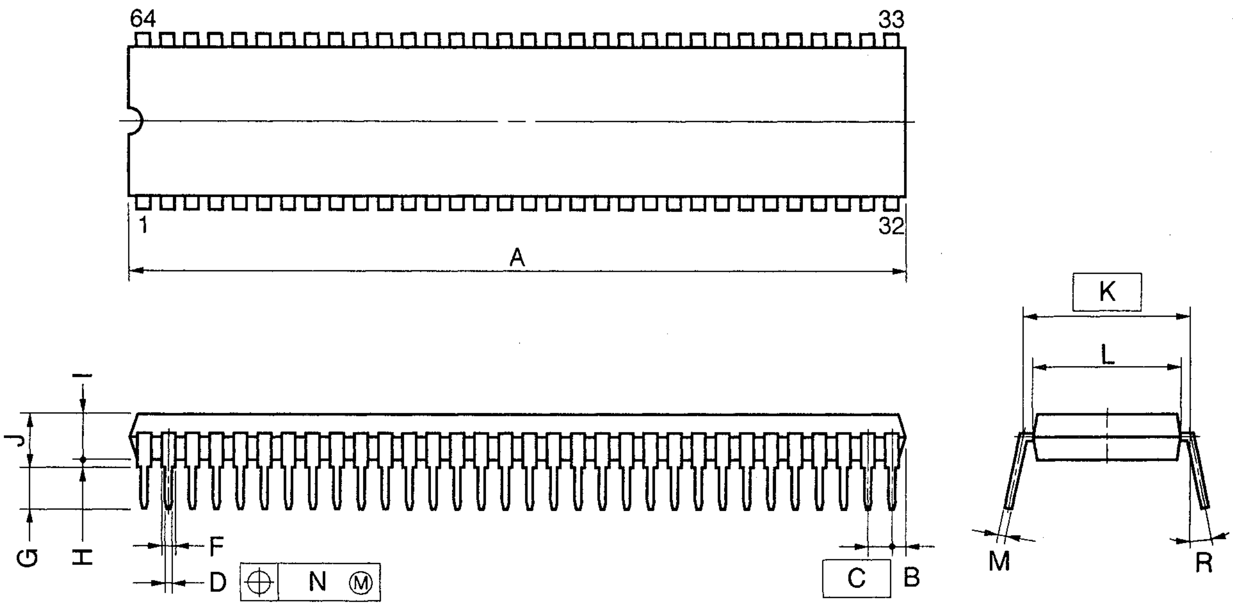


Data Retention Characteristics



6. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



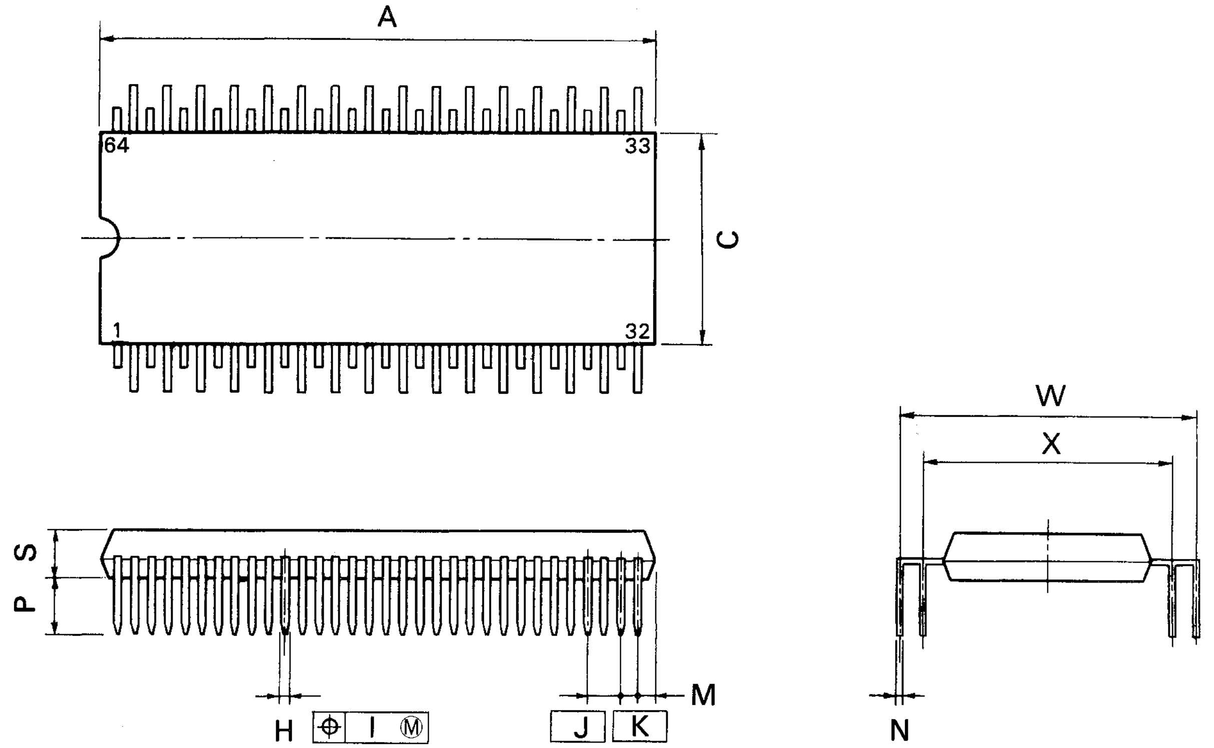
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QUIP



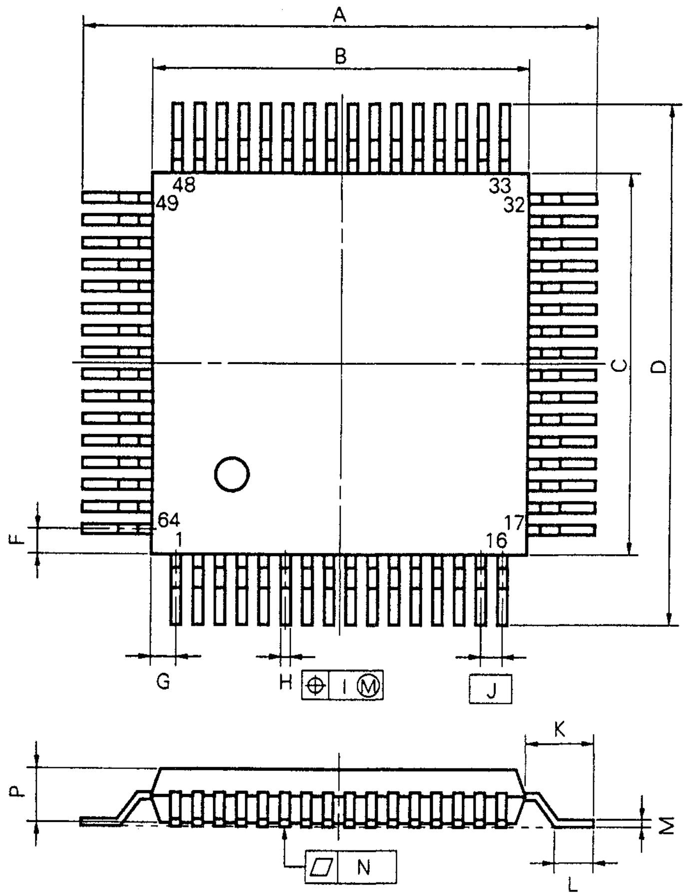
P64GQ-100-36

NOTE

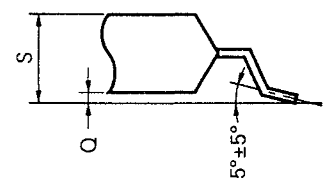
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

64 PIN PLASTIC QFP (□14)



detail of lead end



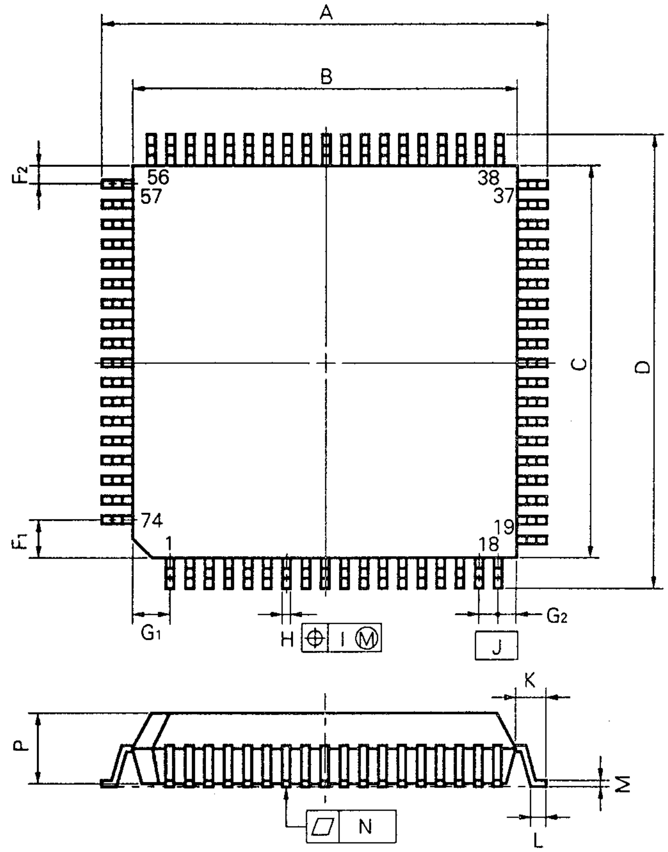
P64GC-80-AB8-3

NOTE

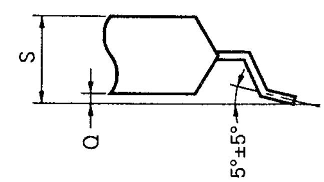
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

74 PIN PLASTIC QFP (□20)



detail of lead end



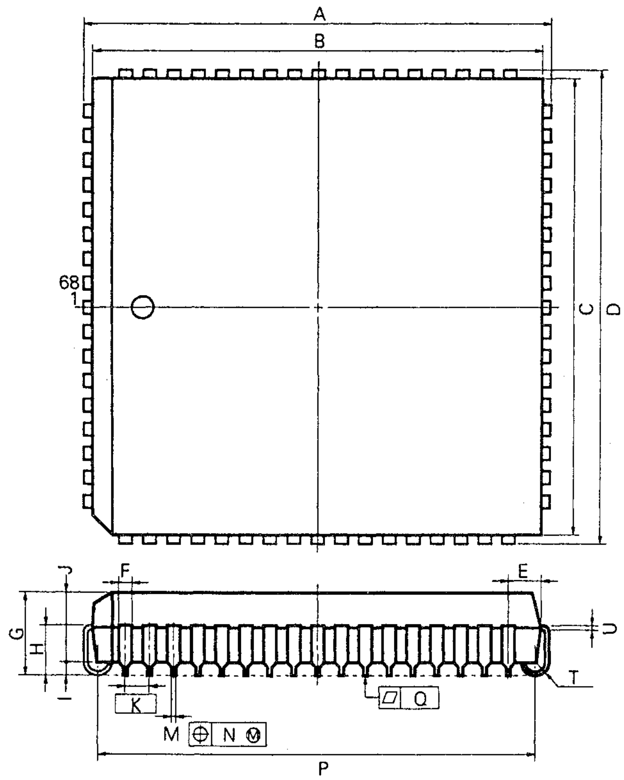
S74GJ-100-5BJ-2

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	2.0	0.079
F_2	1.0	0.039
G_1	2.0	0.079
G_2	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

68 PIN PLASTIC QFJ (□950 mil)



P68L-50A1-2

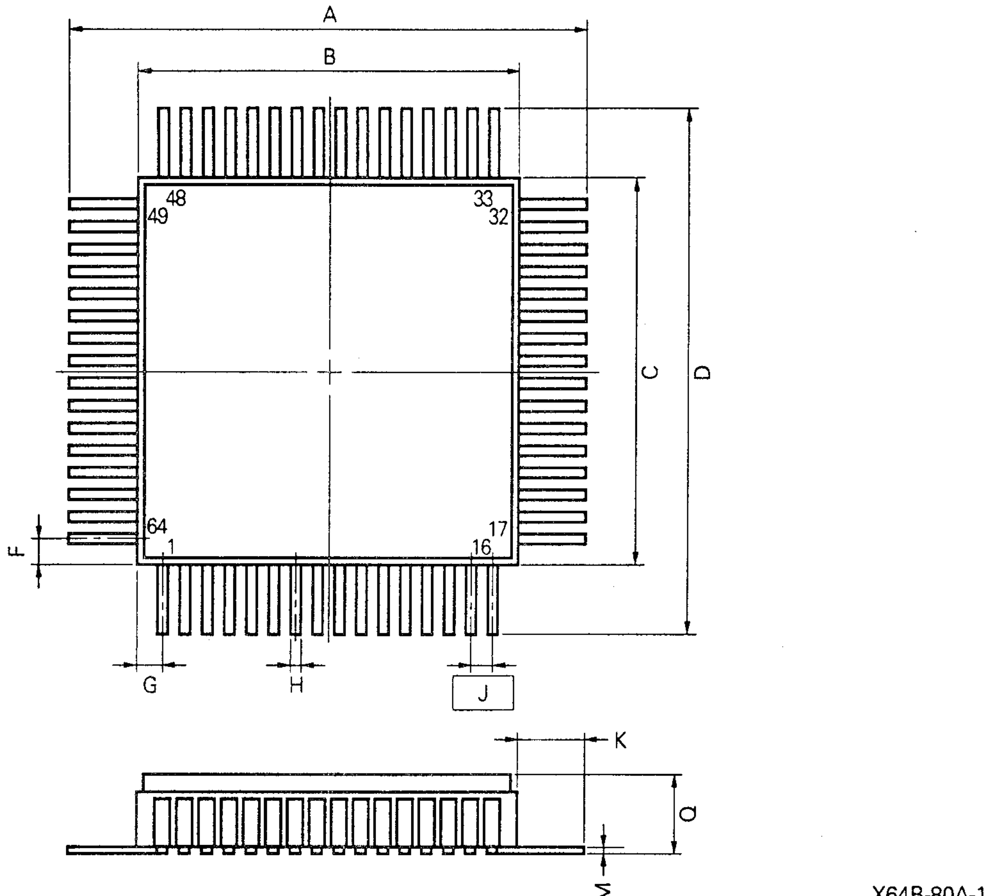
NOTE

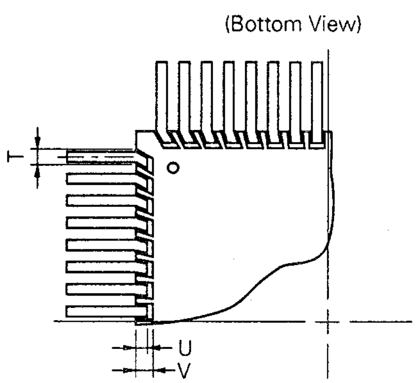
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

μPD78212GC-xxx-AB8, 78214GC-xxx-AB8

64 PIN CERAMIC QFP (14 × 14) (FOR ES)





ITEM	MILLIMETERS	INCHES
A	22.0±0.4	0.866±0.016
B	14.0	0.551
C	14.0	0.551
D	22.0±0.4	0.866±0.016
F	1.0	0.039
G	1.0	0.039
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	4.0±0.15	$0.157^{+0.007}_{-0.006}$
M	0.25	0.01
Q	3.0 MAX.	0.119 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

7. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document "Surface Mount Technology Manual" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 7-1 Surface Mounting Type Soldering Conditions

(1) μPD78212GC-xxx-AB8 : **64-pin plastic QFP (14 × 14 mm)**
μPD78213GC-AB8 : **64-pin plastic QFP (14 × 14 mm)**
μPD78214GC-xxx-AB8 : **64-pin plastic QFP (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C or above) Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	VP15-162-1
Wave Soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max. Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C) Preliminary heating temperature: 120°C max. (package surface temperature)	WS60-162-1
Pin part heating	Pin part temperature: 300°C max., Duration: 3 sec. max. (per lead side)	——

(2) μPD78212GJ-xxx-5BJ : **74-pin plastic QFP (20 × 20 mm)**
μPD78213GJ-5BJ : **74-pin plastic QFP (20 × 20 mm)**
μPD78214GJ-xxx-5BJ : **74-pin plastic QFP (20 × 20 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C or above) Number of times: Once	IR30-00-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Once	VP15-00-1
Pin part heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per lead side)	——

(3) μPD78213L : **68-pin plastic QFJ (□950 mil)**
μPD78214L-xxx : **68-pin plastic QFJ (□950 mil)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	VP15-162-1
Pin part heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per lead side)	——

* For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 7-2 Insert Type Soldering Conditions

μPD78212CW-xxx, 78213CW, 78214CW-xxx : 64-pin plastic shrink DIP
μPD78213GQ-36, 78214GQ-xxx-36 : 64-pin plastic QUIP

Recommended Condition Symbol	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260°C max., Duration: 10 sec. max.

Note Ensure that the application of wave soldering is limited to the lead part and no solder touches the main unit directly.

Notice

A version of this product with improved recommended soldering conditions is available.
For details (improvements such as infrared reflow peak temperature extension (235°C), number of times: twice, relaxation of time limit, etc.) contact NEC sales personnel.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78212, 78213 and 78214.

Language Processing Software

RA78K/II*1, 2, 3	78K/II series common assembler package
CC78K/II*1, 2, 3	78K/II series common C compiler package
CC78K/II-L*1, 2, 3	78K/II series common C compiler library source file

PROM Programming Tools

PG-1500	PROM programmer
PA-78P214CW PA-78P214GC PA-78P214GJ PA-78P214GQ PA-78P214L	Programmer adapters connected to PG-1500
PG-1500 controller*1, 2	PG-1500 control program

Debugging Tools

IE-78240-R-A IE-78240-R*4 IE-78210-R*4	μPD78214 subseries common in-circuit emulators
IE-78200-R-BK	78K/II common break board
IE-78210-R-EM*4 IE-78240-R-EM IE-78200-R-EM*4	μPD78214 subseries evaluation emulation boards
EP-78210CW*4 EP-78240CW-R EP-78210GC*4 EP-78240GC-R EP-78210GJ*4 EP-78240GJ-R EP-78210GQ*4 EP-78240GQ-R EP-78210L*4 EP-78240LP-R	μPD78214 subseries common emulation probes
EV-9200G-74 EV-9200GC-64	Sockets mounted onto user system board for 74-pin plastic QFP and 64-pin plastic QFP
SD78K/II*1, 2	IE-78240-R-A screen debugger
DF78210*1, 2	μPD78214 subseries device file

Fuzzy Inference Development Support System

FE9000*1, FE9200*5	Fuzzy knowledge data creation tool
FT9080*1, FT9085*2	Translator
FI178K/II*1,2	Fuzzy inference module
FD78K/II*1,2	Fuzzy inference debugger

* **1.** PC-9800 series (MS-DOS™) based.
2. IBM PC/AT™ (PC DOS™) based.
3. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based and EWS-4800 series™ (EWS-UX/V™) based.
4. No longer manufactured and not available for purchase.
5. IBM PC/AT (PC DOS + Windows™) based.

APPENDIX B. RELATED DOCUMENTS

Device Related Document

Document Name		Document No. (Japanese)	Document No. (English)
μPD78214 Series User's Manual Hardware Volume		IEM-5119	IEU-1236
78K/II Series User's Manual Instruction Volume		IEU-754	IEU-1311
78K/II Series Application Note	Basic	IEA-607	IEA-1220
	Application	IEA-700	IEA-1282
	Floating-Point Operation Program	IEA-686	IEA-1273
78K/II Series Selection Guide		IF-304	IF-1160
78K/II Series Instructions		IEM-5101	—
78K/II Series Instruction Set		IEM-5102	—
μPD78214 Series Mode Register Application Table		IEM-5100	—

Development Tool Related Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78240-R-A In-Circuit Emulator		EEU-796	EEU-1395
IE-78240-R In-Circuit Emulator	Hardware	EEU-705	EEU-1322
	Software	EEU-706	EEU-1331
IE-78210-R	Hardware	EEP-640	EEP-1027
	Software	EEM-685	EEM-1024
IE-78210-R System Software	PC-9800 Series Based	EEM-677	EEU-1260
	IBM PC Series Based	EEM-753	EEM-1027
SD78K/II Screen Debugger MS-DOS Based	Basic	EEU-841	—
	Reference	EEU-813	—
SD78K/II Screen Debugger PC DOS Based	Basic	—	—
	Reference	EEU-956	EEU-1447
78K/II Series Development Tools Selection Guide		EF-231	—

Note **The contents of the above related document are subject to change without notice. The latest document should be used for design, etc.**

Built-In Software Related Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
Fuzzy Knowledge Data Creation Tools		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System	Translator	EEU-862	EEU-1444
78K/II Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-860	EEU-1440
78K/II Series Fuzzy Inference Debugger		EEU-917	EEU-1459

Other Related Documents

Document Name	Document No. (Japanese)	Document No. (English)
FQTOP Microcomputer Brochure	IB-5040	—
Package Manual	IEI-635	IEI-1213
Surface Mount Technology Manual	IEI-616	IEI-1207
Quality Grades on Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability & Quality Manual	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Devices Quality Control Guarantee Guide	MEI-603	MEI-1202
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604	—

Note **The contents of the above related document are subject to change without notice. The latest document should be used for design, etc.**

[MEMO]