BARDIA MOHAMMADZADEH

M: 07780009536 **E**: bardia.mzad@gmail.com **L**: London
Online Portfolio : https://bardia01.github.io/

EDUCATION

Imperial College London, September 2020 – June 2024

MEng Electronic and Information Engineering

Current 3rd year student with a grade average of a First-Class Honours.

Woodhouse College, September 2018 – June 2020

A Levels

Mathematics	A*
Further Mathematics	A*
Physics	A*

CAREER ASPIRATIONS / PERSONAL PROFILE

I am in my penultimate year studying Electronic and Information Engineering MEng at Imperial College London. I am keen to develop my career as a hardware engineer.

TECHNICAL SKILLS AND PROGRAMMING LANGUAGES

Fluent:

- Verilog / SystemVerilog
- UVM (Universal Verification Methodology)
- SVA (SystemVerilog Assertions)
- C++
- Python

Intermediate:

- C
- MATLAB
- PyTorch, Pandas, Matplotlib

Skills:

- Digital Design and Design Verification with UVM
- Timing and area analysis

WORK EXPERIENCE

Apple GPU, April 2023 – September 2023

Design Verification Intern – Interconnect team

- Built models based upon architectural specification which aided in bring-up of new features
- Improved testbench performance
- Implemented coverage collection
- Created a packet tracking and packet timeout tool in UVM to aid debug
- Debugged failure signatures using logs and waveform viewers
- Built versatile stimulus using UVM

Graphcore, June 2022 – September 2022

Logical Design Intern – Silicon team

- I spent 3 months at Graphcore designing, verifying, and building multiple hardware modules in SystemVerilog.
- I spent a lot of time learning about designing optimized hardware for floating point arithmetic units. These included implementing multiple advanced optimizations such as clock gating and forced parallelism.
- I had to verify and synthesize my designs myself and hence learned a great deal about the verification and physical teams in Silicon engineering also.

Achievements with Graphcore

- I implemented original optimizations which caused performance increases for which I led a presentation to the entire Silicon team.

TECHNICAL EXPERIENCE

- Designed an arithmetic accelerator deployed on an FPGA to accelerate computations written in C. The designs were iterated and optimised for timing and area. The final design incorporated DMA accesses and a custom hardware block including a CORDIC implementation.
- Designed an image processor on FPGA hardware. This included hardware implementations of filtering, color space conversions and gradient detection.
- Built a self-driving rover which communicated with servers to upload a map of its surroundings which it built through scanning objects. The image processor provided instructions for the rover's movement and data about the objects found by analyzing the video feed from a camera.
- Built, optimized, and verified a double precision floating point multiplier with multiple rounding modes which met IEEE754 standards which was heavily optimized for speed.
- Created scripts for use in trial synthesis of digital modules. These included writing area and timing budgets.
- Used industry standard EDA tools to analyze physical builds of digital modules. This involved timing and area analysis.
- Built a live multiplayer game hosted on AWS using the Unity game engine, which used a DE10-Lite FPGA as a controller with tilt, button, and switch control inputs. I used python to create an API to integrate the controller inputs with Unity.
- Built a C compiler to the ANSI-C standard using C++ which output MIPS-32 5.4 assembly language.
- Designed and simulated a Turing-complete dual core CPU with floating point arithmetic and a serial input port based on a reduced ARM ISA