Bardia Barabadi

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OBJECTIVE

Knowledgeable and detail-oriented Electrical Engineer with an extensive background in Signal Processing, Hardware/Software design and Machine Learning. Looking forward to make my skills practical in the Canadian industry.

SKILLS

Programming Languages & Tools:

- Top Skills: Matlab, Verilog, Python, C++, Assembly, Linux
- Other Languages: C, VHDL, Bash, LaTeX, JAVA
- Tools & IDEs: iPython, atollic TrueStudio, PyCharm, Vim
- ASIC & FPGA: Vivado & HLS, ISE, Quartus
  Modelsim, Isim, Synopsys Design Compiler
  NIOS II on Altera DE2 & MicroBlaze on Xilinx Spartan
- Microcontrollers: AVR AT-Family, Arduino, ARM STM
- Embedded Linux: Raspberry pi-3 (Raspian, Ubuntu Mate)
- Parallel Platforms: CUDA, Pthread, MPI, OpenMP
- Machine Learning: TensorFlow, Keras, Matlab Deep-Learning Toolbox

EDUCATION

M.A.Sc. in Electrical Engineering at University of Victoria Sep 2018 - Now

- Thesis Title: Phase Unwrapping Optimization Algorithm Enhancement

B.Sc. (Hons.) in Electrical Engineering Sep 2013 - Apr 2018

- Sharif University of Technology, Tehran, Iran
- Major: Digital System Design - Project Title: FPGA Implementation of IMAT

EXPERIENCE

University of Victoria

Encoded Video Quality Enhancement Using CNNs 2020

- Convolutional Neural Nets (CNNs), Keras, Tensorflow, Python and FFmpeg

Scale-Invariant Super-Resolution Using CNNs 2019

- Convolutional Neural Nets (CNNs), Bash, Tensorflow and Python

Dual-Stage Phase-Unwrapping 2018

- MITACS Funded Intern - 3vGeomatics, Vancouver, BC
- Improving Primal-Dual algorithm used in Satellite Imagery Analysis
- C++, Python, Bash, MPI & pthreads

Sharif University of Technology

ASIC & FPGA Implementation of IMAT 2017-2018

- Iterative Method w. Adaptive Threshold, Sparse Signal Reconstruction Algorithm
- Proof-of-Concept Hardware Implementation, Optimized for 180^{nm} ASIC & FPGA
- Verilog, Modelsim, Vivado, Xilinx ISE, Synopsys Design Compiler, MATLAB

Smart Light Socket 2017

- Internship, Bluetooth Low Energy (BLE) based smart socket, built from scratch
- ARM Embedded SoC (nRF51xxx), C, nRFgo Studio, Mixed Signal PCB

DVB-T Transmitter and Receiver on 180^{nm} ASIC 2017
- Verilog, MATLAB (Fixed-Point Designer), Modelsim, Synopsys Design Compiler

Critical Object Recognition in Millimeter Wave Imagary 2016
- MATLAB, PCA, Artificial Neural Networks (ANNs) and Bash

Hardware Accelerated K-means Algorithm 2016
- Platform: Xilinx Spartan-IV Micro-Blaze Soft Core Processor, AXI Interconnect
- Xilinx Platform Studio (XPS), ISE, Modelsim, C, Matlab (UART & Validation)

Superscalar MIPS Rev-5 Microprocessor on FPGA 2015
- 4-way Superscalar Architecture with Pre-fetcher, Cache & Assembler
- Verilog, VHDL, Xilinx ISE, Altera Quartus, JAVA (for Assembler)

Contracts & Freelance

E-Learning System for new Employees 2015
- Contract, Monenco Co., Tehran, Iran
- Action Script 3.0, Adobe Flash, Lightroom and Photoshop

Fluid Color Sensitive Motor Controller 2014
- Freelance, ChemiCar Contest, Tabriz University, Iran
- AVR, C, Mixed-Signal PCB design

Teaching Experience

University of Victoria: Teaching Assistant 2018-2019
- Positions: Lab TA*4
- Courses: Real-Time Computer System Design, Computer Architecture
- Received excellent teaching certification owing to students evaluation

Sharif University of Technology: Teaching Assistant 2016-2018
- Positions: Head TA*2, Lab TA*5, Verilog Tutor*2, Marker*1
- Courses: Computer Architecture, Logic Circuits, ASIC-FPGA, Microprocessor

AE High School: Robotics Teacher & Mentor 2016-2018
- Subjects: Algorithms, AVR Microcontrollers, PCB Design, C language
- Achievement: 1st Place Iran Open 2016, CoSpace league

Volunteer Experience

Sharif Cup III robotic contest: Referee, Executive committee 2016

Sharif Cup II robotic contest: Executive committee 2015

Publication

1. **B. Barabadi**, M. Gara, A. Jooya, A. Baniasadi, NJ. Dimopoulos, “Dual-Stage Phase Unwrapping”, IEEE NorCAS (2019).
2. K. Helal, **B. Barabadi**, A. Baniasadi, NJ. Dimopoulos, “Scale Invariant Super-Resolution Methods”, IEEE APCCAS (2019).
3. **B. Barabadi**, M. Gara, A. Baniasadi, NJ. Dimopoulos, “Employing Machine Learning Optimization Techniques In Radar Imagery Phase Unwrapping”, American Geophysical Union Fall Meeting (2019). Poster

Hobbies

Photography, Hiking, Cycling, Poker, Piano, Volleyball, Billiards

REFERENCE

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