Assignment 7: Effect of Cache Design on performance

This assignment is based on DineroIV cache simulator which can be compiled using the source code uploaded on moodle. See the instructions in README to install the simulator on your machines. The folder also includes a subfolder named traces which contains the relevant files you need to answer questions in this assignment. Get familiar with the simulator by running it using these trace files. You can use -help option with the executive to get the details about all command line options.

Submission Instructions: Make a directory named with your roll number. Write your results and observations with appropriate numbering in a file named report.txt and include it in your directory. Other than this, include all the files you think are relevant e.g., the images showing plots, excel sheet (or any other format) for tables etc. Finally submit a tar.gz i.e., [roll-no.].tar.gz (as follows) on moodle:

```
[roll-no.]
   |----report.txt
   |----[images for the asked plots]
   |----[files including your tables]
   |----[other files you think are relevant]
```

Use the DineroIV cache simulator to answer the following using each of the three programs – spice circuit simulator, cc compiler and tex word processor. Trace files (.din) for all these programs can be found in traces subfolder of dineroIV. Prepare a table showing the number of memory references and number of misses including break-up of compulsory, capacity and conflict misses. Show instruction and data statistics separately. Also include the miss rate (of course!). There should be a separate row for each of the following. (If the row is too large, use two rows for each item below). Create separate tables for the three benchmarks.
In each case, use 500,000 (or more) memory references.

1. 8K unified direct-mapped L1 cache with block size = 16 bytes
2. 16K unified direct-mapped L1 cache with block size = 16 bytes
3. 16K unified L1 cache with block size = 16 bytes and associativity = 2
4. 16K unified L1 cache with block size = 32 bytes and associativity = 2
5. 16K split L1 cache (8K data + 8K instruction) with block size = 32 bytes and associativity = 2
6. 16K split L1 cache (8K + 8K) with block size = 32 bytes, associativity = 2 and 128K L2 cache

P1. Plot MR (miss rate) versus block size (for block sizes = 8, 16, 32, 64, 128 bytes) for 4, 8, 16 and 32 K unified caches (on the same plot). Use any benchmark.

P2. Plot MR versus associativity (for associativity = 1, 2, 4, 8 and 16) for 4, 8, 16 and 32 K unified caches (on the same plot). Use any benchmark.

R. Study all results from your experiments and report the top 10 most interesting (and possibly surprising!) conclusions. List the conclusions in decreasing order of importance in report.txt file.