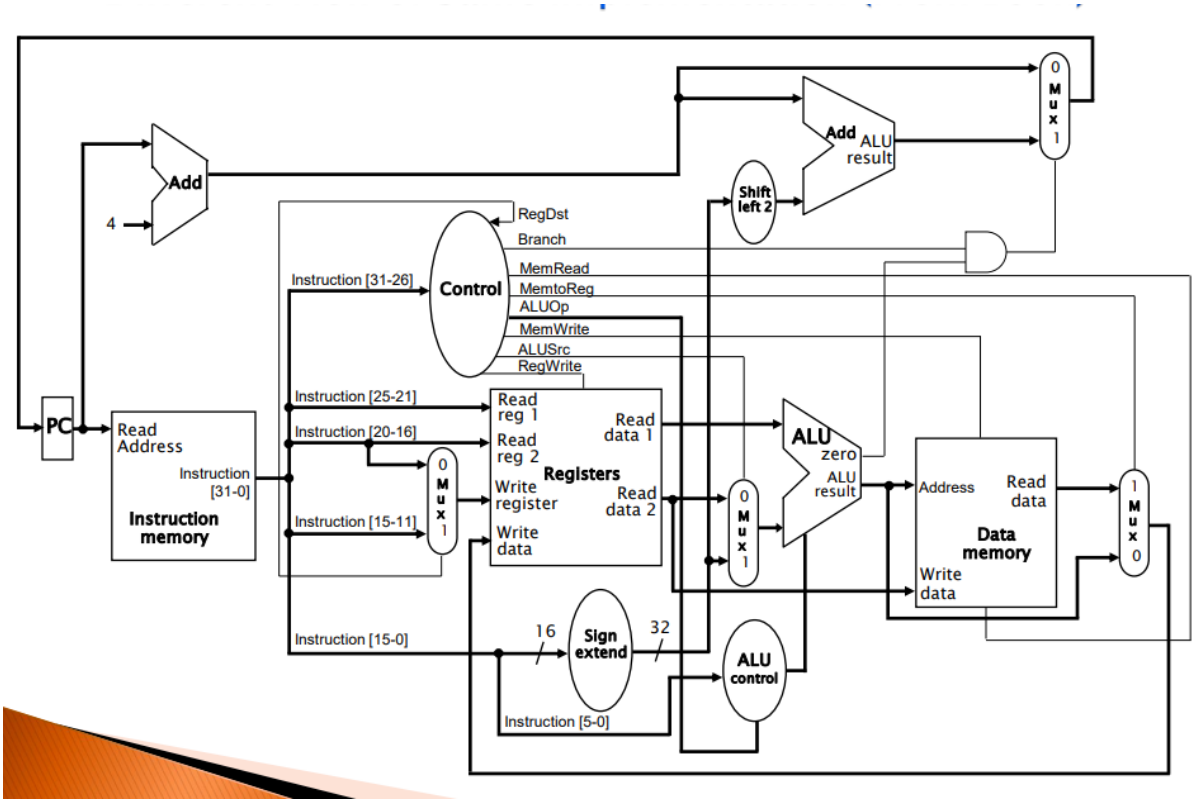
Barış Ayyıldız
1901042252
CSE 331
Homework 4 Report



I tried to build this datapath. But verilog gave me various, nonsense errors during the implementation. So I just gave up.

I used the same components from the previous homework for the ALU. I have also implemented register but for only reading data. But I could not connect the pieces together inside **MiniMIPS.v** file.

I have also added state tables that I was planning to use for control unit outputs and ALUControl.