step-1 :

3 operation + maintain

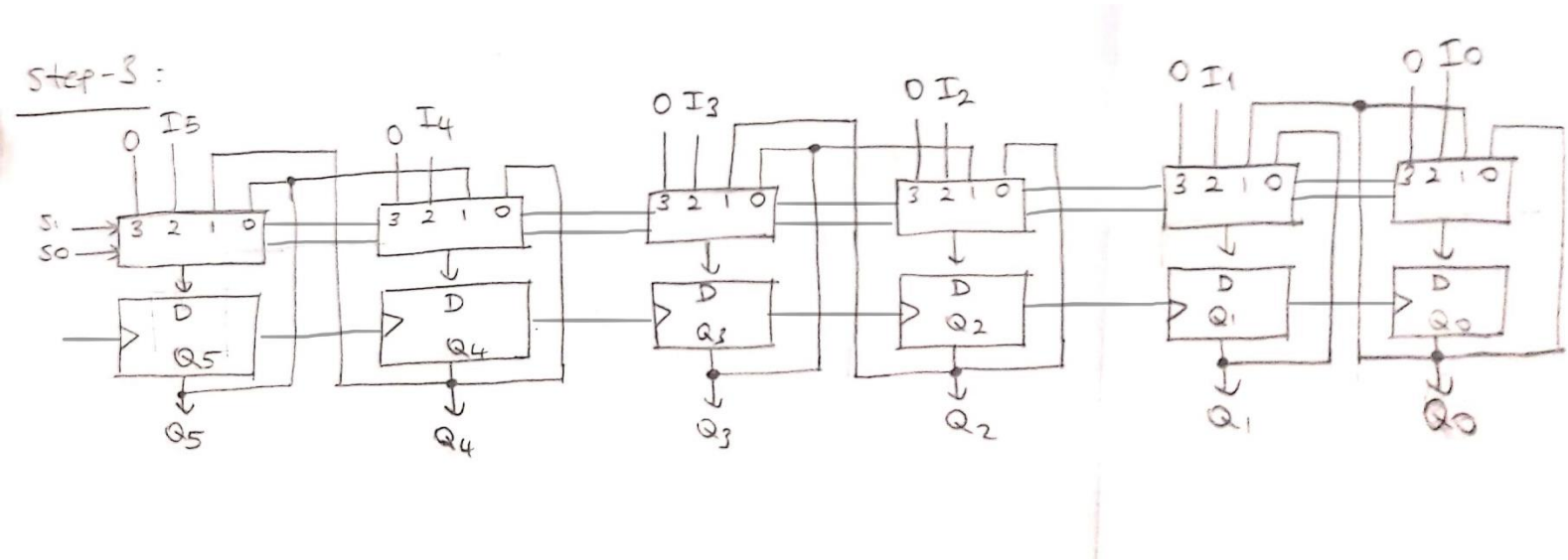
= 4 operations

→ Use 4 x 1 mux

Step-2

s1	s0	Operation
0	0	maintain present state
0	1	swap the consecutive bits
1	0	load data to register
1	1	load registers with 0

Step-3

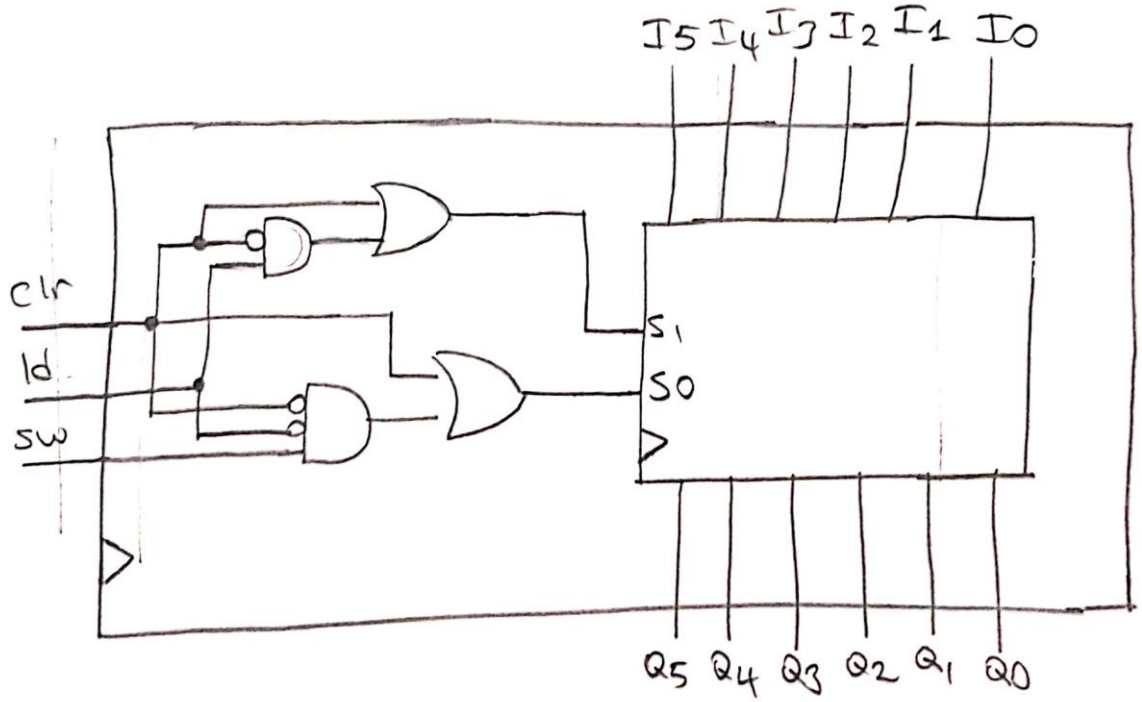


Step-4

Inputs			Outputs		
clr	**ld**	**sw**	**s1**	**s0**	**operation**
0	0	0	0	0	maintain present state
0	0	1	0	1	swap the consecutive bits
0	1	x	1	0	load data to register
1	x	x	1	1	load registers with 0

$S_1 = Clr' * ld + Clr$

$S_0 = Clr' * ld' * sw + Clr$



Barış Ayyıldız

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