INSTRUCTION SET

Arithr	netic Opera	tions	byles	OS Perior
ADD	A,Rn		1	1
ADD	A,@Ri	add source to A	1	2
ADD	A,direct	add source to A	2	2
ADD	A,#data		2	2
ADDC	A,Rn		1	1
ADDC	A,@Ri	add with carry	1	2
ADDC	A,direct	aud with carry	2	2
ADDC	A,#data		2	2
SUBB	A,Rn		1	1
SUBB	A,@Ri	subtract from A	1	2
SUBB	A,direct	with borrow	2	2
SUBB	A,#data		2	2
INC	A		1	1
INC	Rn		1	1
INC	@Ri	increment	1	2
INC	direct	1	2	2
INC	DPTR *		1	3
DEC	Α		1	1
DEC	Rn	decrement	1	1
DEC	@Ri	uecrement	1	2
DEC	direct		2	2
MUL	AB	multiply A by B	1	9
DIV	AB	divide A by B	1	9

decimal adjust 1 2 INC DPTR increments the 24bit value DPP/DPH/DPL

Boole	an Var	iable Manipulation	th/les	OS Perio
CLR	С	clear bit to zero	1	1
CLR	bit	clear bit to zero	2	2
SETB	С	set bit to one	1	1
SETB	bit	set bit to one	2	2
CPL	С		1	1
CPL	bit	complement bit	2	2
ANL	C,bit	AND bit with C	2	2
ANL	C,/bit	AND (NOTbit) with C	2	2
ORL	C,bit	OR bit with C	2	2
ORL	C,/bit	OR (NOTbit) with C	2	2
MOV	C,bit	move bit to bit	2	2
MOV	bit,C	move bit to bit	2	2
JC	rel	jump if C set	2	3
JNC	rel	jmp if C not set	2	3
JB	bit,rel	jump if bit set	3	4
JNB	bit,rel	jmp if bit not set	3	4
JBC	bit,rel	jmp&clear if set	3	4

Progr	am Branchi	ng	194,	026
ACALL	addr11	call subroutine	2	3
LCALL	addr16	can subroutine	3	4
RET		return from sub.	1	4
RETI		return from int.	1	4
AJMP	addr11		2	3
LJMP	addr16	jump	3	4
SJMP	rel	Jump	2	3
JMP	@A+DPTR		1	3
JZ	rel	jump if A = 0	2	3
JNZ	rel	jump if A not 0	2	3
CJNE	A,direct,rel	compare and	3	4
CJNE	A,#data,rel	jump if not	3	4
CJNE	Rn,#data,rel	equal	3	4
CJNE	@Ri,#data,rel	equai	2	4
DJNZ	Rn,rel	decrement and	2	3
DJNZ	direct, rel	jump if not zero	3	4
NOP		no operation	1	1

Legend

register addressing using R0-R7				
8bit internal address (00h-FFh)				
indirect addressing using R0 or R1				
8bit constant included in instruction				
16bit constant included in instruction				
8bit direct address of bit				
signed 8bit offset				
11bit address in current 2K page				
16bit address				

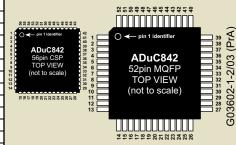
Data Transfer Op	PAGE	0,50,	
MOV A,Rn		1	1
MOV A,@Ri		1	2
MOV A,direct		2	2
MOV A,#data		2	2
MOV Rn,A		1	1
MOV @Ri,A		1	2
MOV direct,A		2	2
MOV Rn,direct	move	2	2
MOV direct,Rn		2	2
MOV direct, direct		3	3
MOV Rn,#data		2	2
MOV @Ri,#data		2	2
MOV direct,#data		3	3
MOV DPTR,#data16		3	3
MOVC A,@A+DPTR	move from	1	4
MOVC A,@A+PC	code memory	1	4
MOVX A,@Ri		1	4
MOVX A,@DPTR	move to/from	1	4
MOVX @Ri,A	data memory	1	4
MOVX @DPTR,A		1	4
PUSH direct	push onto stack	2	2

			•	- \
ANL	A,Rn		1	1
ANL	A,@Ri	1	2	
ANL	A,direct	logical AND	2	2
ANL	A,#data	logical AND	2	2
ANL	direct,A		2	2
ANL	direct,#data		3	3
ORL	A,Rn		1	1
ORL	A,@Ri		1	2
ORL	A,direct	logical OR	2	2
ORL	A,#data	logical OR	2	2
ORL	direct,A		2	2
ORL	direct,#data		3	3
XRL	A,Rn		1	1
XRL	A,@Ri		1	2
XRL	A,direct	logical XOR	2	2
XRL	A,#data	logical XOR	2	2
XRL	direct,A		2	2
XRL	direct,#data		3	3
CLR	Α	clear A to zero	1	1
CPL	Α	complement A	1	1
RL	Α	rotate A left	1	1
RLC	Α	through C	1	1
RR	Α	rotate A right	1	1
RRC	Α	through C	1	1
SWAP	A	swap nibbles	1	1

INSTRUCTIONS THAT AFFECT FLAGS

I	INCOME IN	/ (7.1.27.00
ADD A,x	C = carry out of bit 7	DAx	C = (x>100 or C=1)
	AC = carry out of bit 3 OV = carry out of bit 6, but not 7	RRC A	C = ACC.7
ADDC A v	C = carry out of bit 7	RLCA	C = ACC.0
ADDC A,X	AC = carry out of bit 3	SETB C	C = 1
l	OV = carry out of bit 6, but not 7	CLR C	C = 0
SUBB A,x	C = borrow into bit 7	ANL C,bit	C = C and bit
l	AC = borrow into bit 3 OV = borrow into bit 6, but not 7	ANL C,/bit	C = C and NOTbit
MULAB	C = 0	ORL C,bit	C = C or bit
WIULAB	OV = result>255	ORL C,/bit	C = C or NOTbit
DIV AB	C = 0	MOV C,bit	C = bit
	OV = divide by zero	CJNE x,y,rel	C = x <y< td=""></y<>

PIN FUNCTIONS



15	P1.6 / ADC6	
16	P1.7 / ADC7	
17	RESET	
18	P3.0 / RxD	
19	P3.1 / TxD	
20	P3.2 / INT0	
21	P3.3/INT1/MISO/PWM1	
22	DV _{DD}	
23	DGND	
24	P3.4 / T0 / PWMC / PWM0 / EXTCLK	
25	P3.5 / T1 / CONVST	
26	P3.6 / WR	
27	P3.7 / RD	
28	SCLOCK	

Mate es

1 56 P1.0 / ADC0 / T2

3 2 P1.2 / ADC2

4 3 P1.3 / ADC3 5 4,5 AV_{DD}

6 6,7,8 AGND

7 9 CREF

8 10 VREF

13

14 15 16

18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |

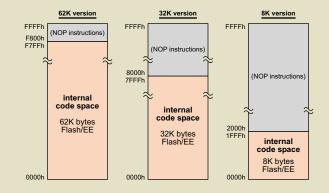
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9 11 DAC0 10 12 DAC1 11 13 P1.4 / ADC4 12 14 P1.5 / ADC5 / SS

P1.1 / ADC1 / T2EX

MOF	ેલ્ડ		MOE	ર દુ	
27	29	SDATA / MOSI	40	43	ĒĀ
28	30	P2.0 / A8 / A16	41	44	PSEN
29	31	P2.1 / A9 / A17	42	45	ALE
30	32	P2.2 / A10 / A18	43	46	P0.0 / AD0
31	33	P2.3 / A11 / A19	44	47	P0.1 / AD1
32	34	XTAL1 (in)	45	48	P0.2 / AD2
33	35	XTAL2 (out)	46	49	P0.3 / AD3
34	36	DV _{DD}	47	50	DGND
35	37,38	DGND	48	51	DV _{DD}
36	39	P2.4 / A12 / A20	49	52	P0.4 / AD4
37	40	P2.5 / A13 / A21	50	53	P0.5 / AD5
38	41	P2.6/A14/A22/PWM0	51	54	P0.6 / AD6
39	42	P2.7/A15/A23/PWM1	52	55	P0.7 / AD7

CODE MEMORY SPACE OPTIONS



INTERRUPT VECTOR ADDRESSES

Interrupt Bit	Interrupt Name	Vector Address	Priority within Level
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
ADCI	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I2C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

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ANALOG DEVICES

ADuC842

MicroConverter® **Quick Reference Guide**

a "Data Acquisition System on a Chip"

the ADuC842 is: ADC: 12bit, 5µs, 8channel, self calibrating

0.5LSB INL & 70dB SNR

DAC: dual, 12bit, 15µs, voltage output 1LSB DNL

Flash/EEPROM: 62K bytes Flash/EE program memory

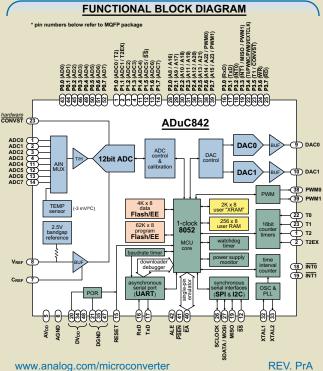
4K bytes Flash/EE data memory

microcontroller:

"single-cycle" 8052 32 I/O lines, programmable PLL clock (131KHz to 16.8MHz from 32KHz crystal)

other on-chip features: temperature sensor, power supply monitor,

watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8/16bit PWM, power-on-reset



DATA MEMORY: RAM, SFRs, user Flash/EE (all read/write)

decimal address	HEX address			ı	OWI	ER R	AM					
127	7Fh				l .							
		Ger	neral Pu Area	rpose	MSB address							LSB address
48	30h				MS			(bit add	resses)			age
47	2Fh				7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
46	2Eh				77h	76h	75h	74h	73h	72h	71h	70h
45	2Dh				6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
44	2Ch				67h	66h	65h	64h	63h	62h	61h	60h
43	2Bh				5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
42	2Ah				57h	56h	55h	54h	53h	52h	51h	50h
41 40	29h	Bit	Addres: Area	sable	4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
	28h				47h	46h	45h	44h	43h	42h	41h	40h
39 38	27h				3Fh	3Eh 36h	3Dh	3Ch 34h	3Bh 33h	3Ah 32h	39h 31h	38h 30h
37	26h 25h				37h 2Fh		35h 2Dh	2Ch	2Bh	2Ah	29h	28h
36	24h				2FII 27h	2Eh 26h	25h	20h	28h	22g	29fi 21h	20h
35	23h				1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
34	22h				17h	16h	15h	14h	13h	12h	11g	10h
33	21h				0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
32	20h				07h	06h	05h	04h	03h	02h	01h	00h
31	1Fh	R7										رت
30	1Eh	R6										
29	1Dh	R5	بر 3									_
28	1Ch	R4	Register Bank 3	1		D.	ATA	MEM	ORY	SPA	CE	
27	1Bh	R3	ster				(re	ead/w	rite a	rea)		
26	1Ah	R2	Segi:	١.								
25	19h	R1	"									
24	18h	R0		3FI	-h =(r	age 102	23)			FFFF	FFh [
23	17h	R7			₹		$\frac{1}{2}$				$\stackrel{\downarrow}{\approx}$	
22	16h	R6	٠,		Ĭ		Ĩ				Ĭ	
21	15h	R5	, ž			4K byte K page						
20	14h	R4	Register Bank 2			data						
19	13h	R3	jiste			lash/E		`				
18	12h	R2	, g			througl	h					
17	11h	R1				SFRs)					$\overline{}$	
16	10h	R0						7	FFh [\neg	
15	0Fh	R7		000	0h <u>E (</u>	page 0) =		1			
14	0Eh	R6	-						γ		T	
13	0Dh	R5	ank					\forall		NEOC 15		DE00406
12	0Ch	R4	Register Bank	FF	12	8 bytes		ere-		FG842.	U=1 C	DFG842.0=
11	0Bh	R3	gist		upp	er RAI		SFRs direct		interna	al	external
10	0Ah	R2	8		(ir	ndirect Iressin	add	dressing	g	data	ry	data memory
9 B	09h	R1				only)		only)				
7	08h 07h	R0 R7			12	8 bytes				2K byte		(16M bytes Iddressable
r S	07h	R6			low	er RAI	И					
5	05h	R5	<u>×</u>			irect or idirect						
1	04h	R4	Bank	100	044	ressing	3)	0	00h			
3	03h	R3		že e								
2	02h	R2	Register									
1	01h	R1	nž									
0	00h	R0										
			lo	wer RA details	м				SFR	details	5	

SFR MAP & RESET VALUES

				3			ω i\i			LOL	.5				
(reserved)	SPIDAT F7h 00h	ADCCON1 EFh 40h	(reserved)	PSMCON DFh DEh	PLLCON D7h 53h	(reserved)	3L EADRH 00h C7h 00h	EDATA4 BFh 00h	SPH B7h 00h	ON CFG842 00h AFh 00h	DPCON A7h 00h	(pesn tou)	(pesn tou)	(reserved)	PCON 87h OOh
(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EADRL C6h 00h	EDATA3 BEh 00h	(not used)	PWMCON AEh 00h	INTVAL A6h 00h	T3CON 9Eh 00h	(not used)	(reserved)	(reserved)
DACCON FDh 04h	ADCCON3 F5h 00h	(reserved)	(reserved)	(reserved)	(reserved)	TH2 CDh 00h	(reserved)	EDATA2 BDh 00h	(not used)	(reserved)	HOUR A5h 00h	T3FD 9Dh 00h	(not used)	TH1 8Dh 00h	(reserved)
	ADCGAINH F4h *00h	(reserved)	(reserved)	(reserved)	DMAP D4h 00h	2H TL2 00h CCh 00h	(reserved)	EDATA1 BCh 00h	PWM1H B4h 00h	(reserved)	MIN A4h 00h	(not used)	(not used)	00h 8Ch 00h	DPP 84h OOh
0H DAC1L DAC1H 00h FBh 00h FCh 00h	ADCOFSL ADCOFSH ADCGAINL ADCGAINH ADCCON3 F1h '00h F2h '20h F3h '00h F5h 00h	(reserved)	(reserved)	(reserved)	DMAH 00h D3h 00h	RCAF CBh	(reserved)	(reserved)	PWM1L B3h 00h	(reserved)	EC SEC 00h A3h 00h	00h 9Bh 55h	I2CADD3 93h 00h	00h 88h 00h	P DPL DPH
PAP	ADCOFSH F2h *20h	(reserved)	(reserved)	ADCCON2 ADCDATAL ADCDATAH D8h 00h D9h 00h DAh 00h	DMAL D2h 00h	RCAP2L CAh 00h	CZh 2Xh	(reserved)	PWM0H B2h 00h	(reserved)	HTHS A2h	F I2CDAT 00h 9Ah 00h	I2CADD2 92h 00h	APP APP	DPL 82h 00h
DAC0L F9h 00h		(reserved)	(reserved)	ADCDATAL D9h 00h	(reserved)	(reserved)	(reserved)	ECON 89h 00h	PWM0L B1h 00h	IEIP2 00h A9h A0h	TIMECON A1h 00h	SBU 99h	I2CADD1 FFh 91h 00h	TMOD 89h 00h	SP OZh
SPICON F8h 04h	B F0h 00h	I2CCON E8h 00h	ACC E0h 00h	ADCCON2 D8h 00h	PSW D0h	T2CON C8h 00h	WDCON COh 10h	IP 00h	P3 B0h FFh	IE A8h 00h	P2 A0h FFh	SCON 98h 00h	P1 90h FFh	TCON 88h 00h	PO ROP FEB
Δ	otin	otin	otin	otin	otin	otin	otin	otin	otin	otin	otin	otin	otin	otin	$\sqrt{}$
SPR0 0 F8h 0	0 F0h 0	(0 E0h 0	0 D8h 0	a 400	CAP2	O CON O	0 B8h 0	RXD 1	0 A8h 0	1 A0h	0 88h 0	12 1 90h	0 HSB 0	1 80h
SPR1	£	12CTX E9h (#	CS1	E #	CNT2 C9h 0	WDI C1h	PT0	X #	ET0	A1h	⊢	T2EX	E0	
CPHA Fah	F2h 0	I2CRS EAh 0	E2h 0	CS2 DAh 0	0V	TR2	WDS C2h 0	PX1 BAh 0	1NT0 B2h 1	AAh 0	A2h 1	RB8 9Ah 0	92h 1	1T1 8Ah 0	82h
CPOL FBh 0	F3h 0	I2CM EBh 0	E3h 0	CS3 DBh 0	0 D3h 0	EXEN2 CBh 0	WDIR cah 0	PT1 BBh 0	INT1 B3h 1	ET1 ABh 0	A3h 1	TB8	93h 1	IE1 0	1 83h 1 82h 1
SPIM PGh 0	F4h 0	I2CID0 Ech MDI 0	E4h 0	_	RS1 0	TCLK cch o	PRE0 C4h 1	PS BCh 0	T0 184h	ES OACh 0	A4h 1	REN 9Ch 0	94h 1	TR0 8Ch 0	84h
SPE o HDI	F5h 0	I2CID1 EDhMC0 ₀	E5h 0	CCONV SCONV	F0	RCLK CDh 0	PRE1 C5h 0	PT2 BDh 0	1 B5h 1	ET2 ADh 0	A5h 1	SM2 9Dh 0	95h 1	TF0 8Dh 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
WCOL FEh 0	FGh 0	I2CGC EEh MDE 0	E6h 0	DMA DEh 0	AC Deh 0	EXF2 CEh 0	PRE2 C6h 0	PADC BEh 0	WR 1	EADC AEh 0	A6h 1	SM1	96h 1	TR1 0	1 198
ISPI FFh 0	F7h 0	I2CSI EFhMDO ₀	E7h 0	ADCI DFh 0	CΥ	TF2 0 CFh 0	PRE3 c7h 0	PSI BFh 0	RD 1	EA 0	A7h 1	SM0 9Fh 0	97h 1	TF1	87h 1
	these bits are contained in this byte mnemonic SPR1 SPR0 SPICON mnemonic address F8h 0 F8h 0 H8h 0 Odh reset value														

SFR DESCRIPTIONS						
ADCCON1 ADC Control register #1 ADCCON1.7 ADC mode (0=off, 1=on)	T3FD Timer 3 Fractional Divider register T3FD = (2·F _{CORE}) / (baudrate·2 ^{DIV}) - 64					
ADCCON1.6 external Vref select bit (0=on-chip Vref) ADCCON1.5 conversion time = 16 / ADCcl ADCCON1.4 ADCclk = 16,777,216Hz / [2,4,8,32]	CHIPID Chip ID Register (6X hex = ADuC842)					
ADCCON1.3 acquisition time select bits ADCCON1.2 acq time = [1,2,3,4] / ADCck ADCCON1.1 Timer2 convert enable	CFG842 ADuC842 Configuration Register CFG842.7 extended stack-pointer enable (0=disable)					
ADCCON1.0 external CONVST enable	CFG842.6 PWM pins select (0=P2.6/P2.7,1=P3.4/P3.3) CFG842.5 DAC output buffer bypass (0=buffer enabled)					
ADCI ADC interrupt flag						
DMA DMA mode enable CCONV continuous conversion enable bit SCONV single conversion start bit	CFG842.2 (this bit must contain 0) CFG842.1 (this bit must contain 0) CFG842.1 select SPI pins (0=default, 1=P3.3/P3.4/P3.5) CFG842.0 internal XRAM select (0=external XRAM)					
SCONV single conversion start bit CS3 input channel select bits: CS2 0 - 7 = ADC0 - ADC7 CS1 8 = temperature sensor	WDCON Watchdog Timer control register					
CS1 8 = temperature sensor CS0 9=DAC0, A=DAC1, B=AGND ADCCON3 ADC Control register #3	PRE2 0-7=[15.6,31.2,62.5,125,250,500,1000,2000]ms					
ADCCON3.7 busy indicator flag (0=ADC not active) ADCCON3.6 gain calibration disable (0=gain cal enabled)	WDIR watchdog interrupt response bit					
ADCCON3.5 number of averages selection bits: ADCCON3.4 [15,1,31,63] ADCCON3.3 cal clock divide select (0=ADCclk, 1=ADCclk/2)	WDS watchdog status flag (1 indicates watchdog timeout) WDE watchdog enable control (0=disabled) WDWR watchdog write enable bit (set to enable write)					
ADCCON3.2 cal mode select (0=device, 1=system) ADCCON3.1 cal type select (0=offset, 1=gain)	PSMCON.6 PSM status bit (1=normal / 0=fault) PSMCON.5 PSM interrupt bit					
ADCDATAH	PSMCON.5 PSM interrupt bit PSMCON.4 trip point select bits PSMCON.3 [4.63V, 3.08V, 2.93V, 2.63V] PSMCON.2 (this bit must contain zero)					
ADC Data registers	PSMCON.2 (this bit must contain zero) PSMCON.1 (reserved) PSMCON.0 PSM powerdown control (1=on / 0=off)					
DMAP, DMAH, DMAL DMA address pointer	Stack Pointer					
ADCGAINL ADC Gain calibration coefficients	SPH Stack Pointer High byte					
ADCOFSH ADC Offset	IE Interrupt Enable register #1 enable inturrupts (0=all inturrupts disabled) EADC enable ADCI (ADC interrupt)					
ADCOFSL calibration coefficients	ET2 enable TF2/EXF2 (Timer2 overflow interrupt) ES enable RI/TI (serial port interrupt)					
DACCON.7 DAC Control register	ET1 enable TF1 (Timer1 overflow interrupt) EX1 enable IE1 (external interrupt 1) ET0 enable TF0 (Timer0 overflow interrupt)					
DACCON.5 DAC0 RangeSelect (0=V _{REF} , 1=V _{DD}) DACCON.4 Clear DAC1 (0=0V. 1=normal operation)						
DACCON.3 Clear DAC0 (0=0V, 1=normal operation) DACCON.2 SynchronousUpdate (1=asynchronous) DACCON.1 PowerDown DAC1 (0=off, 1=on)	EIP2.6 priority of TII interrupt (time interval) priority of PSMI interrupt (power supply monitor)					
DACCON.0 PowerDown DAC0 (0=off, 1=on) DAC1H,DAC1L DAC1 data registers	IEIP2.4 priority of ISPI interrupt (serial interface) (IEIP2.3 (this bit must contain zero) (IEIP2.2 enable TII interrupt (time interval)					
DAC0H,DAC0L DAC0 data registers	IEIP2.1 enable PSMI (power supply monitor interrupt) IEIP2.0 enable ISPI interrupt (serial interface)					
PLLCON PLL Control register PLLCON.7 oscillator powerdown control bit (0=XTAL on)						
PLLCON.6 PLL lock indicator flag (0=out of lock) PLLCON.5 (this bit must contain zero)						
	PS priority of RI/TI (serial port interrupt) PT1 priority of IET (Timer1 overflow interrupt) PX1 priority of IET (external interrupt 1)					
PLLCON.1 f _{CORE} = 16,777,216Hz / 2 ^{CD}	PT0 priority of TF0 (Timer0 overflow interrupt) PX0 priority of IE0 (external interrupt 0) TMOD Timer Mode register					
TIMECON Time Interval Counter Control Register	TMOD.3/.7 gate control bit (0=ignore INTx) TMOD.2/.6 counter/limer select bit (0=timer)					
TIMECON.5 INTVAL timebase select bits TIMECON.4 [128th sec, seconds, minutes, hours] TIMECON.3 single time interval control bit (0=reload&restart)	TMOD.1/.5 timer mode selecton bits TMOD.0/.4 [13bitT, 16bitT/C, 8bitT/Creload, 2x8bitT] (upper nibble = Timer1, lower nibble = Timer0)					
TIMECON.2 time interval interrupt bit, "TII" TIMECON.1 time interval enable bit (0=disable&clear)	TCON Times Control register					
TIMECON.0 time clock enable bit (0≖disable) INTVAL TIC Interval Register	TF1 Timer1 overflow flag (auto cleared on vector to ISR) TR1 Timer1 run control (0=off, 1=run)					
HTHSEC TIC Elapsed 128th Second Register	Timer overflow flag (auto cleared on vector to ISR) Timer 1 cur control (bed. in-cur) Timer 1 cur					
TIC Elapsed Seconds Register TIC Elapsed Minutes Register	IT1 IE1 type (0=level trig, 1=edge trig) IE0 external INT0 flag (auto cleared on vector to ISR) IT0 IE0 type (0=level trig, 1=edge trig)					
HOUR TIC Elapsed Hours Register	TH0,TL0 Timer0 registers					
Data Flash/EE comand register 01h READ page 82h PROGRAM byte	TH1,TL1 Timer1 registers					
01h READ page 82h PROGRAM byte 02h PROGRAM page 0Fh EXIT ULOAD mode 04h VERIFY page F0h ENTER ULOAD mode 05h ERASE page (all others reserved) 06h ERASE ALL	T2CON Timer2 Control register TF2 overflow flag EXF2 external flag					
EADRH, EADRL Data Flash/EE address registers	EXF2 external flag RCLK receive clock enable (0=Timer1 used for RxD clk) TCLK transmit clock enable (0=Timer1 used for TxD clk) EXEN2 external enable (0=ignore T2EX, 1=cap/rid on T2EX)					
EDATA1,EDATA2,EDATA3,EDATA4						
Data Flash/EE data registers SPICON SPI Control register	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capture/reload select (0=reload, 1=capture) TH2,TL2 Timer2 register					
SPICON SPI Control register SPI SPI inturrupt (set at end of SPI transfer) WCOL write collision error flag SPE SPI enable (0= 2C enable, 1=SPI enable)	RCAP2H,RCAP2L Timer2 Reload/Capture					
SPE SPI enable (0=I2C enable, 1=SPI enable) SPIM master mode select (0=slave) CPOL clock polarity select (0=SCLK idles low)	P0 Port0 register (also A0-A7 & D0-D7)					
CPHA clock phase select (0=leading edge latch) SPR1 SPI bitrate select bits	P1 Port1 register (analog & digital inputs) T2EX timer/counter 2 capture/reload trigger					
SPR0 bitrate = Fcore / [2,4,8,16] (slave: SPR0=SS) SPIDAT SPI Data register	T2 timer/counter 2 external input P2 Port2 register (also A8-A15 & A16-A23)					
I2CCON I2C Control register (in slave mode)	P3 Port3 register					
I2CSI	RD external data memory read strobe WR external data memory write strobe T1 timer/counter 1 external input					
	T0 timer/counter 0 external input INT1 external interrupt 1 INT0 external interrupt 0					
I2CTX transmission direction status (0=RX,1=TX) I2CI serial interface interrupt	TxD serial port transmit data line RxD serial port receive data line					
I2CCON I2C Control register (in master mode) MDO master mode SDATA output bit	SCON Serial communications Control register SM0 UART mode control bits baud rate:					
MDE master mode SDATA output enable (0=disable) MCO master mode SCLK output bit MDI master mode SDATA input bit	SM1 00 - 8bit shift register - Fosc/12 01 - 8bit UART - variable 10 - 9bit UART - Fosc/64(x2) 11 - 9bit UART - variable					
I2CM master mode select bit (0=slave mode) I2CADD I2C slave Address register	SM2 in modes 2&3, enables multiprocessor communication receive enable control bit TB8 in modes 2&3, 9th bit transmitted					
I2CADD1,I2CADD2,I2CADD3						
I2C secondary slave Address registers I2CDAT I2C Data register	TI transmit interrupt flag RI receive interrupt flag					
PWMCON PWM Control register	SBUF Serial port Buffer register PCON Power Control register					
PWMCON.6 PWM mode bits [0=disabled, 1=single/var.res.,	PCON 7 double baud rate control					
PWMCON.5 2=twin/8bit, 3=twin/16bit, 4=dual/16bitNRZ, PWMCON.4 5=dual/8bit, 6=dual/16bitRZ, 7=(reserved)] PWMCON.3 PWM clock divide bits PWMCON.2 PWM counter = clock / 11.4.16.64	PCON.4 ALE disable (0=normal, 1=forces ALE high) PCON.3 general purpose flag PCON.2 general purpose flag PCON.1 power-down control bit (recoverable with hard reset)					
PWMCON.1 PWM clock source bits [1=F _{XTAL} /15, 2=F _{XTAL} , PWMCON.0 3=T0 ext.int.rate, 4=F _{VCO} (16.777MHz)]	PCON.1 jober-down control on it (recoverable with nard reset) PCON.0 idle-mode control (recoverable with enabled interrupt) PSW Program Status Word					
PWM0H,PWM0L PWM0 data registers	CY carry flag					
PWM1H,PWM1L PWM1 data registers DPCON Data Pointer Control register	F0 general purpose flag 0 RS1 register bank select control bits					
	RS0 active register bank = [0,1,2,3] OV overflow flag F1 general purpose flag 1					
DPCON.4 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl] DPCON.3 main data pointer mode control bits	P parity of ACC DPP Data Pointer Page					
DECON.O data politici select [0=Itialit, 1=Stradow]	DPH,DPL (DPTR) Data Pointer					
T3CON Timer 3 Control register T3CON Timer 3 haud rate enable (fludisable)	ACC Accumulator					
T3CON.2 binary divide factor (DIV) T3CON.1 DIV = log[F _{CORE} /(32 baudrate)] / log2	B auxiliary math register					
T3CON.0 (rounded down)	ED CORE OPTIMIZED COL					