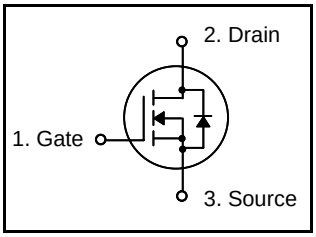
Pb Free Plating Product

P75NF75

75V,80A Heatsink Planar N-Channel Power MOSFETs

FEATURES

* $R_{DS(ON)}$ = 9.5mΩ @V_{GS} = 10 V(Typical)
* Ultra low gate charge (typical 117 nC)
* Fast switching capability
* Low reverse transfer Capacitance (C_{RSS}= typical 240 pF)
* Avalanche energy Specified
* Improved dv/dt capability, high ruggedness



BV_{DSS} = 75V

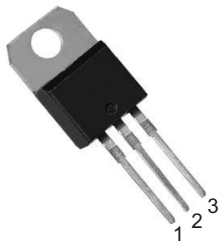
$R_{DS(ON)}$ = 0.011 ohm

I_D = 80A

General Description

This N-channel enhancement mode field-effect power transistor using THINKI Semiconductor advanced planar stripe, DMOS technology intended for off-line switch mode power supply.
Also, especially designed to minimize rds(on) and high rugged avalanche characteristics. The TO-220M-SQ pkg is well suited for adaptor power units,amplifiers,inverters and SMPS application.

TO-220M-SQ



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	75	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	80	A
Pulsed Drain Current (Note 2)		I_{DM}	320	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	700	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	12	V/ns
Power Dissipation	TO-220/TO-263	P_D	300	W
	TO-220F		45	W
Junction Temperature		T_J	+175	°C
Storage Temperature		T_{STG}	-55 ~ +175	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by safe operating area
3. Starting T_J=25°C, I_D=40A, V_{DD}=37.5V
4. I_{SD}≤80A, di/dt≤300A/μs, V_{DD}≤BV_{DSS}, T_J≤T_{JMAX}

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-263	θ_{JA}	62.5	°C /W
	TO-220F		62.5	°C /W
Junction to Case	TO-220/TO-263	θ_{JC}	0.5	°C /W
	TO-220F		3.33	°C /W

■ ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise specified)

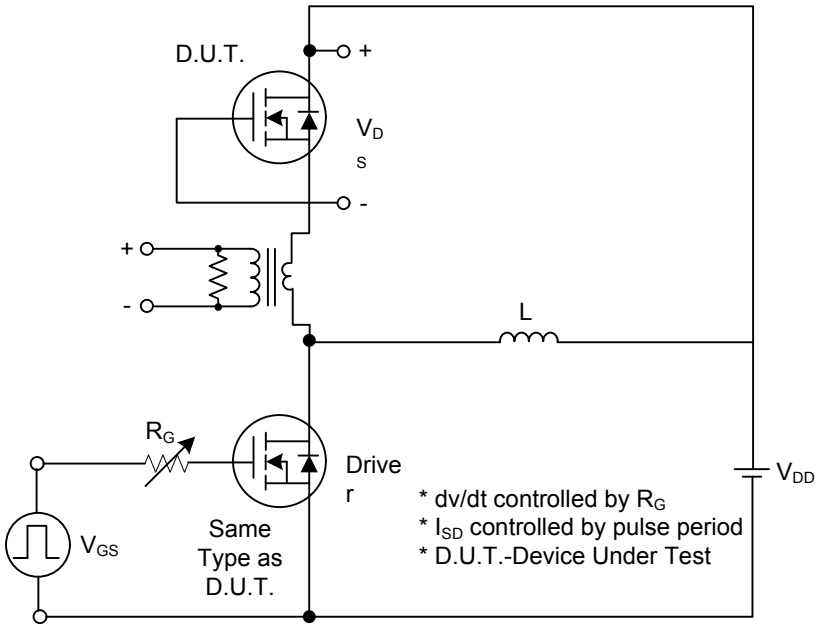
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	75			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS} = 20V, V_{DS} = 0 V			100	nA
	Reverse		V_{GS} = -20V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 40 A		9.5	11	mΩ
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{GS} = 0 V, V_{DS} = 25 V f = 1MHz		3700		pF
Output Capacitance		C_{OSS}			730		pF
Reverse Transfer Capacitance		C_{RSS}			240		pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD} = 37.5V, I_D =45A, V_{GS}=10V, R_G=4.7Ω		25		ns
Turn-On Rise Time		t_R			100		ns
Turn-Off Delay Time		$t_{D(OFF)}$			66		ns
Turn-Off Fall Time		t_F			30		ns
Total Gate Charge		Q_G	V_{DS} = 60V, V_{GS} = 10 V I_D = 80A		117	160	nC
Gate-Source Charge		Q_{GS}			27		nC
Gate-Drain Charge		Q_{GD}			47		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

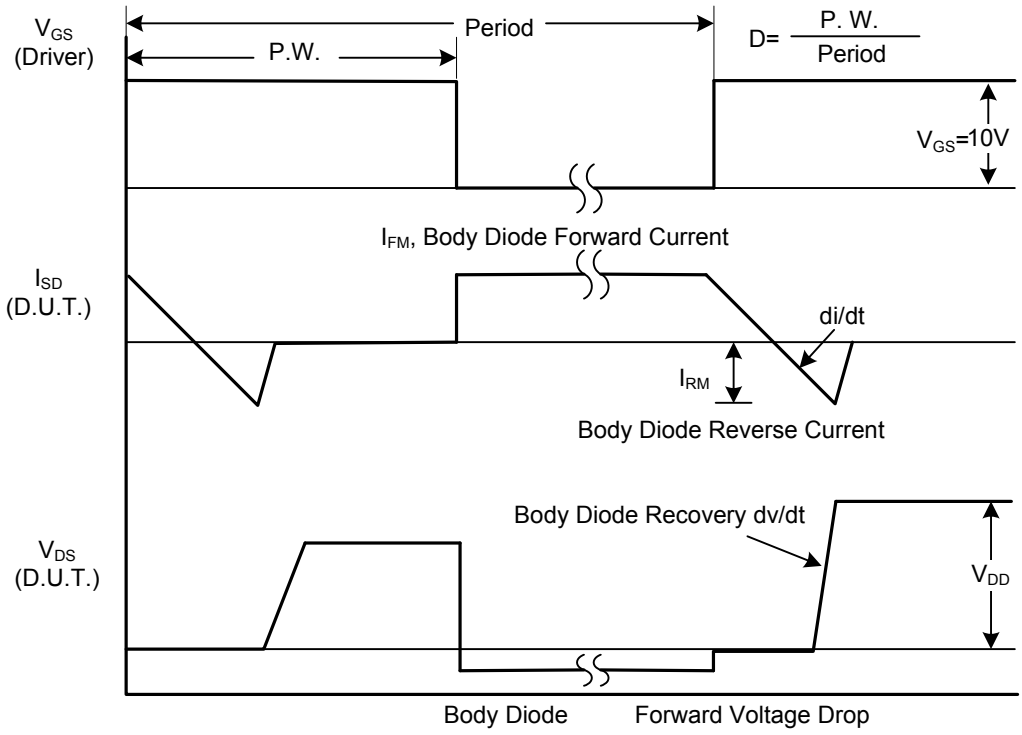
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage (Note 2)	V_{SD}	V_{GS} = 0 V, I_S = 80A			1.5	V
Continuous Source Current	I_S				80	A
Pulsed Source Current (Note 1)	I_{SM}				320	A
Reverse Recovery Time	t_{RR}	I_S = 80A, V_{DD} = 25 V dI_F / dt = 100 A/μs		132		ns
Reverse Recovery Charge	Q_{RR}			660		μC

Note: 1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%

■ TEST CIRCUITS AND WAVEFORMS

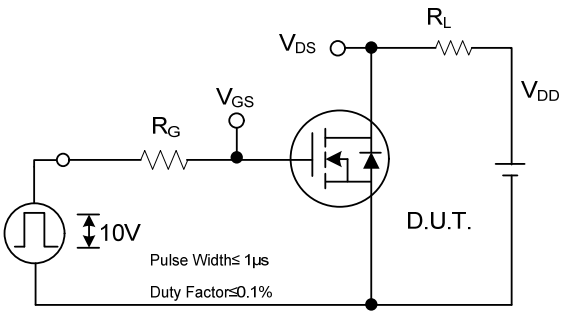


1A Peak Diode Recovery dv/dt Test Circuit

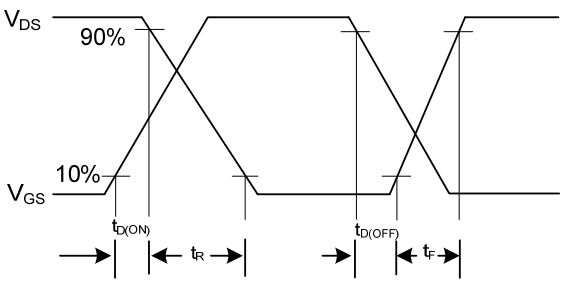


1B Peak Diode Recovery dv/dt Waveforms

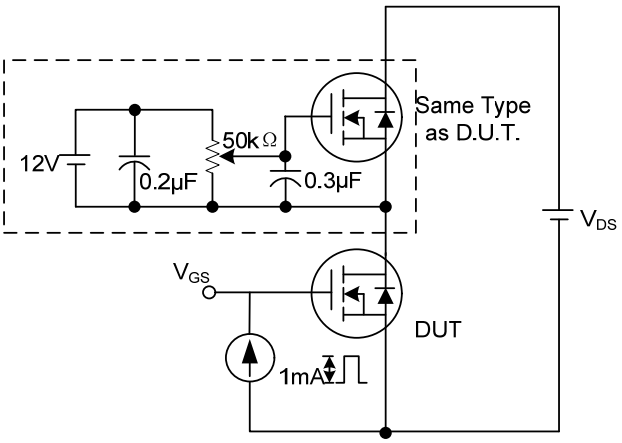
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



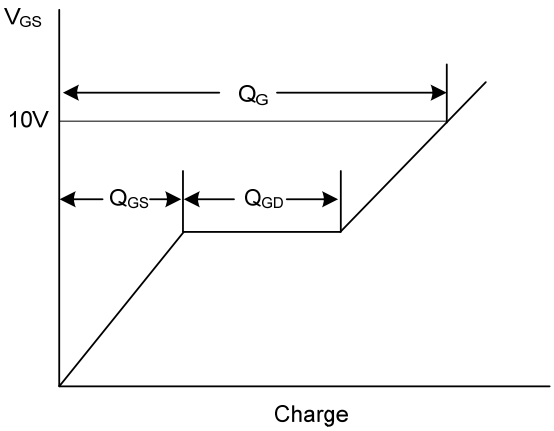
2A Switching Test Circuit



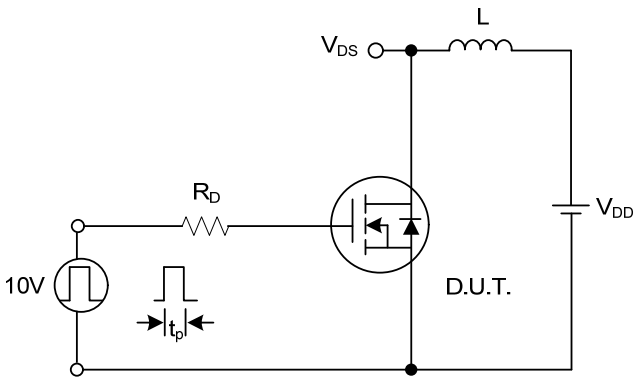
2B Switching Waveforms



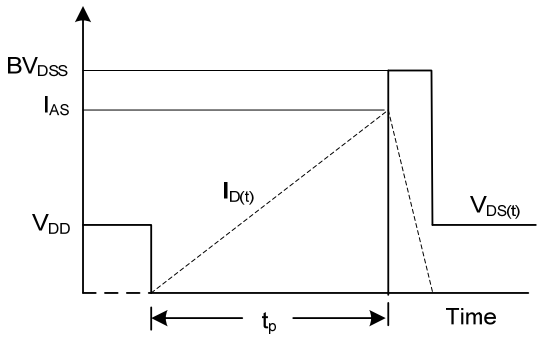
3A Gate Charge Test Circuit



3B Gate Charge Waveform



4A Unclamped Inductive Switching Test Circuit



4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS