



1. Description

1.1. Project

Project Name	Run_Fire
Board Name	NUCLEO-F746ZG
Generated with:	STM32CubeMX 6.3.0
Date	09/28/2021

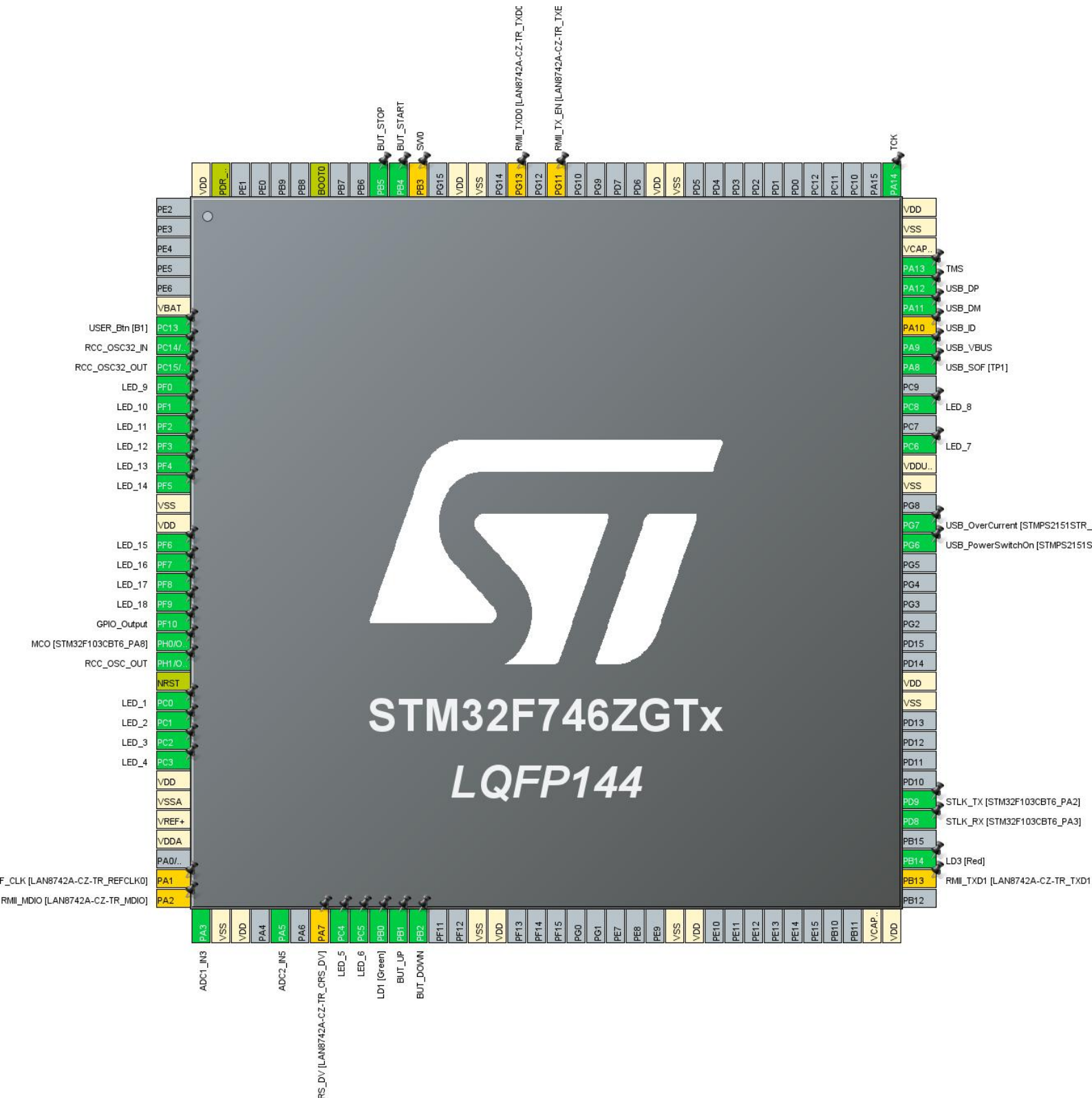
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Output	LED_9
11	PF1 *	I/O	GPIO_Output	LED_10
12	PF2 *	I/O	GPIO_Output	LED_11
13	PF3 *	I/O	GPIO_Output	LED_12
14	PF4 *	I/O	GPIO_Output	LED_13
15	PF5 *	I/O	GPIO_Output	LED_14
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	LED_15
19	PF7 *	I/O	GPIO_Output	LED_16
20	PF8 *	I/O	GPIO_Output	LED_17
21	PF9 *	I/O	GPIO_Output	LED_18
22	PF10 *	I/O	GPIO_Output	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	LED_1
27	PC1 *	I/O	GPIO_Output	LED_2
28	PC2 *	I/O	GPIO_Output	LED_3
29	PC3 *	I/O	GPIO_Output	LED_4
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1 **	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
36	PA2 **	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ- TR_MDIO]
37	PA3	I/O	ADC1_IN3	
38	VSS	Power		

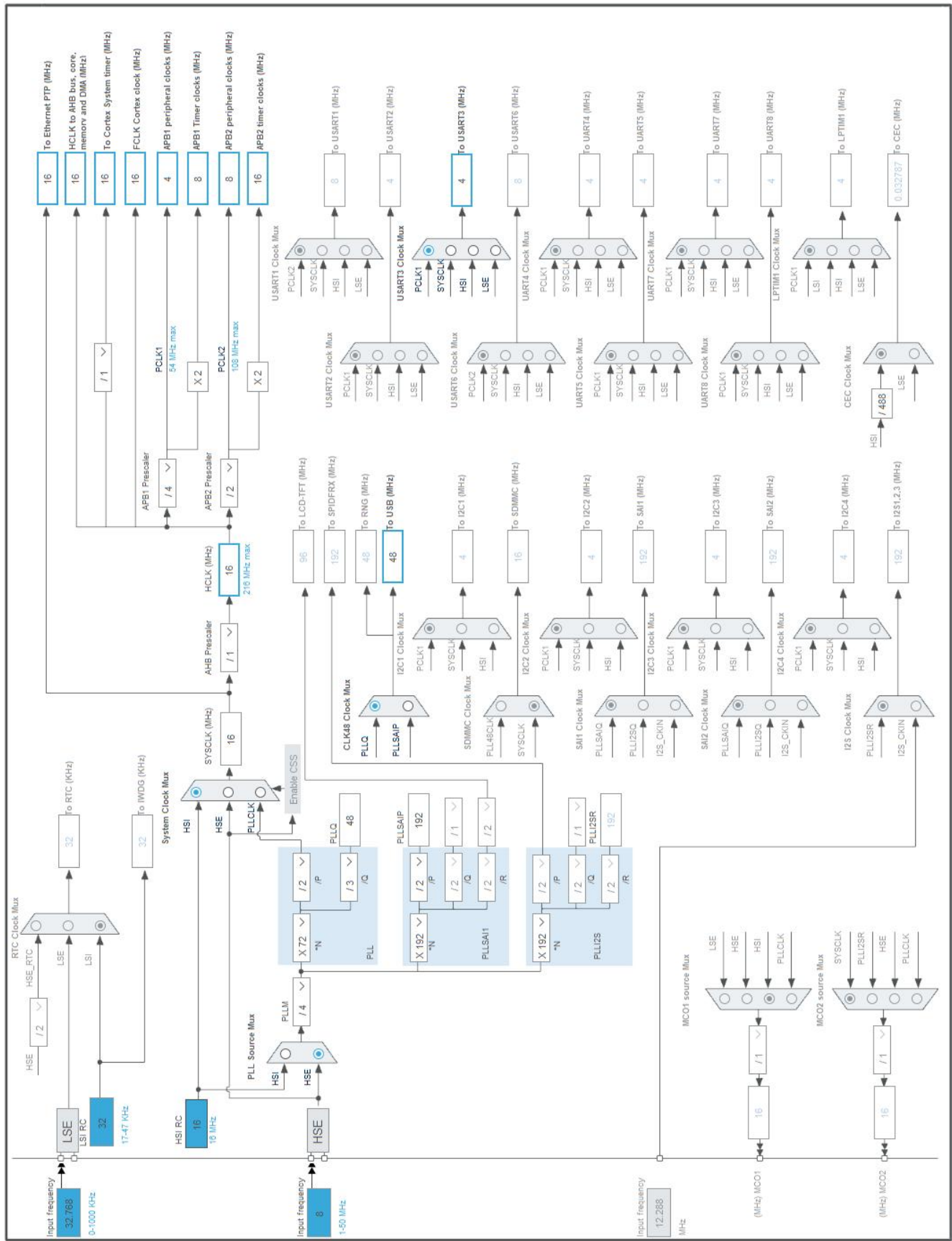
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	VDD	Power		
41	PA5	I/O	ADC2_IN5	
43	PA7 **	I/O	ETH_CRSDV	RMII_CRSDV [LAN8742A- CZ-TR_CRSDV]
44	PC4 *	I/O	GPIO_Output	LED_5
45	PC5 *	I/O	GPIO_Output	LED_6
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
47	PB1 *	I/O	GPIO_Input	BUT_UP
48	PB2 *	I/O	GPIO_Input	BUT_DOWN
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
74	PB13 **	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ- TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMP2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMP2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
96	PC6 *	I/O	GPIO_Output	LED_7
98	PC8 *	I/O	GPIO_Output	LED_8
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
120	VSS	Power		
121	VDD	Power		
126	PG11 **	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]
128	PG13 **	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ- TR_TXD0]
130	VSS	Power		
131	VDD	Power		
133	PB3 **	I/O	SYS_JTDO-SWO	SW0
134	PB4 *	I/O	GPIO_Input	BUT_START
135	PB5 *	I/O	GPIO_Input	BUT_STOP
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Run_Fire
Project Folder	F:\RUNNING_FIRE\Run_Fire
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x2000
Minimum Stack Size	0x4000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_USART3_UART_Init	USART3
5	MX_TIM7_Init	TIM7
6	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
7	MX_ADC2_Init	ADC2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	DS10916_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

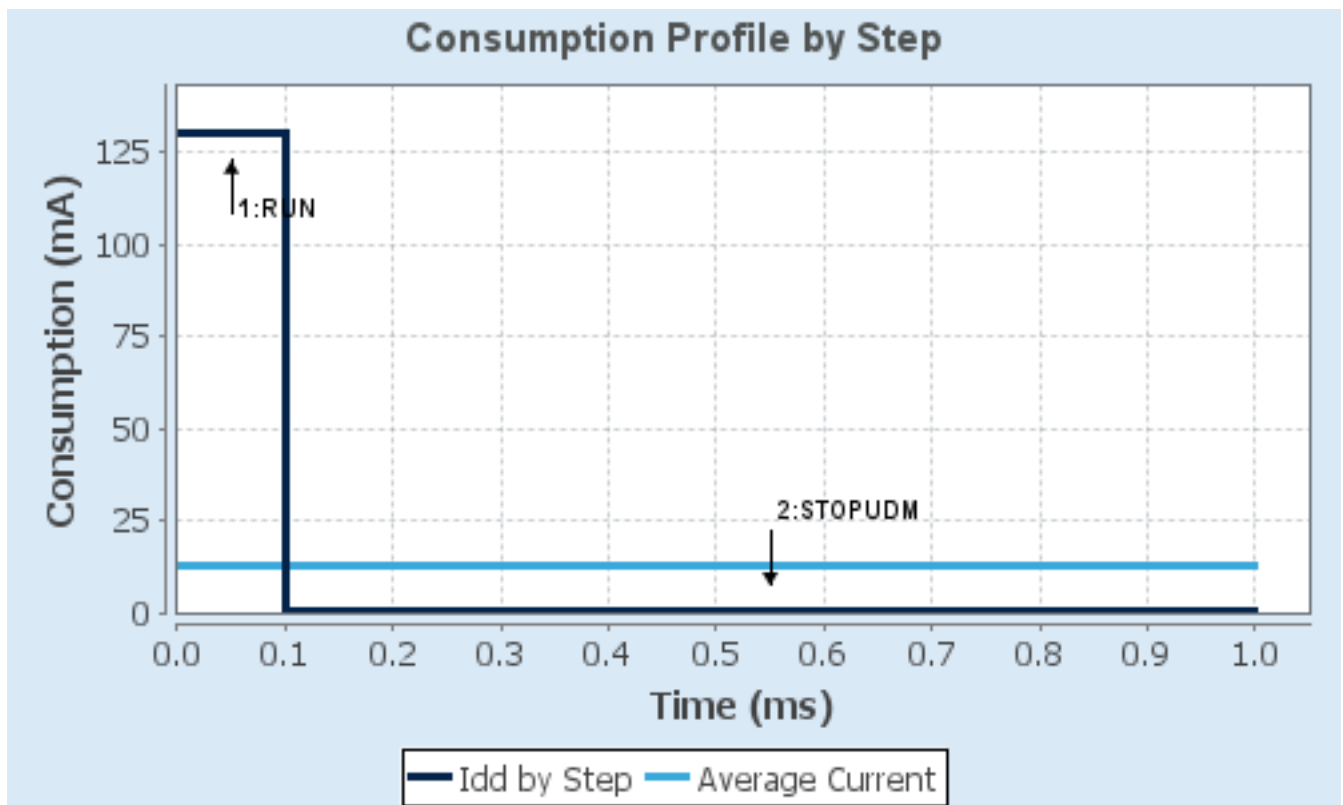
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	87.84	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN3

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 3

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. ADC2

mode: IN5

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode	Disabled
Continuous Conversion Mode	Enabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : BYPASS Clock Source

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

7.4. SYS

Debug: Serial Wire

Timebase Source: TIM11

7.5. TIM7

mode: Activated

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	15 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1999 *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.6. USART3

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. USB_OTG_FS

Mode: Device_Only

mode: Activate_VBUS

mode: Activate_SOF

7.7.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

7.8. FREERTOS

Interface: CMSIS_V2

7.8.1. Config parameters:

API:

FreeRTOS API	CMSIS v2
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Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled

ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.8.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled

vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.8.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA5	ADC2_IN5	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_TX [STM32F103CBT6_PA2]
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DP
Single Mapped Signals	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PA10	USB_OTG_FS_I	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_ID

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		D			*	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SW0
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_9
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_10
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_11
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_12
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_13
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_14
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_15
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_16
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_17
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_18
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_2
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_3
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_4
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_5
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_6
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PB1	GPIO_Input	Input mode	Pull-up *	n/a	BUT_UP
	PB2	GPIO_Input	Input mode	Pull-up *	n/a	BUT_DOWN
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_7
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_8
	PB4	GPIO_Input	Input mode	Pull-up *	n/a	BUT_START
	PB5	GPIO_Input	Input mode	Pull-up *	n/a	BUT_STOP

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC global interrupt	true	5	0
ADC1, ADC2 and ADC3 global interrupts	true	5	0
TIM1 trigger and commutation interrupts and TIM11 global interrupt	true	15	0
TIM7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
RCC global interrupt	false	true	false
ADC1, ADC2 and ADC3 global interrupts	false	true	true
TIM1 trigger and commutation interrupts and TIM11 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
TIM7 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
FREERTOS						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7	ADC1	TIM7	USART3			
DMA	ADC2		USB_FS			
GPIO						
IVIC						
RCC						
SYS						

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00166116.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00124865.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00145382.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00337702.pdf
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