



FTL

India vs SMI

Hugo

03/11/2021

A large, detailed photograph of an industrial factory interior, showing complex machinery, pipes, and structural elements. The image is partially obscured by a blue diagonal shape that frames the text on the left and bottom.

**INDUSTRIAL
ONLY**

Overview

■ Architecture of India

■ FTL Schema

- Logical address & Physical address
- Table Recovery
 - Invert record
- Swap Data
 - Garbage Collect, Wear Leveling, over ECC / bad block...
- Performance
 - overlap
 - Memoization

■ SMI vs India

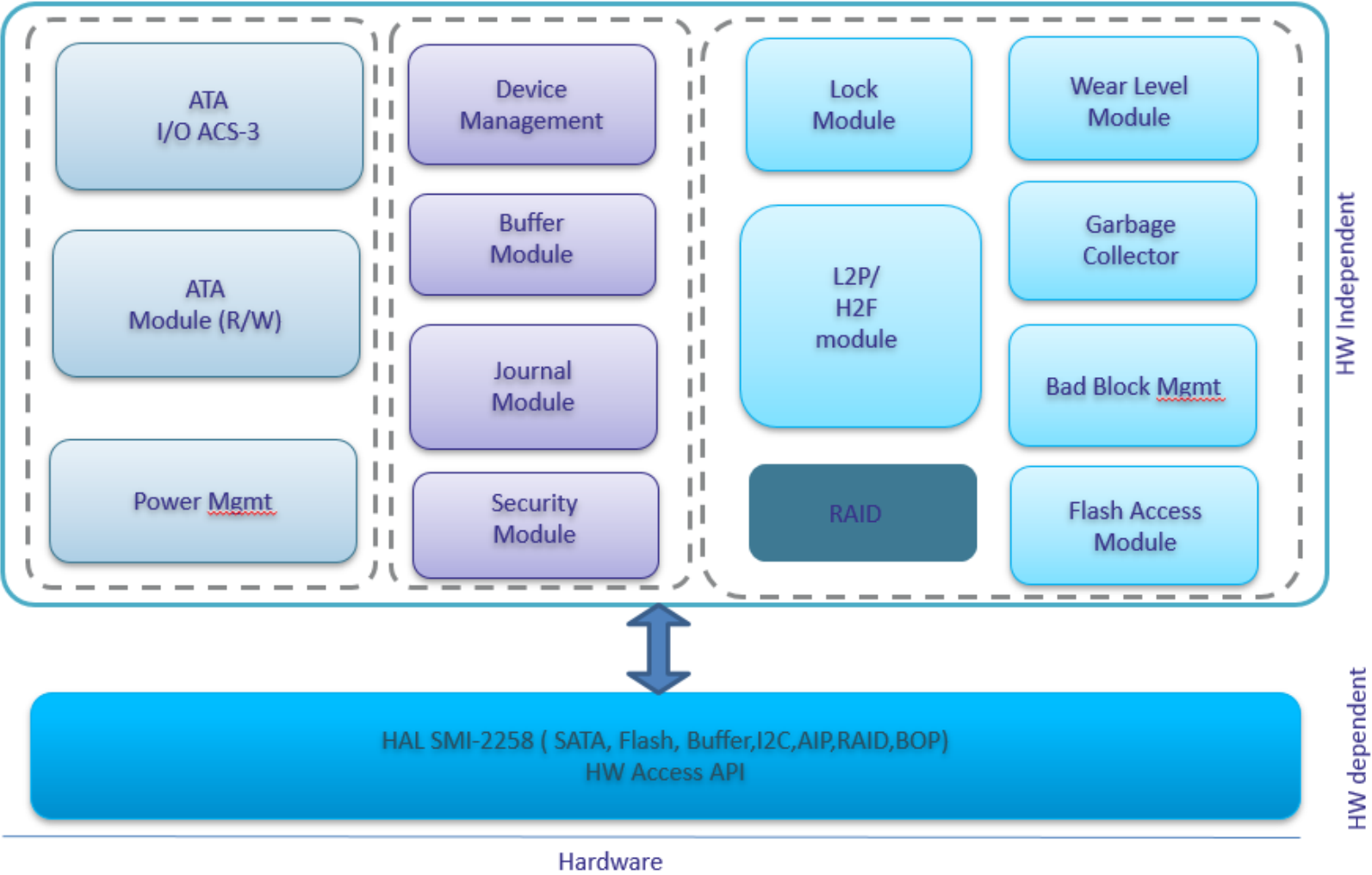
- L2P Table entry format
- Block management
- Invert table
- Table write flow
- Data flow
 - Host In
 - Swap data

■ Discuss (Q & A)

Architecture of India



Architecture of India



FTL Schema



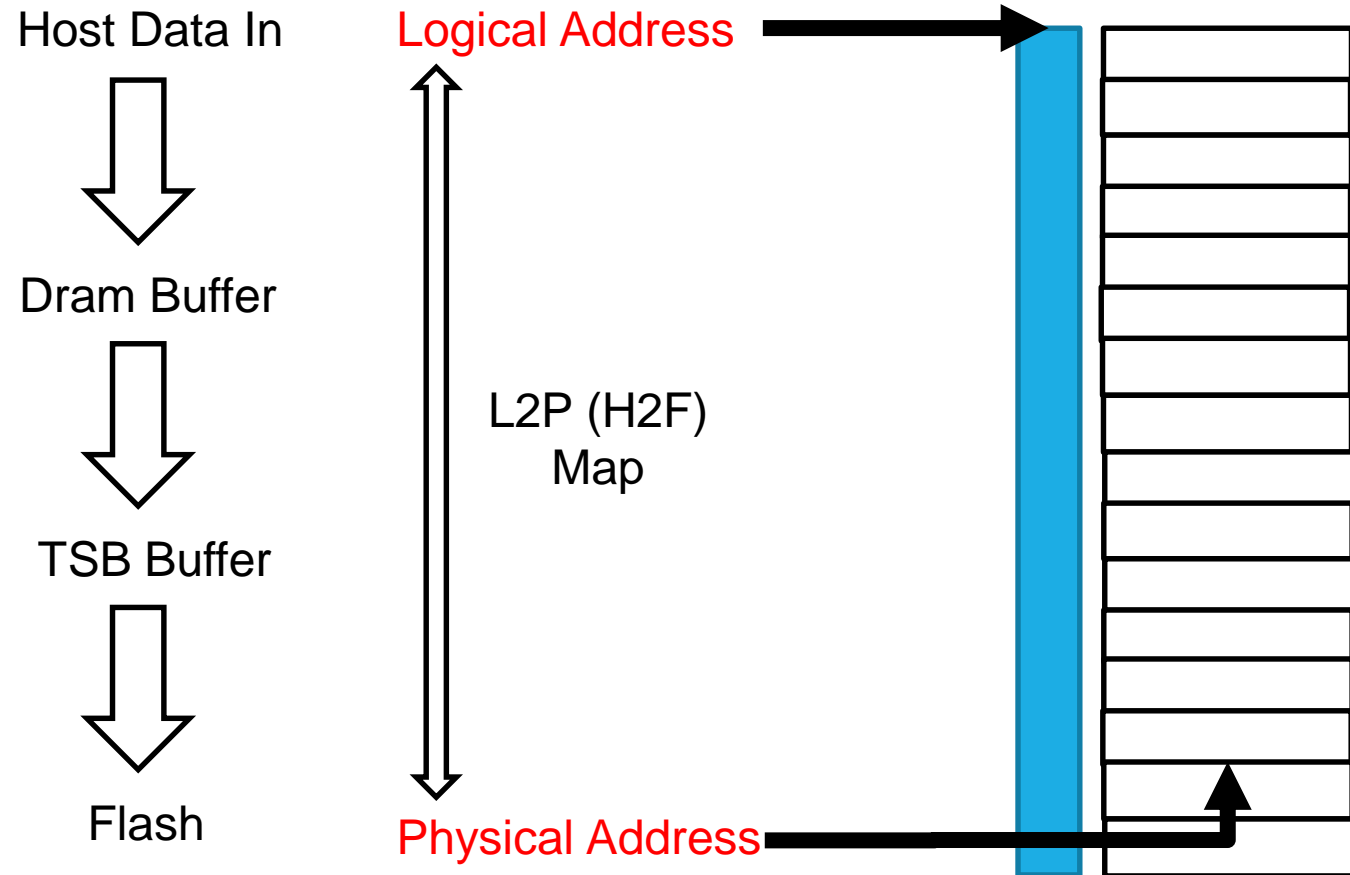
LBA Management (1)

■ Logical Address

- Host In address
- H2F
- L2P

■ Physical Address

- Flash Address
- H2F
- L2P



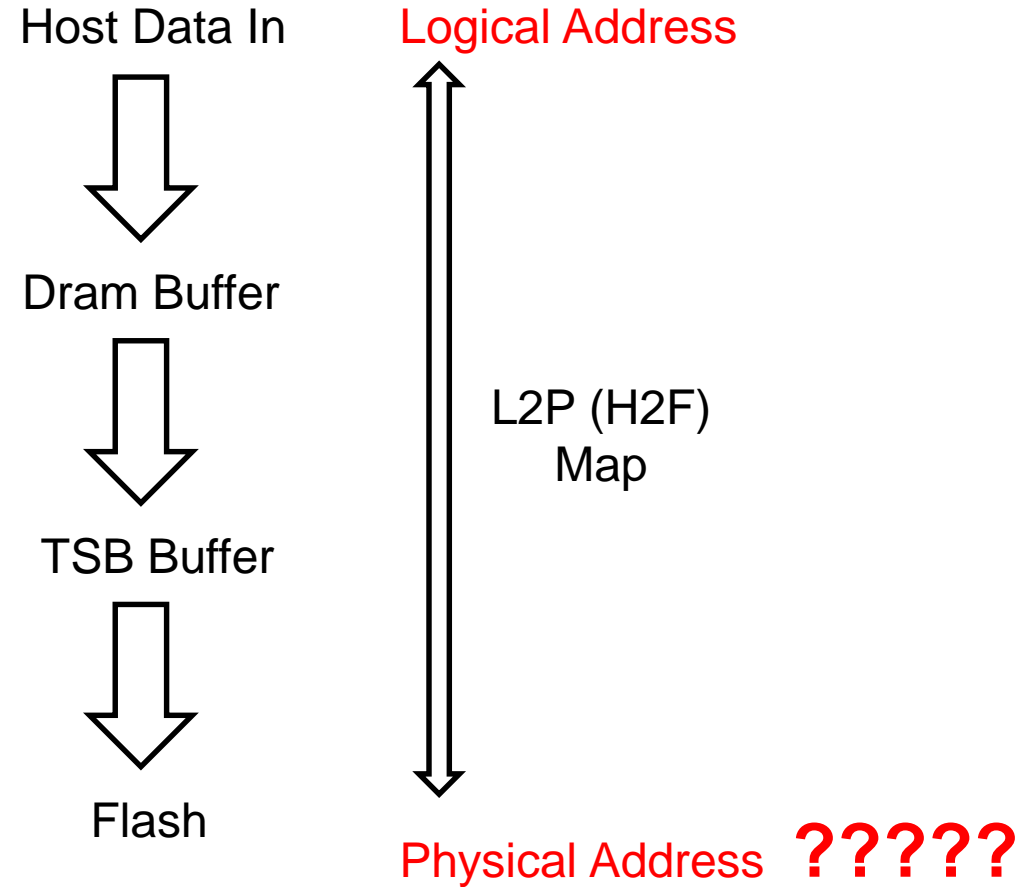
LBA Management (1)

■ Logical Address

- ☐ Host In address
- ☐ H2F
- ☐ L2P

■ Physical Address

- ☐ Flash Address
- ☐ H2F
- ☐ L2P



LBA Management (2)

■ Middle Address

- For Firmware Management
- Replacement
- Super block

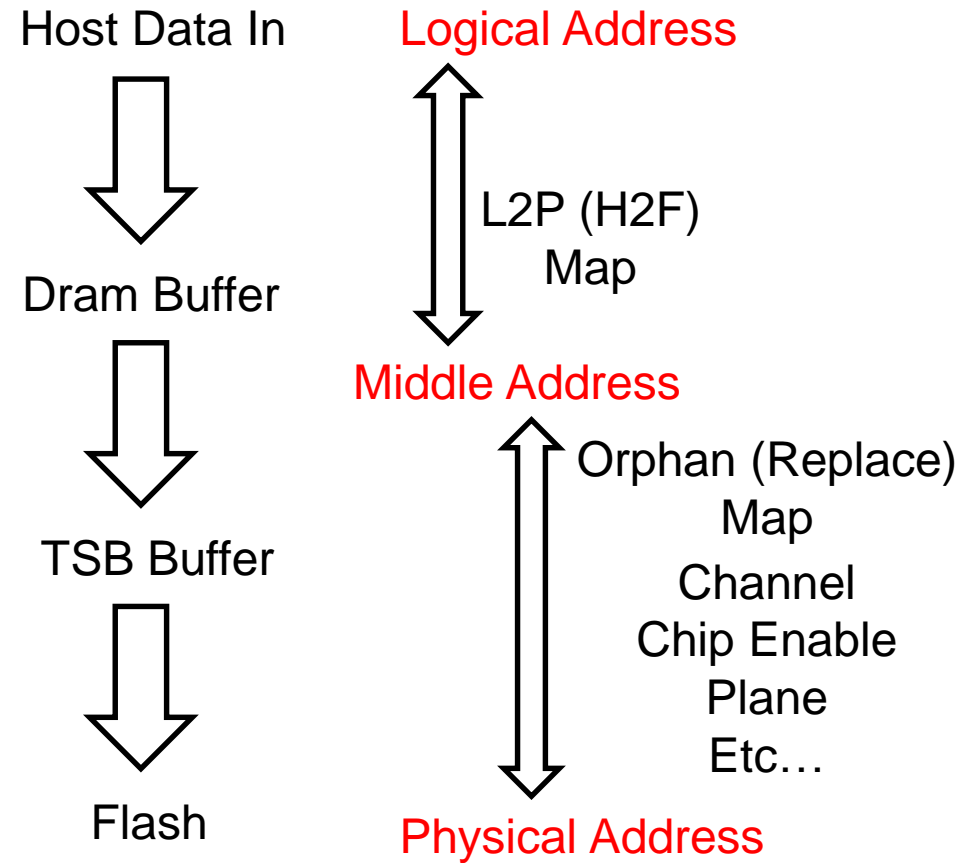


Table Recovery

■ Invert information

- Meta data
- Sequence Number
 - block
 - host in
- Finished tag
 - Used or unused
 - As T4 tag (Write Start/Stop)

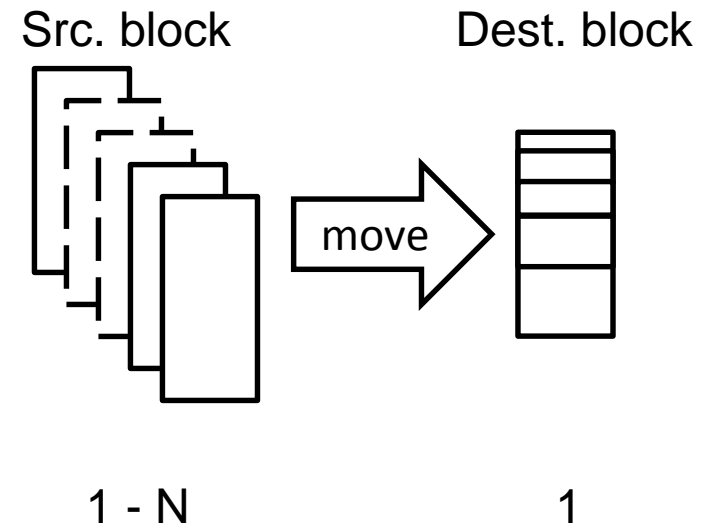
Data Swap

■ Source Blocks : Destination Blocks

□ 1-N : 1

■ Overhead

- Valid judgment
- data move
- flash active time
- extra work
 - Table adjust



Performance

■ Overlap (Synchronize)

- ☐ DMA
- ☐ Multi-core
- ☐ Multi channel
- ☐ Multi CE
- ☐ Ping pong
- ☐ Pipeline

■ Memoization

- ☐ Buffer
- ☐ F2H
- ☐ valid table

SMI vs India



L2P Table entry format

■ SMI

Type	Bit 31	Bit 30	Bit 29	Bit 28 – 16 (x)	Bit 15 (x) – 0
Dummy Page		1	1		
DRAM Source	UNC	1	0	Latest Cache Location (B)	Original Cache Location (P)
Flash Source	UNC	0	0	Block Address (B)	Unit Page Address (P)

■ India

Type	Bit 31	Bit 30	Bit29	Bit 28	Bit 27 - 25	Bit 24	Bit 23	Bit 22 - 16	Bit 15 - 14	Bit 13 - 2	Bit 1 - 0
Lock Mode		1	F	Pf_w_idx					Buffer idx		
Entry Mode		0	Channel	target	lun	Plane	Block	Page	Pf		

Middle Address

Block Management (1 SMI)

■ Super block

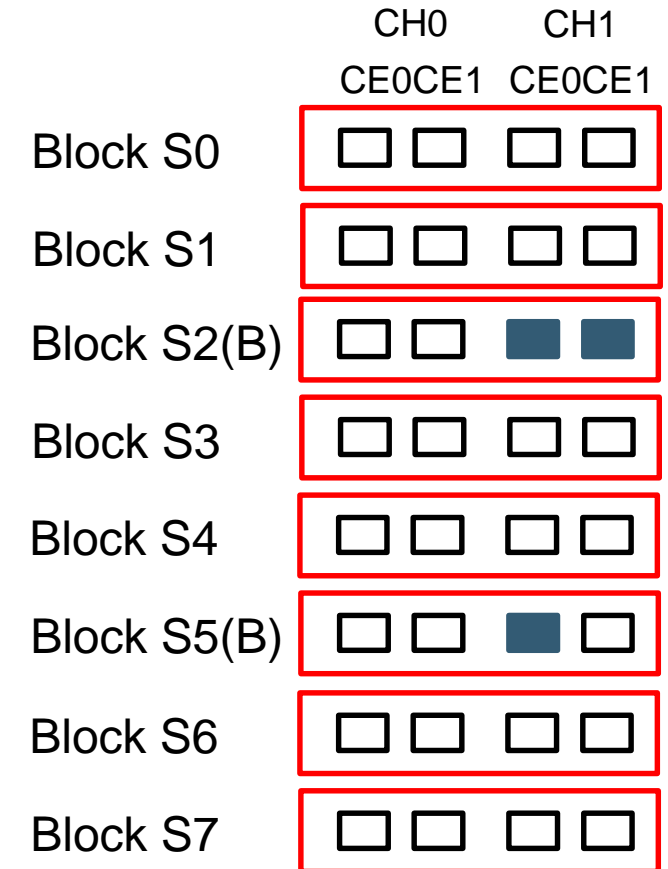
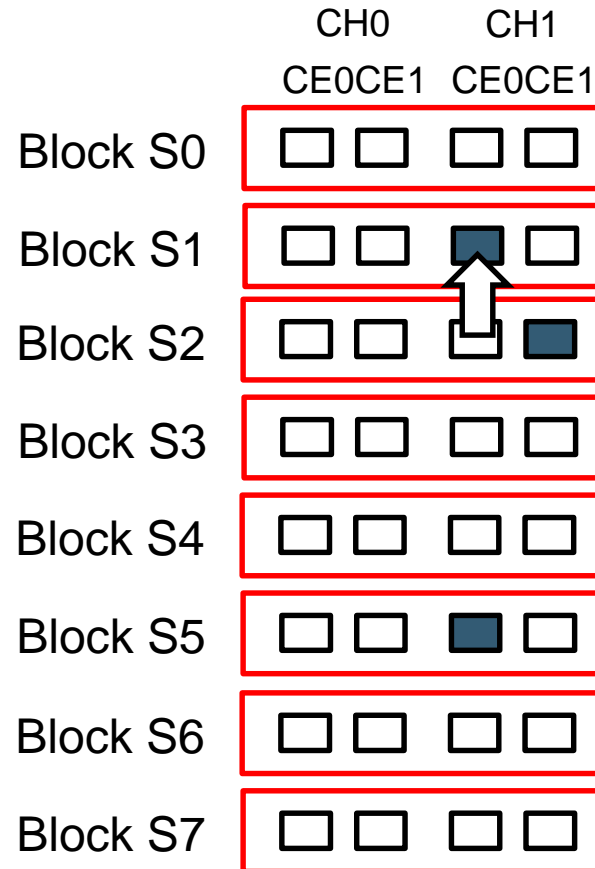
■ Orphan table

□ Plane replace

□ RTBB

● Super block

● Plane



Block Management (2 India)

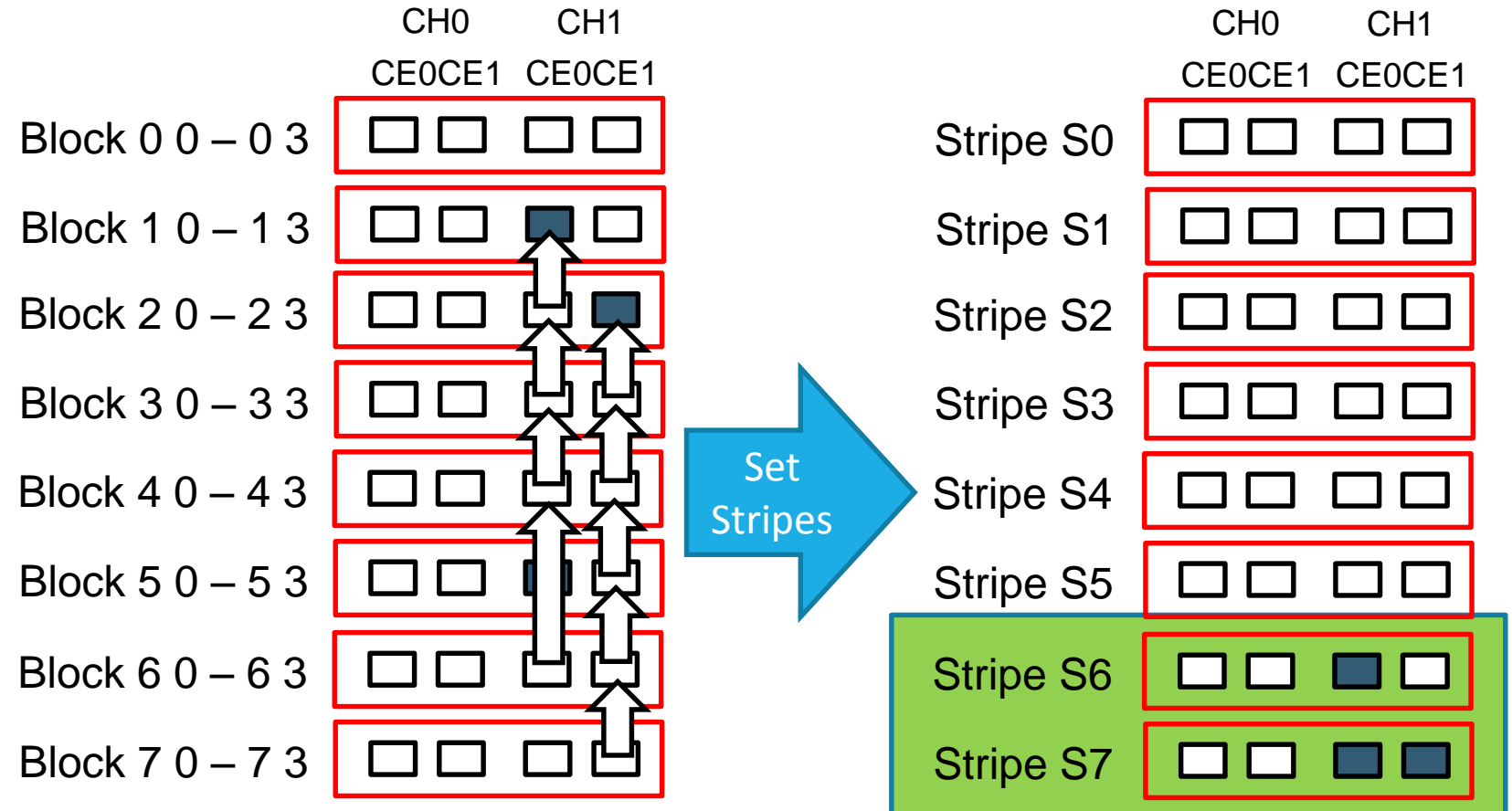
Stripes

□ Journal (Static)

□ Data (Dynamic)

■ No block combination

■ No replacement



Invert Table

■ Meta (Spare data)

□ SMI

- F2H
- EOB

□ India

- Snapshot

	L2P Entry Number	Value (Flash Address)
	4 Bytes	4 Bytes
0	L2P Entry Number	Value (Flash Address)
1	L2P Entry Number	Value (Flash Address)
2	L2P Entry Number	Value (Flash Address)
3	L2P Entry Number	Value (Flash Address)
4	L2P Entry Number	Value (Flash Address)
5	L2P Entry Number	Value (Flash Address)
6	L2P Entry Number	Value (Flash Address)
2047	L2P Entry Number	Value (Flash Address)

Table write flow (1)

■ SMI

□ EOB

- F2H
- Erase count

□ Map

- L2P (H2F): Diff
- G2F

□ Map block Infor

□ Infor Block

- Valid count

□ Index Block

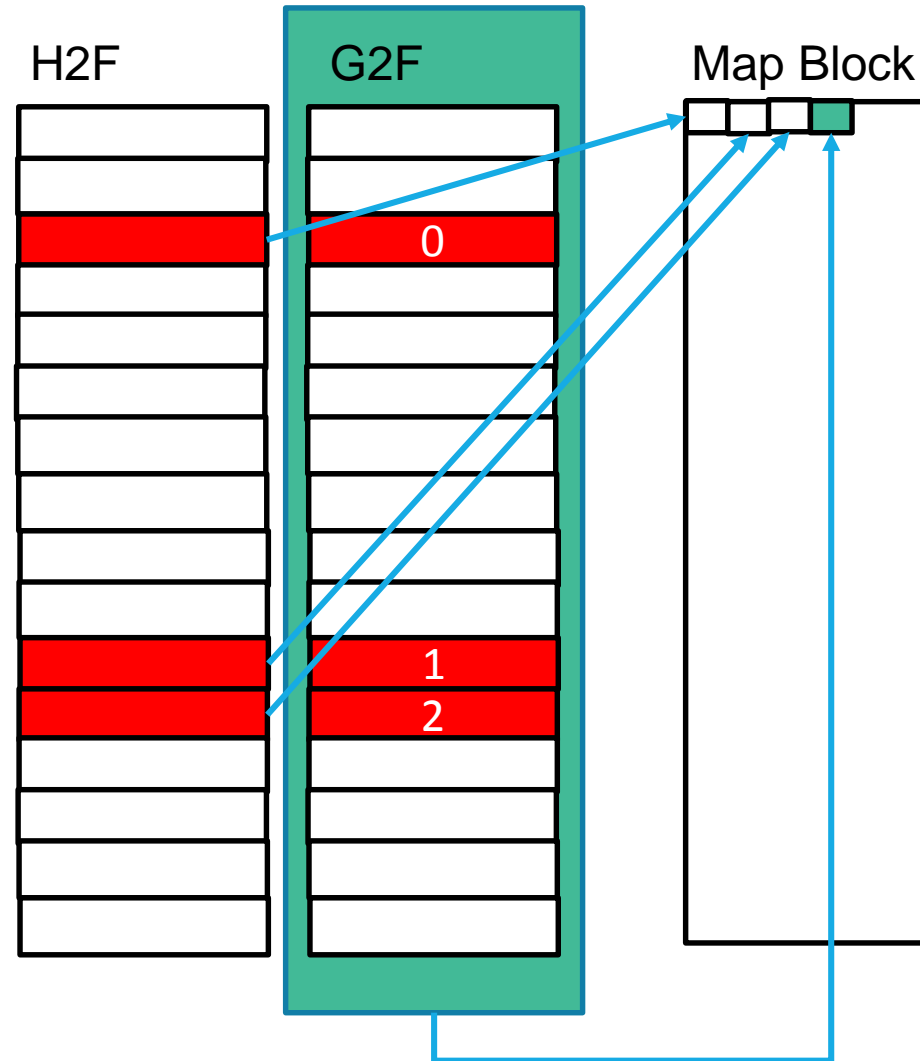


Table write flow (2)

```
typedef enum
{
    SYSTEM_PARAMS=0x0,
    SYSTEM_DATA,
    VDF_DATA,
    L2P_TABLE_DATA,
    L2P_INDIFF_START,
    L2P_ADIFF_START,
    CONFIG_DATA
}snapshot_data_type_e;
```

// Valid data frame bitmap.
 // Logical to physical table.
 // L2P Diff Snaps in base open pogram
 // L2P Difference After Base close update

Journal Module Components

BASE

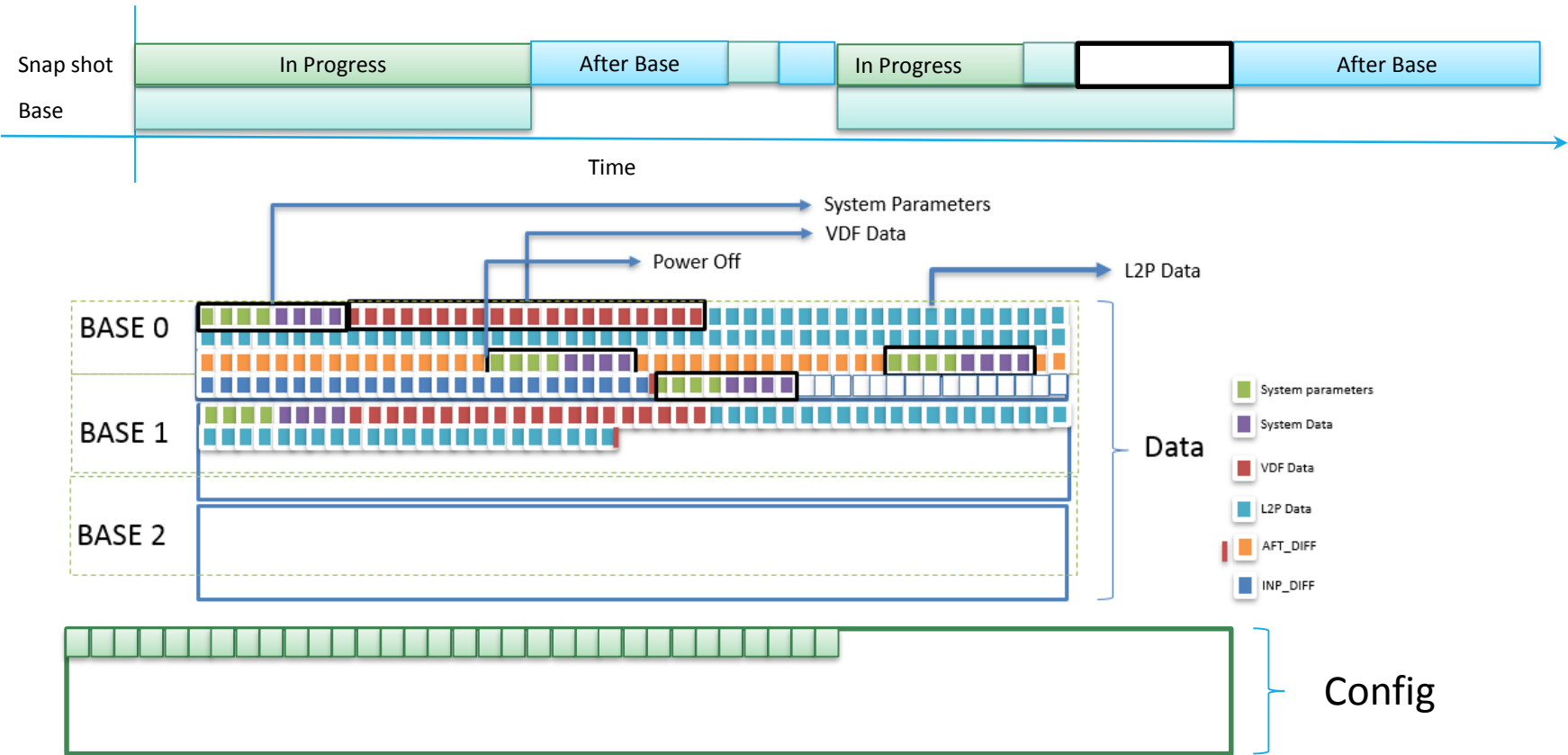
- System Parameters
- System Data
- VDF Data (P)
- L2P Data (P)
- **Partial write**
 - In base open progress

SNAP SHOT

- Base in Progress.
- After Base Write

Config

- Base and Snap info



Write unit

■ Super page (SMI)

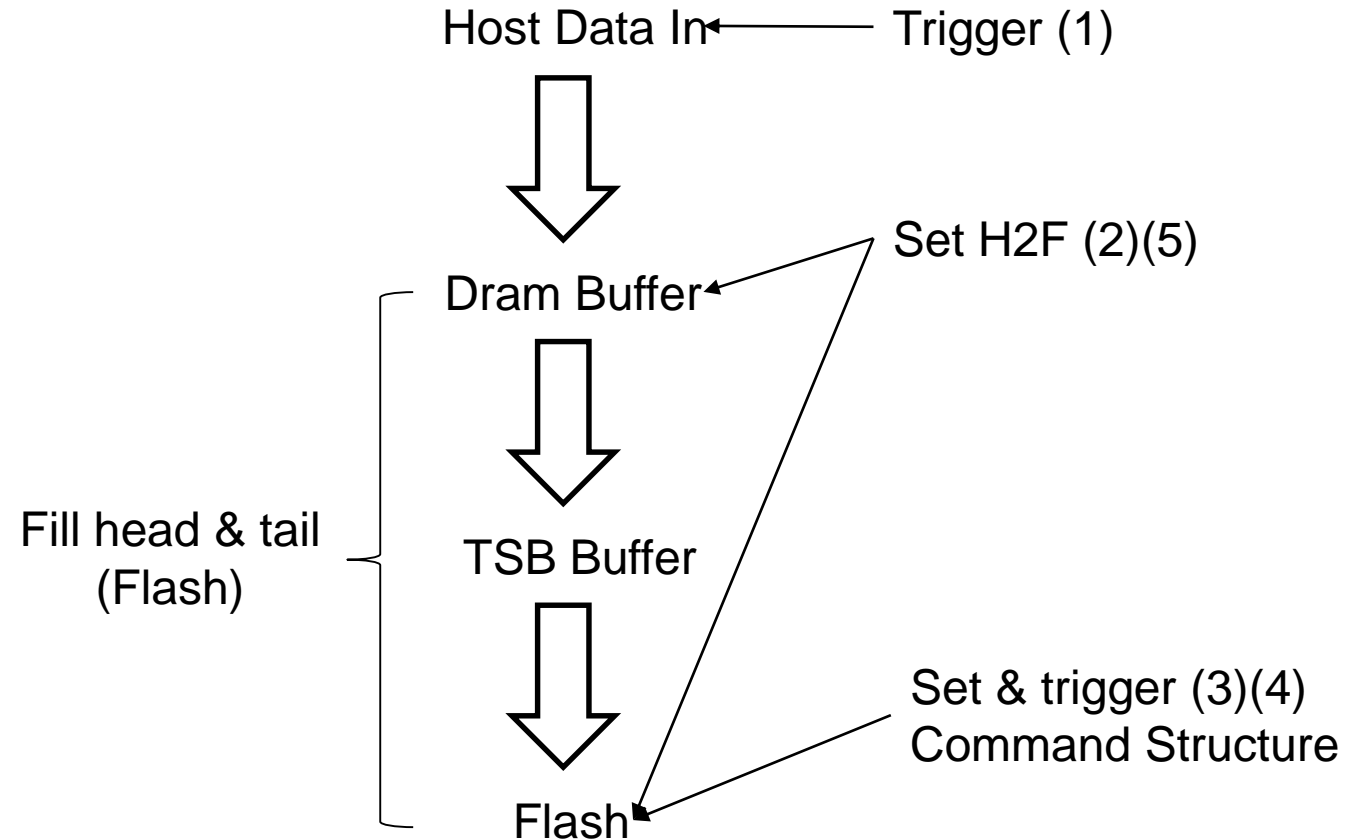
- ☐ > 1.5 super page trigger
 - Length
- ☐ Collect valid unit
- ☐ Write to flash

■ Stripe (India)

- ☐ Equal active target size (SLC/TLC)
 - Valid count
- ☐ Write to flash

Write flow (1)

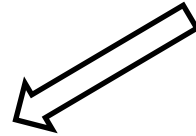
- Trigger to Dram
- Set H2F (DRAM)
- Fill head & tail
 - 4K align
 - Read/Move from source
- Set multi-write command
- Set H2F (Flash)
- Write to flash (flash service)



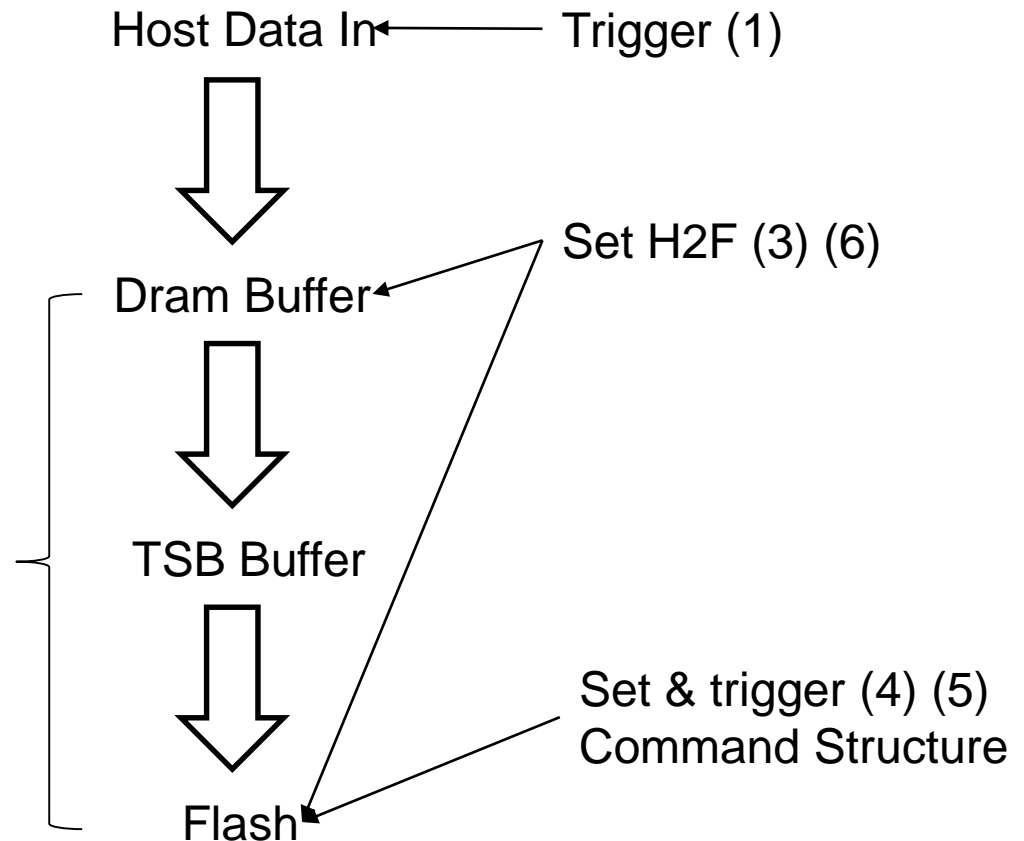
Write flow (2 SMI)

- Trigger to Dram
- Set H2F (DRAM)
- **Fill head & tail**
 - 4K align
 - Read/Move from source
- Set multi-write command
- Set H2F (Flash)
- Write to flash (flash service)

size > 1.5-2.0 super page



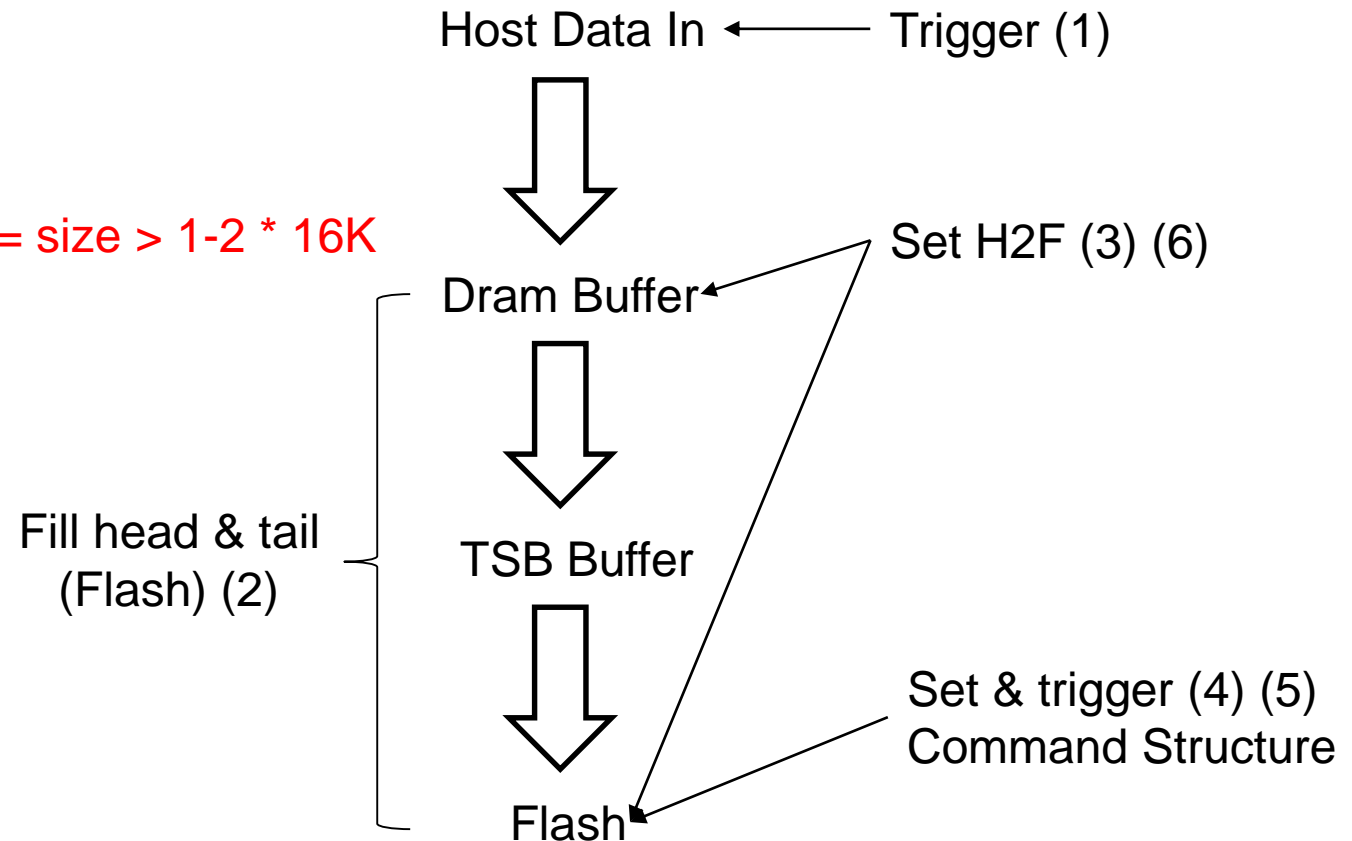
Fill head & tail
(Flash) (2)



Write flow (3 ATP India)

- Trigger to Dram
- Set H2F (DRAM)
- **Fill head & tail**
 - 4K align
 - Read/Move from source
- Set multi-write command
- Set H2F (Flash)
- Write to flash (flash service)

← $2 * \text{Super} \geq \text{size} > 1 - 2 * 16K$



Data Swap (SMI)

■ Each super page write

□ Partial Collect

■ Valid Group

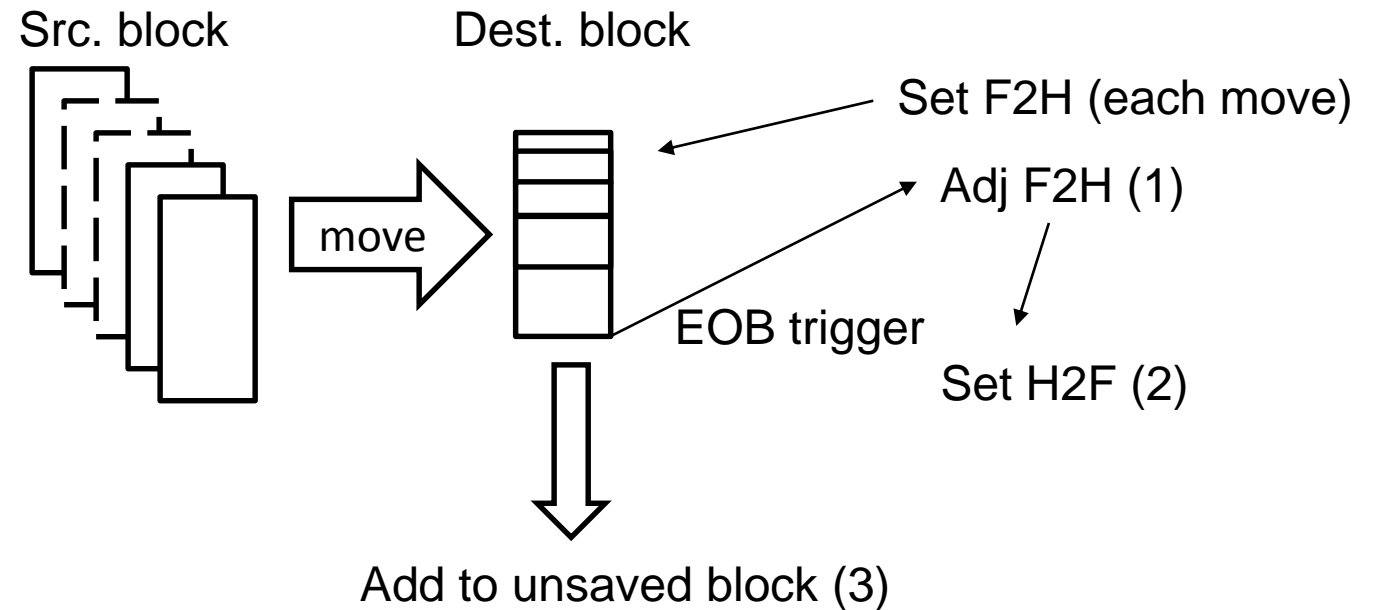
□ F2H => H2F

- F2H ⇔ H2F (valid)
- invalid

□ H2F => F2H

- F2H ⇔ H2F (valid)
- Error

■ GC Finished



Data Swap (India)

■ Each collect write back

□ Host In

□ GC Collect

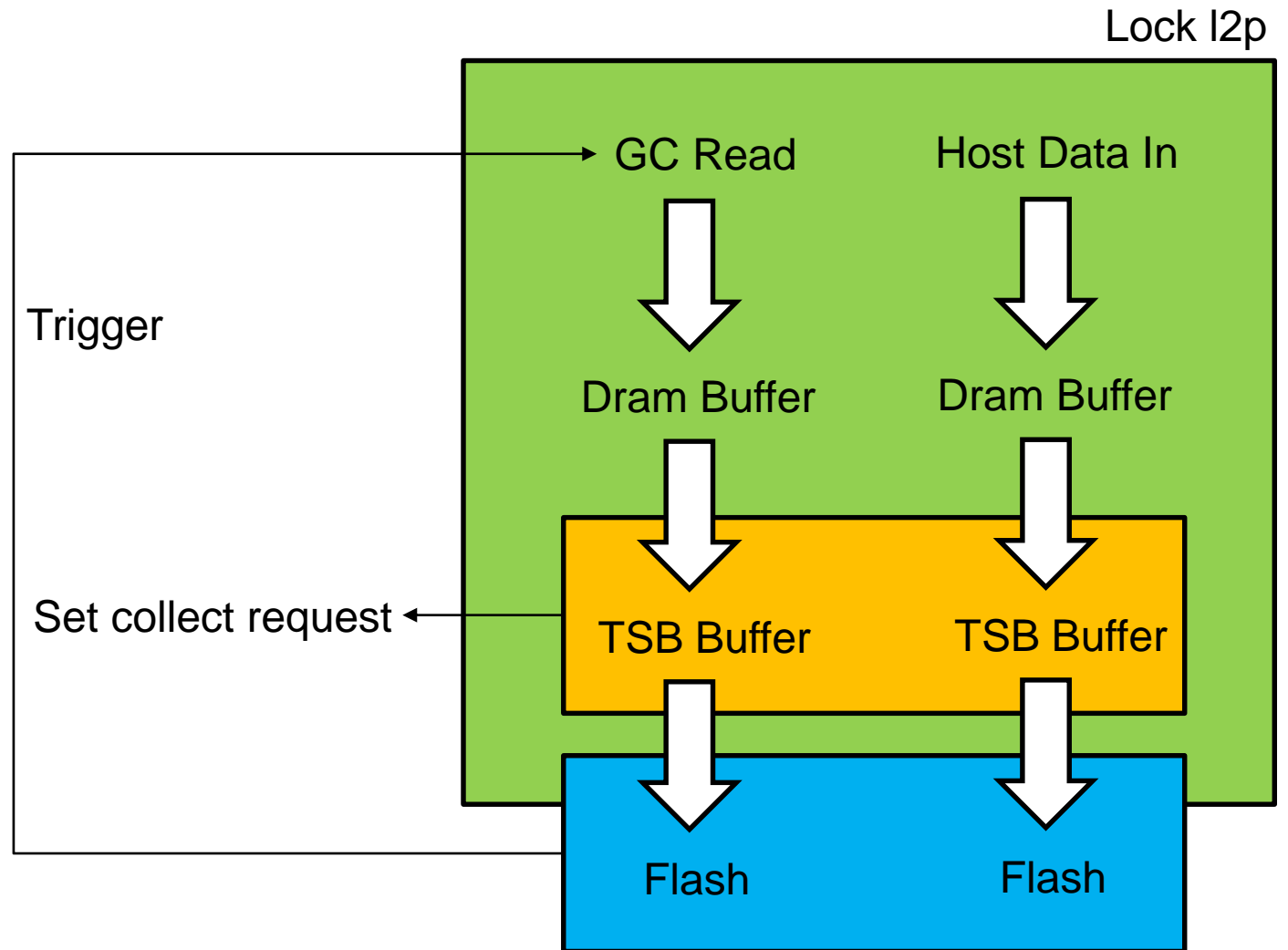
■ Set GC collect request

■ Collect Read

□ Trigger by flash r/w request

■ Valid Group

□ Valid group table



Lock module

■ Consistency

■ L2P lock

☐ Partial read

- head
- tail

■ DBuffer lock

■ RBuffer lock

■ Flash lock

Q & A



Discuss

■ Multi dimension L2P

- 在什麼狀況下需要以多維陣列呈現 ??

■ Orphan Table Adjust

- 調整的替換來源, 以及影響??

■ Stripe

- 討論Stripe

■ Snapshot vs F2H

- 限制?? 優缺??

■ Other



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