DATASHEET

SD/SDIO 3.0 Combo AHB Controller

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1 INTRODUCTION

SD/SDIO Combo Device IP core is an SD memory controller and an SDIO controller with an AHB interface. Combining with the optional Arasan NAND Flash Controller IP, the SD/SDIO Combo Device IP provides an integrated SD memory solution for designs that utilize NAND flash memory.

1.1 Overview

The SD/SDIO Combo-AHB controller IP is a full/high speed card suitable for memory cards and I/O card applications such as WLAN, Bluetooth and mobile devices with low power consumption. The full-speed card supports SPI, 1-bit and 4-bit SD transfer modes at a full clock range of 0-50Mhz. The Arasan SD/SDIO Combo Device IP has an AHB interface, which allows the ARM processor to configure the operational registers residing inside the AHB slave core.

To support NAND flash memory, Arasan provides an optional NAND Flash Controller for direct interfacing with the SD/SDIO Combo Controller IP. The Arasan NAND flash controller handles all command, address and data sequences. It also manages all the hardware protocols and allows the users to access the NAND flash memory simply by reading or writing into the Operational registers. The Arasan NAND flash controller acts as a master or a slave device on the AHB bus.

1.2 Features

- Compliant to SDIO card specification version 3.0 and SD Memory Card Physical Layer Specification version 3.0
- AMBA AHB Specification Rev 2.0
- Supports SDHC and SDHS cards
- Supports SDHC combo cards
- Supports SPI, 1-bit and 4-bit SD modes
- Allows card to interrupt host in SPI, 1-bit, and 4-bit SD modes
- Up to 200-Mbit/s read and write rates using 4 parallel data lines
- 0 to 208 MHz host clock
- CRC7 for commands and optional CRC16 for data integrity checking in SPI mode
- Application specific commands
- Comfortable erase mechanism
- Password protection of cards
- Write protect feature using mechanical switch
- Built-in write protection features
- Hot card insertion and removal
- Switch function command supports high-speed
- Card responds to direct read/write (IO52) and extended read/write(IO53) transactions
- Read Wait Control, Suspend/Resume operations
- Supports up to 8 banks of NAND flash devices
- Programmable access timing

2 ARCHITECTURE

This section describes the overall architecture of SD3.0 COMBO Device Controller.

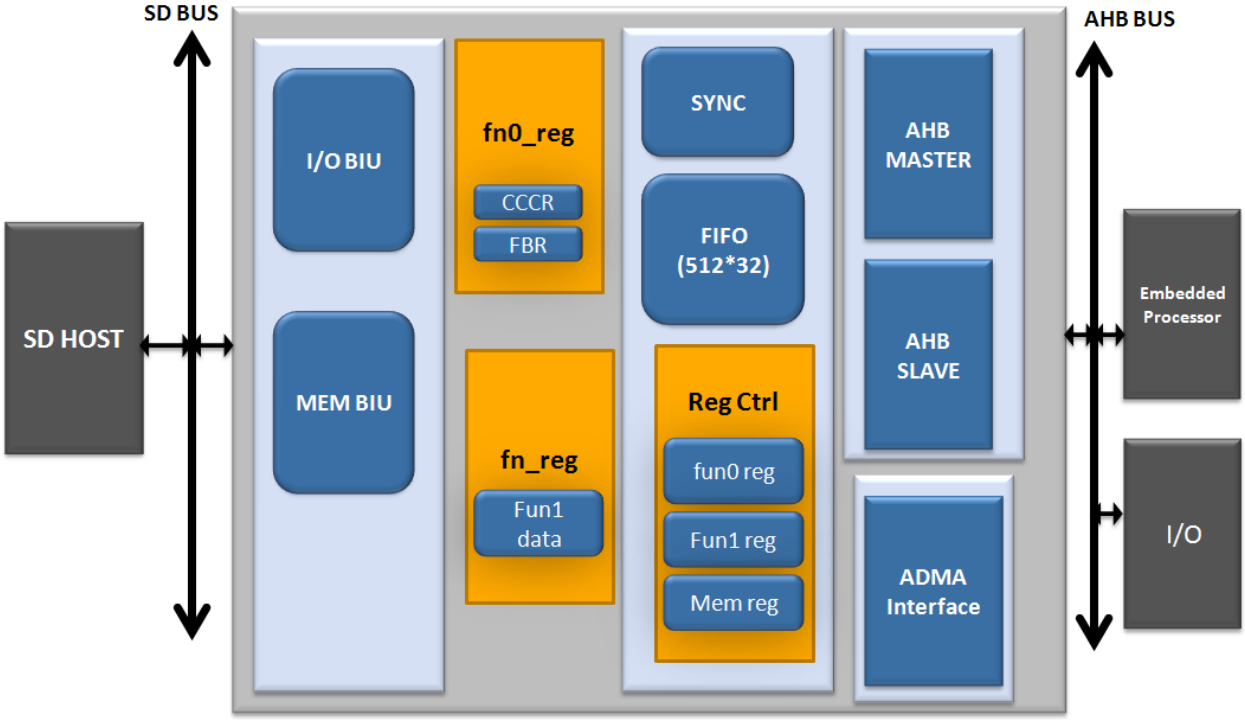

Figure 1: SD3.0_SDIO3.0 Functional Core Block Diagram

2.1 Bus Interface Unit (BIU)

The BIU communicates with the SD Host through the SD bus. SD1, SD4, SPI and 8 bit mode for embedded device are supported. The BIU houses the 16 bit CRC generator and checker for the data lines, 7 bit CRC generator and checker for the command and response lines, transmitter state machine, receiver state machine, interrupt state machine, BIU master state machine, command decoder, and the response generator. The BIU bus capability is determined by bit values programmed in the R/W CCCR registers. The Mem BIU bus capability is determined when the Mem Card registers are programmed with appropriate bit values.

2.2 fn0_register

The fn0_register module contains the CIA (Common I/O Area). There are three distinct register structures supported within the CIA. They are Card Common Control Registers (CCCR), Function Basic Registers (FBR) and Card Information Structure (CIS). The CIA is

accessed by the Host via I/O reads and writes to function 0. The registers within the CIA also provided to enable/disable the operation of the I/O function(s), control the generation of interrupts. The registers in the CIA also provide information about the function(s) abilities and requirements.

2.3 fn_register

The fn_reg module contains the funcion1 Host access registers. These registers are accessed by the Host via I/O reads and write to function 1. Whenever Interrupt is asserted from the controller Host should read these Registers to identify the source of interrupt. Host can also write these registers using cmd52 and cmd53. Host can also use these registers to send a message to ARM.

2.4 Synchronization module (sync_mod)

This block has handshake logic to communicate with the BIU and on the other side communicates with the AHB Master and Slave Core.

2.5 FIFO Control

This block contains one dual port FIFO for performing both read and write transactions. During write transaction (data transferred from Host to ARM), the data will be filled in to the first and second half of the FIFO alternatively. When data from first half of the FIFO is transferring to ARM, the second half of the FIFO will be filled and vice versa. The two FIFO's are alternatively used to store data which will give maximum throughput.
During a read transaction (data transferred to ARM to Host) the data from ARM will be written in to the two half of the FIFO's alternatively. When data from one half of the FIFO is transferring to Host, the second half of the FIFO will be filled and vice-versa and thereby the throughput will be maximum.

Note: FIFO depth can be varied using parameter defined in ram_params.v based on that maximum block size supported will change. If the maximum block size supported is 1K then the FIFO size should be 2K. Two 1k FIFO's are used to support ping pong mechanism

2.6 Reg Control

The Reg control block contains the function0, function1, memory ARM access Registers. ARM Processor read/write these registers through AHB slave interface.

2.7 AHB Interface

The AHB Master is responsible for transferring data between the ARM Processor and Arasan SD-Combo-AHB bridge for read and write operations using Scatter Gather DMA. AHB Slave Block houses the AHB slave interface signals. All the operational registers are in the reg control module. Reading and writing of these registers are handled by SD-Combo-AHB bridge or the ARM Processor. The ARM Processor should set the function ready bit in ESW Fun Ready register when it is ready to operate, indicating to the SD Host that all initialization has been done and Function is ready to operate.

2.8 ADMA Interface

This ADMA interface is responsible for controlling the ADMA transaction with system memory. It gives control signals to AHB Master Interface to initiate the AHB Bus transaction. This interface performs ADMA fetch transaction with system memory whenever the described data length is over. It decodes the data address from the descriptor table and loads the same to AHB Master and also gets the data length from descriptor table and loads the number of bytes to AHB Master. If ADMA end bit is set in the descriptor table it will assert ADMA excausted interrupt to ARM.

3 SIGNAL INTERFACES

The Arasan SDIO Combo Controller has four main interface groups,

1. SD Interface
2. AHB Slave Interface
3. AHB Master Interface
4. System interface.

Table 1: SD Interface

Signal name	Direction	Description
clk_sd	Input	SD Clock
clk_sd_inv	Input	Inverted SD Clock
SD_CMD cmd_di sel_sd_resp sel_resp_en	INOUT IN OUT OUT	*SD4 bit mode*: Command Line *SD1 bit mode*: Command Line *SPI mode*: Data Input Command Input Command Output Command Output Enable
SD_DAT0 dat0_do sel_tx_dat0 sel_tx_dat0_en	INOUT IN OUT OUT	*SD4 bit mode*: Data Line 0 *SD1 bit mode*: Data Line *SPI mode*: Data Output Data0 Input Data0 Output Data0 Output Enable
SD_DAT1 dat1_irq sel_tx_dat1 sel_tx_dat1_en	INOUT IN OUT OUT	*SD4 bit mode*: Data Line1 or Interrupt (optional) *SD1 bit mode*: Interrupt *SPI mode*: Interrupt Data1 Input Data1 Output Data1 Output Enable
SD_DAT2 dat2_rw sel_tx_dat2 sel_tx_dat2_en	INOUT IN OUT OUT	*SD4 bit mode*: Data Line2 or Read Wait (optional) *SD1 bit mode*: Read Wait (optional) *SPI mode*: Not Used Data2 Input Data2 Output Data2 Output Enable
SD_DAT3 dat3_cs sel_tx_dat3 sel_tx_dat3_en	INOUT IN OUT OUT	*SD4 bit mode*: Data Line 3 *SD1 bit mode*: Not Used *SPI mode*: Card Select Data3 Input Data3 Output Data3 Output Enable

Table 2: AHB Slave Interface

Signal name	Direction	Description
clk_ahb	Input	AHB System Clock
ahb_sdio_hsel	Input	Slave Select
ahb_sdio_haddr[16:0]	Input	Address Bus (Byte Addresses)
ahb_sdio_hwdata[31:0]	Input	Write Data Bus
ahb_sdio_hrdata[31:0]	Output	Read Data Bus
ahb_sdio_hwrite	Input	Write or Read Direction Indication
ahb_sdio_hsize[2:0]	Input	Size (Byte, Half Word or Word)
ahb_sdio_htrans[1:0]	Input	Transfer Type
ahb_sdio_hready_glb	Input	Global Ready
ahb_sdio_hready	Output	Slave Ready
ahb_sdio_hresp[1:0]	Output	Transfer Response
int_to_arm	Output	Interrupt to Processor

Table 3: AHB Master Interface

Signal name	Direction	Description
ahb_sdio_dma_hbusreq	Output	AHB Bus Request
ahb_sdio_dma_hgrant	Input	AHB Bus Grant
ahb_sdio_dma_haddr[31:0]	Output	AHB Slave DMA address (byte addresses)
ahb_sdio_dma_hwdata[31:0]	Output	AHB write data
ahb_sdio_dma_hrdata[31:0]	Input	AHB read data
ahb_sdio_dma_hwrite	Output	Write / Read Direction Indication
ahb_sdio_dma_hsize[2:0]	Output	Size (byte, half word or word)
ahb_sdio_dma_hburst[2:0]	Output	Burst Size
ahb_sdio_dma_hrdyglb	Input	Global ready signal
ahb_sdio_dma_htrans[1:0]	Output	Transfer type
ahb_sdio_dma_hresp[1:0]	Input	Transfer response

Table 4: System Interface

Signal name	Direction	Description
pwr_on_rst_n	Input	Active Low Asynchronous Hardware reset from the External environment
ahb_clk_wkup	Output	Active high signal to wakeup AHB clock. At power-on-reset this signal will be asserted to 1'b1 as the chip is in manual mode when manual clk enable bit is set to 1'b1 in Clock wakeup register. When auto clk enable bit in Clock wakeup register is 1'b1, SDIO controller will enable the ahb_clk_wkup depending on the activity on the bus when required
pullup_en	Output	Pull-up Enable from the Arasan SD-Combo-AHB bridge for Card Detection
scan_mode	Input	Active Low. If set as 1'b1 - bypass all reset pulses generated internally 1'b0 - POR will be asserted asynchronously

4 SoC LEVEL INTEGRATION

4.1 Verification Environment

The Verification Environment of the SD3.0 and SDIO3.0 block diagram shows the integration of the SD_Combo_AHB_controller. SD-Combo_AHB core has been verified in the simulation environment using the behavioral models of the surrounding environment (RTL verification). The RTL verification environment for SDIO_AHB core consists of the behavioral models to emulate the SD host and ARM processor interface.

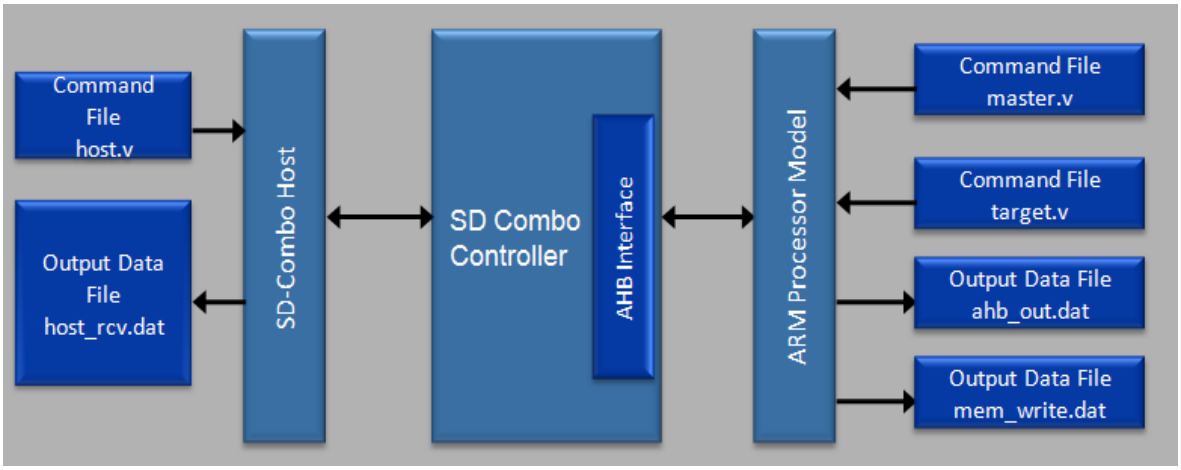

Figure 2:SD3.0_SDIO3.0 Verification Diagram

4.2 IP Deliverables

The IP package consists of the following:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

5 RELATED PRODUCTS

- SD 3.0 Device
- SDIO 3.0 Device
- SDIO Stack

