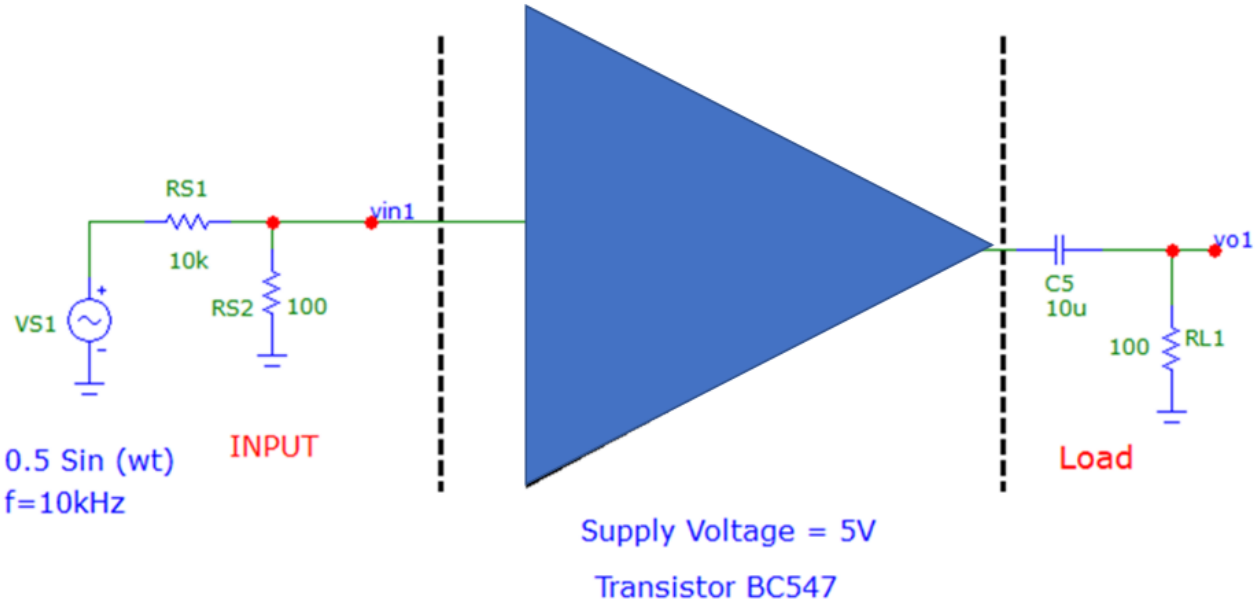
Exp.6: BJT Amplifier Design

Name: Barkha Agrawal; Roll Number: 200263

Q. Design the amplifier (shown as the solid triangle) for the given input condition and output load resistance.



Theory: First we will implement a CE amplifier action in place of the triangle, using the values mentioned below, and check if the requirements are met. We know that a single CE stage is insufficient; a common collector output stage is required. The second stage may be coupled to the first through a capacitor or directly as we will do in the second part of the experiment. The second stage acts as a load to the first stage. While designing the CC stage, we have to ensure the dc emitter voltage and bias current are sufficient so that Q2 remains conducting during the negative swing of output voltage.

$$I_{CQ} = \frac{V_{CC}\frac{R_2}{R_1+R_2} - V_{BE}}{R_E + \frac{R_B}{\beta}}$$

$$R_B = R_1 || R_2$$

$$A_V = -g_m \times R_C || R_L$$

$$g_m = \frac{I_{CQ}}{VT}$$

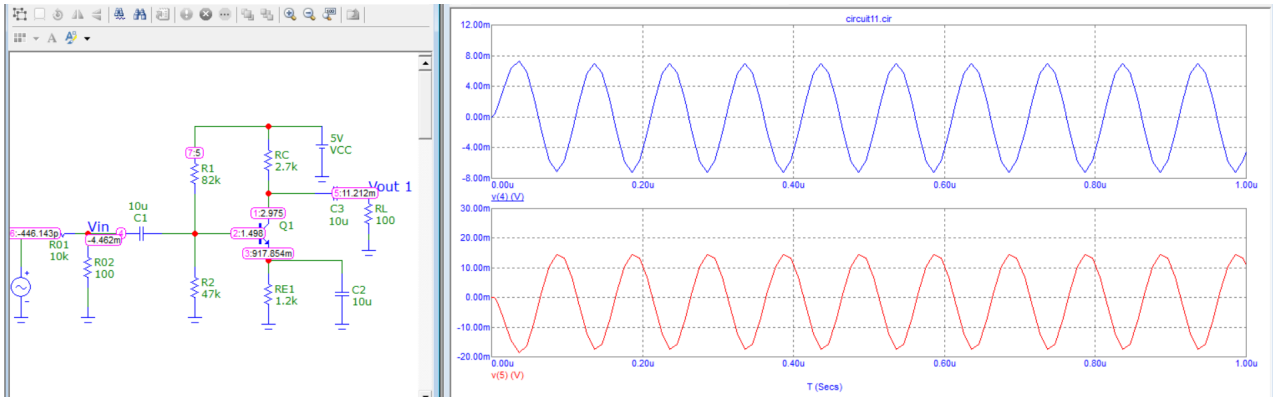
To keep transistor out of saturation

$$V_{CEQ} > vo + V_{CEsat}$$

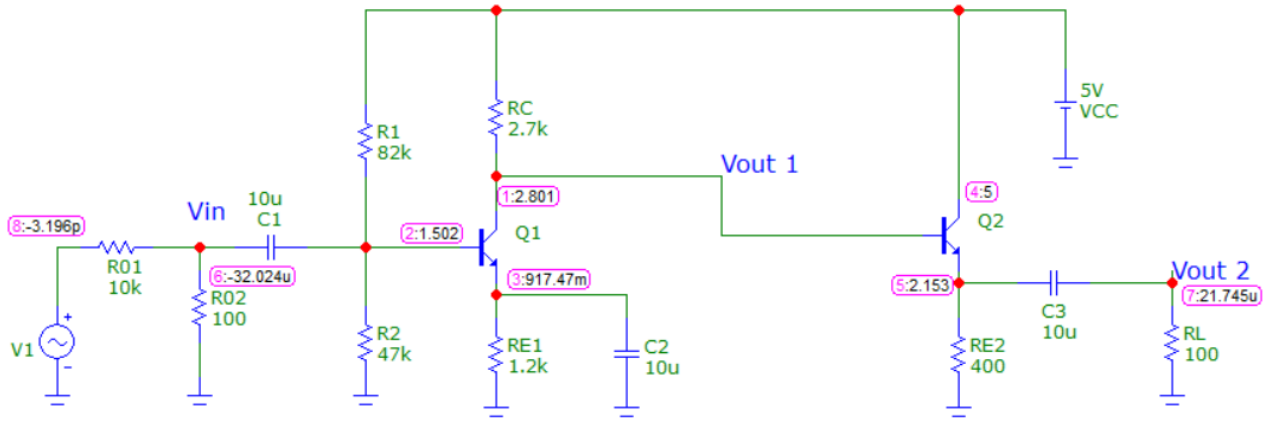
Requirements to build the circuit: 2 capacitors-10μF, DC voltage source, Sinusoidal voltage source, 8 resistors- R1 = 82 KOhm, R2 = 47 KOhm, Rc = 2.7 KOhm, RE1 = 1.2. KOhm, RL = 100 Ohm, RE2 = 400, Rs1 = 10 KOhm, Rs2 = 100 Ohm.

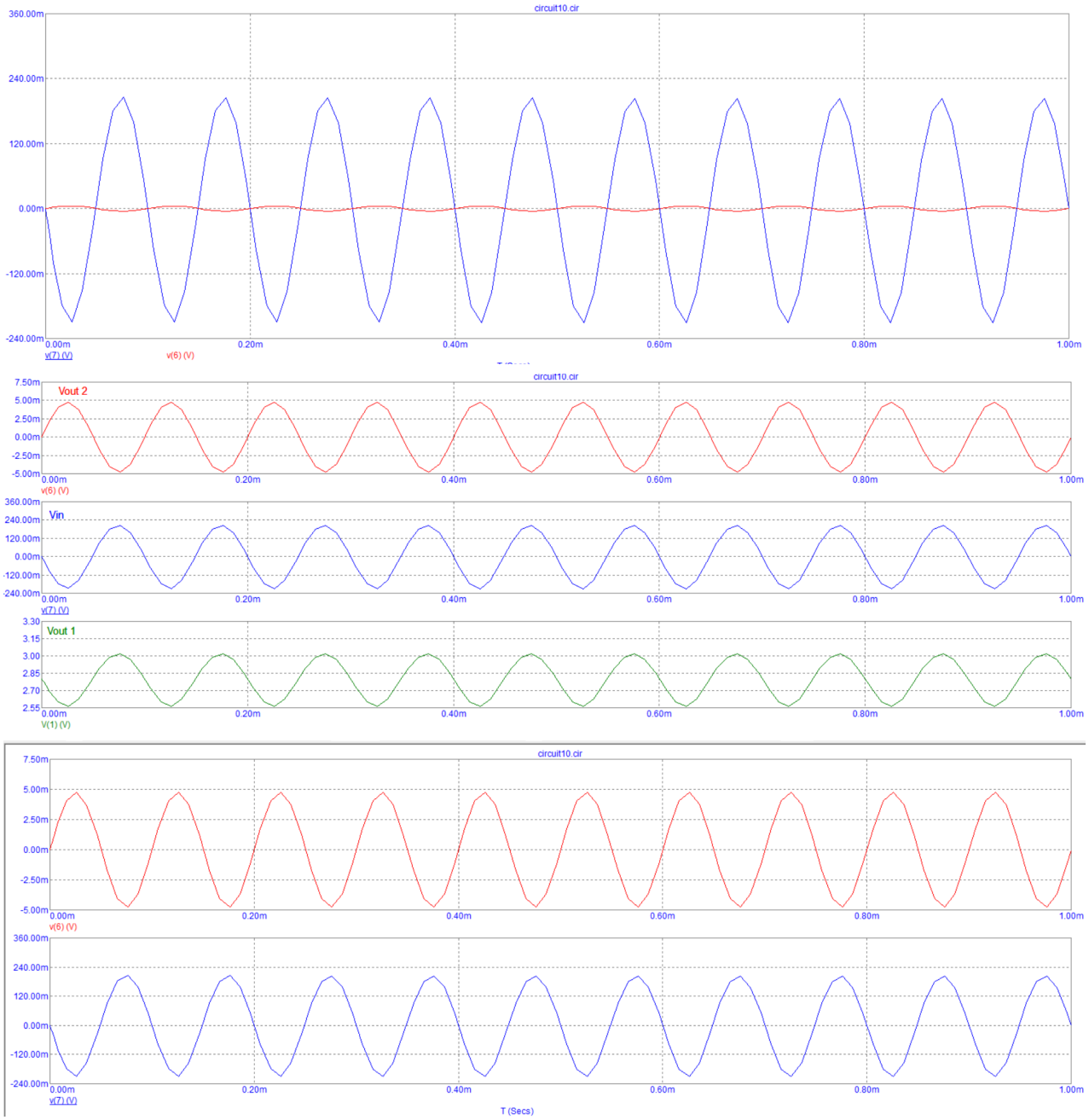
Circuit connection: Considering the above values, we first consider a CE stage amplifier in place of the triangle as in the question. Then in the second stage, we further expand the circuit to the CE-CC stage by connecting the base of the second BJT to the collector of the first BJT, such that the CC stage acts as a load to the CE stage.

Prelab work - 1:



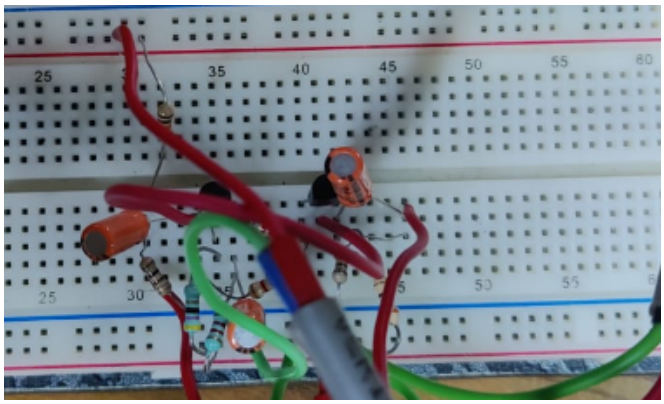
Pre-lab work - 2 :

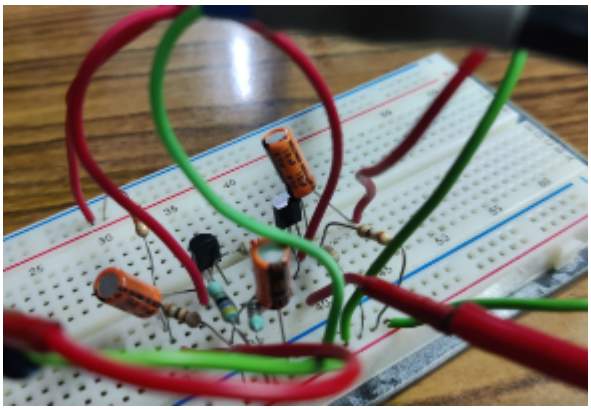


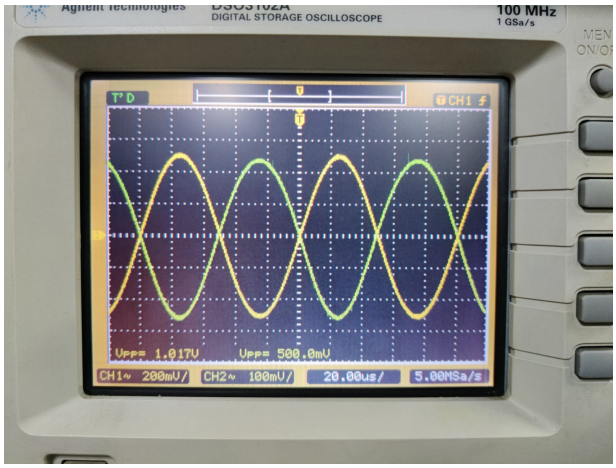


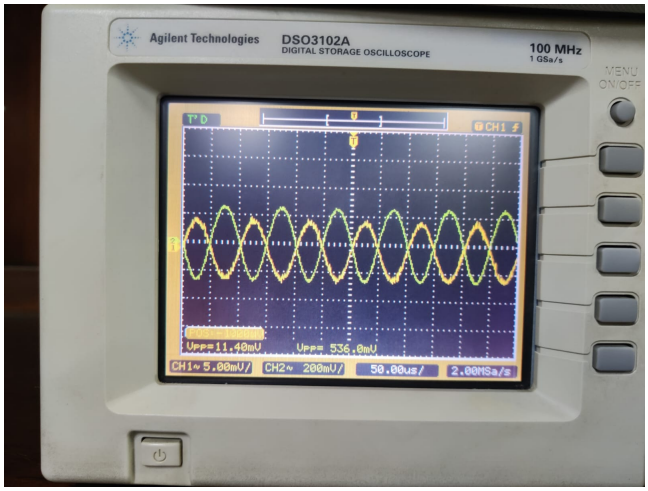
In lab work:

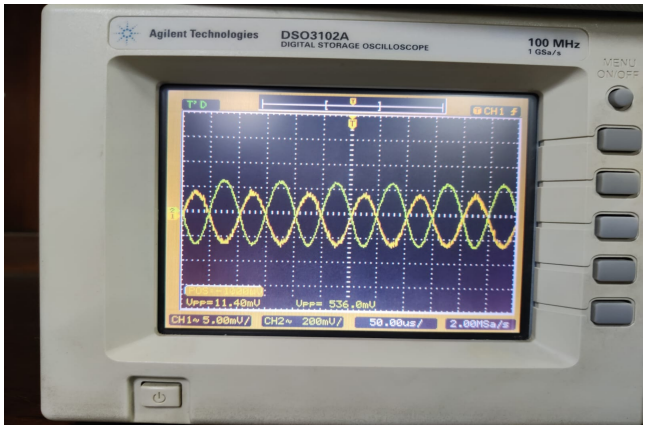
R1 = 82 KOhm, R2 = 47 KOhm, Rc = 2.7 KOhm, RE1 = 1.2. KOhm, RL = 100 Ohm
C1 = C2 = 10μF, F = 10 KHz, Vs = 1V (Peak-to-peak)

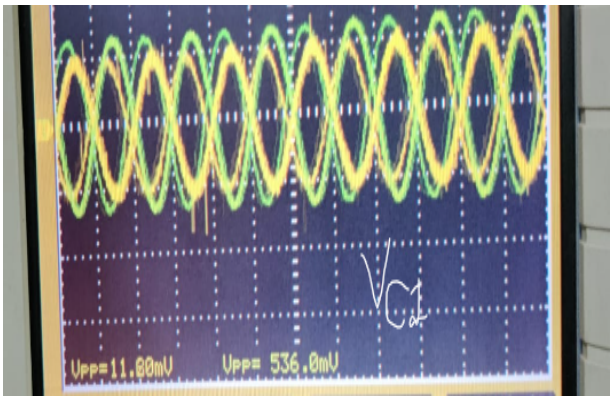


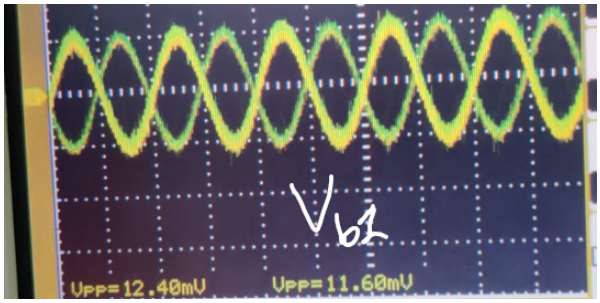


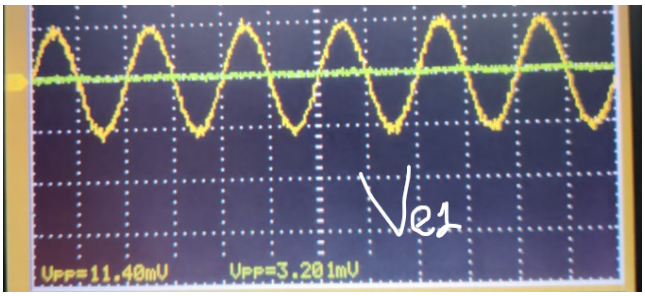

DIGITAL STORAGE OSCILLOSCOPE
100 MHz
1 GSa/s
Vpp= 1.017V
Vpp= 500.0mV
CH1~ 200mV/
CH2~ 100mV/
20.00us/
5.00MSa/s

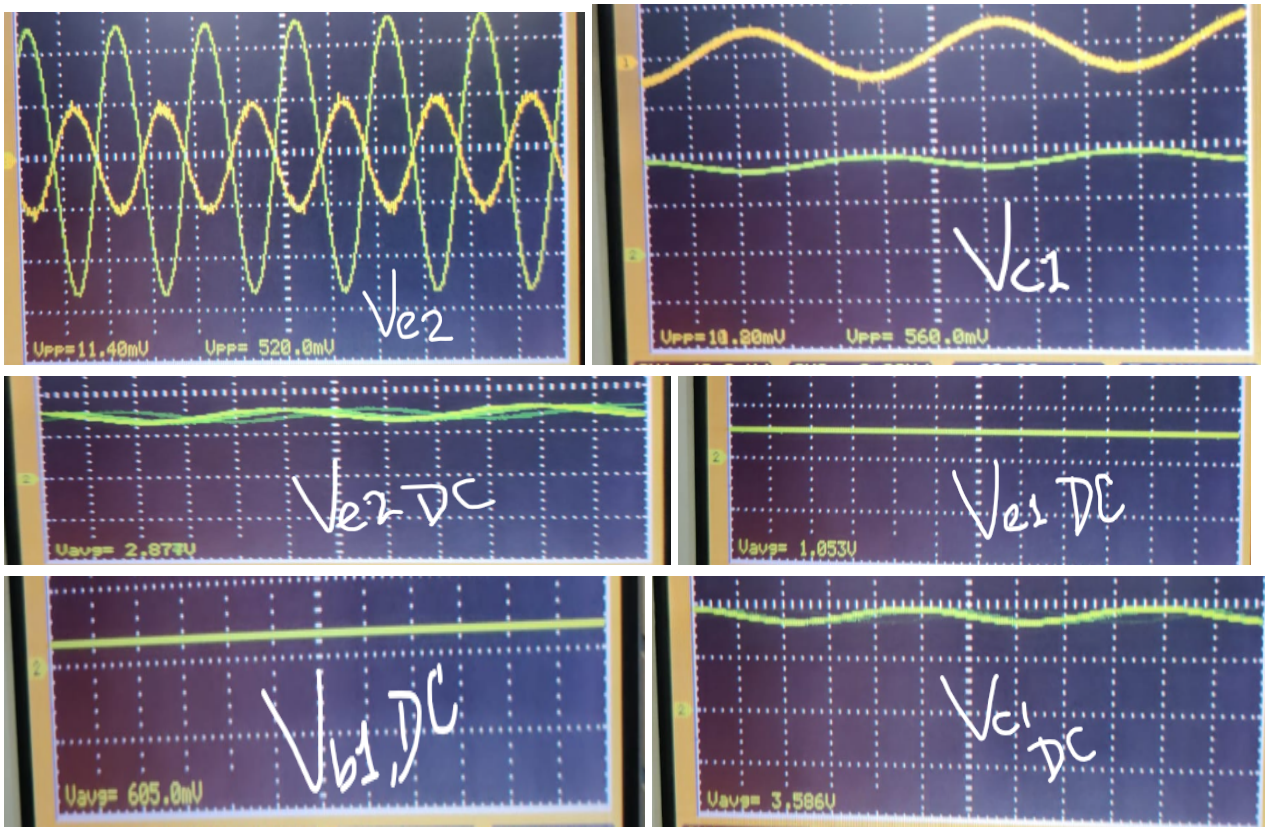

Agilent Technologies
DSO3102A
DIGITAL STORAGE OSCILLOSCOPE
100 MHz
1 GSa/s
Vpp=11.40mV
Vpp= 536.0mV
CH1~ 5.00mV/
CH2~ 200mV/
50.00us/
2.00MSa/s


Agilent Technologies
DSO3102A
DIGITAL STORAGE OSCILLOSCOPE
100 MHz
1 GSa/s
Vpp=11.40mV
Vpp= 536.0mV
CH1~ 5.00mV/
CH2~ 200mV/
50.00us/
2.00MSa/s


Vc1
Vpp=11.60mV
Vpp= 536.0mV


Vb1
Vpp=12.40mV
Vpp=11.60mV


Ve1
Vpp=11.40mV
Vpp=3.201mV



Experimental values:

Vin = 11.4mV, Vout = 504mV, Vout1 = 528mV
AC: VC1 = 536mV, VB1 = 11.6mV, VE1 = 3.2mV, VE2 = 520mV
DC: VC1 = 3.586V, VB1 = 605mV, VE1 = 1.05mV, VE2 = 2.883V
Gain = Vout / Vin = 528/11.4 = 46.316

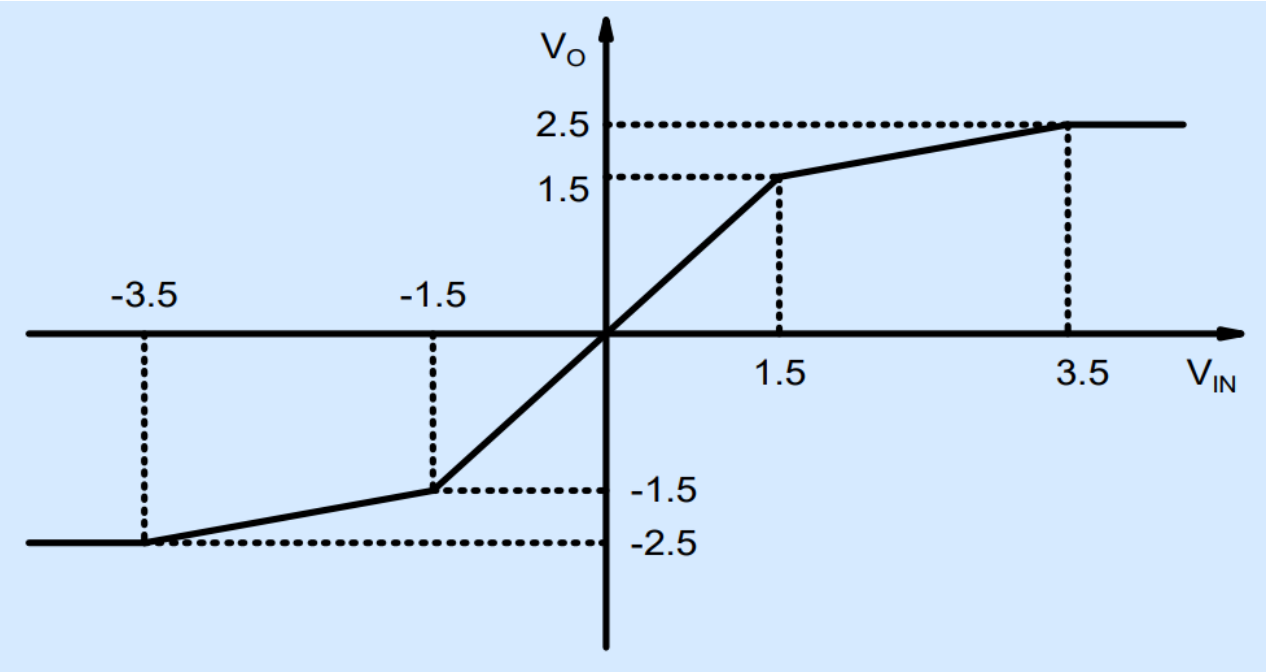
Observations:

This result is quite close to our theoretical value, and a high input resistance is observed, as expected.

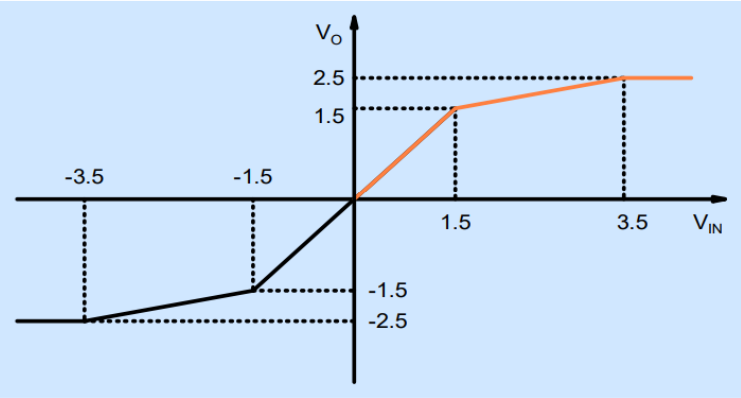
Exp. 7: Wave-Shaping

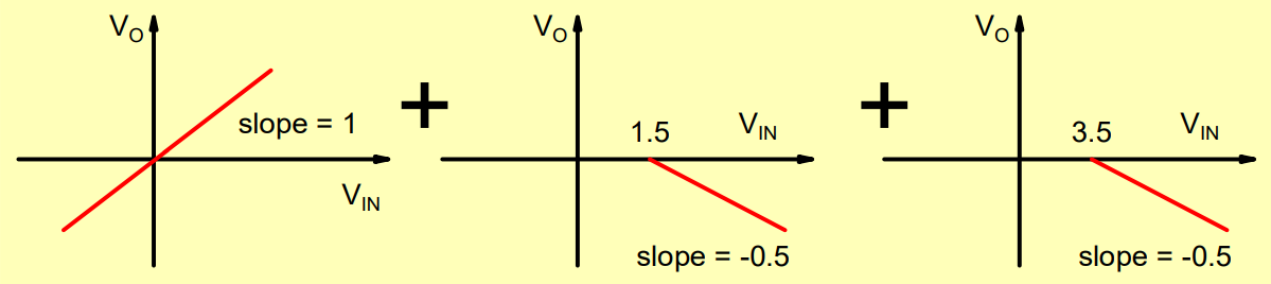
Name: Barkha Agrawal; Roll Number: 200263

OBJECTIVE: **Design a circuit with the following characteristics:**



Theory: A clipper circuit is used to cut out a specific amount of the input signal in order to produce the appropriate output wave shape. Rectifier diodes can be used in op-amp clipper circuits to clip off certain portions of the input signal. In clamper circuits, the input voltage is increased by a predetermined dc level. They are sometimes known as restorers or dc inserters. Schmitt trigger, a hysteresis-added comparator circuit, is created by giving positive feedback to a comparator's non-inverting input.

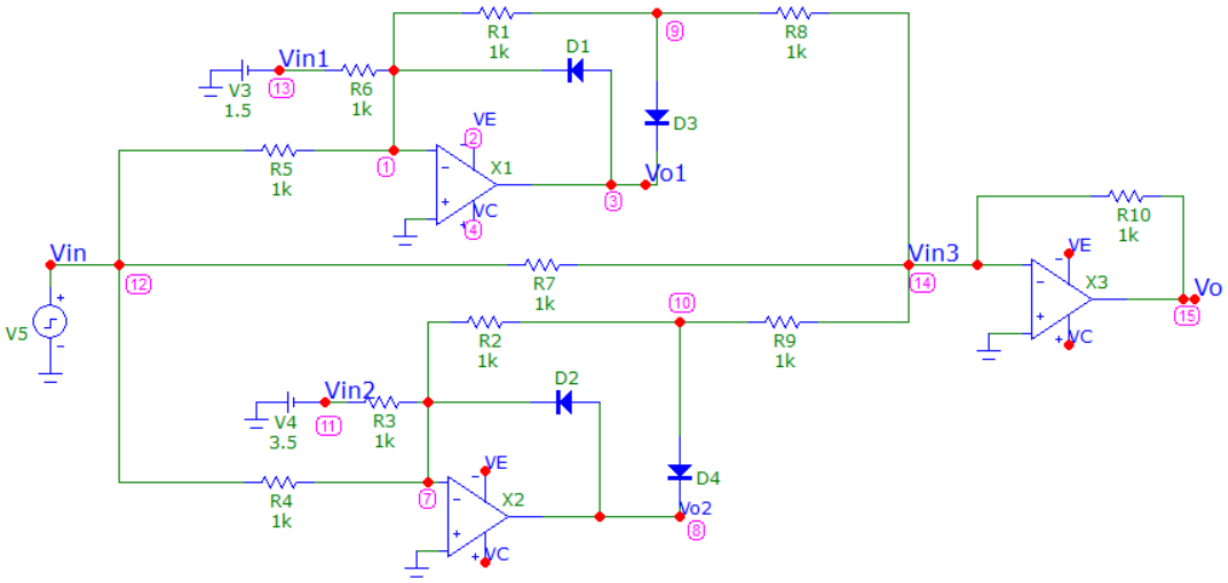


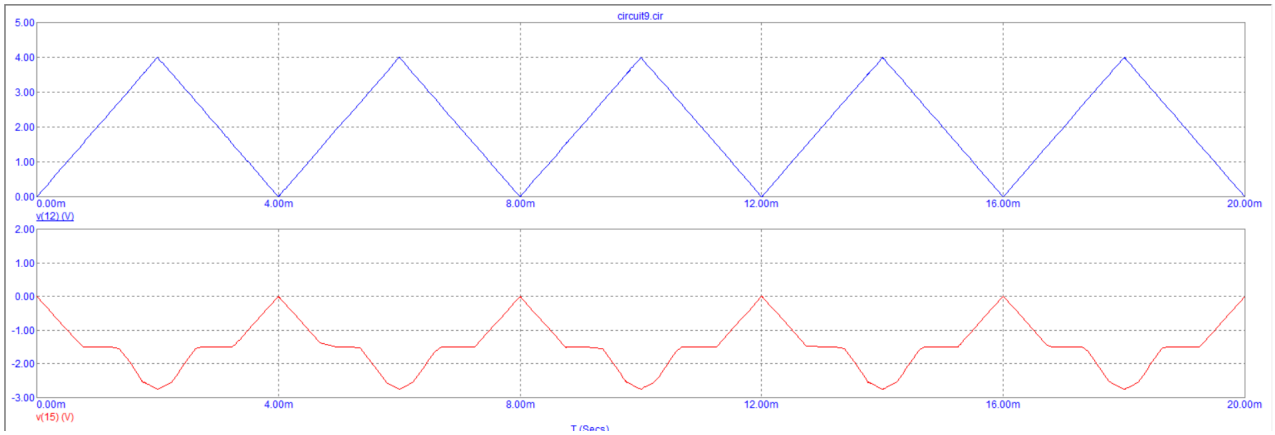


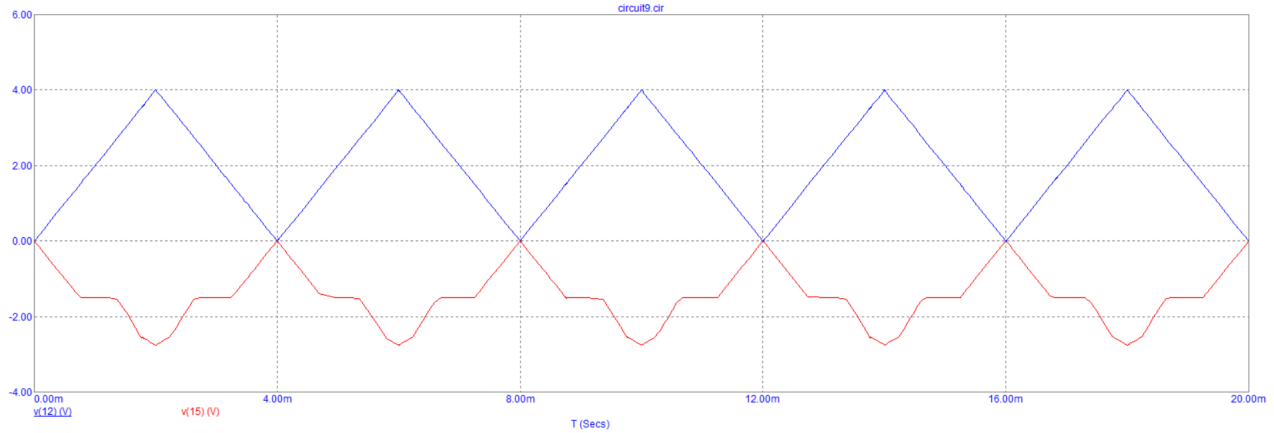
Requirements to build the circuit: 7 resistors - 1KOhm, 2 resistors - 2KOhm, 3 OpAmps, DC voltage source , Pulse Source.

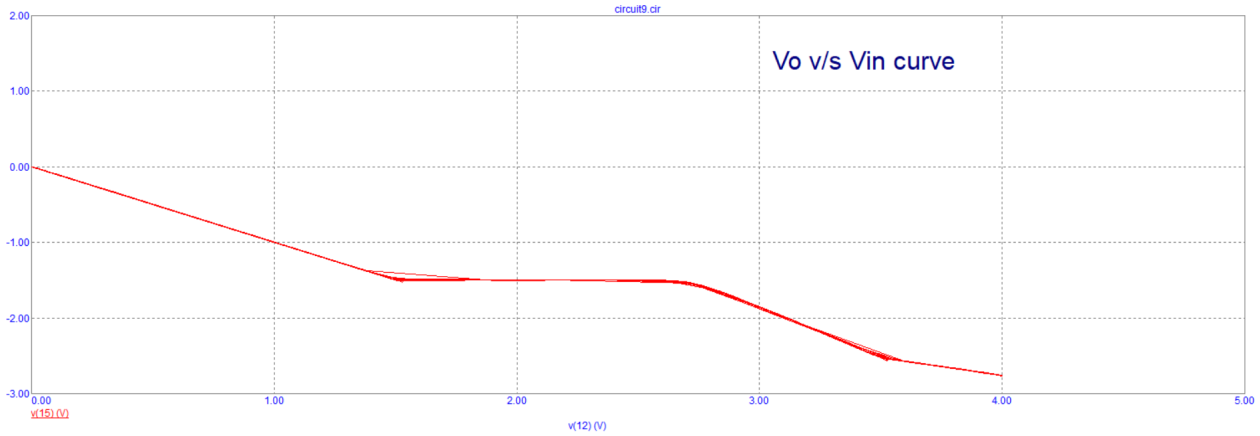
Circuit connection: Connections are made such that the output of the first two op-amps is fed as an additive input to the third op-amp. The connections can be done as shown in the circuit below.

Prelab work:

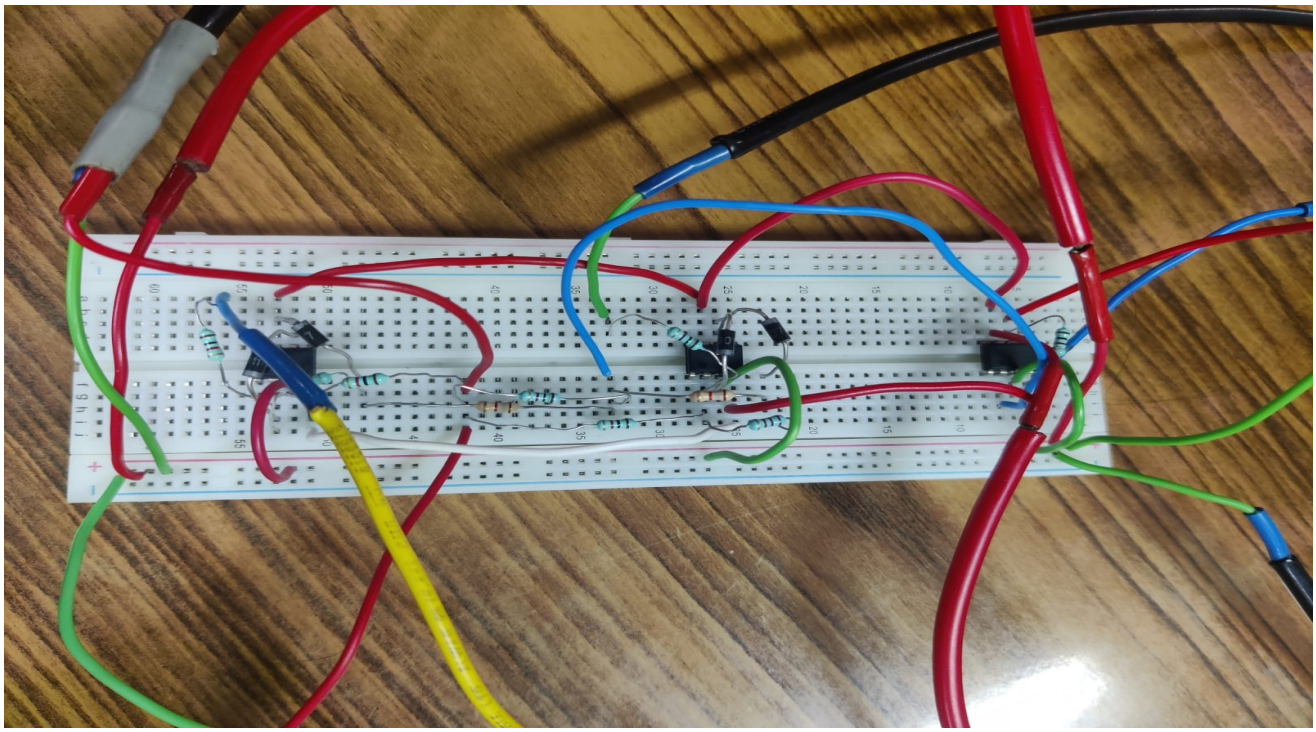

R1
1k
D1
9
R8
1k
Vin1
V3
1.5
13
R6
1k
D3
VE
2
R5
1k
1
X1
Vo1
3
VC
4
R10
1k
Vin
12
R7
1k
Vin3
14
VE
X3
Vo
15
V5
10
R2
1k
R9
1k
VC
D2
Vin2
V4
3.5
11
R3
1k
D4
VE
R4
1k
7
X2
Vo2
8
VC


circuit9.cir
5.00
4.00
3.00
2.00
1.00
0.00
0.00m
4.00m
8.00m
12.00m
16.00m
20.00m
v(12) (V)
2.00
1.00
0.00
-1.00
-2.00
-3.00
v(15) (V)
T (Secs)

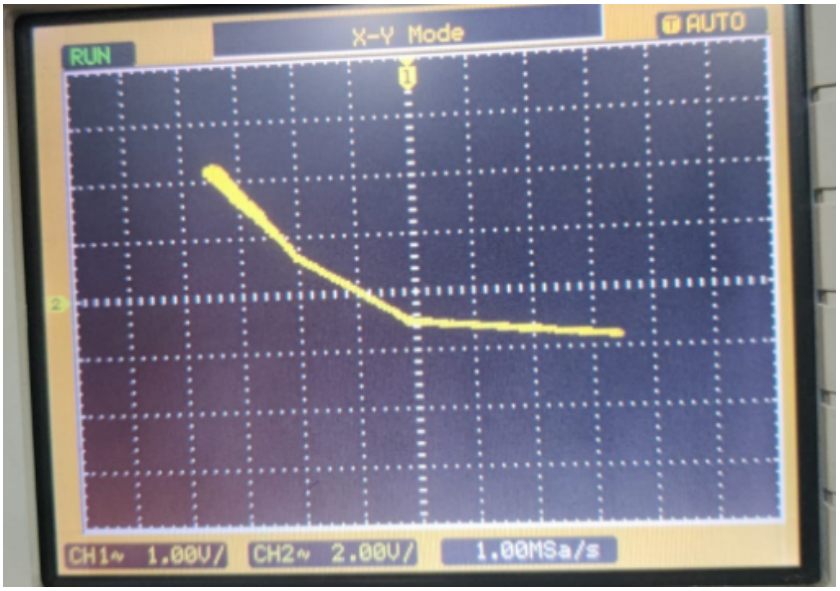

circuit9.cir
6.00
4.00
2.00
0.00
-2.00
-4.00
0.00m
4.00m
8.00m
12.00m
16.00m
20.00m
v(12) (V)
v(15) (V)
T (Secs)

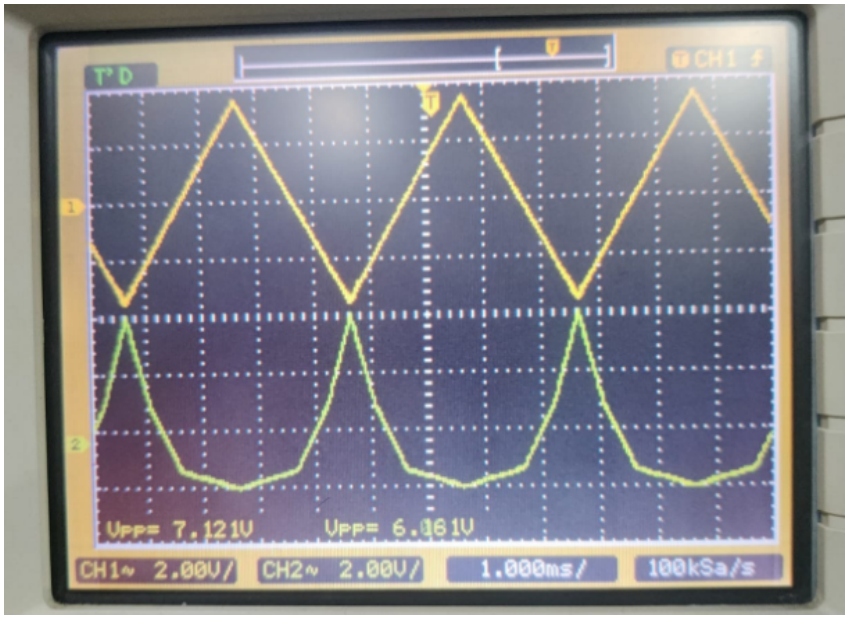


In lab work:



Experimental result:





Post-lab work:

Discussion: Wave shaping is obtained. The triangular wave is converted to an almost sinusoidal wave, with three different slopes. This result is quite close to our theoretical value.

THE END