

CS 223

Section: 2

Lab: 3

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Behavioral Module For 2 to 4 Decoder:

```
module bh_2to4_decoder(  
    input a0,  
    input a1,  
    output y0,  
    output y1,  
    output y2,  
    output y3  
);  
  
    assign y0 = ~a0 && ~a1;  
    assign y1 = a0 && ~a1;  
    assign y2 = ~a0 && a1;  
    assign y3 = a0 && a1;  
Endmodule
```

Test Bench For 2 to 4 Decoder:

```
module tb_2to4_decoder();  
  
    logic a0, a1, y0, y1, y2, y3;  
  
    bh_2to4_decoder uut ( .a0(a0), .a1(a1), .y0(y0), .y1(y1), .y2(y2), .y3(y3) );  
  
    initial begin
```

```
a0 = 0;
a1 = 0;
#10;//00

a0 = 1;
a1 = 0;
#10;//01

a0 = 0;
a1 = 1;
#10;//10

a0 = 1;
a1 = 1;
#10;//11
end
endmodule
```

Behavioral Module For 4 to 1 Multiplexer:

```
module bh_4to1_mux(
    input logic a0,
    input logic a1,
    input logic a2,
    input logic a3,
    input logic s0,
    input logic s1,
    output logic y
```

```

);
assign y = a0 && ~s0 && ~s1
          || a1 && s0 && ~s1
          || a2 && ~s0 && s1
          || a3 && s0 && s1;
Endmodule

```

Test Bench For 4 to 1 Multiplexer:

```

module tb_4to1_mux(
);

logic a0, a1, a2, a3, s0, s1, y;

bh_4to1_mux uut(.a0(a0),
                .a1(a1),
                .a2(a2),
                .a3(a3),
                .s0(s0),
                .s1(s1),
                .y(y) );

initial
begin

a0 = 0;
a1 = 0;
a2 = 0;

```

a3 = 0;

s0 = 0;

s1 = 0;

#10;

a0 = 1;

#10;

s0 = 1;

s1 = 0;

#10;

a1 = 1;

#10;

s0 = 0;

s1 = 1;

#10;

a2 = 1;

#10;

s0 = 1;

s1 = 1;

#10;

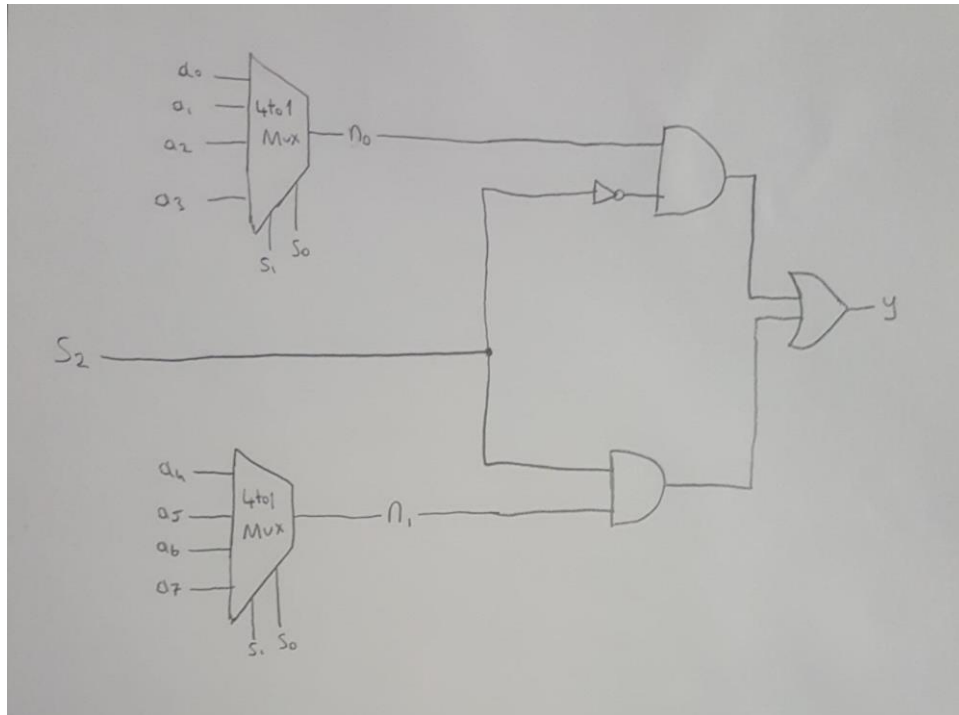
a3 = 1;

#10;

end

Endmodule

Schematic For 8 to 1 Multiplexer:



Behavioral Module For 8 to 1 Multiplexer:

```
module bh_8to1_mux(  
    input [7:0] a,  
    input [2:0] s,  
    output y  
); //try using seperate inputs instead of bus  
    logic n0, //output of mux_0  
          n1; //output of mux_1  
  
    bh_4to1_mux mux_0 ( a[0], a[1], a[2], a[3], s[0], s[1], n0 );  
    bh_4to1_mux mux_1 ( a[4], a[5], a[6], a[7], s[0], s[1], n1);  
  
    assign y = n0 && ~s[2]
```

```
    || n1 && s[2]; //if s2 = 0 y = n0, else y = n1
endmodule
```

Test Bench For 8 to 1 Multiplexer:

```
module test_8to1_mux( );

    logic [7:0] a;
    logic [2:0] s;
    logic out;

    bh_8to1_mux uut( .a(a), .s(s), .y(out));

    initial
        begin

            a = 8'b00000000;
            s = 3'b000;
            #10;
            a = 3'b00000001;
            #10;//000 a0 = 1

            s = 3'b001;
            #10;
            a = 8'b00000010;
            #10;//001 a1 = 1;

            s = 3'b010;
            #10;
            a = 8'b00000100;
```

```
#10;//010 a2=1;
```

```
s = 3'b011;
```

```
#10;
```

```
a = 8'b00001000;
```

```
#10;//011 a3=1
```

```
s = 3'b100;
```

```
#10;
```

```
a = 8'b00010000;
```

```
#10;//100 a4 = 1
```

```
s = 3'b101;
```

```
#10;
```

```
a = 8'b00100000;
```

```
#10;//101 a5 = 1
```

```
s = 3'b110;
```

```
#10;
```

```
a = 8'b01000000;
```

```
#10;//110 a6 = 1
```

```
s = 3'b111;
```

```
#10;
```

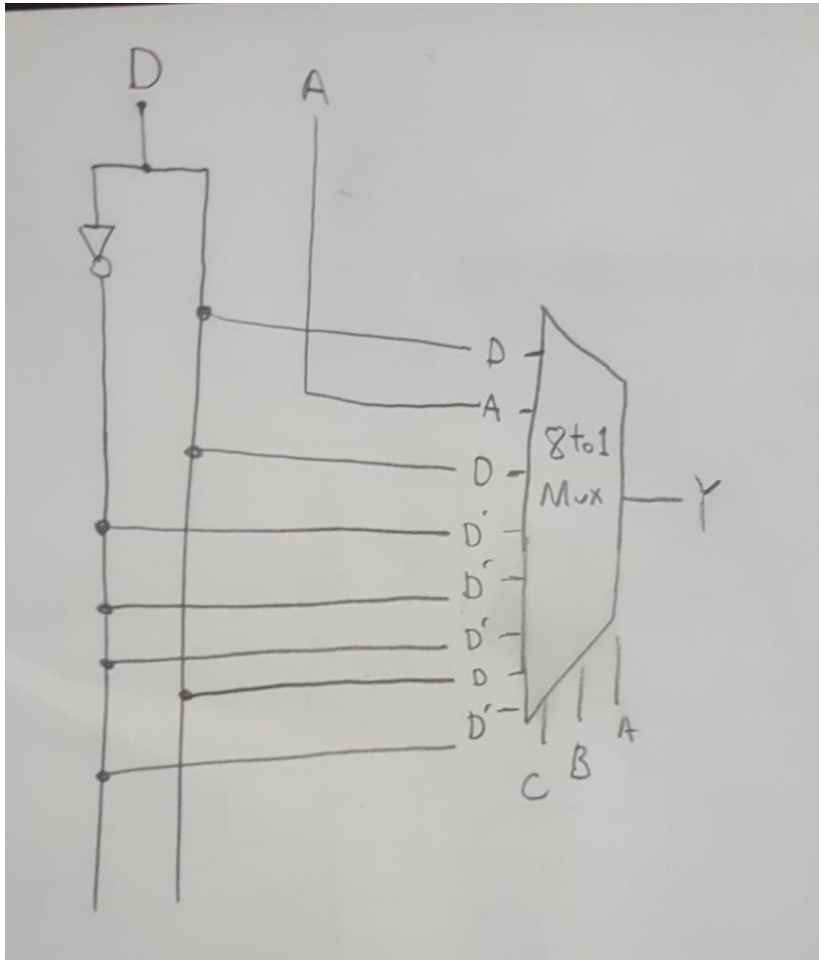
```
a = 8'b10000000;
```

```
#10;//111 a7 = 1
```

```
end
```

```
Endmodule
```


Schematic For Function:



Behavioral Module For Function:

```
module bh_lab02_function(
```

```
    input A,
```

```
    input B,
```

```
    input C,
```

```
    input D,
```

```
    output Out
```

```
);
```

```
tb_8to1_mux fun( D, A, D, ~D, ~D, ~D, D, ~D, Out );// s0=A, s1=B, s2=C
```

```
endmodule
```

Test Bench For Function:

```
module tb_lab02_function();
```

```
    logic a, b, c, d, y;
```

```
    bh_lab03_function dut( .A(a), .B(b), .C(c), .D(d), .Out(y) );
```

```
    initial begin
```

```
        a = 0;
```

```
        b = 0;
```

```
        c = 0;
```

```
        d = 0;
```

```
        #10;//0000
```

```
        a = 0;
```

```
        b = 0;
```

```
        c = 0;
```

```
        d = 1;
```

```
        #10;//0001
```

```
        a = 0;
```

```
        b = 0;
```

```
        c = 1;
```

```
        d = 0;
```

```
        #10;//0010
```

```
a = 0;  
b = 0;  
c = 1;  
d = 1;  
#10; //0011
```

```
a = 0;  
b = 1;  
c = 0;  
d = 0;  
#10; //0100
```

```
a = 0;  
b = 1;  
c = 0;  
d = 1;  
#10; //0101
```

```
a = 0;  
b = 1;  
c = 1;  
d = 0;  
#10; //0110
```

```
a = 0;  
b = 1;  
c = 1;  
d = 1;  
#10; //0111
```

```
a = 1;  
b = 0;  
c = 0;  
d = 0;  
#10; //1000
```

```
a = 1;  
b = 0;  
c = 0;  
d = 1;  
#10; //1001
```

```
a = 1;  
b = 0;  
c = 1;  
d = 0;  
#10; //1010
```

```
a = 1;  
b = 0;  
c = 1;  
d = 1;  
#10; //1011
```

```
a = 1;  
b = 1;  
c = 0;  
d = 0;
```

```
#10;//1100
```

```
a = 1;
```

```
b = 1;
```

```
c = 0;
```

```
d = 1;
```

```
#10;//1101
```

```
a = 1;
```

```
b = 1;
```

```
c = 1;
```

```
d = 0;
```

```
#10;//1110
```

```
a = 1;
```

```
b = 1;
```

```
c = 1;
```

```
d = 1;
```

```
#10;//111
```

```
end
```

```
endmodule
```