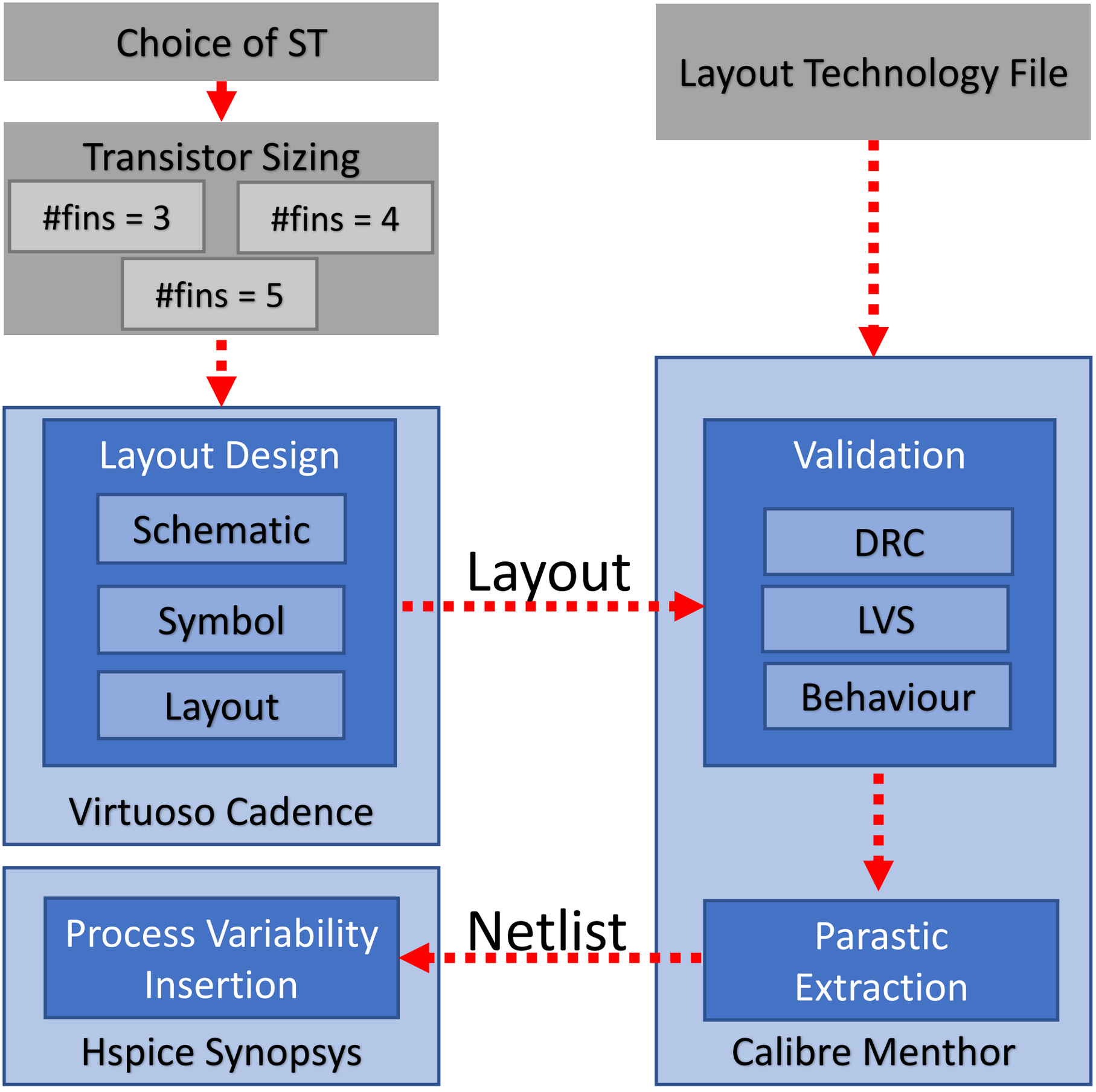
Choice of ST
Transistor Sizing
#fins = 3
#fins = 4
#fins = 5
Layout Technology File
Layout Design
Schematic
Symbol
Layout
Virtuoso Cadence
Layout
Validation
DRC
LVS
Behaviour
Process Variability Insertion
Hspice Synopsys
Netlist
Parastic Extraction
Calibre Menthor