

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

LEONARDO BARLETTE MORAES

**Schmitt Trigger Dimensioning Under
Variability and Voltage Scaling for
Minimum Energy Operation.**

Thesis presented in partial fulfillment
of the requirements for the degree of
Master of Microelectronics

Advisor: Prof. Dr. Ricardo Reis
Coadvisor: Profa. Dra. Cristina Meinhardt

Porto Alegre
May 2020

CIP — CATALOGING-IN-PUBLICATION

Moraes, Leonardo Barlette

Schmitt Trigger Dimensioning Under Variability and Voltage Scaling for Minimum Energy Operation. / Leonardo Barlette Moraes. – Porto Alegre: PGMICRO da UFRGS, 2020.

147 f.: il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica, Porto Alegre, BR-RS, 2020. Advisor: Ricardo Reis; Coadvisor: Cristina Meinhardt.

1. Formatação eletrônica de documentos.
2. L^AT_EX.
3. ABNT.
4. UFRGS. I. Reis, Ricardo. II. Meinhardt, Cristina. III. Título.

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL

Reitor: Prof. Rui Vicente Oppermann

Vice-Reitora: Prof^a. Jane Fraga Tutikian

Pró-Reitor de Pós-Graduação: Prof. Celso Giannetti Loureiro Chaves

Diretora do Instituto de Informática: Prof^a. Carla Maria Dal Sasso Freitas

Coordenadora do PGMICRO: Prof. Fernanda Gusmão de Lima Kastensmidt

Bibliotecária-chefe do Instituto de Informática: Beatriz Regina Bastos Haro

CONTENTS

LIST OF ABBREVIATIONS AND ACRONYMS.....	4
LIST OF FIGURES	7
ABSTRACT	10
RESUMO	11
1 INTRODUCTION.....	12
2 VARIABILITY EFFECTS AND MITIGATION TECHNIQUES	15
3 FINFET TECHNOLOGY AND VARIABILITY IMPACT	21
4 CONSIDERED DESIGNS	27
4.1 6T Traditional ST.....	27
4.1.1 Three Inverter Schmitt Trigger (TIST)	28
4.1.2 Stacked Inverter Gate (SIG).....	29
5 OBJECTIVES	34
6 METHODOLOGY	35
6.1 Layout Design.....	37
6.2 Electrical Simulation	42
7 RESULTS.....	46
7.1 Over robustness enhancing circuits.....	46
7.2 Energy Consumption and Deviation	49
7.3 Static Noise Margins	57
7.4 Over ST technique applied on Full Adders	65
7.4.1 Nominal Operation.....	65
7.4.2 Near-Threshold Operation	69
7.4.3 Penalties	70
8 CONCLUSIONS	74
REFERENCES.....	75
ANNEX A — INVERTER DESIGNS LAYOUTS	82
ANNEX B — FULL ADDERS.....	103
ANNEX C — ENERGY MEASURES DISTRIBUTIONS	116
ANNEX D — EXTRACTED NETLISTS FROM LAYOUTS	146

LIST OF ABBREVIATIONS AND ACRONYMS

IoT	Internet of Things
CMOS	Complementary Metal Oxide Semiconductor
ULP	Ultra Low Power
FinFET	Fin Field Effect Transistor
SCE	Short Channel Effect
RDF	Random Dopant Fluctuation
ST	Schmitt Trigger
FA	Full Adder
V_T	Threshold Voltage
NBTI	Negative Bias Temperature Instability
HCI	Hot Carrier Injection
CMP	Chemical-Mechanical Polishing
LER	Line-Edge Roughness
WF	Work Function
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PVT	Process Voltage and Temperature
WID	Within-Die
SIMD	Single Instruction Multiple Data
PDP	Power Delay Product
TGA	Transmission Gate Adder
TFA	Transmission Function Adder
CPL	Complementary Pass Transistor Logic
CNFET	Carbon Nanotube Field Effect Transistor

FDSOI	Fully Depleted Silicon On Insulator
OTS	Optimal Transistor Sizing
L	Gate Length
W_{FIN}	Fin Width
H_{FIN}	Fin Height
T_{OX}	Oxide Thickness
SOI	Silicon On Insulator
WFF	Work Function Fluctuation
SRAM	Static Random Access Memory
GOBD	Gate Oxide Break Down
ECC	Error Correcting Code
SNM	Static Noise Margin
UDSM	Ultra-Deep Sub-Micron
VTC	Voltage Transfer Curve
DRC	Design Rule Checking
LVS	Layout Versus Schematic
EDA	Electronic Design Automation
PDK	Process Design Kit
ASAP	Arizona State Predictive PDK
FEOL	Front End Of Line
MOL	Middle End Of Line
BEOL	Back End Of Line
SDT	Source-Drain Trench
LIG	Local-Interconnect Gate
LISD	Local-Interconnect Source-Drain
V0	Via 0

M1 Metal 1
M2 Metal 2
MC Monte Carlo
EDP Energy Deviation Product
TIST Triple-Inverter ST
SIG Stacked-Inverter Gate

LIST OF FIGURES

Figure 2.1 Levels of abstraction from a ideal transistor concept towards a realistic and "atomistic" device concept. (a) Depicts a the current approach of semiconductor device simulation, with continuous dopant charge and smooth boundaries. (b) Depicts a 20-nm MOSFET, with less than 50 Si atoms along the channel. RDF, interface roughness and LER introduce considerable intrinsic parameter fluctuation. (c) Depicts a 4-nm MOSFET, with less than 10 Si atoms along the channel.	17
Figure 3.1 Structural comparison between (a) planar MOSFET and (b) FinFET transistors.	21
Figure 3.2 Structural comparison between (a) bulk and (b) SOI FinFETs.	22
Figure 3.3 Metal fabrication ideal and real aspects.....	23
Figure 3.4 Electrostatic potential in a generic 30-nm MOSFET with the surface potential shown below. The metal gate has two grains with the grain boundary diagonally across the channel.	24
Figure 4.1 ST inverter leakage suppression (LOTZE; MANOLI, 2017).	28
Figure 4.2 TIST schematic (RABAЕY; CHANDRAKASAN; NIKOLIC, 2002)	28
Figure 4.3 SIG schematic (BOSE; JOHNSTON, 2018)	29
Figure 4.4 Full Adders with internal inverters to be replaced highlighted.	32
Figure 4.5 Original and modified Low Power STs (LPST) side-by-side.....	33
Figure 6.1 Design flow of the experiments.	37
Figure 6.2 1 to 5 fins (left to the right) ST layout comparison.	38
Figure 6.3 1 to 5 fins (left to the right) ST layout comparison.	38
Figure 6.4 1 to 5 fins (left to the right) SIG layout comparison.....	38
Figure 6.5 From the left to the right, 2, 4 and 6 maximum fins TIST layout comparison.	39
Figure 6.6 Technology layers and 3-fins transistors 6T ST layout	40
Figure 6.7 TAP-Cell Layout.....	41
Figure 6.8 Noise margins measurements.	44
Figure 6.9 Test Bench.	45
Figure 6.10 Test Bench for the Full Adders simulation.	45
Figure 7.1 Frequency decrease over variability scaling for each design.....	47
Figure 7.2 Propagation times deviation for each design in relation to the WFF level considering all scenarios.	48
Figure 7.3 Layout comparison for each scenario considering the energy metrics for the inverter.....	53
Figure 7.4 Layout comparison for each scenario considering the energy metrics for the ST.	53
Figure 7.5 Layout comparison for each scenario considering the energy metrics for the SIG.	54
Figure 7.6 Layout comparison for each scenario considering the energy metrics for the TIST at 2:1 proportion.	54
Figure 7.7 Layout comparison for each scenario considering the energy metrics for the TIST at 3:1 proportion.	55
Figure 7.8 Low energy layouts energy metrics comparison for each design.	56
Figure 7.9 High robustness layouts energy metrics comparison for each design.	56
Figure 7.10 CB layouts energy metrics comparison for each design.....	57

Figure 7.11 Current ratio (left) and current ratio deviation (right) design comparison across variability scaling.....	59
Figure 7.12 Leakage current scaling (left axis) and standard deviation (right axis) for the inverter.....	60
Figure 7.13 Average on and off-current increase over all designs through variability scaling. The scaling is normalized in relation to the 1% WFF level measures.....	61
Figure 7.14 Output gain value across voltage scaling.....	61
Figure 7.15 Voltage Transfer Curve slopes through supply voltage scaling for each design.....	62
Figure 7.16 Voltage Transfer Curves for all designs at 0.1V.....	62
Figure 7.17 Voltage Transfer Curves for all designs at 0.7V.....	63
Figure 7.18 Design hysteresis ratio comparison (left) and hysteresis ratio normalized deviation (right), across variability scaling.....	64
Figure 7.19 Hysteresis curves for all designs at nominal supply voltage.....	64
Figure 7.20 Design hysteresis ratios comparison across supply voltage scaling.....	65
Figure 7.21 Energy measures distribution for the inverter at different levels of variability at 0.2V.....	66
Figure 7.22 Energy measures distribution for the inverter at different levels of variability at 0.4V.....	67
Figure 7.23 Energy measures distribution for the inverter at different levels of variability at 0.7V.....	68
Figure 7.24 Average delay measures for nominal operation and their respective normalized deviation (variability sensitivity).....	72
Figure 7.25 Average energy measures for nominal operation and their respective normalized deviation (variability sensitivity).....	72
Figure 7.26 Average delay measures for near-threshold operation and their respective normalized deviation (variability sensitivity).....	73
Figure 7.27 Average energy measures for near-threshold operation and their respective normalized deviation (variability sensitivity).....	73
 Figure A.1 1 fin inverter layout.....	83
Figure A.2 2 fins inverter layout.....	84
Figure A.3 3 fins inverter layout.....	85
Figure A.4 4 fins inverter layout.....	86
Figure A.5 5 fins inverter layout.....	87
Figure A.6 1 fin ST layout.....	88
Figure A.7 2 fins ST layout.....	89
Figure A.8 3 fins ST layout.....	90
Figure A.9 4 fins ST layout.....	91
Figure A.10 5 fins ST layout.....	92
Figure A.11 1 fin SIG layout.....	93
Figure A.12 2 fins SIG layout.....	94
Figure A.13 3 fins SIG layout.....	95
Figure A.14 4 fins SIG layout.....	96
Figure A.15 5 fins SIG layout.....	97
Figure A.16 2 fin max., proportion 2:1 TIST layout.....	98
Figure A.17 3 fin max., proportion 3:1 TIST layout.....	99
Figure A.18 4 fin max., proportion 2:1 TIST layout.....	100
Figure A.19 6 fin max., proportion 3:1 TIST layout.....	101
Figure A.20 6 fin max., proportion 2:1 TIST layout.....	102

Figure B.1	Traditional Mirror Full Adder layout	104
Figure B.2	Mirror Full Adder layout with internal inverters replaced by ST1.....	105
Figure B.3	Mirror Full Adder layout with internal inverters replaced by ST2.....	106
Figure B.4	Traditional Transmission Full Adder layout	107
Figure B.5	Transmission Full Adder layout with internal inverters replaced by ST1..	108
Figure B.6	Transmission Full Adder layout with internal inverters replaced by ST2. .	109
Figure B.7	Traditional Transmission Gate Adder layout	110
Figure B.8	Transmission Gate Adder layout with internal inverters replaced by ST1.	111
Figure B.9	Transmission Gate Adder layout with internal inverters replaced by ST2. 112	
Figure B.10	Traditional Hybrid Full Adder layout.	113
Figure B.11	Hybrid Full Adder layout with internal inverters replaced by ST1.	114
Figure B.12	Hybrid Full Adder layout with internal inverters replaced by ST2.	115
Figure C.1	Inverter energy measures distribution operating at 0.2V.....	116
Figure C.2	Inverter energy measures distribution operating at 0.4V.....	117
Figure C.3	Inverter energy measures distribution operating at 0.7V.....	118
Figure C.4	Inverter energy measures dispersion operating at 0.2V.....	119
Figure C.5	Inverter energy measures dispersion operating at 0.4V.....	120
Figure C.6	Inverter energy measures dispersion operating at 0.7V.....	121
Figure C.7	ST energy measures distribution operating at 0.2V.	122
Figure C.8	ST energy measures distribution operating at 0.4V.	123
Figure C.9	ST energy measures distribution operating at 0.7V.	124
Figure C.10	ST energy measures dispersion operating at 0.2V.	125
Figure C.11	ST energy measures dispersion operating at 0.4V.	126
Figure C.12	ST energy measures dispersion operating at 0.7V.	127
Figure C.13	SIG energy measures distribution operating at 0.2V.....	128
Figure C.14	SIG energy measures distribution operating at 0.4V.....	129
Figure C.15	SIG energy measures distribution operating at 0.7V.....	130
Figure C.16	SIG energy measures dispersion operating at 0.2V.....	131
Figure C.17	SIG energy measures dispersion operating at 0.4V.....	132
Figure C.18	SIG energy measures dispersion operating at 0.7V.....	133
Figure C.19	TIST 2:1 energy measures distribution operating at 0.2V.....	134
Figure C.20	TIST 2:1 energy measures distribution operating at 0.4V.....	135
Figure C.21	TIST 2:1 energy measures distribution operating at 0.7V.....	136
Figure C.22	TIST 2:1 energy measures dispersion operating at 0.2V.....	137
Figure C.23	TIST 2:1 energy measures dispersion operating at 0.4V.....	138
Figure C.24	TIST 2:1 energy measures dispersion operating at 0.7V.....	139
Figure C.25	TIST 3:1 energy measures distribution operating at 0.2V.....	140
Figure C.26	TIST 3:1 energy measures distribution operating at 0.4V.....	141
Figure C.27	TIST 3:1 energy measures distribution operating at 0.7V.....	142
Figure C.28	TIST 3:1 energy measures dispersion operating at 0.2V.....	143
Figure C.29	TIST 3:1 energy measures dispersion operating at 0.4V.....	144
Figure C.30	TIST 3:1 energy measures dispersion operating at 0.7V.....	145
Figure D.1	Inverter extracted netlist for all sizings.....	147

ABSTRACT

The emergence of IoT alongside with the increased process variability impact in modern technology nodes, is the main reason to control variability impact over metrics. Given the large set of IoT devices working in battery-oriented environments, energy consumption should be minimal and the operation regime reliable. Schmitt Trigger inverters are traditionally used for noise immunity enhancement, and have been recently applied to mitigate radiation effects and process variability impact. However, Schmitt Trigger operation at the nominal voltage introduces high degradation on power consumption. Thus, this work main contribution is to identification of the relationship between transistor sizing, supply voltage, energy, and process variability robustness to get a minimal energy consumption circuit while keeping robustness. The results are extracted from 7-nm FinFET Schmitt Trigger layouts under different levels of process variability, supply voltages, and sizing. Also, a maximum frequency scaling under a failure threshold was performed. On average, the supply voltage decreases in layouts with a smaller number of fins, while maintaining acceptable robustness in high variability scenarios. Exploring voltage and transistor sizing made possible a reduction of about 24.84% of power consumption.

Keywords: Formatação eletrônica de documentos. L^AT_EX. ABNT. UFRGS.

**Dimensionamento de Schmitt Trigger Sob Influência de Variabilidade e
Escalonamento da Tensão de Alimentação para Operação com Consumo Mínimo
de Energia**

RESUMO

Palavras-chave: O surgimento da Internet das Coisas juntamente com o aumento do impacto da variabilidade de processo nos nós modernos de tecnologia é o principal motivo para controlar o impacto da variabilidade sobre as métricas. Dado o grande conjunto de dispositivos envolvidos na Internet das Coisas que funcionam em ambientes orientados para baterias, o consumo de energia dever ser o mínimo possível e o regime de operação confiável. Os inversores Schmitt Trigger na tensão nominal introduzem uma alta degradação no consumo de energia. Assim, a principal contribuição deste trabalho é a identificação da relação entre o dimensionamento do transistor, a tensão de alimentação, a energia e a robustez à variabilidade de processo para obter um circuito com consumo mínimo de energia, mantendo a robustez. Os resultados são extraídos de leiautes FinFET Schmitt Trigger de 7-nm sob diferentes níveis de variabilidade de processo, tensões de alimentação e dimensionamento. Além disso, foi executada uma calibração da frequência máxima sob um limiar de falha. Em média, a tensão de alimentação diminui em leiautes com um número menor de fins, mantendo robustez aceitável em cenários de alta variabilidade. A exploração da calibragem da tensão de alimentação e dimensionamento do transistor possibilitou uma redução de até 24.84% do consumo de energia. .

1 INTRODUCTION

The Internet of Things (IoT) has emerged to be one of the major mainstream trends, shaping technology development and the industry. The IoT concept englobes the shift from an internet which used to interconnect end-user devices to, nowadays, interconnect physical objects that communicate with each other and/or with humans (MIORANDI et al., 2012). The IoT rise alongside battery technology improvements has provided us with portable, powerful and useful equipment for our daily routine, with wireless communication making information available anytime and anywhere (MANOLI, 2010).

IoT devices have been applied in many different scenarios, from improving building maintenance, to sensoring remote areas for environmental observation and even in cars, for better safety and comfort. However, while many devices have to be connected to the power grid, sensor nodes are expected to be self-sufficient. Additionally, batteries, the traditional means of powering self-sufficient systems, need to be replaced and/or charged, which means maintenance must be frequently performed (BLEITNER et al., 2018). Given that, energy harvesting in combination with rechargeable batteries has become a viable way to alleviate the power source and consumption dilemma (MANOLI, 2010).

Energy harvesting makes use of readily available power sources in the vicinity as for example motion or vibration induced kinetic energy, solar and electromagnetic or temperature gradients. A number of viable solutions are already present on the market, like self powered wireless light switches and electro-magnetic generators, which converts vibrations available in industrial plants for powering wireless monitoring sensors (MANOLI, 2010) (BLEITNER et al., 2018). Although, regardless of the sensors power supply, it will be always restricted by its power budget, with devices which are able to perform their functionality under heavy power constraints being essential for IoT. In traditional Complementary Metal Oxide Semiconductor (CMOS) circuit design aimed at Ultra Low Power (ULP) applications, the ideal circuit is the one that performs a given task or functionality while consuming the least amount of energy. Such circuits are achieved under transistor sizing and supply voltage tuning, and are technology and application-dependent.

Nevertheless, the performance of a system operating in its minimum energy per operation point may exceed the power budget of a given application. For example, with an application such as presented in (FOJTIK et al., 2013), where the device is only active

once per hour, with 80% of its power consumption being due to standby power. In such a case, the minimization of energy-per-operation seems to be suboptimal in comparison to a idle power minimization kind-of solution. The minimization of supply voltage brings advantage for certain energy harvesting approaches such as thermo-electric. Such harvesting technique can result in DC voltage levels from tens to even hundreds of milivolts (KHAN; DAHIYA; LORENZELLI, 2014).

Technology scaling is a major factor in the ascendance of IoT, providing higher transistor densities and voltage scaling due to the miniaturization of gate dimensions, internal capacitances and resistances. These two parallel events contributed for the emergence of IoT (ISLAM et al., 2010). Alongside, with the advance of transistor technology, new challenges were introduced due to the scale down, as aging effects, high power consumption due to leakage current and an increase in the sensibility to transient faults due to radiation and variability (ABBAS et al., 2015).

The Fin Field Effect Transistor (FinFET) transistor technology has been adopted to overcome those challenges. FinFET devices present superior channel control due to the reduced Short Channel Effects (SCE) and low (if none) Random Dopant Fluctuation (RDF) effect due to the fully depleted channel (FARKHANI et al., 2014). Although, at deep technology nodes, variability is one of the most challenging factors, including on FinFET devices. Variability introduces behavior changing geometrical inconsistencies to the final manufactured product. Such variations influence the circuits metrics, hastening its degradation and deviating from its correct operation regime (ABBAS et al., 2015) (NASSIF, 2008).

Given the energy constraints of IoT applications and the variability impact on recent nodes, the Schmitt Trigger (ST) circuit has been pointed as an alternative. The classical ST has been employed as a key element for several ULP circuits (KULKARNI; KIM; ROY, 2007; HAYS, 2012; MELEK et al., 2017; LOTZE; MANOLI, 2017) and for variability mitigation, mainly attenuating the deviation on the power consumption. ST was applied replacing internal inverters of full adders (FAs) in (DOKANIA; ISLAM, 2015) where spreads in major metrics were successfully limited. Also, the same experiment was executed at electrical and layout levels considering FinFET technology, and showed a considerable decrease in overall variability impact on metrics (TOLEDO et al., 2018; MORAES et al., 2018). However, with a considerable increase in delay and power consumption. In addition to previous work, this work will present further analysis related to the Schmitt Trigger technique applied on FAs, with the classical ST being considered,

apart from the original analysis with only a low power ST. Furthermore, a considerable part of this work consists of evaluations about the behavior of the classical ST, the Stacked Inverter Gate (SIG) (BOSE; JOHNSTON, 2018) and Triple Inverter Schmitt Trigger (TIST) (LUO et al., 2017) over several scenarios of sizing, supply voltage, and process variability level, in order to identify the most appropriate set of characteristics for each design.

This work is divided into five further sections: Variability Effects and Mitigation Techniques, where a theoretical foundation about variability is laid with several related works about mitigating its impact, FinFET Technology and Variability Impact, will show the characteristics of FinFET devices and how process variability presents itself in the device. A section about the considered circuits will explain their functionality and applications. Objectives section, will lay the main objectives based on the beforehand laid concepts. The Methodology section will explain the experimental setup which will be employed to generate the results. A Results section is present, showing some preliminary results and analysis. Lastly, there are a Conclusions and Future Works sections.

2 VARIABILITY EFFECTS AND MITIGATION TECHNIQUES

As process technology scaling advanced, decreasing the transistor dimensions, the ratio between device size and atom-size have been decreasing as well. Multiple techniques have been developed to reduce the loss of precision due to the manufacturing process at different end-of-lines. However, as the quantum-mechanical limit approaches, manufacturing-induced imprecision impact rises (ASENOV, 1999).

Variability consists of characteristic deviations, internal or external to the circuit, which can determine its operational features and can be divided by three types concerning its sources:

Environmental Factors or use-induced variation is mostly external to the circuit, it englobes variations in the power supply voltage and temperature. Voltage drops mainly occur due to abrupt changes in the switching activity, inducing large current transients in the system both locally or globally across the die. Local temperature within the die can cause variations in the device mobility and threshold voltages (V_T), and wire resistance. It is highly design dependent with timing constants similar to clock frequency (NASSIF, 2008) (BERNSTEIN et al., 2006).

Reliability Factors are related to the aging process of the circuit. Circuit aging is defined by numerous phenomena: Negative Bias Temperature Instability (NBTI) which mines the performance of p-channel due to the weakening of Si-H bonds in the oxide generating interface states and trapping positive charges while the device is operating (WANG et al., 2008), electromigration due to high enough current densities causing the gradual movement of metal ions due to the electron-ion momentum transfer (YOUNG; CHRISTOU, 1994), time dependent dielectric breakdown due to current flowing through gate oxides (LOMBARDO et al., 2005) and Hot Carrier Injection (HCI) trapping electrons on oxide which degrades n-MOSFET on-current (TAKEDA; SUZUKI, 1983) (NASSIF, 2008) (BERNSTEIN et al., 2006).

Physical Factors are caused by the manufacturing process, consequence of imprecisions in the manufacturing process, resulting in characteristic deviations of active and passive components. Those variations can be:

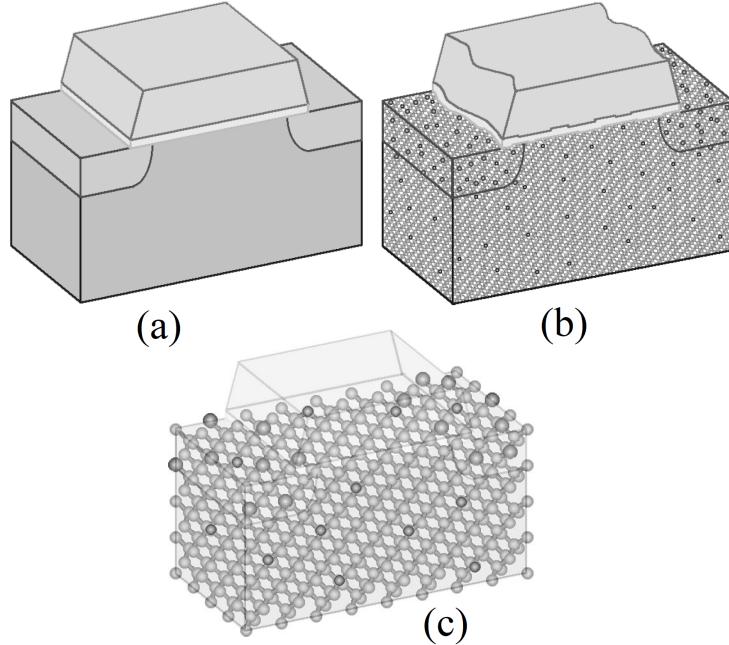
- Systematic or extrinsic: is related to unintentional imprecisions in the manufacturing process, not associated with fundamental atom-related problems. Extrinsic variability can present itself in multiple ways, from different lots, from different wafers within a lot, across wafers and even from chip to chip. The main contrib-

utor for extrinsic variation is the chip to chip variability, with its sources being both by-wafer and by-reticle process steps. By-wafer variability is caused by three manufacturing steps: rapid thermal anneal - with a uneven temperature distribution across the wafer, photoresist development and etching and by-reticle variability can contribute due to changes in the focus as the mask is stepped across the wafer in the photolithography process. The focus can suffer deviations due to exposure tool lens astigmatisms or by wafer nonplanarity. Additionally, the within-chip variability can be divided into two types. The similar-structure variability, consists of across-wafer and across-reticle variations that each chip ends up intercepting, and the dissimilar-structure which consists of variations caused by processing steps that differ by structure and layout variations of structure (difference of orientation for the same structures in the layout as well as variations in polygon densities) (BERNSTEIN et al., 2006).

- Design dependent: variations related to the placement can results in changes in the electrical parameters of active and passive devices. The sources of such type of variability include manufacturing related deviations. Manufacturing variability may be systematic, having a well-known relationship between design or layout and the final electrical parameters values. Chemical-Mechanical Polishing (CMP) relationship between the thickness of the metal and the layout feature density (STINE; BONING; CHUNG, 1997). The main difference between systematic and random variability is the way it is treated at design time. Systematic variability can be modeled and anticipated, allowing the designer to tune the layout or timing for mitigation. Random variations, however, require the designer to add time margins in order to guard against the worst timing possible (NASSIF, 1998).
- Random or intrinsic: consists of atomic-level deviations between devices (even when they are identical in layout and geometry). These deviations appear in dopant profiles, thickness variations, and Line-Edge Roughness (LER). Dopant fluctuations are the main cause to V_T variations (ASENOV et al., 2003), with the removal of doping from the channel contributing for the V_T variation reduction, introducing the necessity to set the V_T by gate-metal Work Function (WF) or by biased back gate (FRANK et al., 2001; WONG et al., 1999). Fluctuations in doping levels and device features cause variations in the source/drain regions, which affects the overlap capacitance and the source resistance (FRANK; WONG, 2000). LER arises from variations in the total number of incident photons during lithography. Such

roughness introduction into the polygons geometry may determine the effective gate width as one moves along the x axis of a Field Effect Transistor (FET) (BRUNNER, 2003). Another source of intrinsic device variability rises from the atomic-scale oxide thickness variation. It can introduce variations in the V_T (ASENOV et al., 2003), in the oxide tunneling current, and may cause mobility degradation due to the potential variation across the Metal Oxide Semiconductor FET (MOSFET) channel (BERNSTEIN et al., 2006). Fig. 2.1, depicts the transistor intrinsic variability.

Figure 2.1: Levels of abstraction from a ideal transistor concept towards a realistic and "atomistic" device concept. (a) Depicts a the current approach of semiconductor device simulation, with continuous dopant charge and smooth boundaries. (b) Depicts a 20-nm MOSFET, with less than 50 Si atoms along the channel. RDF, interface roughness and LER introduce considerable intrinsic parameter fluctuation. (c) Depicts a 4-nm MOSFET, with less than 10 Si atoms along the channel.



Source: Asenov et al. (2003)

Table 2.1: Impact of variability on performance and power.

Property	Ease of measuring	Variability	Effects of variability	Effect of missing specification
Performance	Medium	Medium: up to 60%	L, W, R, C, V_T , μ	Slower product, yield, timing error
Leakage Power	Easy	Large: up to 148%	L, V_T , μ , t_{ox}	Shorter battery life, yield, heat
Dynamic Power	Difficult	Workload dependent	C, α	Shorter battery life, heat

Source: Rahimi, Benini and Gupta (2016)

Table 2.1 illustrates the variations impact on performance and power. As a way to handle timing errors due to variations in the path delay, circuit designers commonly

add safety timing margins to the voltage and/or the clock frequency (guardband). Such practice leads to overly conservative designs due to the guardband overlapping and accumulation in the ever increasing multi-corner analysis (AUSTIN et al., 2005).

In (JEONG; KAHNG; SAMADI, 2009) the impact of each individual variability source: Process, Voltage and Temperature (PVT) is quantified concerning a standard inverter cell through SPICE simulations. A 1.8x delay variations was observed, with 1.46x, 1.25x and 0.97x coming from the process, voltage and temperature variations, respectively. Under the same operation conditions smaller supply voltages for a 80-core Intel processor, it was observed a normalized deviation of 5.93%, 6.37% and 8.64% for 1.2 (nominal), 0.9, and 0.8V, respectively. The lowering from 1.2 to 0.8V increases the critical path variability up to 45% (DIGHE et al., 2011).

Near-threshold operation has become a popular technique to achieve energy-efficient digital circuits. Although, operating at low voltages exacerbates the effects of delay variations (JEON et al., 2012; DRESLINSKI et al., 2010; RITHE et al., 2011; KAKOEE; LOI; BENINI, 2012; PAWLOWSKI et al., 2012). The measurement of Within-Die (WID) delay was performed for a 45nm Single Instruction Multiple Data (SIMD) processor, showing that reducing V_{DD} from 1.0 to 0.53 V increases delay variation by 6x (PAWLOWSKI et al., 2012).

Given the increase in performance variation, there is the need for mitigation methods to make the design resilient to timing errors, especially for circuits at low voltage operation regimes. There are several approaches to how and when errors should be manipulated as well as their abstraction levels. Among the steps there are: Predicting and Preventing, Detecting and Correcting, and Accepting. And among the abstraction levels there are Application Algorithm, Software, Architecture and Circuit. Since this work aims to investigate variability impact at layout level, some circuit-level techniques will explained next with higher level techniques being thoroughly explained at (RAHIMI; BENINI; GUPTA, 2016).

Tuning CMOS knobs consists of several approaches to tune electrical characteristics (e.g., power and delay) of circuit by interfering with the body bias supply voltage and clock frequency, for example. Forward body biasing reduces the V_T (improving performance and increasing leakage power) while reverse body bias increases the V_T (reducing performance and leakage power). Given so, a slow circuit block can have its performance improved upon forward body biasing while a leaky circuit can be reverse body biased. Additionally, voltage and/or the circuit's frequency can be tuned to compensate variations

(DIGHE et al., 2011; TSCHANZ et al., 2002; BORKAR et al., 2004).

There are topology changes employed during design time CAD optimizations in order to enhance the circuit resiliency against timing errors. Due to the general presence of clusters of critical paths in circuits some approaches focus on uncertainty-aware circuit optimizations (BAI; VISWESWARIAH; STRENSKI, 2002). Optimization such as upsizing and downsizing of gates, use of multiple V_T cells, and restructuration of the path delay distribution (KAHNG et al., 2010).

Lastly, asynchronous circuits have been proposed since there is no need for a clock signal to determine a starting time for computation. In (CHANG et al., 2013) both versions (synchronous and asynchronous) of 8051 microcontroller are designed. When PVT and workload variations are introduced, the synchronous version required 4x, 1.5x, and 2x delay margins while the asynchronous version operated at nominal performance.

In order to mitigate variability impact, many works try to indicate the most robust design for a given type of circuit. For example, in (DOKANIA; IMRAN; ISLAM, 2013) twelve different FA topologies are analyzed considering delay, power and Power-Delay-Product (PDP) variability. It is used a 16nm bulk CMOS technology node in SPICE simulations with PVT variability being considered and Monte Carlo simulations performed. The authors concluded that Cell A, CLRCL and Cell B FAs presented the best results for all three metrics (Delay, Power and PDP).

In (AMES et al., 2016) the effects of PVT variability in different FA designs are investigated. The simulations are performed in HSPICE with the bulk CMOS 32nm node technology. With Transmission Gate Adder (TGA) and Transmission Function Adder (TFA) architectures showing acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested FAs - 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) FA.

In (ISLAM; HASAN, 2011) various popular 1-bit digital summing circuits functionality and robustness are analyzed in light of PVT variations with the best FA being simulated in Carbon Nanotube Field Effect Transistor (CNFET) technology for comparison with the bulk CMOS version. The simulations are carried at the 22nm bulk CMOS and CNFET technology node in HSPICE. Its results show that the TGA has the strongest PVT variability robustness and its CNFET version provides over 3x, 1.14x and 1.1x less propagation delay, power dissipation and energy delay product (EDP) variations, respectively. This work does not consider the total power consumption of each FA separately.

Some articles analyze the adoption of new technologies: (GUDURI; ISLAM,

2015) proposes a hybrid of bulk CMOS and CNFET FA at 16nm in deep subthreshold operation region for ULP applications simulated in SPICE which showed some improvement over its bulk CMOS FA counterpart achieving 5% and 1% improvement in power, power-delay and energy-delay products and their variability, respectively. In (ISLAM; AKRAM; HASAN, 2011) a new subthreshold-FinFET FA is proposed and compared over multiple FAs showing huge metric improvements provided by the FinFET technology up to 2.22x improvement in power variability. It was simulated in 32nm predictive technology model on HSPICE.

It is notable that none of these works consider a layout approach for its simulations and do not address any novel general technique which can be applied to a range of different types of circuits. Although, some works introduce novel designs.

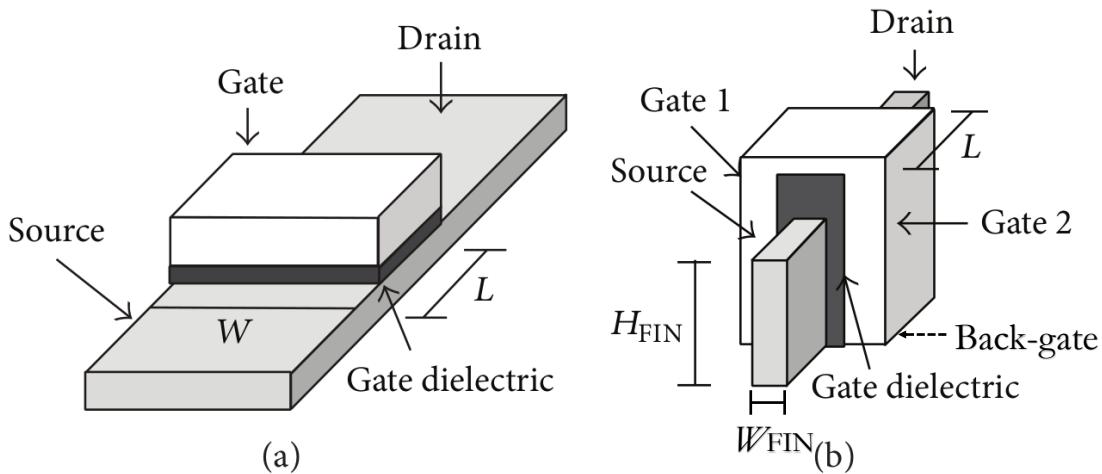
(FEDERSPIEL et al., 2012) presents reliability comparison between 28nm bulk CMOS and Fully Depleted Silicon On Insulator (FDSOI) technologies at layout level, with FDSOI showing 32% improved performance, 40% reduced power consumption and improved matching, with its intrinsic reliability behavior similar to 28nm bulk at the device level. (ALIOTO; PALUMBO, 2007) presents a study about the delay variability caused by supply variations in the TGA. The experiments were performed at 90nm and 180nm bulk CMOS Technology in Spectre at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TGA presenting worse results 15% (25%) for the 90 nm (180 nm) in comparison to static logic.

Some works focus on evaluating techniques: In (ZIMPECK et al., 2016) three transistor sizing techniques are applied on a set of cells and their impact on variability robustness is analyzed. The simulations were performed considering a 14nm FinFET technology using HSPICE tool. The authors concluded that the Optimized Transistor Sizing (OTS) technique has the best ratio between nominal PDP and PDP under process variability. (AHMADI; ALIZADEH; FOROUZANDEH, 2017) introduces a new technique to improve the performance of digital circuits in the presence of variations. It consists of a hybrid of two former methods to prevent errors due to delay variations. The simulations were performed with a 45nm predictive technology using HSPICE and applied on ITC'99 and ISCAS'89 benchmarks circuits. The results show that the hybrid technique can tolerate process variations up to 27.3% better than previous state-of-the-art techniques.

3 FINFET TECHNOLOGY AND VARIABILITY IMPACT

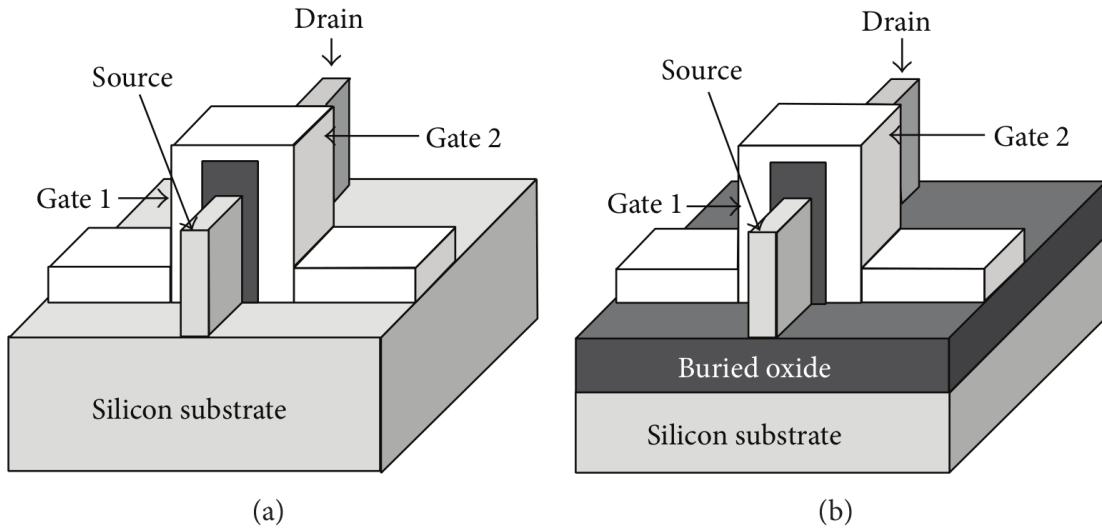
New commercial technologies have been developed for mitigation of variability impact. The Fin Field Effect Transistor (FinFET) remains as one promising new technology for variability mitigation while maintaining technology scaling. The FinFET main geometric parameters are the gate length (L or L_G), fin width (W_{FIN} , T_{FIN} or T_{SI}), fin height (H_{FIN}) and Oxide Thickness (T_{OX}). FinFET transistors can be built on a traditional bulk or on a Silicon on Insulator (SOI) substrate with a conducting channel that rises above the level of the insulator, creating a thin silicon structure, the gate, as shown in Figures 3.1 and 3.2. FinFET devices can be shorted-gate (3 gate nodes) or independent-gate (4 gate nodes). The shorted gate model is similar to the traditional MOSFET given that the front-gate and back-gate are connected and controlled by the gate signal. The independent gate has 4 nodes, making possible to connect the front and back gate to different voltage values.

Figure 3.1: Structural comparison between (a) planar MOSFET and (b) FinFET transistors.



Source: Bhattacharya and Jha (2014)

Figure 3.2: Structural comparison between (a) bulk and (b) SOI FinFETs.



Source: Bhattacharya and Jha (2014)

The channel being surrounded from three dimensions by the gate results in a superior control, reduced SCE and RDF effect due to the fully depleted channel that causes less sensitivity to process variations (TAUR; NING, 2013). FinFETs also present relative immunity to gate LER, a major source of variability in planar nanoscale FETs (KING, 2005). The disadvantage over MOSFETs is the harder manufacturing process due to difficulty in the lithography steps as it is increasingly difficult to print small patterns, the increased variability impact due to the further miniaturization of dimensions, in comparison to MOSFET and a more costly manufacturing process due to the need of techniques to address the manufacturing imprecision and, in the case of SOI FinFET, to change the CMOS substrate process to support a SOI substrate manufacturing process (KING, 2005) (MANOJ et al., 2007).

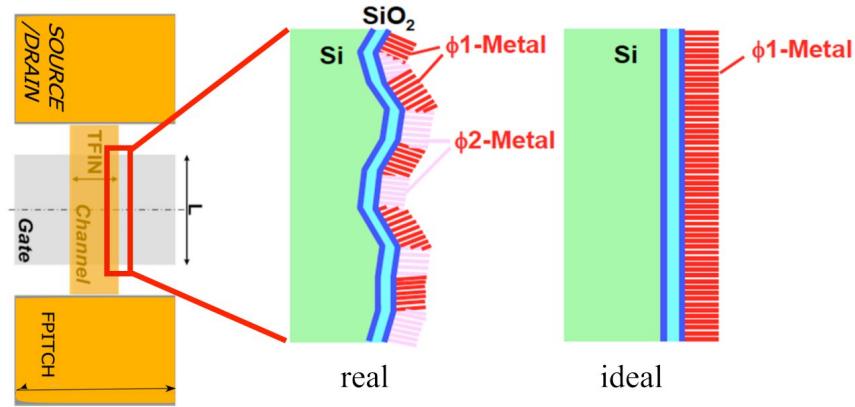
Given the elevated levels of gate leakage due to the scaling down of the gate oxide, insulating materials with higher dielectric constant (high-k) have been introduced. Although, with the high-k dielectric adoption, challenges such as Fermi level pinning (HOBBS et al., 2004) and phonon scattering (GUSEV; NARAYANAN; FRANK, 2006) rised, being necessary the replacement of the traditional polysilicon gate electrode by a metal gate electrode (GUSEV et al., 2001; DATTA et al., 2003).

In the bulk FET devices in nanotechnologies, the variations in the gate length was the dominant parameter related to I_{ON} deviations due to the RDF effects. Although, as a results of the shapes of the fin-like structures in FinFET, the channel is prefered to be low-doped in order to minimize threshold voltage variations. Given so, threshold voltage

is mainly set by the workfunction.

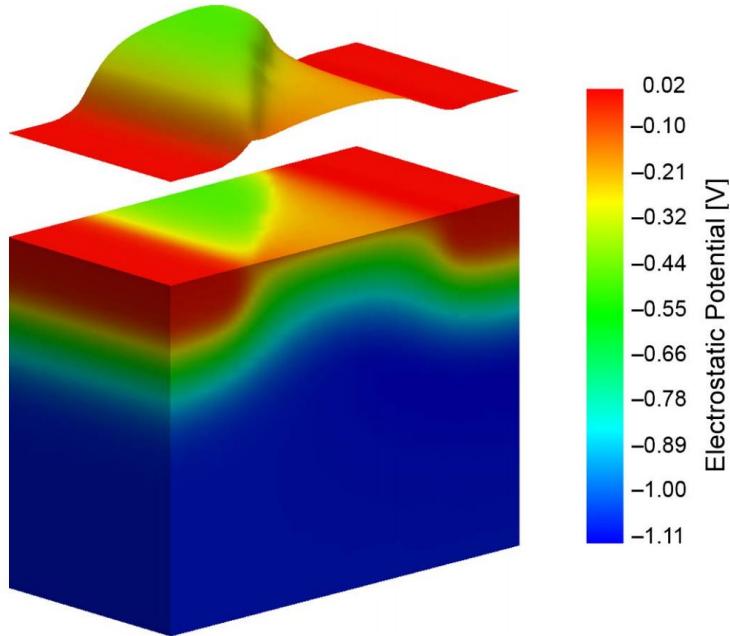
Metals exist *in natura* in the form of crystals where each atom has several bonds with adjacent atoms. Although, due to defects and disorientations, several crystals are formed, with "grain boundaries" between regions of regularity (crystal grains) in the metal (DADGOUR; DE; BANERJEE, 2008), as shown in Fig. 3.3. The electrostatic potential (e.g. V_T) varies depending on each grain boundary, as shown in Fig. 3.4. At Table 3.1 a example of possible orientation, probability and WF is given. Between several technology nodes - FD-SOI, Bulk and FinFET - the latter showed the lowest V_T variation due to the much larger gate area (DADGOUR; DE; BANERJEE, 2008).

Figure 3.3: Metal fabrication ideal and real aspects.



Source: Meinhardt, Zimpeck and Reis (2014)

Figure 3.4: Electrostatic potential in a generic 30-nm MOSFET with the surface potential shown below. The metal gate has two grains with the grain boundary diagonally across the channel.



Source: Brown et al. (2010)

Table 3.1

Orientation	Probability	Work Function
<200>	60%	4.6 eV
<111>	40%	4.4 eV

Source: Brown et al. (2010)

The WFF impact can be better understood when considering the equation 3.1, where the threshold voltage for multigate devices is expressed, where Q_{SS} represents the charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} represents metal-semiconductor work-function difference between the gate electrode and the semiconductor, f_f is the fermi potential. Additionally, the fermi potential for the P-type silicon is given by equation 3.2, where N_A is the acceptor concentration and n_i is the intrinsic carrier concentration (COLINGE et al., 2008). The effects of Q_D and Q_{SS} onto the threshold voltage (V_{th}) are almost negligible compared to f_f , in ultrathin body and lightly doped devices, like the FinFET. Additionally, V_{in} is the additional surface potential to $2f_f$, of ultrathin body devices, that is needed to accumulate enough inversion charges into the channel region of the transistor to reach the threshold point (MUSTAFA;

BHAT; BEIGH, 2013).

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3.1)$$

$$f_f = \frac{kT}{q} \ln \frac{N_A}{n_i} \quad (3.2)$$

Several works analyze the FinFET reliability. It is shown in (MEINHARDT; ZIMPECK; REIS, 2014) the major influence that WF Fluctuations (WFF) exercise over V_T variations of several standard cells. In addition, in (WANG et al., 2011) it was shown the high correlation between the I_{ON} and I_{OFF} currents and V_T fluctuations due to the granularity of the metal gate.

In (HARRINGTON et al., 2018) it is shown, at 14/16nm fabricated bulk FinFET technology, that for high energy charged particles, the drive current is the dominant factor to the transient fault pulse width and cross-section. And low energy particles have a greater dependence on secondary transistor and circuit design factors (number of fins, transistor arrangement, etc).

In (REN et al., 2018) the HCI effect is analyzed in pass-gate FinFET transistors. The tests were executed using commercial FinFET technology showing a 50% chance of errors due to HCI in pass-gate transistors. In (XIONG; BOKOR, 2003) a analysis of the sensitivity of double-gate and FinFET devices to process variations is shown. It is concluded that for 20nm FinFET devices large channel doping concentration is necessary to obtain suitable values of V_T if heavily doped polysilicon gates are used. Due to the small volume of the channel the channel doping will bring unacceptable V_T fluctuations. Given that, heavily doped polysilicon may not be a viable choice with the work function adjustment being a better approach.

In (ZHANG et al., 2017) the modeling of the reliability degradation of a FinFET-based Static Random Access Memory (SRAM) is shown. It is concluded that the probability of failure due to NBTI and Gate Oxide Break Down (GOBD) is relatively lower in comparison to HCI-induced failures. They also show the improvement of lifetime due to Error-Correcting Code (ECC) memory. In (LIAO et al., 2008) a investigation on reliability characteristics of NMOS and PMOS FinFETs is conducted. Based on fabricated FinFETs transistor with 17-27 nm width, it was shown that the life time of FinFET is very dependable of its dimensions. The predicted lifetime for a 50nm gate length NMOS FinFET was 133 years, for the first HCI event. While a 27nm fin-width PMOS FinFET

showed 26.84 years of lifetime which is reduced to 2.76 years when reducing its fin-width from 27 to 17 nm for a NBTI event, showing the huge reliability challenge introduced by technology scaling.

4 CONSIDERED DESIGNS

STs circuits present a hysteresis characteristic. This hysteresis exists in the presence of two switching V_T . If the input level is within the hysteresis region, the ST shall not switch. Such characteristic gives a higher static noise margin (SNM) in comparison to traditional inverters, ensuring a high noise immunity.

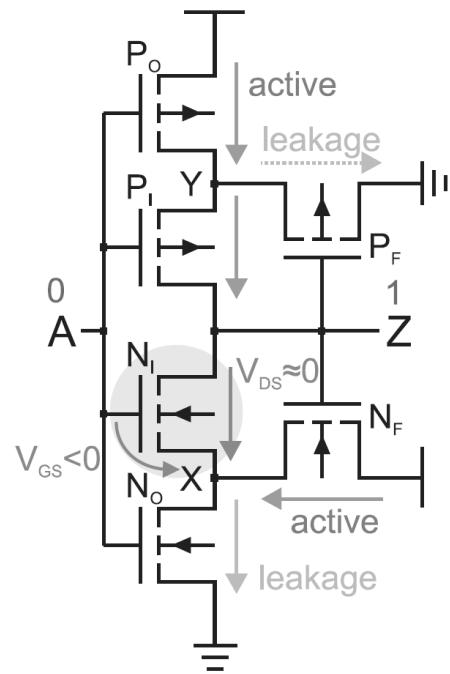
Variations in physical parameters became alarming at ultra-deep sub-micron (UDSM) nodes because the node scaling was accompanied by a supply voltage scaling, making the circuits more susceptible to noise and electromagnetic interference due to the deterioration in SNM (PAL; ISLAM, 2018). Given that, this work explores a two types of STs.

4.1 6T Traditional ST

The first is the 6T traditional ST where the main difference from the most common versions is the presence of P_F and N_F devices as shown in Fig. 4.1 (DOKI, 1984). These transistors are responsible for a feedback system. For example, if the output is in a high level, the N_F is on, pulling the node X to a high potential, and forcing the drain-source voltage of transistor N_I almost zero and its gate-source voltage into the negative region. This kind of arrangement reduces the leakage current N_I exponentially, increasing the on-to-off current ratio, and minimizing the output degradation (LOTZE; MANOLI, 2017).

The main effect of process variability is a shift on the voltage transfer curve (VTC) due to the threshold voltage variation. Usually, the input voltage, where a device starts delivering current, is directly dependent on the V_T . Thus, the variability impact on VTC is reduced in the ST as a result of the high influence of the gate-source voltage of the inner transistor (N_I and P_I) over its switching point (LOTZE; MANOLI, 2017).

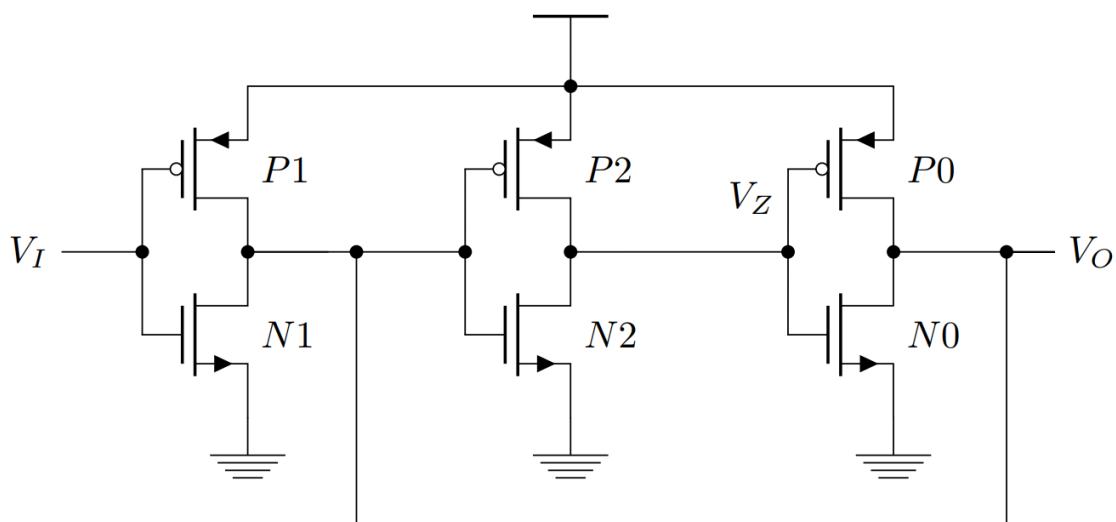
Figure 4.1: ST inverter leakage suppression (LOTZE; MANOLI, 2017).



4.1.1 Three Inverter Schmitt Trigger (TIST)

The TIST, shown in Fig. 4.2 is a ST implementation, most common in textbooks. It has been mostly unexplored for low power applications. It consists of a CMOS inverter followed by a latch.

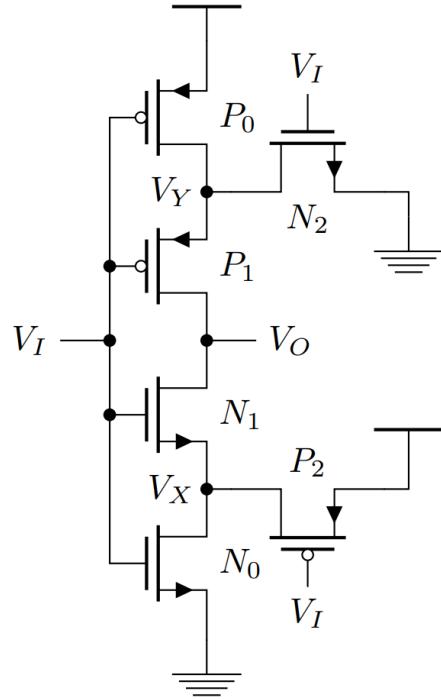
Figure 4.2: TIST schematic (RABAHEY; CHANDRAKASAN; NIKOLIC, 2002)



4.1.2 Stacked Inverter Gate (SIG)

SIG, shown in Fig. 4.3, is a circuit composed of unbalanced inverters without positive feedback, referred to as stacked, or redundant, inverters. It presented improvements over the CMOS inverter regarding voltage gains (BOSE; JOHNSTON, 2018; LUO et al., 2017).

Figure 4.3: SIG schematic (BOSE; JOHNSTON, 2018)



A variety of CMOS STs have been proposed and implemented over the years based on different requirements. A higher performance ST is proposed in (STEYAERT; SANSEN, 1986) where, by a different design, a smaller load capacitor value is achieved, decreasing the slew rate of the ST internal node. In (PFISTER, 1992) a ST with a programmable hysteresis is proposed. The programmable hysteresis is achieved by adding a P and N transistors in series with the 6T ST P_F and N_F transistors, respectively, both receiving the same gate signal. (KIM; KIH; KIM, 1993) proposes a 10T ST which its hysteresis interval does not depend on transistors width/length ratios being, consequently, more robust to process variations.

A low-power ST is proposed at (AL-SARAWI, 2002) with low short circuit current achieved by the presence of only one path to each power rail, being recommended for low power, very low frequency applications. In (PEDRONI, 2005) proposes a low-power ST by having only one transistor transmitting (at stable output values), considerably reducing

power consumption. STs can be optimised by adequate dimensioning as well as stated in (TACHE et al., 2018) where the OTS technique presented the best metrics for low power applications, in accordance to (ZIMPECK et al., 2016).

In (DOKANIA; ISLAM, 2015) a novel technique based on the replacement of FA's internal inverters with low voltage STs for PVT variability robustness improvement is originally introduced and applied on seven different FA designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in PDP. Although, the improvements occur at the cost of an increase in the area and power dissipation of each design.

Alongside, in (TOLEDO; ZIMPECK; MEINHARDT, 2016) the ST technique is applied on four FAs. It presented promising results regarding the power deviation due to the process variability with a decrease up to 79% with a drawback of a significant increase in average energy consumption. The simulations were performed with the 16nm technology predictive technology model in NGSPICE.

This technique is tested in several works: In (AHMAD et al., 2016) it is presented a novel Schmitt-trigger-based single-ended 11 Transistor SRAM cell. It analyses its performance against seven different SRAM topologies. The novel cell showed the least energy consumption per operation with the smallest leakage power and a 6.9x higher I_{ON}/I_{OFF} ratio. Further PVT variability simulations confirmed the robustness of the design regarding read and write operation. The simulations were carried in 22nm predictive technology using HSPICE. (MOGHADDAM; MOAIYERI; ESHGHI, 2017) presents a ST buffer using CNFET. It was evaluated against other two buffers and showed, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain considering PVT variability robustness. The simulations were carried in 16nm Stanford CNFET model using HSPICE.

In previous work (MORAES et al., 2018) the ST technique is evaluated considering 4 different FAs layouts at 7nm FinFET. 64.74% and 66.6% reduction in delay and power deviation was achieved.

STs are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. On a typical input (non-ST), its binary value will switch at the same point on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit causing a shift in

the threshold voltage.

If the threshold shifts, it will cross the input causing it to switch again. It can go indefinitely causing oscillation. The same thing can happen if there is noise on the input. STs are applied in these cases to filter noise introducing superior and inferior threshold voltages.

For the experiments, there were considered four different types of Full Adders topologies to evaluate their robustness to process variability with their internal inverters replaced by Schmitt Triggers. The Full Adders listed below have been chosen due to their promising results in related and previous works (AMES et al., 2016; DOKANIA; ISLAM, 2015; DOKANIA; IMRAN; ISLAM, 2013; MORAES et al., 2018):

1. Complementary MOSFET Adder (CMOS)
2. Transmission Gate Adder (TGA)
3. Transmission Function Adder (TFA)
4. Hybrid Full Adder

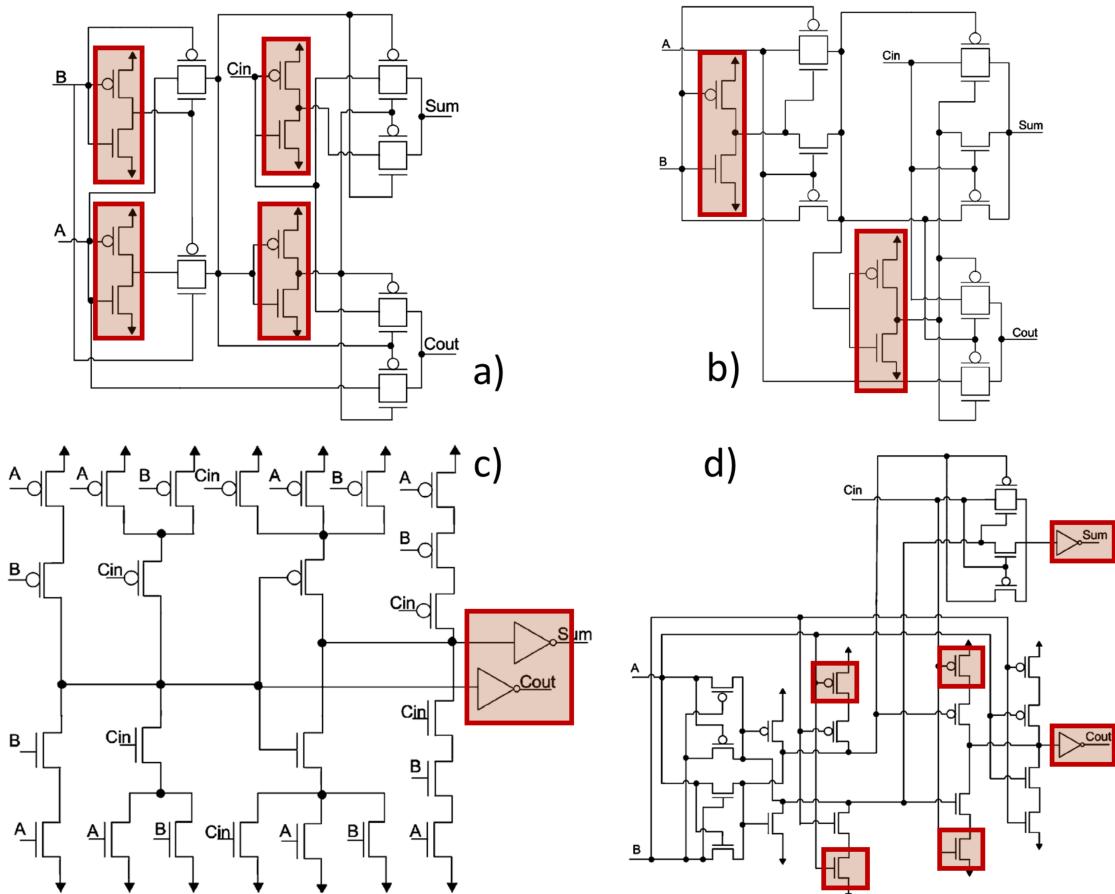
The Mirror Full Adder is considered the most traditional Full Adder topology containing 28 Transistors arranged in a pull-up and pull-down networks, which are logically complementary. It has a full voltage swing and buffered Sum and Cout signal and the advantages of good conductibility and robustness when working with novel technologies and low voltages. However, it has high capacitance because each input is connected to the gate of at least a p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) device additionally, it shows the impact of the pull-up network that makes the circuit slower due to the low mobility of its holes (BECKETT, 2002) (DEVADAS; KISHORE, 2017) (ISLAM; HASAN, 2011).

Transmission Gate Full Adder (WESTE; ESHRAGHIAN, 1985) contains 16 transistors, and is a high speed and low power design. However, shows low driving capability which may be unacceptable in some cases where there is a long chain of full adders due to the increase in delay (ISLAM; HASAN, 2011). The Transmission Function Adder is based on transmission gates as well, containing 20 transistors, working satisfactorily with low voltages but losing performance when cascaded due to the lack of supply/ground contacts and, consequently, driving capability (NAVI et al., 2009). Both TFA and TGA generate the XOR function ($H = A \text{ XOR } B$) followed by an inverter which produces the XNOR function (H'). H and H' are used to control the transmission gates generating the Sum and Cout outputs. The inverter generates delay between H and H' , which will cause

the transmission gates to behave as pass transistors, that may introduce glitches and consequently, increase the power consumption of these cells. Additionally, TGA contains three inverters, one more than TFA. The inverters switching introduce more short-circuit power (SHAMS; BAYOUMI, 2000).

Inspired by CMOS and CPL Full Adders architectures, the Hybrid Full Adder (NAVI et al., 2009) contains 26 transistors, with the main advantage of a high output signal and low power properties. Although, the design shows high input capacitance for specific input vectors. The Full Adder designs are shown in Figure 4.4.

Figure 4.4: Full Adders with internal inverters to be replaced highlighted.

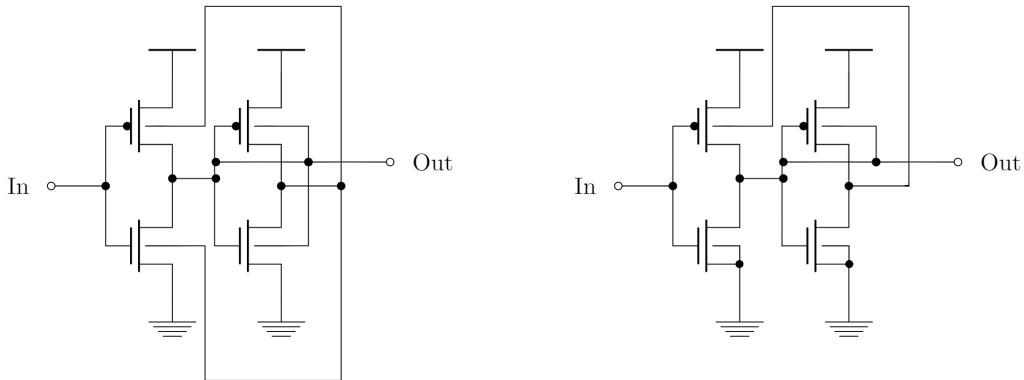


Transmission Gate Adder (a), Transmission Function Adder (b), Mirror CMOS Adder (c) and Hybrid Full Adder (d). Source: Toledo, Zimpeck and Meinhardt (2016)

The additional ST inverter circuit used in this work was inspired by (ZHANG; SRIVASTAVA; AJMERA, 2003) and modified in (DOKANIA; ISLAM, 2015) to achieve the desired inverting characteristic, as shown in Figure 4.5a. It is designed for operation at a supply voltage of 0.4V in order to achieve low power consumption, and consists of the junction of two inverters where the output from the second one will be the bulk for the first one.

In this design a dynamic body-bias technique is applied through a feedback mechanism to a standard CMOS inverter circuit, thus allowing a change in the threshold voltages of two MOSFETs, implying a change in the switching voltage.

Figure 4.5: Original and modified Low Power STs (LPST) side-by-side



(a) LPST Inverter from Dokania and Islam (2015) (b) Modified LPST Inverter applied in this work.
Source: From the author.

5 OBJECTIVES

Given the laid concepts, this work has two objectives. The first is to identify an appropriate layout, considering the number of fins, and supply voltage in order to achieve a minimum energy device. The considered circuits will be the traditional 6T ST, SIG, TIST and, for the sake of comparison, a traditional inverter. Multiple levels of process variability will be considered. Therefore, depending on manufacturability quality, different recommended layouts and supply voltages can arise. There will be considered the means, standard deviations and normalized standard deviations for each metric, energy, delays on and off currents, current ratios and hysteresis interval (when applicable), respectively.

While, the second objective is to apply the ST technique into FAs, in the case, the CMOS, TFA, TGA and Hybrid FAs. The two ST applied are the traditional 6T ST and the low-power back-gating-based ST from (ZHANG; SRIVASTAVA; AJMERA, 2003). The technique consists of the replacement of the FAs internal inverters with the respective STs. All layouts will be designs with a fixed number of transistors and two levels of supply voltages. All simulations will be performed at the same level of process variability. There will be considered the means, standard deviations and normalized standard deviations for each metric, energy and delays, respectively.

6 METHODOLOGY

To provide an extensive exploration of the process variability effects on the circuits characteristics, this work will evaluate: 1) Circuits operating at multiple combinations of supply voltages; 2) the impact of different levels of process variability; 3) the influence of the transistor sizing; and 4) the impact of these parameters on the maximum achievable frequency within a failure threshold.

The transistor sizing consisted of layouts from 1 to 5 fins through 1-fin steps for the CMOS inverter, the traditional ST and the SIG, since all circuits worked as expected. Since the TIST did not present an adequate behaviour, with its output value getting stuck, a different approach was adopted. The TIST consists of a traditional inverter (transistors P_1 and N_1) followed by a latch (transistors P_0 , P_2 , N_0 and N_2), given so, the inverter transistors were resized following a proportion between their size and the size of the latch transistors. It was adopted two proportions: 2:1 and 3:1, resulting in five different layouts. Three layouts follow a 2:1 proportion with the inverter transistors containing 2, 4, and 6 fins and the latch transistors containing 1, 2, and 3 fins, respectively. Two layouts follow a 3:1 proportion with the ST transistors containing 3 and 6 fins, and the latch transistors containing 1 and 2 fins, respectively. For the sake of simplicity TIST layouts will be referred to as TIST2F1F, TIST4F2F, TIST6F3F, TIST3F1F and TIST6F2F. With such sizing, the TIST worked properly in most cases, with near-threshold voltage operations presenting the highest number of failures.

According to (FERNANDES, 2019), given the small signal analysis presented, depending on the supply voltage of the TIST design, it will present an amplifier or hysteresis behavior with a discontinuous transition between regions where an infinite gain will be present. Furthermore, it was shown that the higher the ratio between the size of the respective inverter and latch transistors, lower is the supply voltage needed to achieve the given region of infinite gain. Given that, the majority of the TIST failures, at nominal operation, occurred around the threshold voltage, and that an increase in the proportion between its inverter and latch transistors decreased the number of failures considerably, the failures are related to the proportion of its transistors and the infinite gain region.

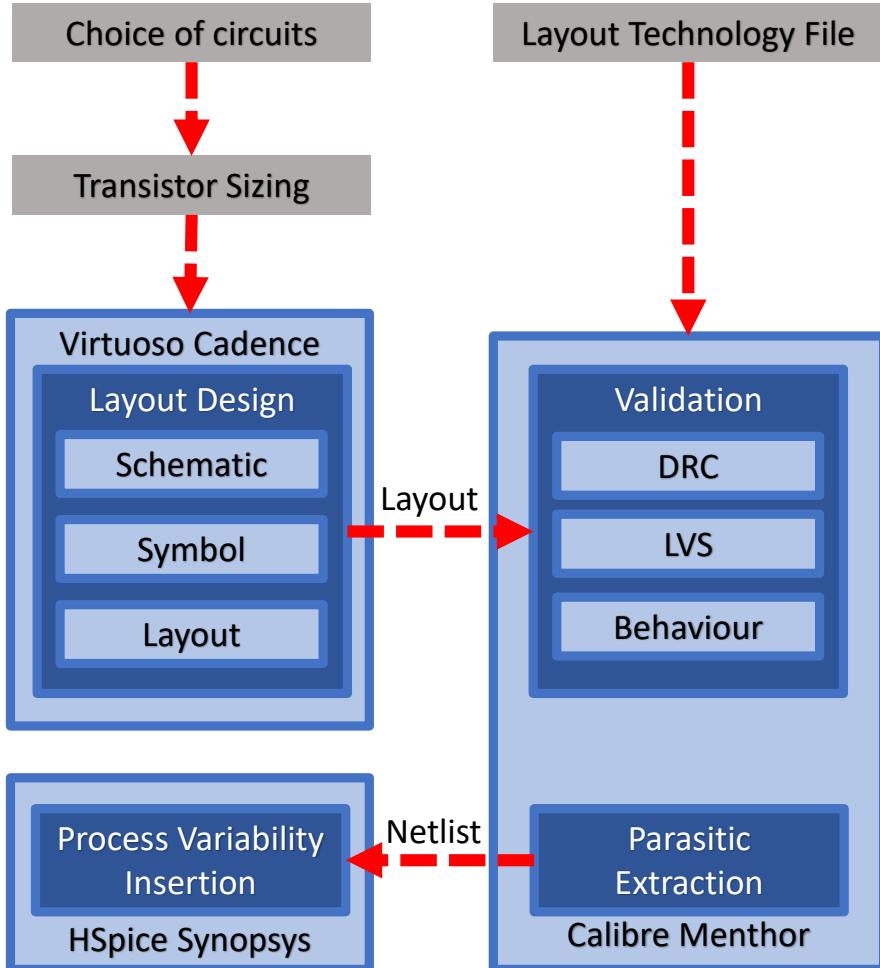
Due to technology restriction it is not possible to decrease the cell height when considering layout with a fin count below 3. In the case of the ST, for the layouts with a fin count below 3, M2 was applied to connect the source/drain of the P_F and N_F transistors to the X and Y layout nodes. For the TIST, for the layouts with less than 3 fins, M2 was

necessary to connect the output signal to the P_2 and N_2 transistors gate. Given the smaller area to work with, it was necessary to apply M2 in order to respect the M1 spacing rules, bringing to light one of the challenges related to a smaller layout. The M2 usage in those cases will increase the design parasitics from the necessary extra vias connecting M1 and M2.

For all the Full Adders layouts it was used a dense 7.5 M2 (Metal 2) track cell, baseline resulting in a 270nm cell height. This corresponds to three fins for each transistor.

The project was divided into two main steps: the layouts designing and electrical simulations. After finishing the layout design process, each layout passed through validation which consisted of a Design Rule Checking (DRC) to detect if the layout obeys the technology geometry restrictions and layer rules, Layout Versus Schematic (LVS) where layout and schematic are compared to detect their equivalence (same nodes and nets) and a Behavioral test, in order to observe if the circuit works as expected. The design flow is shown at Figure 6.1.

Figure 6.1: Design flow of the experiments.



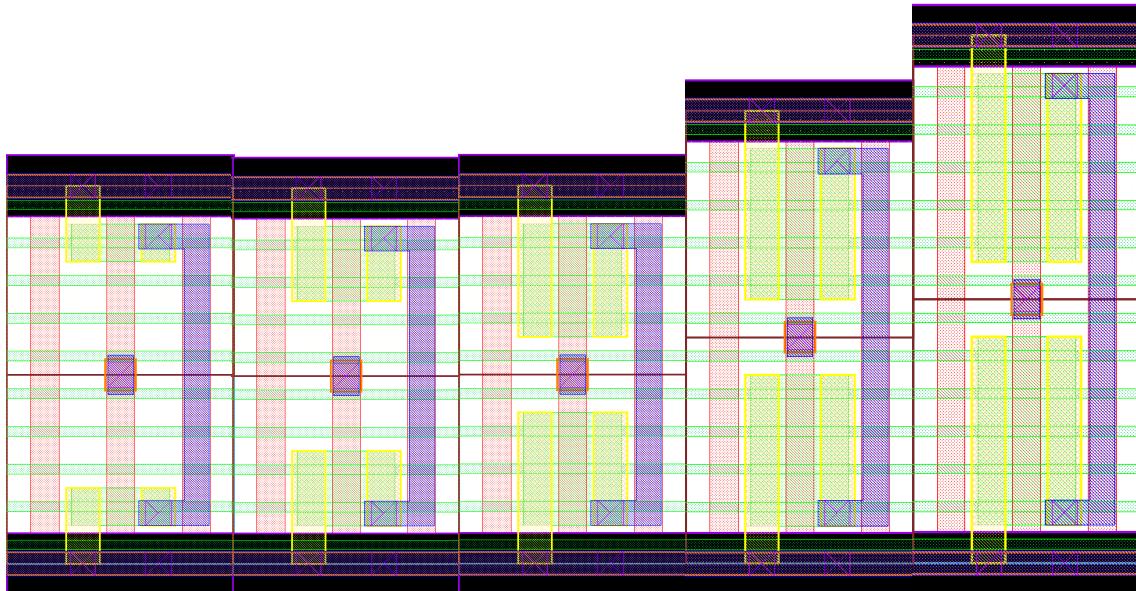
Source: From the author.

6.1 Layout Design

All circuits were designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence® with the process design kit (PDK) of 7-nm FinFET of Arizona State Predictive PDK (ASAP7) from the Arizona State University in partnership with ARM (CLARK et al., 2016). It is the only available 7-nm PDK for academic use. This PDK was chosen due to realistic design conjecture regarding the current design competencies. FinFET technologies present the width quantization aspect (ALIOTO; CONSOLI; PALUMBO, 2015a). With a 27nm fin pitch, high-density layout is achieved with 3-fins transistors. Otherwise, for a higher fin count, there is a lower density and routing complexity (CHAVA et al., 2015). The main PDK rules and lithography assumptions considered in this work are shown in Table I. To exemplify the PDK layers, the 3-fins transistors ST is

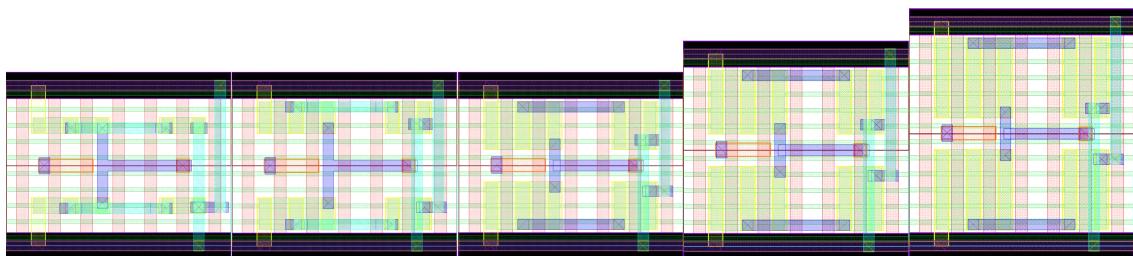
shown in Fig. 6.6. The dimensions and areas related to each layout is shown at Table 6.2. Figs. 6.2, 6.3, 6.4 and 6.5 show comparisons between each circuit layouts. In appendix A all layouts can be seen individually.

Figure 6.2: 1 to 5 fins (left to the right) ST layout comparison.



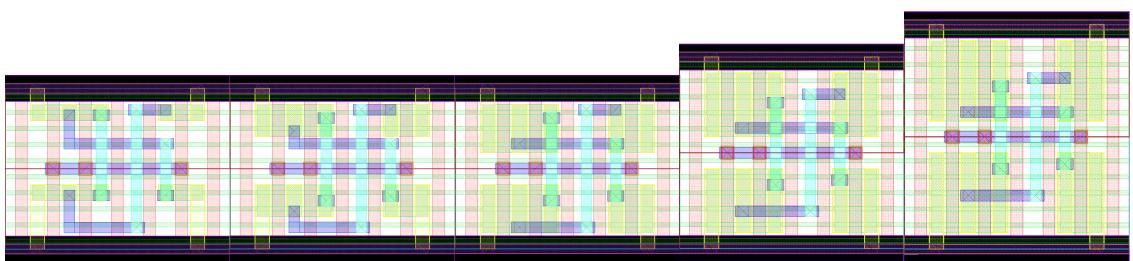
Source: From the author.

Figure 6.3: 1 to 5 fins (left to the right) ST layout comparison.



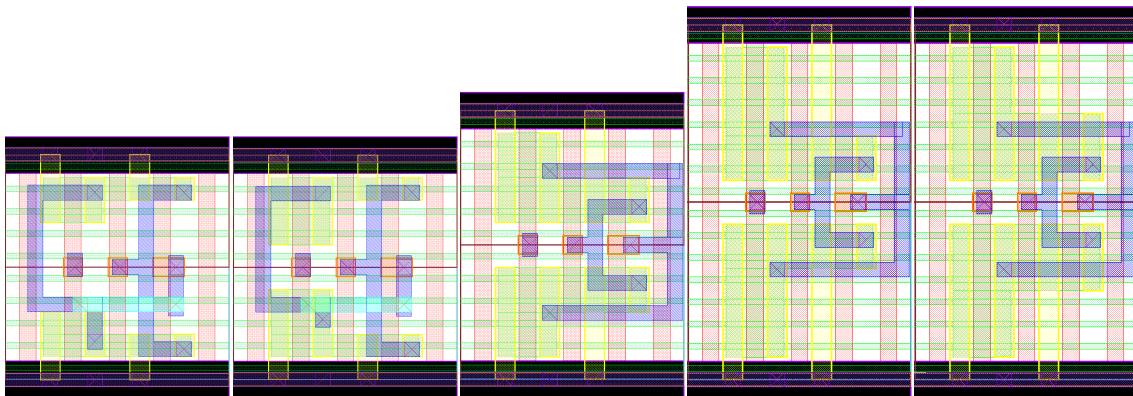
Source: From the author.

Figure 6.4: 1 to 5 fins (left to the right) SIG layout comparison.



Source: From the author.

Figure 6.5: From the left to the right, 2, 4 and 6 maximum fins TIST layout comparison.



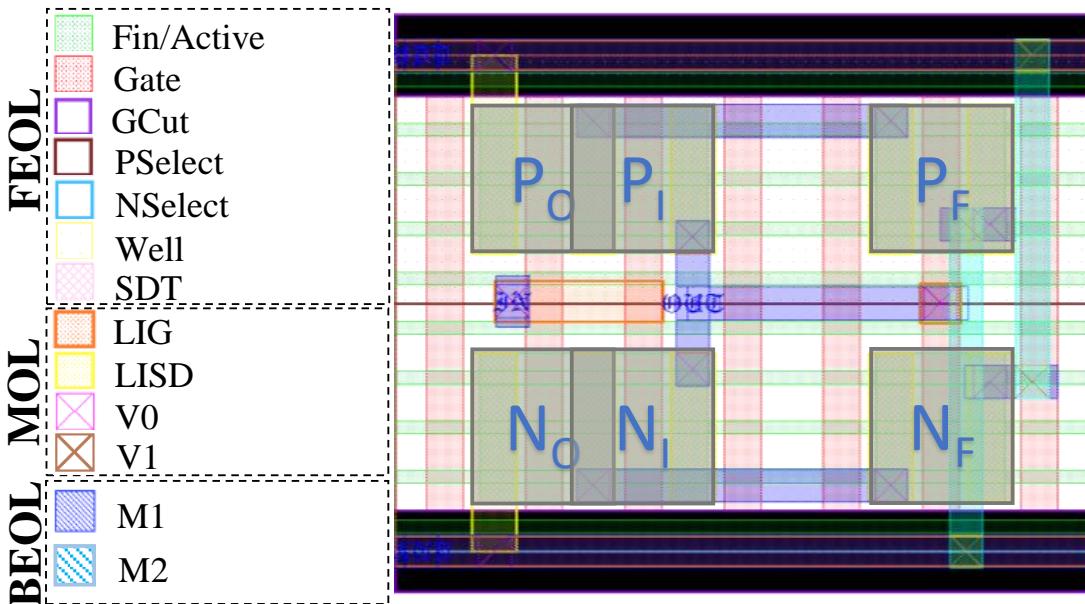
Source: From the author.

Table 6.1: Key layer lithography assumptions, widths and pitches

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

Source: Clark et al. (2016)

Figure 6.6: Technology layers and 3-fins transistors 6T ST layout



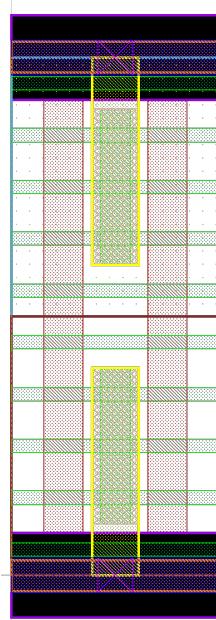
Source: From the author.

The ASAP7 PDK contains the manufacturing process composed by front end of line (FEOL), middle of line (MOL) and back end of line (BEOL). The layouts were developed in a continuous diffusion layer with every gate surrounding another gate in the horizontal axis. The Source-Drain Trench (SDT) connects the active area to the LISD layer. The Local-Interconnect Gate (LIG) is applied to connect the gate terminal, and Local-Interconnect Source-Drain (LISD) is used to connect the source and drain of the transistors. The function of Via 0 (V0) is to join the LIG and LISD to the BEOL layers. The Metal 1 (M1) is used for intra-cell routing and short connections. The Metal 2 (M2) was applied to connect the PF and NF drains to ground and source, respectively. To make the back-gate connections it is necessary a TAP-Cell. It is responsible to connect the NMOS and PMOS back-gates to supply/ground, respectively, being possible to connect the PMOS back-gates to another node. It is a PDK restriction needed for the proper function of the circuit. Its layout has a length of 108nm resulting in an area of $0.02916\mu m^2$ the 3-fins variant is shown in Figure 6.7. In order to build the back-gate connections present in the LPST, it was necessary the insertion of TAP-Cells, greatly increasing the layouts size. Each FA area is shown in Table 6.3 where the LPST and traditional 6T ST are renamed as ST1 and ST2, respectively.

Table 6.2: Each layout proportion/maximum number of fins, dimension and area (the TAP-Cell area is not taken into account).

	Layout	Height (nm)	Width (nm)	Area (nm ²)
INV	1 Fin	270	162	43,740
	2 Fins	270	162	43,740
	3 Fins	270	162	43,740
	4 Fins	324	162	52,488
	5 Fins	378	162	61,236
ST	1 Fin	270	378	102,060
	2 Fins	270	378	102,060
	3 Fins	270	378	102,060
	4 Fins	324	378	122,472
	5 Fins	378	378	142,884
SIG	1 Fin	270	378	102,060
	2 Fins	270	378	102,060
	3 Fins	270	378	102,060
	4 Fins	324	378	122,472
	5 Fins	378	378	142,884
TIST	2 Fins : 1 Fin	270	270	72,900
	4 Fins : 2 Fins	324	270	87,480
	6 Fins : 3 Fins	432	270	116,640
	3 Fins : 1 Fin	270	270	72,900
	6 Fins : 2 Fins	432	270	116,640

Figure 6.7: TAP-Cell Layout.



Source: From the author.

Table 6.3: Each Full Adder area with the ST technique applied where ST1 and ST2 corresponds to the LPST and 6T ST, respectively.

Full Adder	Width (nm)	Height (nm)	Area (nm ²)	Ratio
CMOS	1,188	270	320,760	-
CMOS ST1	2,808		758,160	2.36
CMOS ST2	1,836		495,720	1.55
TGA	1,836		495,720	-
TGA ST1	5,292		1,428,840	2.88
TGA ST2	2,916		787,320	1.59
TFA	1,620		437,400	-
TFA ST1	3,240		874,800	2.00
TFA ST2	2,052		554,040	1.27
HYBRID	1,728		466,560	-
HYBRID ST1	5,292		1,428,840	3.06
HYBRID ST2	2,916		787,320	1.69

6.2 Electrical Simulation

The simulations will be carried out in HSPICE (<https://www.synopsys.com/>) using the netlist obtained after the physical verification flow and the parasitic capacitances extraction. The deviation on the device geometry impacts the electrical parameter WF causing high fluctuations (ZIMPECK et al., 2016). It happens due to the orientation of metal grains randomly aligned in FinFET manufacturing process. In this way, WFF represents the most significant variation beyond the other parameters (MEINHARDT; ZIMPECK; REIS, 2014). The process variability evaluation will be taken through 2000 Monte Carlo (MC) simulations (ALIOTO; CONSOLI; PALUMBO, 2015b) varying the WF of devices according to a Gaussian distribution considering a 3σ deviation and variations from 1% up to 5% with 1% steps on nominal values (NAWAZ et al., 2014). For each step on WF variation, all simulations will be carried from 0.1V to 0.7V supply voltage, with 0.1V steps. The reference values from ASAP7 technology for electrical simulations are shown in Table 6.4.

Table 6.4: Parameters applied in the electrical simulations

Parameter	7nm	
Nominal Supply Voltage	0.7	V
Gate Length (LG)	21	nm
Fin Width (WFIN)	6.5	nm
Fin Height (HFIN)	32	nm
Oxide Thickness (TOX)	2.1	nm
Channel Doping	$1 \times 10^{22} m^{-3}$	
Source/Drain Doping	$2 \times 10^{22} m^{-3}$	
Work Function (eV)	NFET PFET	4.372 4.8108

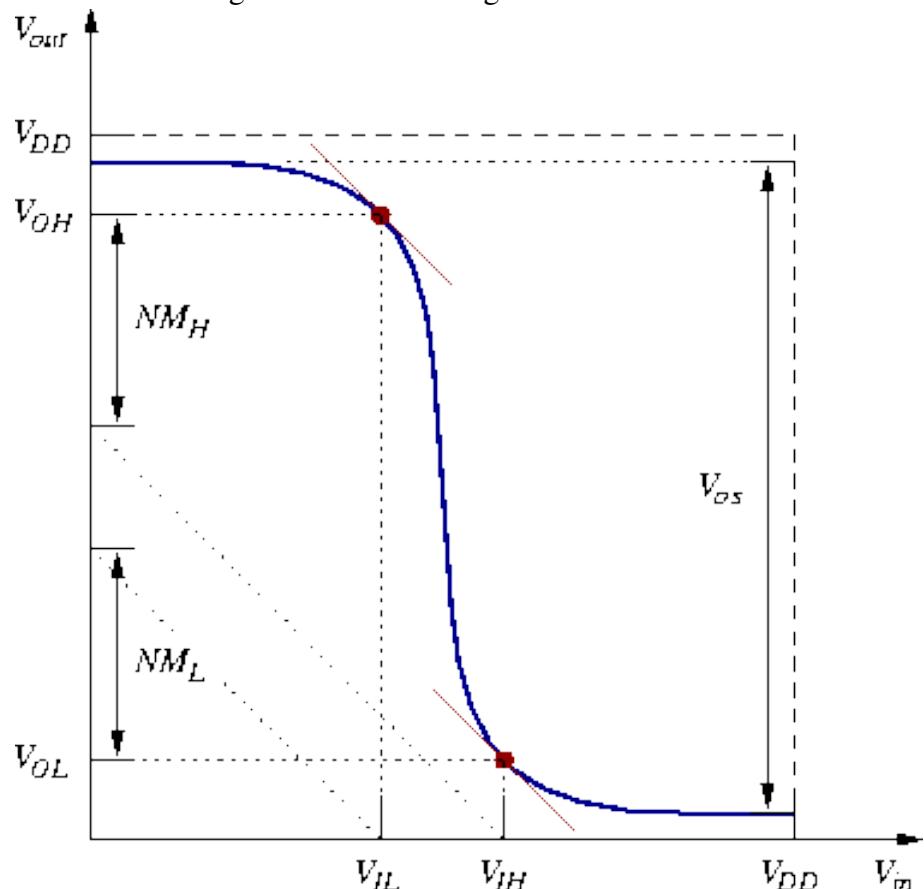
Source: Clark et al. (2016)

For all experiments, it will be observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: hysteresis interval, propagation times, energy, and on and off currents where σ/μ represents the sensibility of the cell to process variability. The energy was calculated by integrating the current through time and multiplying by the supply voltage, and the propagation times were calculated by the timing difference between input and output signals to reach 50% of its value ($V_{DD}/2$). Additionally, noise margins, gains and VTC curve slopes will be presented. The noise margins were calculated as shown in Fig. 6.8 where the margin values are extracted from the VTC curve points where the derivative/slope is -1. The slopes were calculated following the equation 6.1, based on Fig. 6.8.

$$Slope = \frac{V_{OH} - VOL}{V_{IH} - V_{IL}} \quad (6.1)$$

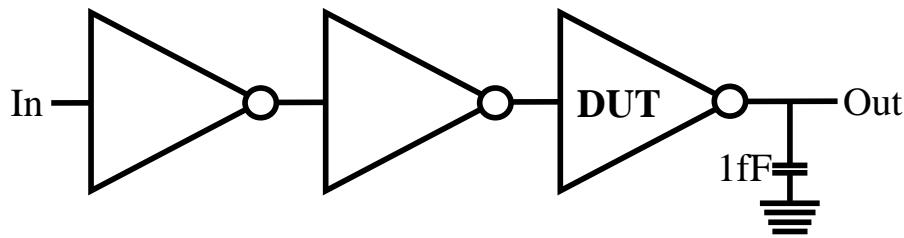
For a more realistic test bench, it will be considered a scenario where the Device Under Test (DUT) receives the signal passing through two inverters in series and having a 1fF output capacitance, as shown in Fig. 6.9. It is essential to consider some details such as: the same supply voltage is applied in the entire testbench, only the DUT suffers from variability, the inverters are the same (3-fins transistors) for all experiments, and they are, like the DUT, simulated from the extracted layout.

Figure 6.8: Noise margins measurements.



Source: Schrom, De and Selberherr (1997).

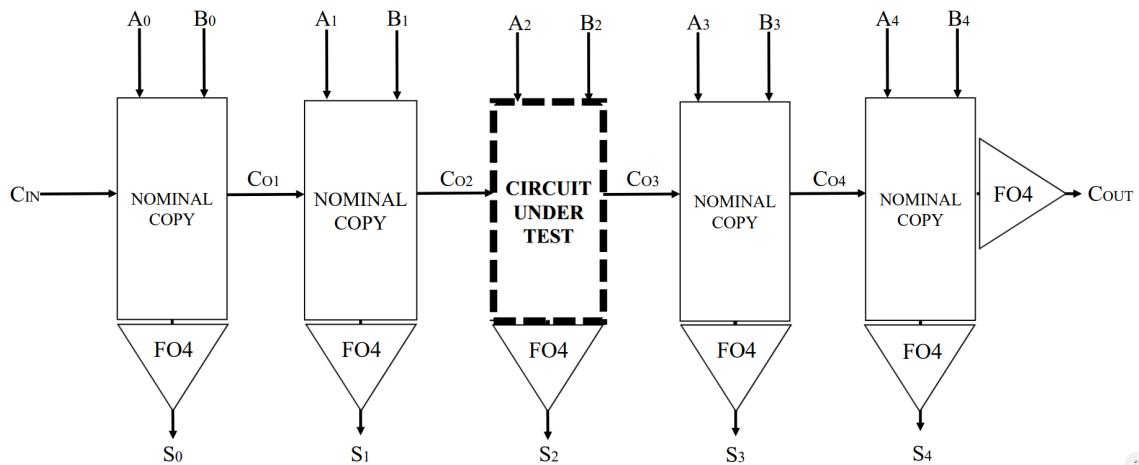
Figure 6.9: Test Bench.



Source: From the author.

For the simulations concerning the Full Adders, it was considered the mean, standard deviations, and normalized standard deviations for the energy and delay measures. The test bench applied consisted of a 5-bit Ripple Carrier Adder with each output (Sum outputs for each FA and last Carry Out) connected to a fan-out of 4 inverters, as shown in Fig 6.10.

Figure 6.10: Test Bench for the Full Adders simulation.



Source: From the author.

7 RESULTS

7.1 Over robustness enhancing circuits

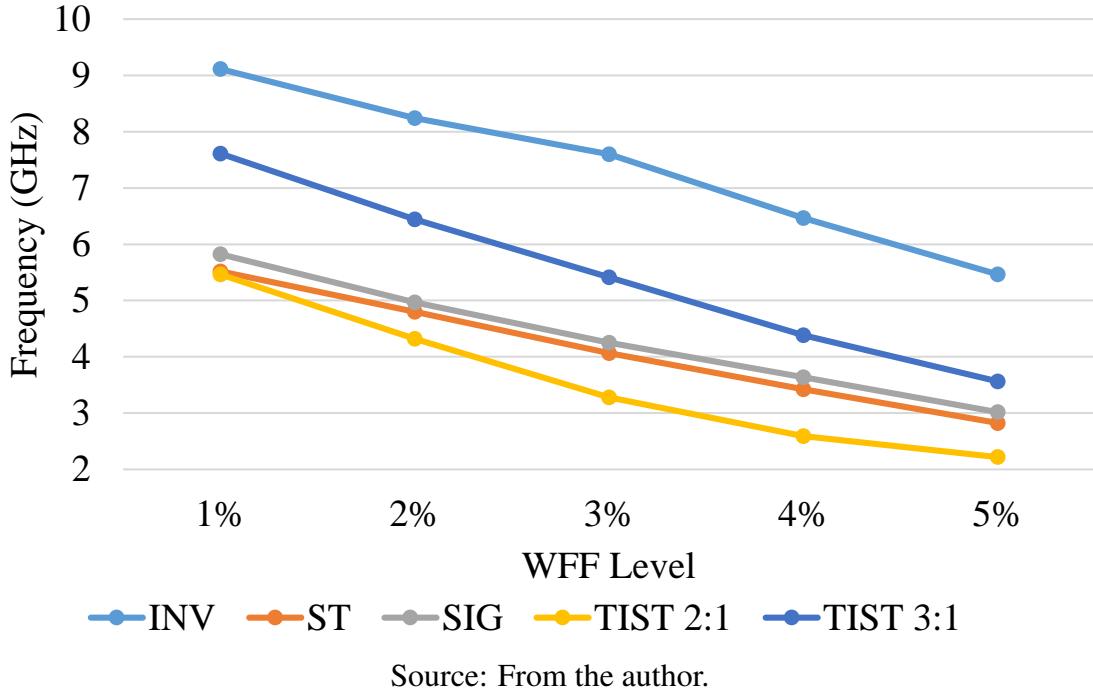
Over all simulations there were non-viable scenarios. Such scenarios kept clustered around the supply voltages of 0.1V, over any scenario above 3% WFF, and 0.2V, over scenarios above 4% WFF for the inverter, ST and SIG. The TIST results presented a discrepancy in relation to the aforementioned designs. For the TIST designs at 2 to 1 and 3 to 1 proportions, the 0.1V scenarios at above 2% WFF level are not viable. For 0.2V and 0.3V the 3 to 1 designs only presented viable scenarios at 1% WFF while the 2 to 1 proportion designs did not operate properly at such supply voltage at any variability level. For the 0.4V the 3 to 1 and 2 to 1 designs worked at below 3% and 2% WFF levels, respectively. For 0.5V the 3 to 1 and 2 to 1 designs worked at below 5% and 3% WFF levels, respectively. Finally, at 0.6V and 0.7V, all scenarios worked properly.

Given so, in overall, each design presented non-viable scenarios at below threshold voltages, with the TIST layouts presenting a much higher number of failures only working properly, at all variability levels, on 0.6V and 0.7V supply voltages. This results shows the lower robustness and more complex way of sizing for the TIST, which may not be advised for critical applications. All scenarios frequencies are shown in Table 7.1.

On average, the ST, SIG and TIST (2:1) operated at around half the inverter's frequency (47.61%, 50.5% and 49.71% respectively) while the TIST (3:1) worked at 65.72% of the inverter frequency. This is expected since their input capacitance is much higher, from a two-transistor design to a six-transistor design and, for the ST and TIST designs, the hysteresis keeps the output from switching much longer than in the other considered designs. The 3:1 TIST designs present a higher frequency, in comparison to its 2 to 1 proportion counterpart, given the higher proportion giving less resistance and higher currents to the circuit, making it faster in charging and discharging its nodes and output.

Considering the impact of variability on the frequency retention, in comparison to a low variability scenario (1% WFF) the inverter, ST, SIG, TIST 2:1 and TIST 3:1 presented up to 40.03%, 48.81%, 48.20%, 59.4%, and 53.17% average decrease on frequencies considering the worst case scenario, respectively. It is important to elucidate that in order to not deflate the decrease results of the TIST designs due to the large number of non-viable scenarios, the results were calculated considering such scenarios to work at 0Hz, as shown in Fig. 7.1.

Figure 7.1: Frequency decrease over variability scaling for each design.



Source: From the author.

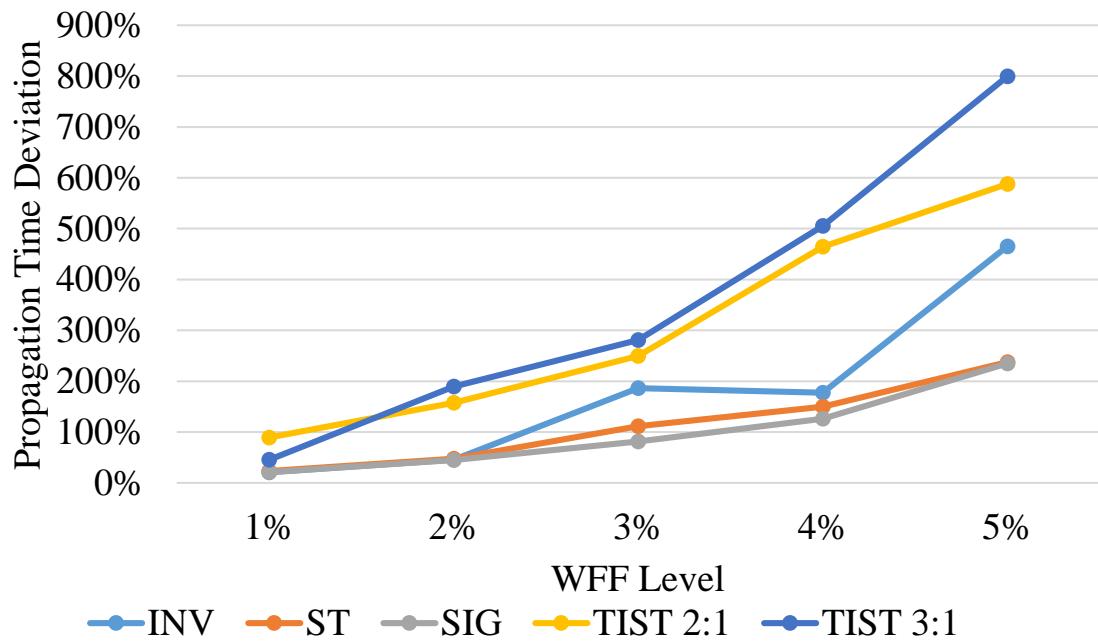
Such performance degradation is expected since process variability will, in many cases, increase the transistors V_{TH} , making necessary to decrease the circuits frequency to work properly. Alongside, in higher transistor count circuits, it is expected a higher impact since the variability effect on transistors will work as a chain reaction, with the previous node own deviation accumulating along the next circuit nodes and so on, until the output node. Given that, it is expected for the ST and SIG to present a higher impact due to the inserted process variability. The TIST present higher decreases due to their higher number of non-viable scenarios.

Given the propagation time deviations for each design, in comparison to the inverter, and considering all scenarios, the ST and SIG presented 36.36% and 43.21% lower sensibility, respectively. While the TIST with 2:1 and 3:1 proportions presented 72.89% and 103.26% higher deviations, respectively, as shown in Fig. 7.2. When considering only scenarios where all designs worked properly, the ST and SIG presented small increases of 8.54% and 7.04% in sensibility, with the TIST 2:1 and 3:1 presenting 146.15% and 36.28% higher sensibility.

Table 7.1: All scenarios frequencies.

Design	WFF	Supply Voltage (V)						
		0.1	0.2	0.3	0.4	0.5	0.6	0.7
INV	1%	2.18MHz	49.4MHz	1.12GHz	6.5GHz	13.6GHz	19.1GHz	23.4GHz
	2%	510KHz	15.4MHz	504MHz	4.95GHz	12GHz	17.9GHz	22.3GHz
	3%	-	4.79MHz	149MHz	4.86GHz	10.3GHz	16.6GHz	21.3GHz
	4%	-	-	47.2MHz	1.77GHz	8GHz	15.1GHz	20.3GHz
	5%	-	-	17.8MHz	360MHz	5.2GHz	13.5GHz	19.2GHz
ST	1%	930KHz	22MHz	510MHz	3.2GHz	7.8GHz	12GHz	15.1GHz
	2%	192KHz	7.2MHz	210MHz	2.3GHz	6.3GHz	10.7GHz	14.1GHz
	3%	-	2.39MHz	74.2MHz	1.3GHz	5GHz	9GHz	13.1GHz
	4%	-	-	28.4MHz	550MHz	3.7GHz	7.9GHz	1.11GHz
	5%	-	-	4.6MHz	170MHz	2.2GHz	6.7GHz	10.7GHz
SIG	1%	1.02MHz	23.8MHz	540MHz	3.5GHz	8.2GHz	12.6GHz	15.9GHz
	2%	268KHz	7.4MHz	216MHz	2.45GHz	6.6GHz	10.7GHz	14.8GHz
	3%	-	2.34MHz	71.4MHz	1.25GHz	5.5GHz	9.7GHz	13.2GHz
	4%	-	-	20.8MHz	540MHz	4GHz	8.5GHz	12.4GHz
	5%	-	-	5MHz	150MHz	2.2GHz	7.3GHz	11.5GHz
TIST 2:1	1%	833KHz	-	-	783MHz	6.37GHz	13.3GHz	17.8GHz
	2%	142KHz	-	-	-	2.86GHz	10.9GHz	16.5GHz
	3%	-	-	-	-	-	8.17GHz	14.8GHz
	4%	-	-	-	-	-	4.93GHz	13.2GHz
	5%	-	-	-	-	-	4.33GHz	11.2GHz
TIST 3:1	1%	1.3MHz	5.5MHz	175MHz	3.3GHz	11.2GHz	17.3GHz	21.3GHz
	2%	275KHz	-	-	600MHz	8.51GHz	15.7GHz	20.3GHz
	3%	-	-	-	-	5GHz	13.9GHz	19GHz
	4%	-	-	-	-	1.1GHz	11.8GHz	17.8GHz
	5%	-	-	-	-	-	8.65GHz	16.3GHz

Figure 7.2: Propagation times deviation for each design in relation to the WFF level considering all scenarios.



Source: From the author.

7.2 Energy Consumption and Deviation

Concerning energy consumption absolute values, the ST, SIG, TIST 2:1 and, TIST 3:1 presented on average, 173.07%, 50.74%, 480.68% and, 310.83% higher consumption compared to the traditional inverter. This is mainly related to the transistor count difference between all designs, and the inverter. The ST higher consumption is justified due to the dependency of its feedback mechanism on the output value in contrast to the SIG feed-forward mechanism being directly dependent on the input value. The dependency over the output value of the ST makes it slower, hence the output dependency over the input itself and the input capacitance, increasing the energy consumption. The difference between different proportions of TIST designs is mainly due to lower frequencies on high variability scenarios for the 2 to 1 designs. The designs with a 2:1 proportion presented up to 40.94% lower frequency in comparison to its 3 to 1 proportion counterparts. Additionally, the higher energy consumption for TIST designs is mainly due to the 6 (3 to the ground and 3 to the source) total paths enabling the circuit to charge/discharge with no mechanism for the minimization of the leakage power.

The energy consumption increase over each variability scenario kept stable over 15.16%, 35.6%, 20.94%, 9.04% and, 7.18% for the inverter, ST, SIG, TIST 2:1 and, TIST 3:1, respectively. Such increase is related to the frequency decrease over variability scaling. The low increase related to the TIST designs is due to many of the low supply voltage scenarios not being taken into account, in comparison to the other designs, since it did not work properly. A more fair analysis would consider only the subset of cases where all designs worked properly. Given such subset, the energy increase over each variability scenario would be 17.59%, 18.16%, 18.62%, 9.04% and 11.59% for the inverter, ST, SIG, TIST 2:1 and, TIST 3:1, respectively.

Concerning robustness, the ST and SIG presented a 55.83%, 47.15% higher sensibility while the TIST 2:1 and 3:1 presented a 42.39% and 52.03% lower sensibility to the process variability impact in comparison to the traditional inverter considering the scenarios where each design presented acceptable behavior. In order to make a fair comparison, considering only the subset of scenarios where all designs worked properly, the ST and TIST 3:1 presented 1.13% and 33.36% lower sensibilities while the SIG and TIST 2:1 presented 5.5% and 7.99% higher variability sensibility. Additionally, considering all cases, even when the circuit did not work properly, the ST, SIG, TIST 2:1, and TIST 3:1 presented 19.85%, 12.09%, 145.96%, and 118.24% higher sensibilities in comparison to

Table 7.2: Recommended layout and supply voltage for each design and variability level.

Design	WFF	Minimum Energy		Highest Robustness		CB	
		Supply (V)	#Fins	Supply (V)	#Fins	Supply (V)	#Fins
INV	1%	0.1	1 or 2	0.7	1	0.7	1
	2%	0.1	1	0.3	4 or 5	0.2	2 to 4
	3%	0.2	1	0.3	5	0.3	3 to 5
	4%	0.3	1 or 2	0.4	5	0.4	5
	5%	0.3	1	0.4	1	0.4	1
ST	1%	0.1	1	0.7	5	0.7	1
	2%	0.2	1	0.7	5	0.7	1
	3%	0.2	1	0.7	4 or 5	0.3	1
	4%	0.3	1	0.4	2	0.4	1 or 2
	5%	0.4	1	0.5	2 to 5	0.5	1 or 2
SIG	1%	0.1	1	0.7	2	0.7	1
	2%	0.2	1	0.3	3 or 4	0.7	1
	3%	0.2	1	0.3	3	0.3	1
	4%	0.3	1	0.4	3	0.4	2 or 3
	5%	0.4	1	0.5	2 or 3	0.5	2
TIST 2:1	1%	0.1	2F1F	0.7	4F2F	0.7	2F1F
	2%	0.1	2F1F	0.6	4F2F	0.6	2F1F
	3%	0.7	2F1F	0.6	2F1F	0.6	2F1F
	4%	0.7	2F1F	0.7	4F2F	0.7	2F1F
	5%	0.7	2F1F	0.7	6F3F	0.7	2F1F
TIST 3:1	1%	0.1	3F1F	0.7	6F2F	0.7	3F1F
	2%	0.1	3F1F	0.7	6F2F or 3F1F	0.7	3F1F
	3%	0.7 or 0.6	3F1F	0.6 or 0.7	6F2F or 3F1F	0.7	3F1F
	4%	0.7 or 0.6	3F1F	0.6	6F2F	0.6	3F1F
	5%	0.7 or 0.6	3F1F	0.6	3F1F	0.6	3F1F

the traditional inverter.

Three types of analysis were performed to identify the most appropriate layout depending on the scenario: 1) layout with the lowest energy consumption, 2) highest robustness and 3) the most Cost-Benefit (CB) oriented layout. The lowest energy layout is identified through the energy measures. The higher robustness layout is identified by the lowest normalized standard deviation concerning energy consumption and the CB layout is identified by the lowest value considering the product between the energy consumption and normalized standard deviation (EDP - Energy Deviation Product). The results are shown at Table 7.2.

Some results will show more than one appropriate layout/supply voltage. Values of energy consumption, energy normalized deviation and EDPs between the respective minimum value and, relatively, 5% higher values were considered in order to provide more flexibility. It is possible to identify patterns concerning the minimum energy and highest robustness layouts. The minimum energy layouts contain only few fins and lower supply voltages. Both low values aim to lower currents and increase resistance, therefore

decreasing energy consumption. As variability rises, the supply voltage rises as well. That is due to the lower frequencies applied in those scenarios and the consequent increase on propagation times, given that energy is the by-product of power and time. A higher supply voltage will decrease propagation times followed by a decrease on energy consumption. The TIST designs present a steep increase on supply voltage, from 0.1V to 0.6V/0.7V due to the lack of possible mid-term (0.2V to 0.5V) viable scenarios.

The robust layouts present a shift on supply voltage. At saturation region, the on-current presents an exponential dependency over the V_{TH} , as shown in equation 7.1, while at the linear region, the on-current presents a linear dependency over the V_{TH} , as shown in equation 7.2. For both equations, the $I_{D,sat}$ is the saturation current, $I_{D,lin}$ is the linear current, μ_p is the p-material electron mobility, C_{ox} is the specific capacitance of the gate, W is the transistor width, L is the transistor length, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, and V_T is the threshold voltage. At low level variability scenarios, a saturation on-current will not present significant variations, while at high variability scenarios the on-current must fall to linear region in order to present lower deviations.

$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \begin{cases} V_{GS} \leq V_T \\ V_{DS} \leq V_{GS} - V_T \end{cases} \quad (7.1)$$

$$I_{D,lin} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2] \begin{cases} V_{GS} \leq V_T \\ V_{DS} > V_{GS} - V_T \end{cases} \quad (7.2)$$

Energy consumption and deviation comparisons between each scenario best layout are shown in Fig. 7.3, Fig. 7.4, Fig. 7.5, Fig. 7.6, and Fig. 7.7. The lines correspond to the energy consumption axis (left), while the bars correspond to the energy deviation axis (right). It is shown that the CB layouts presents similar results in comparison to the high robustness layouts while maintaining a lower energy consumption, for the ST and SIG, with the exception of the inverter. The inverter presents a high deviation for its minimum energy layout at 5% WFF (1 fin layout with a supply voltage of 0.3V). Although, with a little increase on supply voltage, from 0.3V to 0.4V, matching the CB layout, the inverter presents a 8.95% increase on energy consumption while decreasing its energy deviation by 93.49%, as shown in Table 7.3. This result highlights the importance of a cost-benefit analysis in order to bring flexibility, and the best of both low energy and robust layouts.

At the same time, it is important to analyze its drawbacks. The CB layouts for

Table 7.3: Difference in energy metrics between the CB layout and its low energy and high robustness counterparts.

Design	CB Layout comparison (%)							
	Energy				Energy Deviation			
	Low Energy		High Robustness		Low Energy		High Robustness	
	Maximum	Average	Maximum	Average	Maximum	Average	Maximum	Average
INV	260.64	81.44	-37.51	-7.50	-93.49	-76.87	7.42	1.48
ST	80.17	37.38	-78.60	-53.56	-84.05	-60.67	31.98	12.96
SIG	53.09	34.70	-58.92	-24.14	-90.88	-68.28	22.48	7.26
TIST 2:1	308.67	72.48	-39.10	-29.49	-95.04	-41.72	23.89	15.05
TIST 3:1	301.76	74.77	-33.75	-25.24	-92.18	-48.97	13.31	5.39

inverter and TIST layouts presented higher increases on energy consumption, in comparison to the ST and SIG designs. This higher increase is directly related to the much higher maximum values of those designs. Those higher maximum values occurred at 1% WFF and are due to two factors. The first factor is related to the presence of a leakage current suppression system, part to the feed-back circuit, in the ST and SIG designs. Secondly, as WFF increases, the minimum energy values start to rise as well, due to lower frequencies and higher supply voltages. Although, the high robustness layouts energy consumption rises as well, it does not rises as fast as the minimum energy layouts consumption. Given so, with the CB layouts energy consumption always staying between the high robustness and minimum energy layouts, the difference between the energy consumption of the minimum energy layout and the CB layout will be diminished as variability rises.

Considering the difference in energy consumption, the CB inverter shows the lowest decrease compared to the high robustness layout. It is mainly due to the CB layout trending into a more robust approach. It happens due to the higher difference in sensibility caused by sizing. For example, at 0.7V the inverter can show up to 44.4% higher energy deviation, depending on the sizing, while the ST will present a maximum of 21.17% increase in deviation. This makes the inverter less flexible, tightening appropriate setups around more specific sets of sizing and supply voltages. All around, it can be noted huge maximum decreases in energy deviation in comparison to the low energy layout for all designs.

A comparison between each design layout is presented in Fig. 7.8, Fig. 7.9, and Fig. 7.10. The lines correspond to the energy consumption axis (left), while the bars correspond to the energy deviation axis (right). Considering the averages, for the low energy layouts, the inverter presented the lowest energy consumption, followed by the SIG (34.61% higher), ST (68.32% higher), TIST 3:1 (358.84% higher) and TIST 2:1 (487% higher), respectively. The TIST layouts, showed the highest robustness, with the 2:1 vari-

Figure 7.3: Layout comparison for each scenario considering the energy metrics for the inverter.

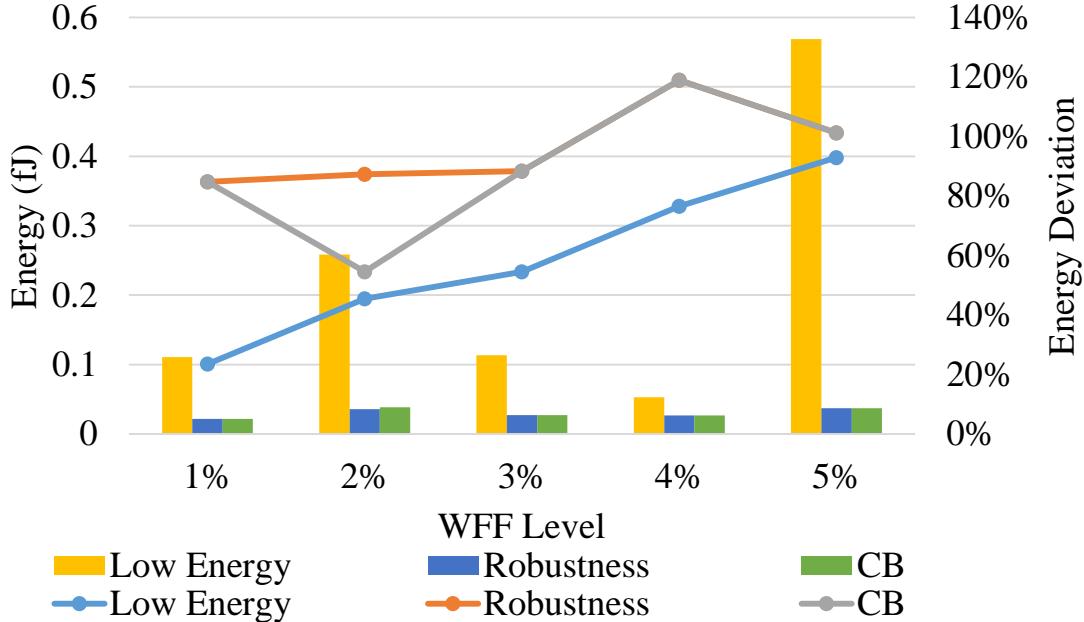


Figure 7.4: Layout comparison for each scenario considering the energy metrics for the ST.

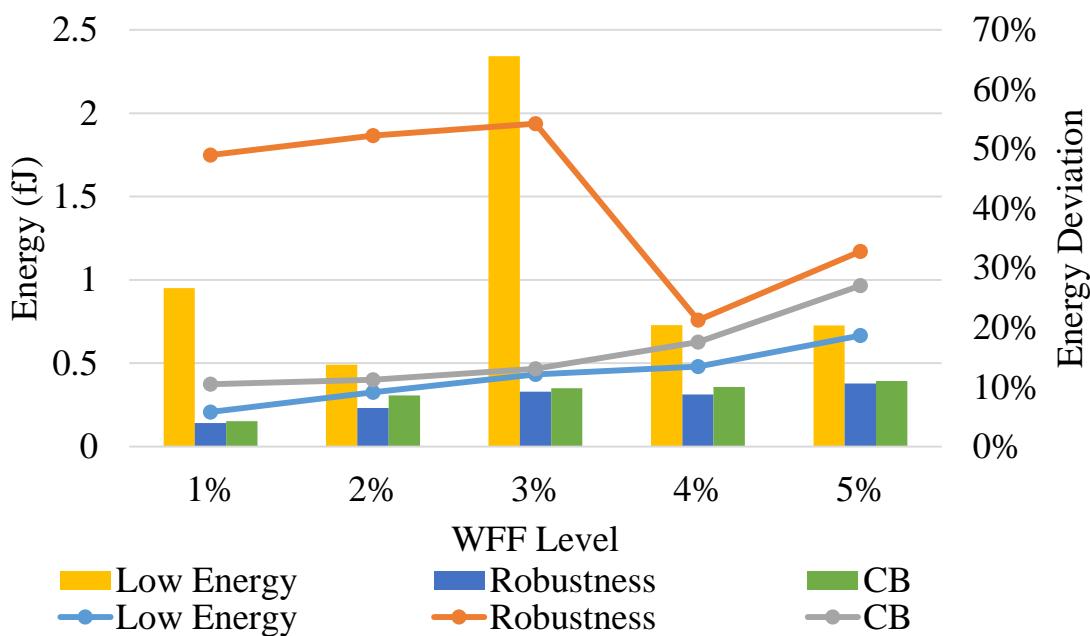


Figure 7.5: Layout comparison for each scenario considering the energy metrics for the SIG.

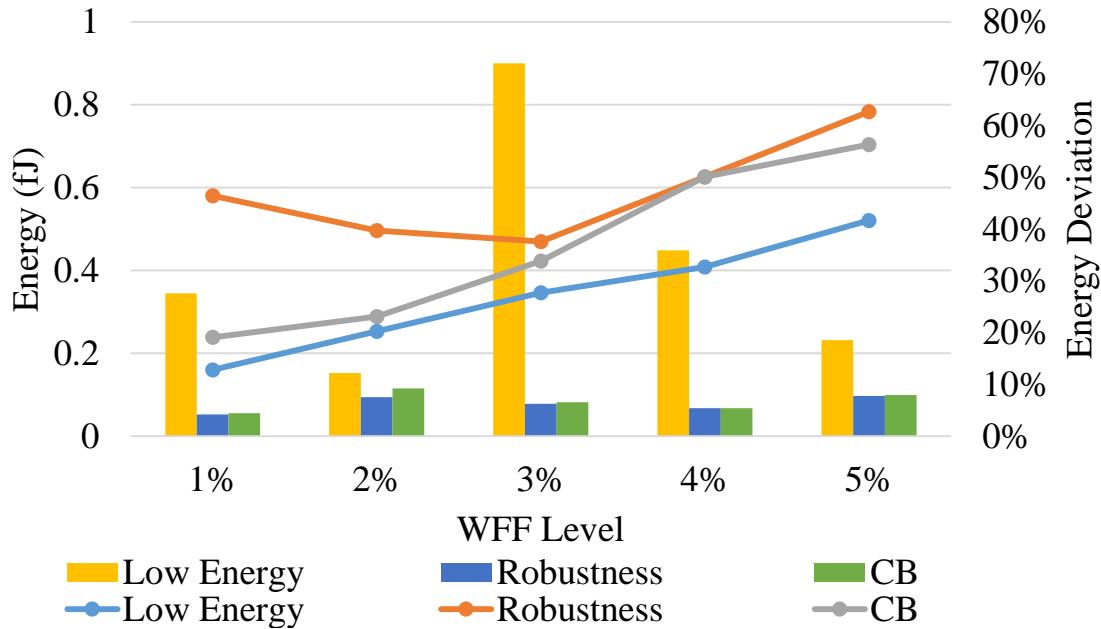


Figure 7.6: Layout comparison for each scenario considering the energy metrics for the TIST at 2:1 proportion.

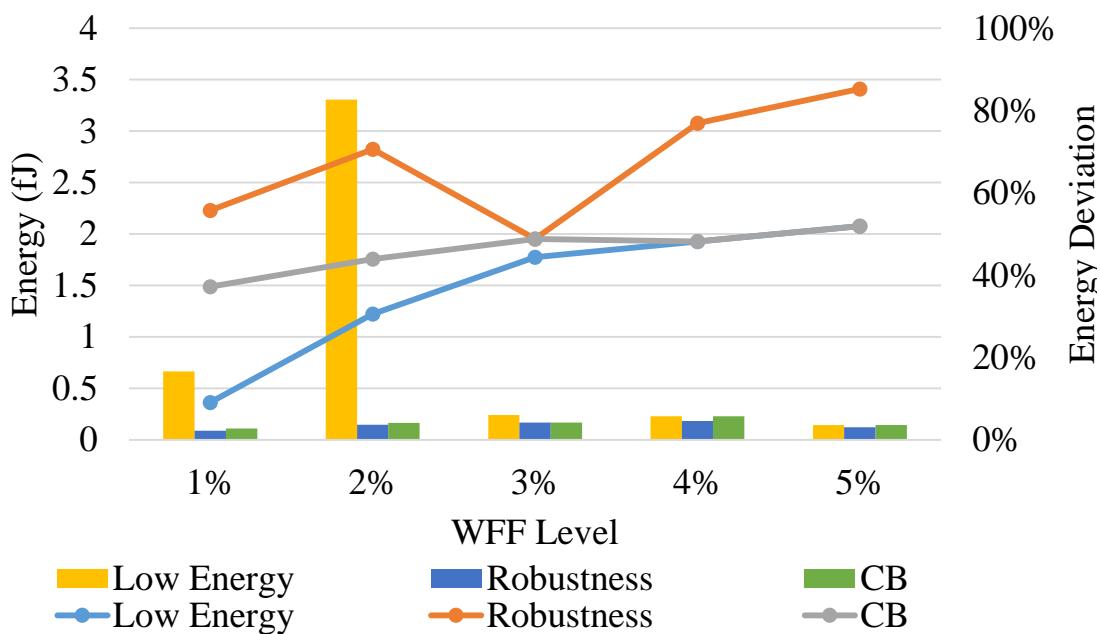
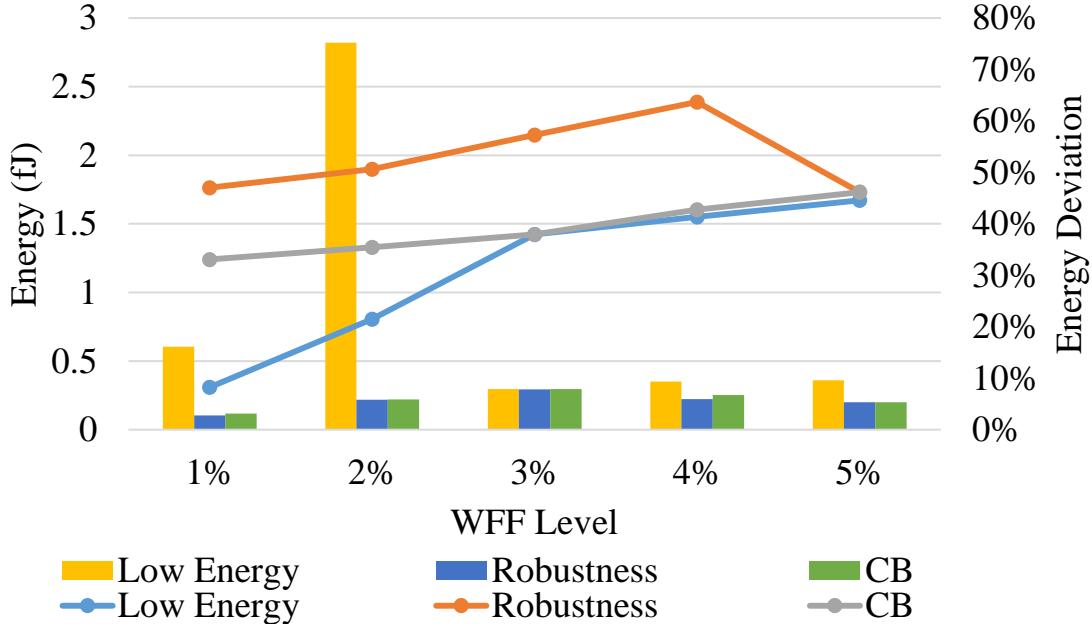


Figure 7.7: Layout comparison for each scenario considering the energy metrics for the TIST at 3:1 proportion.



ants presenting a 22.93% average energy deviation and the 3:1 variants showing a minor increase with its 23.62% average energy deviation. Following the TIST layouts, the ST, SIG and inverter present a 29.34%, 33.25%, and 51.55% energy deviation, respectively. It can be noted that, while the inverter presents the lowest energy consumption it presents the highest energy deviation as well. It is mainly due to its spike on deviation at 5% WFF but even disconsidering this spike, the inverter would show an average deviation of 31.25%, which is still higher than most designs. Given so, the inverter is not entirely recommended for a low energy application where robustness is critical. A more appropriate design would be either ST or SIG, with the ST although presenting higher energy consumption, its hysteresis effect should not be ignored, being of importance for high noise application.

For the high robustness spectrum, the energy consumption difference between designs follows the same behaviour, although with much broader differences. In comparison to the inverter energy consumption each design presented an average increase of 43.52%, 263.24%, 382.12%, and 555.21%, for the SIG, ST, TIST 3:1, and TIST 2:1, respectively. The deviation metrics presented a similar behaviour as well, although the ST presented the highest deviations. The TIST designs presented the lowest deviations with 3.56%, and 5.55% for the TIST 2:1, and 3:1, respectively. Following, the SIG, inverter, and ST, presented 6.23%, 6.93%, and 7.81% deviations. In this case, the inverter is a strong candidate, with the lowest energy consumption, and acceptable robustness.

Figure 7.8: Low energy layouts energy metrics comparison for each design.

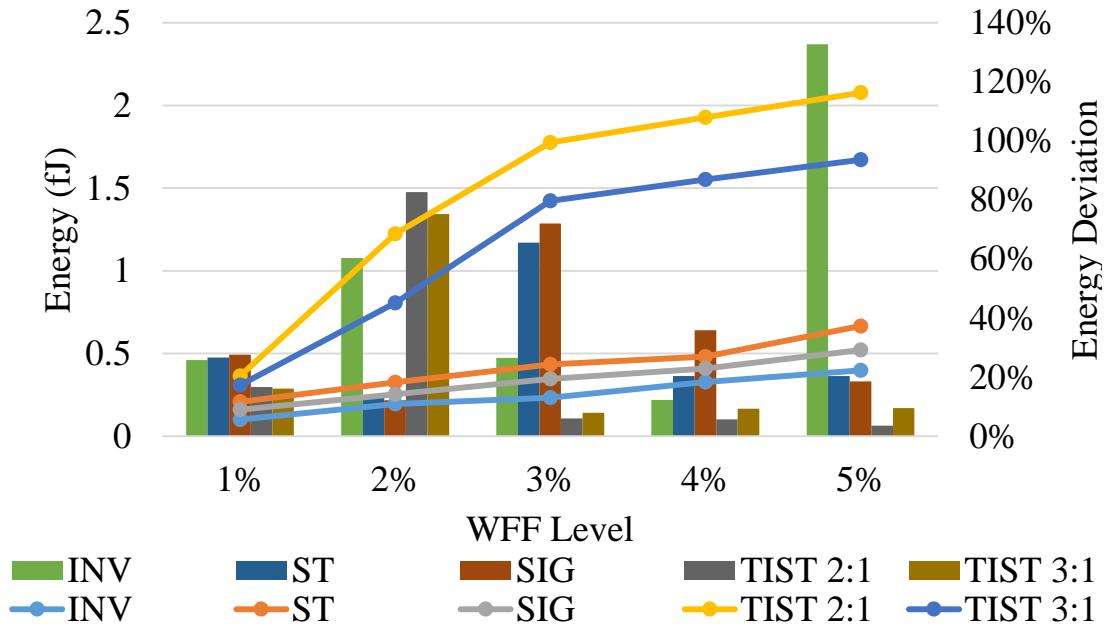


Figure 7.9: High robustness layouts energy metrics comparison for each design.

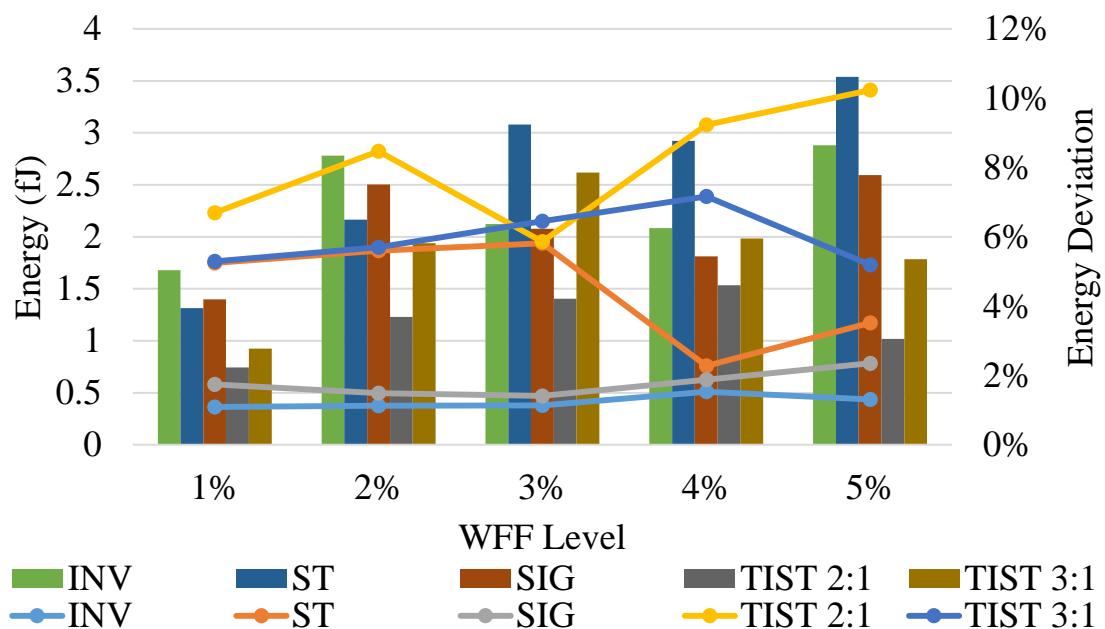
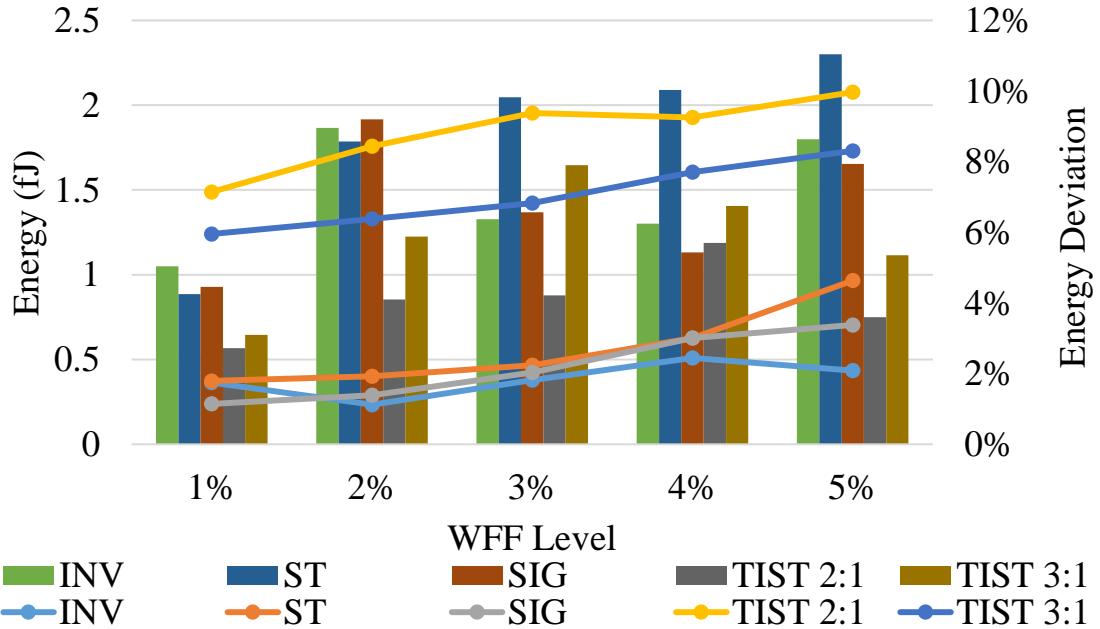


Figure 7.10: CB layouts energy metrics comparison for each design.



Lastly, for the CB layouts, the energy consumption scaling through the designs is the same, although with smaller differences, even in comparison to the low energy layouts. In comparison to the inverter, the SIG, ST, TIST 3:1, and TIST 2:1 presented average increases of 18.84%, 47.74%, 281.85%, and 379.6%. The designs kept the same behaviour as their high robustness variants. The TIST designs presented the lowest deviations with 4.07% and 5.8% for the 2:1 and 3:1 proportions, respectively. The SIG, inverter and ST, presented respectively, 6.72%, 7.05%, and 8.74% deviations on energy. In this case, the SIG, presents a higher energy consumption and much bigger layout, it only provides a minor improvement over deviations (4.91%, relative to the inverter). The ST presented higher energy and bigger area as well, with a increase on deviations (1.69%, absolute and 23.97% relative increases, in comparison to the inverter), although it still presents hysteresis. The TIST designs, consume considerably more energy, with less deviation (although, as stated before, those numbers are deflated), bigger layout area, and less viable scenarios to work with.

7.3 Static Noise Margins

The evaluation of the Static Noise Margins (SNM) are shown at Table 7.4. The inverter and SIG showed identical SNMs, while TIST designs presented higher SNMs than the inverter and SIG at sub-threshold levels, with the 2:1 layouts presenting lower

Table 7.4

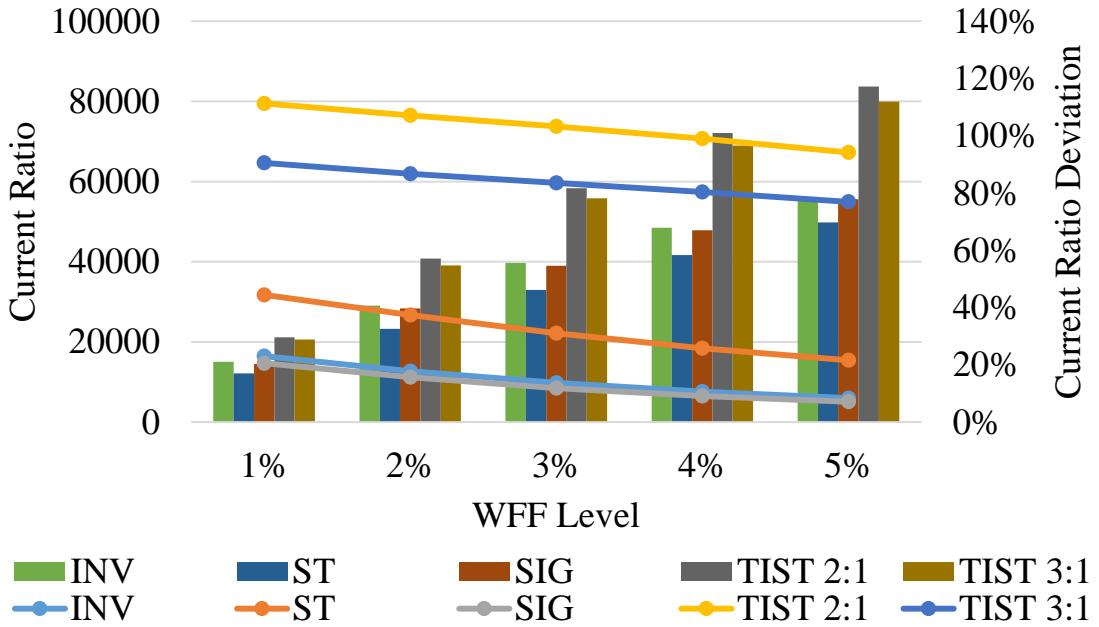
Design	SNM (V)	Supply Voltage (V)						
		0.1	0.2	0.3	0.4	0.5	0.6	0.7
INV	NM_L	0.025	0.074	0.122	0.171	0.217	0.253	0.277
	NM_H	0.025	0.073	0.121	0.169	0.216	0.259	0.299
	Avg.	0.025	0.073	0.122	0.170	0.216	0.256	0.288
SIG	NM_L	0.025	0.074	0.122	0.171	0.217	0.253	0.277
	NM_H	0.025	0.073	0.121	0.169	0.216	0.259	0.299
	Avg.	0.025	0.073	0.122	0.170	0.216	0.256	0.288
ST	NM_L	0.036	0.111	0.178	0.244	0.310	0.376	0.440
	NM_H	0.036	0.077	0.111	0.144	0.178	0.213	0.248
	Avg.	0.036	0.094	0.144	0.194	0.244	0.294	0.344
TIST 2:1	NM_L	0.061	0.161	0.245	0.292	0.319	0.337	0.359
	NM_H	0.014	0.007	0.010	0.038	0.079	0.131	0.189
	Avg.	0.037	0.084	0.128	0.165	0.199	0.234	0.274
TIST 3:1	NM_L	0.051	0.150	0.233	0.277	0.300	0.314	0.341
	NM_H	0.022	0.017	0.022	0.056	0.108	0.173	0.235
	Avg.	0.036	0.084	0.128	0.167	0.204	0.244	0.288

margins. The ST presented higher SNMs overall. In comparison to the inverter, SIG, and TIST 3:1, which presented the same average SNM of 0.164V, the TIST 2:1 presented 2.6% lower SNMs, while the ST showed 17.5% higher SNMs. The ST presents its biggest difference at low supply voltages, with 41.91% and 28.23% higher SNMs at 0.1V, and 0.2V, respectively, in comparison to the inverter.

Concerning the I_{on}/I_{off} ratios, in comparison to the inverter, the ST, TIST 2:1, and TIST 3:1 presented, on average, 118.01%, 600.21%, and 468.7% higher ratios. The SIG is the only design which presented a worsening with a 12.53% lower ratio. While considering deviations into the ratio due to process variability, the ST and SIG presented 11.1% and 6.91% lower deviations, with the TIST 2:1 and 3:1 presenting 49.57% and 42.79% higher deviations, respectively. The current ratios and current ratios deviations are shown in Fig. 7.11, with the marked lines and bars being related to the left and right axis, respectively.

Due to the variability impact, the current ratios tend to decrease. This mainly happens due to the increase of the off-current as variability scales. This behavior is due to the effects of DIBL (Drain-Induced Barrier Lowering) and is a consequence of the short channel present on modern transistors. Due to the decreasing channel length, the depletion regions of drain and source become an increasing fraction of the whole area under the gate. Therefore, the volume of the depletion region effectively controlled by the gate

Figure 7.11: Current ratio (left) and current ratio deviation (right) design comparison across variability scaling.



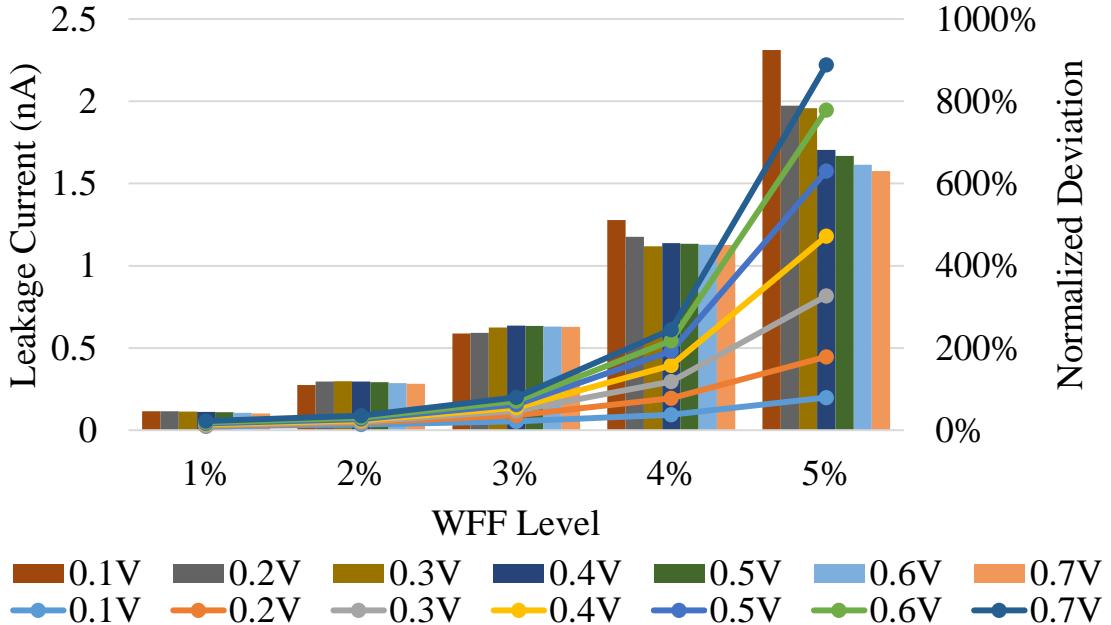
decreases which can be modeled by a threshold voltage decreasing with the gate length. The charge below the gate being not only controlled by the gate but also by the drain and source regions is called the charge sharing effect. A similar effect occurs if the drain potential of the transistor increases: the pn-junction between the drain and the substrate becomes more reverse-biased, so the depletion layer grows and reduces even more the volume controlled by the gate. Given so, a drain bias-dependent threshold voltage can be assumed, as shown in Equation 7.3 (HENZLER, 2006):

$$V_{th} = V_{th,0} - mV_{DS} \quad (7.3)$$

Thus, according to Equation 7.4 (HENZLER, 2006), where $I_{D,sub}$ is the subthreshold current (leakage current), the leakage current (or subthreshold current) is exponentially dependent on the threshold voltage, as shown in Fig. 7.12 for the inverter, although all designs presented the same behavior. The TIST designs presented the lowest decrease, at 15.21%, with the ST, inverter, and SIG presenting much higher losses with 51.44%, 63.59%, 65.54%, respectively. The current ratios present a linear decrease, instead of an exponential decrease, due to the lower, although exponential, increase rate of the *on* current, as shown in Fig. 7.13.

$$I_{D,sub} = I_0 \cdot \exp \left(\frac{V_{GS} - V_{th,0} + mV_{DS}}{\eta \cdot V_T} \right) \quad (7.4)$$

Figure 7.12: Leakage current scaling (left axis) and standard deviation (right axis) for the inverter.



Additionally, it was considered the output gain values for each design, as shown in Fig. 7.14. These measures present the most broader difference across all designs. The TIST and ST designs presented, on average, values up to 8300.60%, and 1246.50% higher, respectively, in comparison to the inverter and SIG designs, which presented the same gains. Additionally, the curve slope measures are shown in Fig. 7.15, where lower slopes can be observed for the TIST, SIG and inverter designs in comparison to the ST. The ST and TIST designs presented 126.24% and 9.43% higher average slopes, respectively, in comparison to the inverter and SIG designs which showed identical measures. Figs. 7.16 and 7.17 show the VTC curves for all designs. It shows how the TIST although presenting higher gain, present lower slopes, given that it takes more time to properly discharge.

The hysteresis ratios of all designs which present the hysteresis characteristic are shown in Fig. 7.18. The hysteresis ratio is the ratio between the hysteresis interval (V) and the supply voltage (V), which will result in a percentage of the current supply voltage. Given so, the TIST designs presented higher average ratios of 18.92% and 15.95% for the 2:1 and 3:1 designs, respectively, with the ST presenting a ratio average of 8.62%. It is important to highlight the ratio losses as well, since due to the variability scaling and its related increase on off-current, the ratios will tend to decrease. Therefore, the TIST designs presented ratio decreases up to 14.68% and the ST presented a better response with a 5.68% decrease. This result is due to the leakage current suppression embedded

Figure 7.13: Average on and off-current increase over all designs through variability scaling. The scaling is normalized in relation to the 1% WFF level measures.

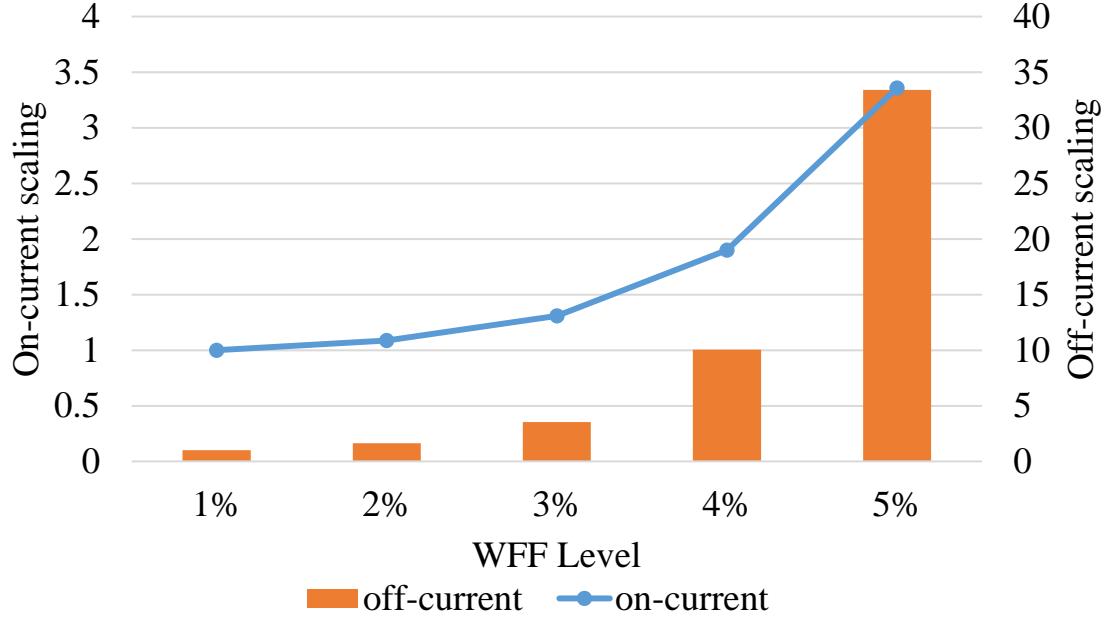


Figure 7.14: Output gain value across voltage scaling.

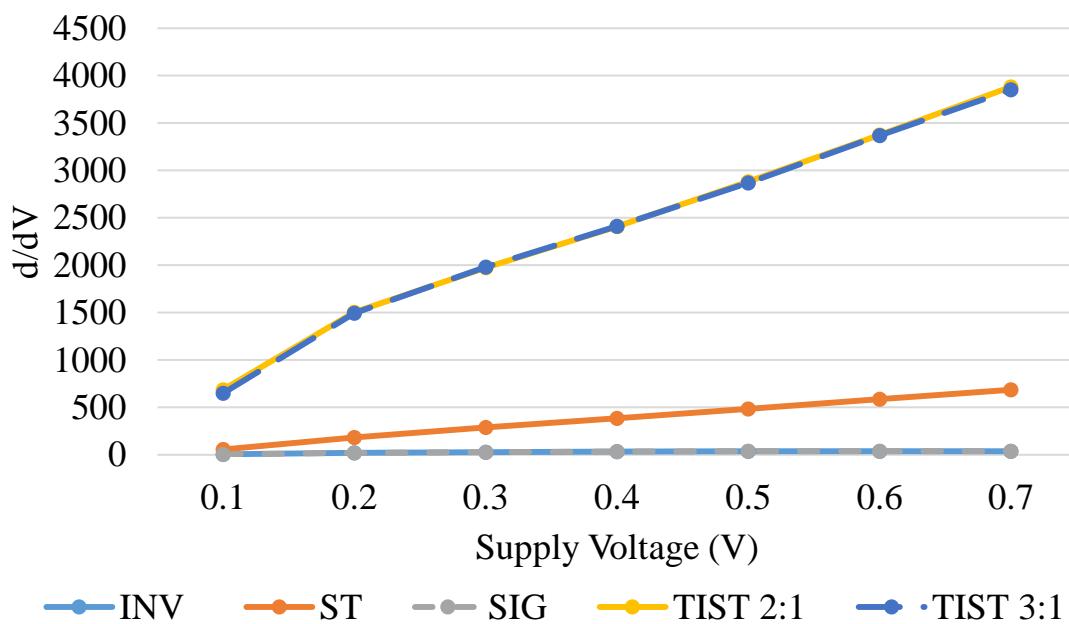


Figure 7.15: Voltage Transfer Curve slopes through supply voltage scaling for each design.

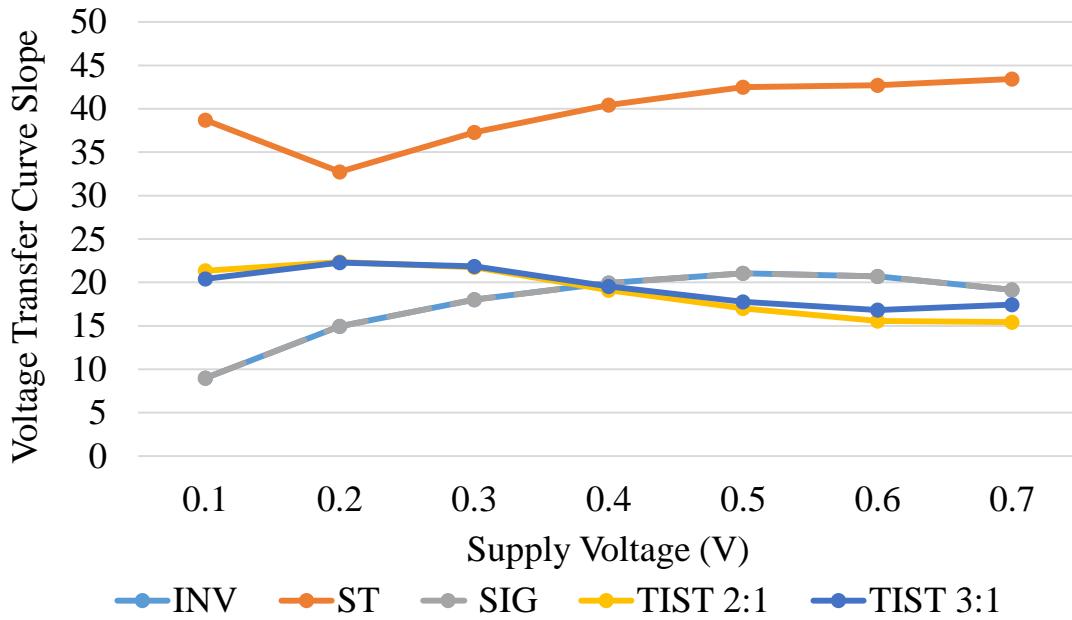


Figure 7.16: Voltage Transfer Curves for all designs at 0.1V.

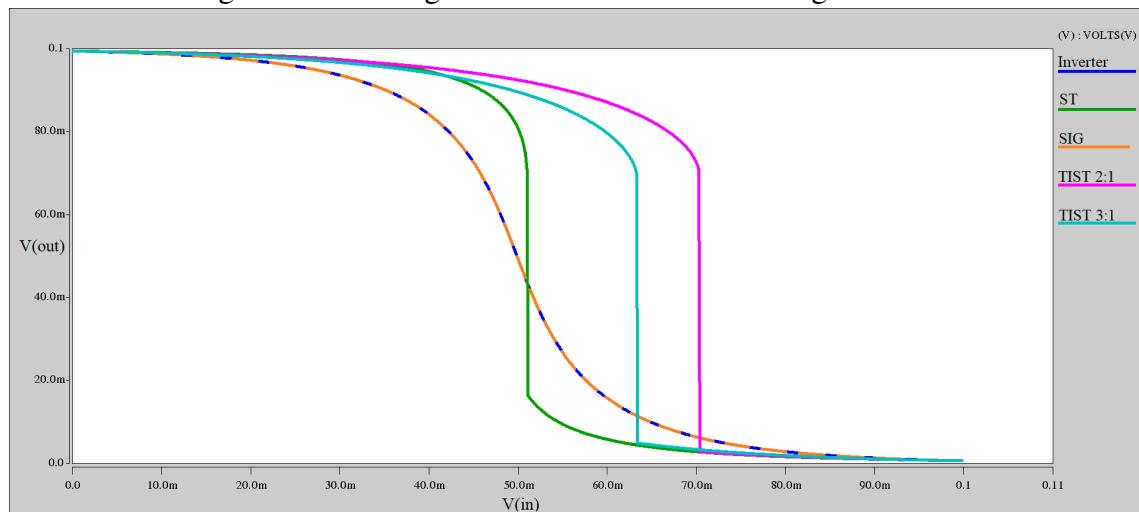
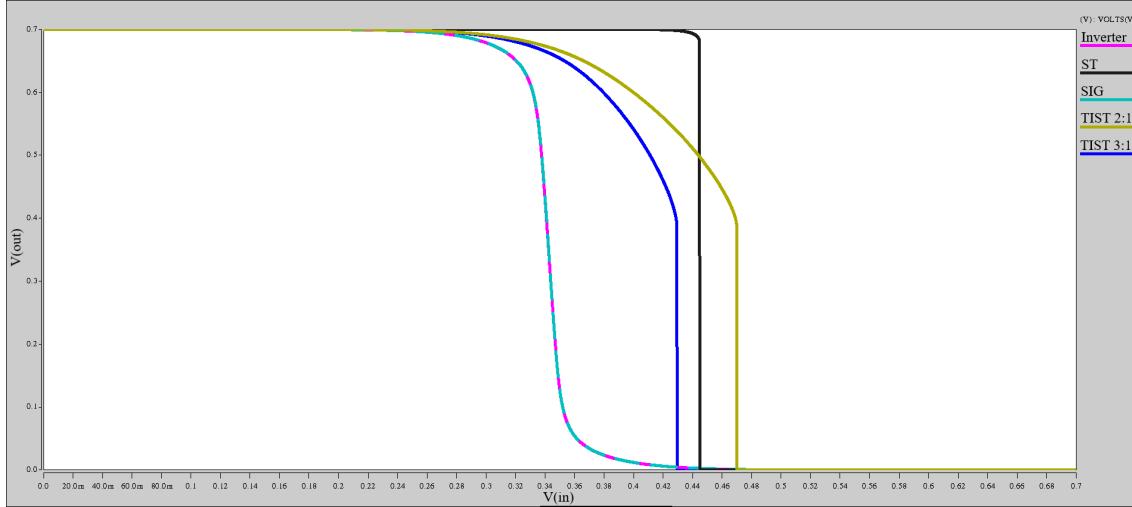


Figure 7.17: Voltage Transfer Curves for all designs at 0.7V.



into the ST design through the feed-back system. The hysteresis curves for all designs at nominal supply voltage are shown in Fig. 7.19. Furthermore, the hysteresis ratios in relation to the supply voltage are shown in Fig. 7.20, it can be observed huge hysteresis intervals for the TIST designs, which are responsible for the circuits failures at working at acceptable frequencies. In order to tackle this problem, further increase of the ratio between the TIST inverter and latch transistors sizes would be necessary, inserting even higher area penalties.

The average hysteresis ratio deviations for each design was 23.44%, 24.83%, and 27.30% for the ST, TIST 2:1 and TIST 3:1. The hysteresis average ratio deviation measures did not present considerable differences between designs, although, at high variability scenarios (5% WFF) the ST presented 16.79% and 21.40% lower deviations, in comparison to the TIST 2:1 and TIST 3:1, respectively.

Figs. 7.21, 7.22, and 7.23, show the distribution of the energy metrics for the inverter over all levels of WFF for 0.2V, 0.4V, and 0.7V supply voltages. For low variability and high supply voltage scenarios it can be observed a normal distribution. While at higher variability and lower supply voltages, a left skew can be noted at first where the majority of the cases stay clustered and as soon as the variability rises, the skew will tend to the left, with extreme cases up to 5 orders of magnitude higher than the mean. Hystograms and dispersion graphs for all designs, are shown in Annex C.

Figure 7.18: Design hysteresis ratio comparison (left) and hysteresis ratio normalized deviation (right), across variability scaling.

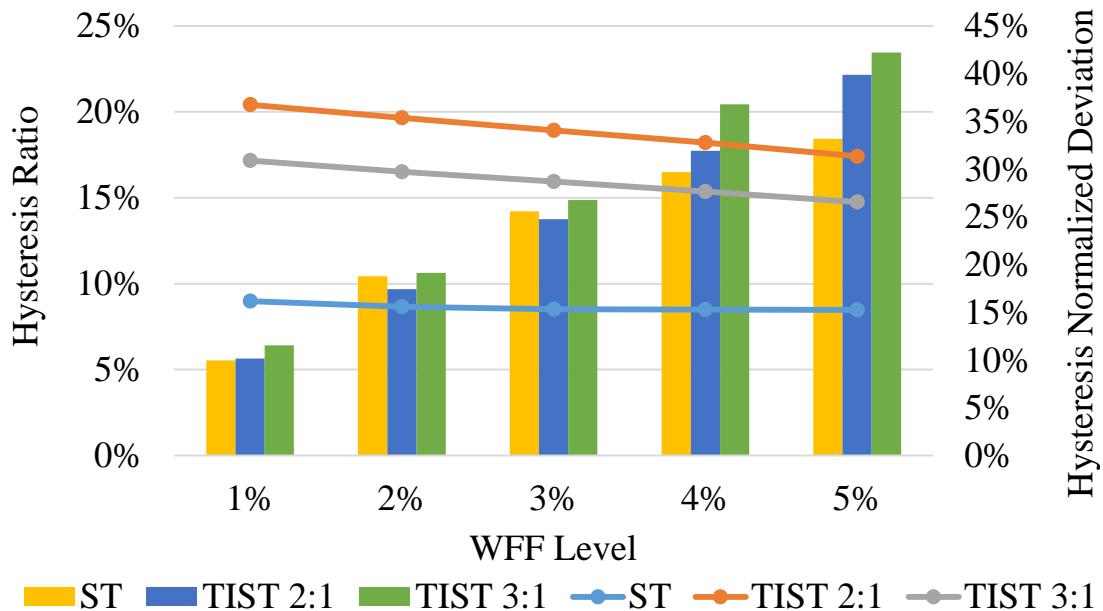


Figure 7.19: Hysteresis curves for all designs at nominal supply voltage.

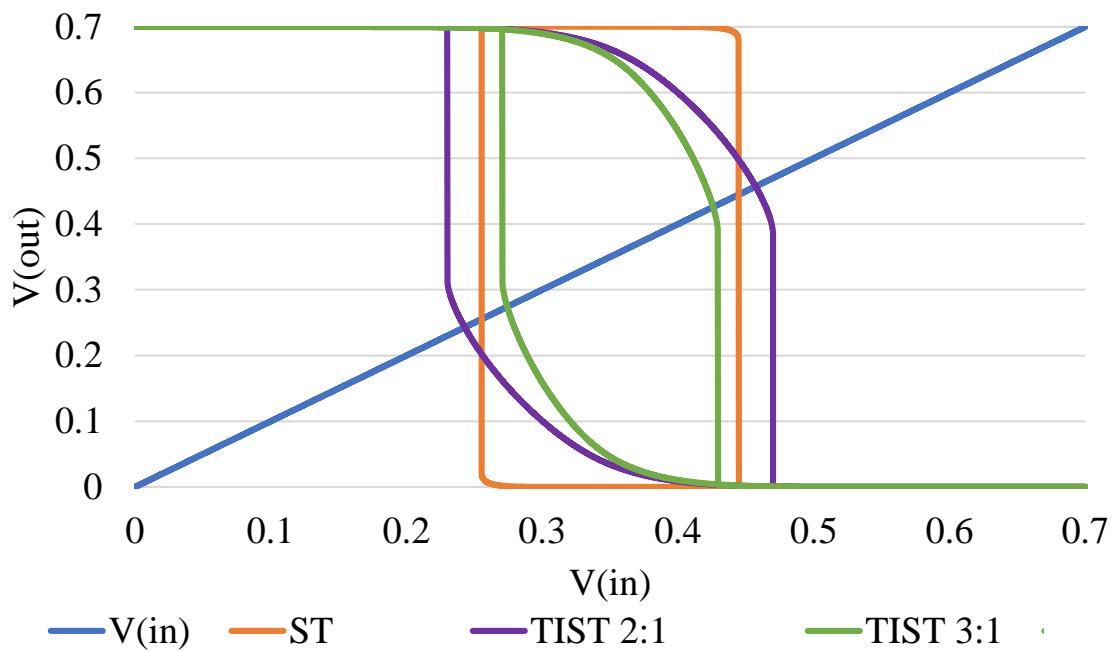
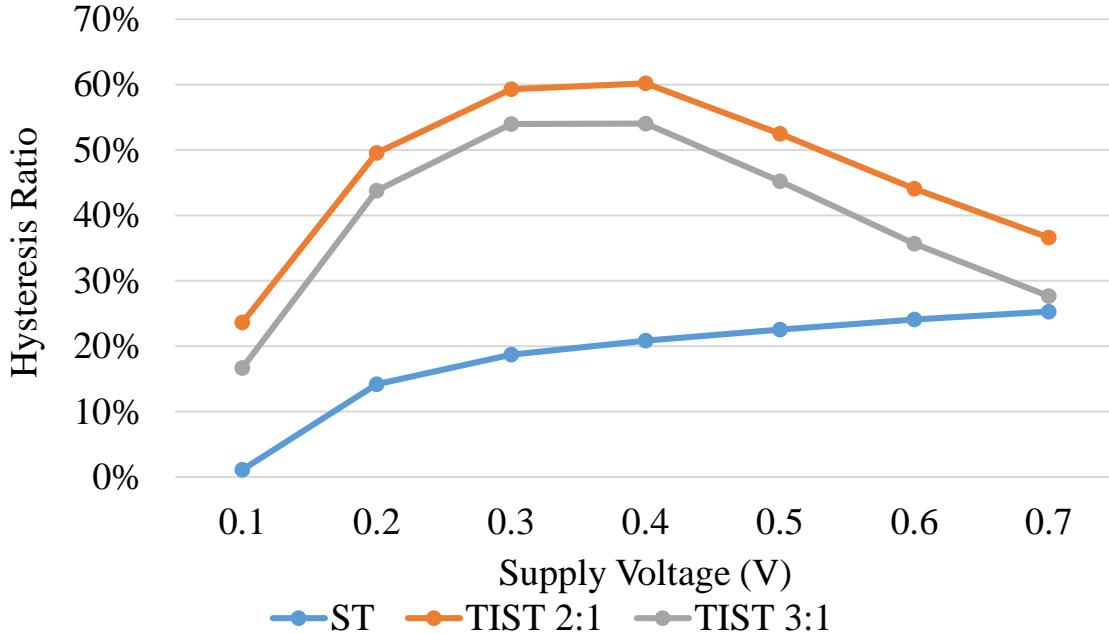


Figure 7.20: Design hysteresis ratios comparison across supply voltage scaling.



7.4 Over ST technique applied on Full Adders

The results are divided into two main analyses, with the set of FAs operating at nominal and near-threshold. In both cases, simulations were performed with and without the ST technique. To better present the improvements (positive values) and drawbacks (negative values) of each ST, results also show a comparison (Δ) between the normalized deviation between the traditional and the circuits with the applied technique.

7.4.1 Nominal Operation

The results concerning propagation times at nominal levels are shown in Table 7.5. It is possible to observe no considerable improvement over variability robustness concerning the propagation times. It can be explained due to the pass-transistor logic present in the TFA, TGA, and Hybrid given further signal degradation as a result of the area increase. Furthermore, it can be observed only a slight improvement over the Mirror FA given its mirroring-based logic with many paths to source and ground.

For the energy results, it was observed considerable improvement over robustness in the Mirror, TFA, and TGA, as shown in Table 7.6. There was a considerable worsening over the Hybrid energy robustness. It is mainly due to its number of transistors, which is comparable to the Mirror FA but it is not entirely based on complementary logic, and

Figure 7.21: Energy measures distribution for the inverter at different levels of variability at 0.2V.

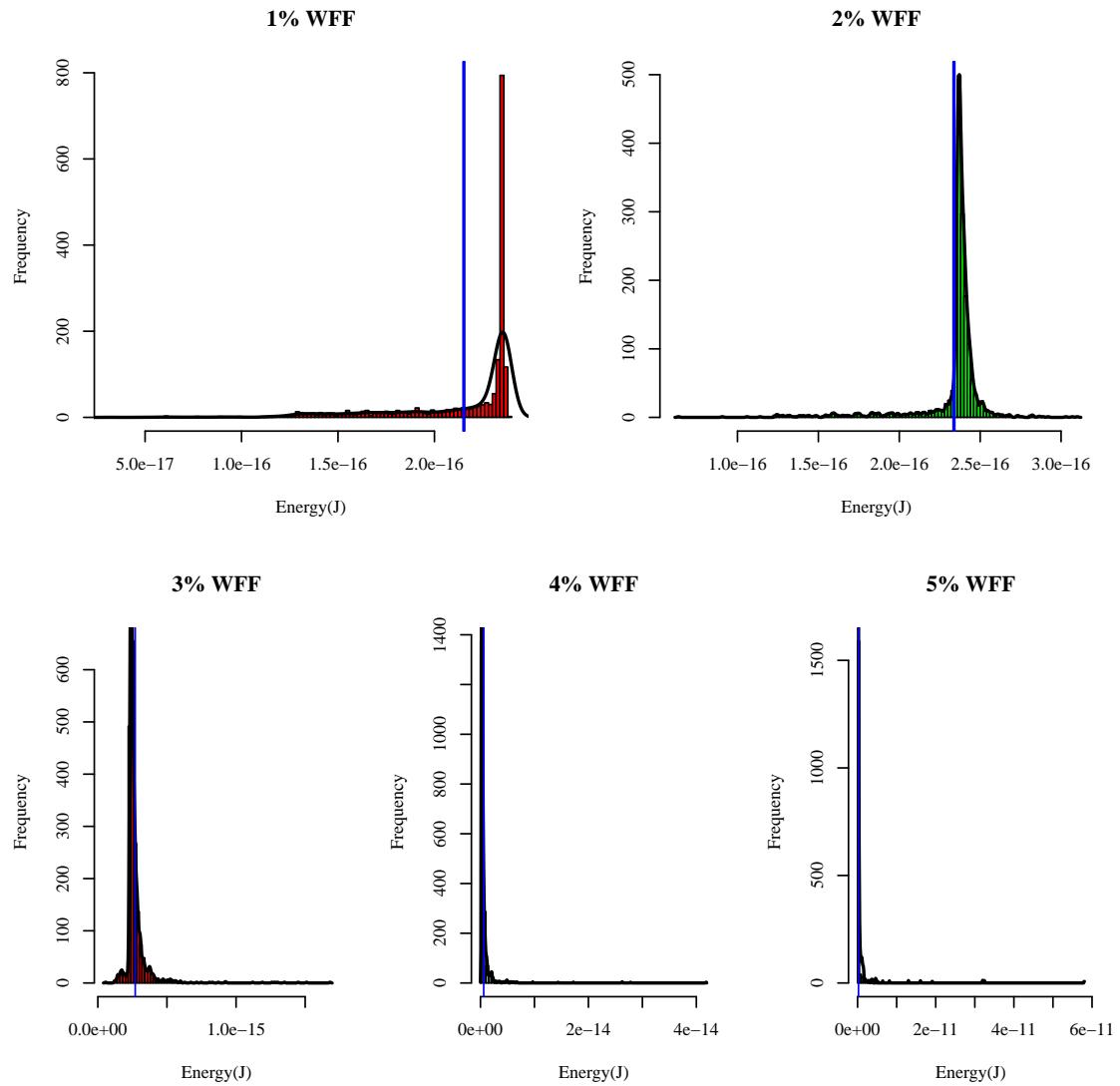


Figure 7.22: Energy measures distribution for the inverter at different levels of variability at 0.4V.

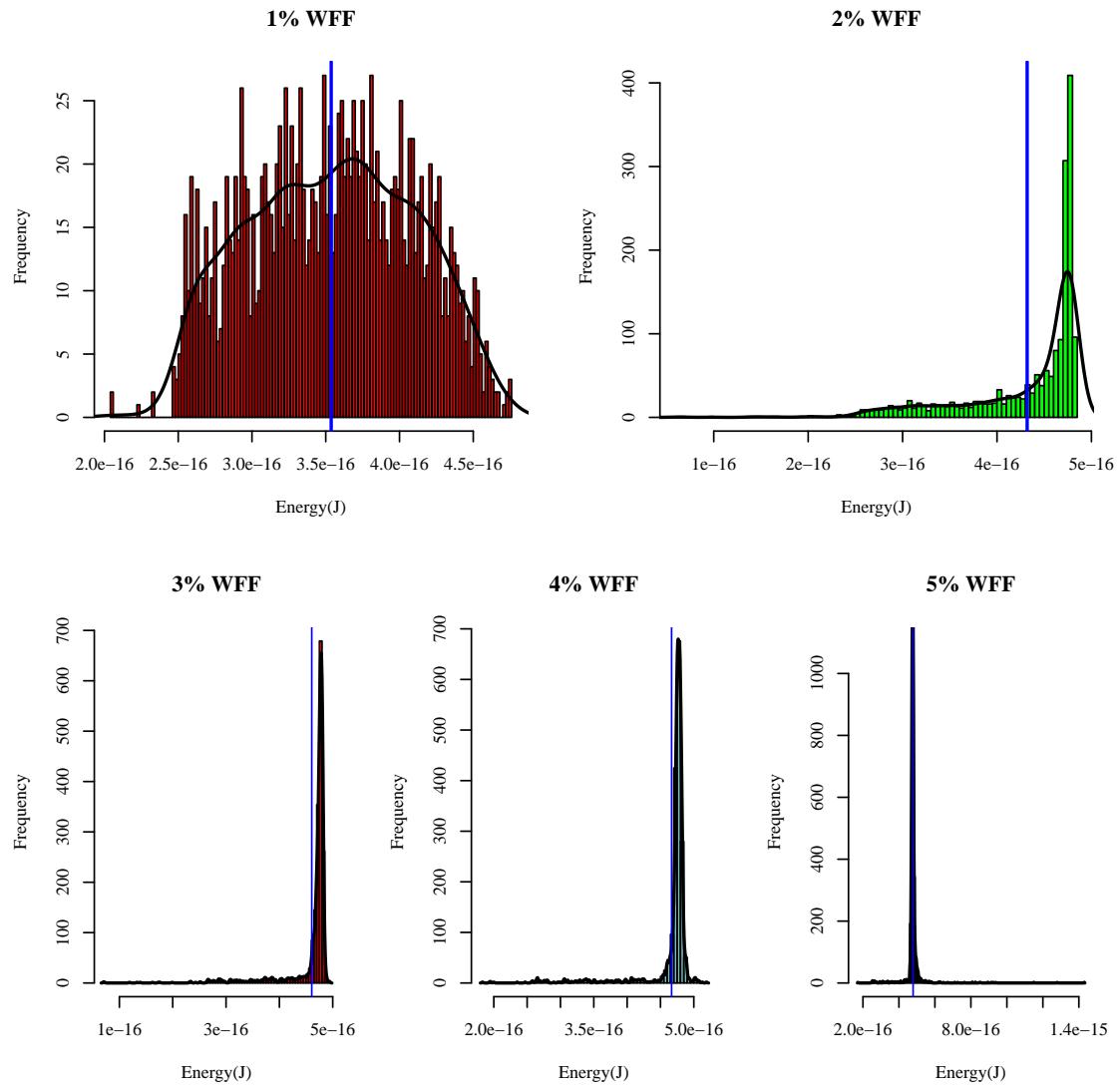


Figure 7.23: Energy measures distribution for the inverter at different levels of variability at 0.7V.

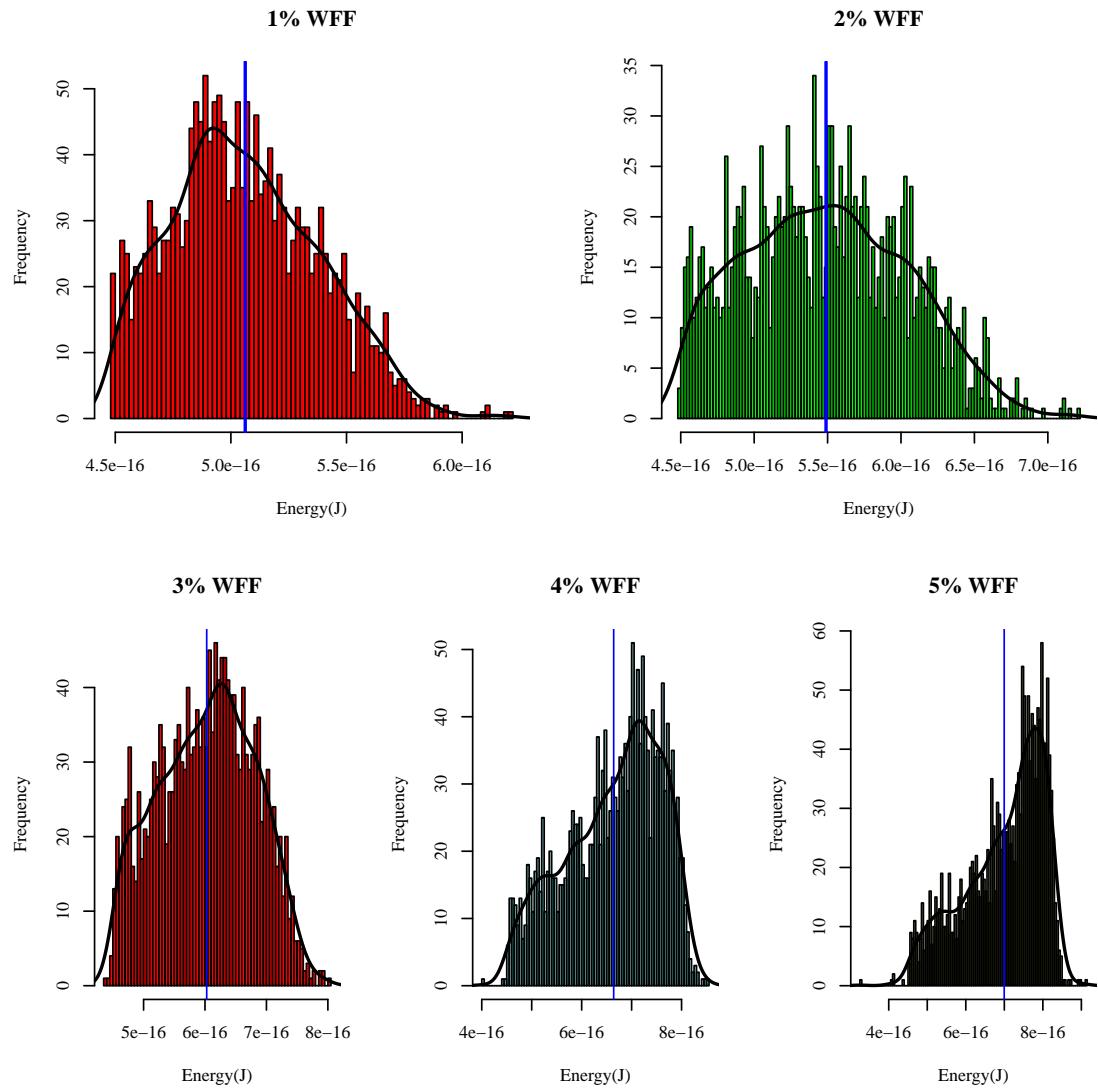


Table 7.5: Delay measures for nominal voltage operation

FA	ST	Delays							
		SUM				CARRY OUT			
		$\mu(\text{ps})$	$\sigma(\text{ps})$	$\sigma/\mu(\%)$	$\Delta(\%)$	$\mu(\text{ps})$	$\sigma(\text{ps})$	$\sigma/\mu(\%)$	$\Delta(\%)$
Mirror	-	22.83	4.82	20.89	-	22.60	4.39	19.38	-
	ST1	27.38	5.75	20.77	0.54	25.31	4.79	18.87	2.63
	ST2	42.28	8.57	20.23	3.13	41.48	7.96	19.17	1.10
TFA	-	20.76	5.51	30.69	-	19.75	4.70	25.74	-
	ST1	24.24	6.43	31.42	-2.37	22.50	5.51	26.74	-3.86
	ST2	42.36	76.87	126.26	-311.36	26.91	6.86	31.45	-22.18
TGA	-	21.56	4.30	22.36	-	22.96	4.70	20.46	-
	ST1	25.32	5.36	26.42	-18.16	26.39	5.41	20.38	0.37
	ST2	97.92	210.62	102.35	-357.80	32.80	7.85	25.70	-25.63
Hybrid	-	24.02	5.31	21.75	-	23.58	4.89	21.65	-
	ST1	60.96	64.91	92.40	-324.90	42.07	21.84	34.84	-60.90
	ST2	69.68	40.87	50.82	-133.72	72.05	25.81	29.23	-35.00

Table 7.6: Energy measures for nominal voltage operation

FA	ST	Energy							
		SUM				CARRY OUT			
		$\mu(\text{fJ})$	$\sigma(\text{fJ})$	$\sigma/\mu(\%)$	$\Delta(\%)$	$\mu(\text{fJ})$	$\sigma(\text{fJ})$	$\sigma/\mu(\%)$	$\Delta(\%)$
Mirror	-	19.30	3.55	18.35	-	27.30	3.99	14.60	-
	ST1	26.80	4.85	18.10	1.37	37.20	5.54	14.87	-1.84
	ST2	36.50	5.50	15.07	17.87	50.80	6.54	12.87	11.84
TFA	-	4.97	1.27	25.59	-	5.15	0.72	13.91	-
	ST1	10.90	1.46	13.38	47.70	10.80	0.98	9.09	34.68
	ST2	17.00	2.02	11.94	53.35	15.30	2.02	13.21	5.05
TGA	-	14.10	3.81	27.07	-	15.70	4.44	28.20	-
	ST1	24.90	6.33	25.46	5.95	26.40	4.21	15.94	43.48
	ST2	32.40	7.49	23.16	14.44	37.60	7.35	19.53	30.74
Hybrid	-	19.30	4.10	21.26	-	26.30	4.55	17.29	-
	ST1	72.50	37.95	52.34	-146.19	94.60	48.21	50.94	-194.62
	ST2	73.20	21.25	29.05	-36.64	95.20	19.89	20.90	-20.88

the number of internal inverters replaced, further increasing its area and signal degradation. Overall, the traditional TFA presented the best performance and, by far, the lowest energy consumption and energy normalized deviation at nominal operation. However, it presented the highest delay deviations.

7.4.2 Near-Threshold Operation

At near-threshold operation, there is little room for noise margin. Given so, it makes full use of the noise immunity characteristic of the STs, as shown in Table 7.7. It can be observed a superior robustness improvement with the ST2, given its smaller area,

Table 7.7: Delay measures for near-threshold operation

FA	ST	Delays							
		SUM				CARRY OUT			
		$\mu(\text{ps})$	$\sigma(\text{ps})$	$\sigma/\mu(\%)$	$\Delta(\%)$	$\mu(\text{ps})$	$\sigma(\text{ps})$	$\sigma/\mu(\%)$	$\Delta(\%)$
Mirror	-	103.49	63.18	60.95	-	91.62	55.41	59.18	-
	ST1	119.98	67.63	56.09	7.97	115.50	73.68	64.11	-8.32
	ST2	155.58	67.03	42.94	29.55	153.50	68.89	44.86	24.20
TFA	-	122.48	117.46	111.51	-	111.64	186.41	236.88	-
	ST1	142.18	146.61	97.85	12.25	118.26	194.03	242.22	-2.26
	ST2	215.93	222.26	117.29	-5.18	165.48	335.16	273.57	-15.49
TGA	-	130.43	109.19	85.78	-	114.78	130.53	138.93	-
	ST1	122.99	98.03	79.75	7.03	128.98	101.51	88.48	36.32
	ST2	187.84	125.13	70.99	17.25	164.06	109.19	72.68	47.68
Hybrid	-	115.90	83.02	70.57	-	111.92	82.45	74.76	-
	ST1	187.36	143.80	78.99	-11.93	116.02	71.26	61.00	18.41
	ST2	207.00	168.04	72.56	-2.81	167.50	66.72	40.94	45.23

and consequently, lower signal degradation. In the case of the TFA it seems that due to its few paths to source and ground, the higher parasitic capacitance and resistance present in ST2 brings higher deviation, with the ST1 presenting better results.

For the energy results, shown in Table 7.8, ST1 showed superior robustness improvement for the TFA and TGA, which can be explained by their pass-transistor based logic and the ST1 smaller parasitics, in comparison to the Mirror and Hybrid FAs which showed no improvement whatsoever.

For the delay results, the Mirror FA showed the lowest means and normalized deviations, which is expected given it is not based on pass-transistor logic, having better driving capabilities. For the energy measures, TFA showed the lowest mean, due to its pass-transistor logic and lower number of transistors. Although, the TFA presented the highest delay normalized deviations. Overall, the TGA showed the lowest normalized deviations in energy and the highest robustness gains concerning delay and energy measures.

7.4.3 Penalties

Overviews for metrics measurements and variability sensitivities are shown in Figs. 7.24 to 7.27. Since it was considered a technique where a single inverter (2 transistors) by ST1/ST2 (4/6 transistors). It is expected penalties concerning delay, energy and area metrics. For the delays, it was observed an average 30% and 97% increase for the ST1 and ST2, respectively. Additionally, for the energy, there was a 123% and 176%

Table 7.8: Energy measures for near-threshold operation

FA	ST	Energy							
		SUM				CARRY OUT			
		$\mu(\text{fJ})$	$\sigma(\text{fJ})$	$\sigma/\mu(\%)$	$\Delta(\%)$	$\mu(\text{fJ})$	$\sigma(\text{fJ})$	$\sigma/\mu(\%)$	$\Delta(\%)$
Mirror	-	10.10	3.04	30.12	-	14.10	2.53	18.00	-
	ST1	13.90	4.05	29.07	3.50	18.60	4.25	22.93	-27.42
	ST2	18.40	4.34	23.60	21.64	25.30	5.73	22.59	-25.53
TFA	-	2.62	0.83	31.49	-	2.71	0.37	13.49	-
	ST1	5.67	1.34	23.69	24.76	5.69	0.63	11.01	18.38
	ST2	9.69	2.11	21.74	30.96	8.80	2.59	29.40	-117.89
TGA	-	6.87	1.56	22.68	-	8.11	2.90	35.70	-
	ST1	12.90	2.37	18.45	18.65	13.50	1.86	13.79	61.37
	ST2	16.10	3.09	19.17	15.48	17.30	2.57	14.86	58.38
Hybrid	-	9.66	3.09	32.02	-	12.80	3.17	24.77	-
	ST1	36.40	17.94	49.30	-53.96	45.80	23.63	51.54	-108.07
	ST2	35.40	12.72	35.91	-12.14	46.60	13.84	29.69	-19.86

average increase for the ST1 and ST2, respectively.

Concerning area penalties, the ST1 increased the FAs area by 157.71%, on average, while the ST2 increased by 52.20%. The ST1 higher increase in area is due to the necessity to use TAP-Cells, which is a technology restriction, in order to explicitly connect the transistor's bulk to specific points of the circuit or source/ground making the ST1 cell more prominent than expected. The ST2 does not apply specific bulk connections, although it was necessary the use of METAL3 for cell routing, increasing parasitic capacitance and resistance.

Considering all scenarios, there can be observed no delay robustness improvement at nominal operation with the ST1 and ST2 showing, on average, 50% and 115.2% worsening on delay robustness, respectively. For energy robustness, at nominal operation, the ST2 presented a considerable average improvement of 11.18% while the ST1 showed an average worsening of 25%. For near-threshold operation, ST1 and ST2 showed 7.79% and 18.173% higher delay robustness. For energy robustness, the ST2 showed a 4.13% improvement while the ST1 presented a worsening of 4.5%.

Figure 7.24: Average delay measures for nominal operation and their respective normalized deviation (variability sensitivity).

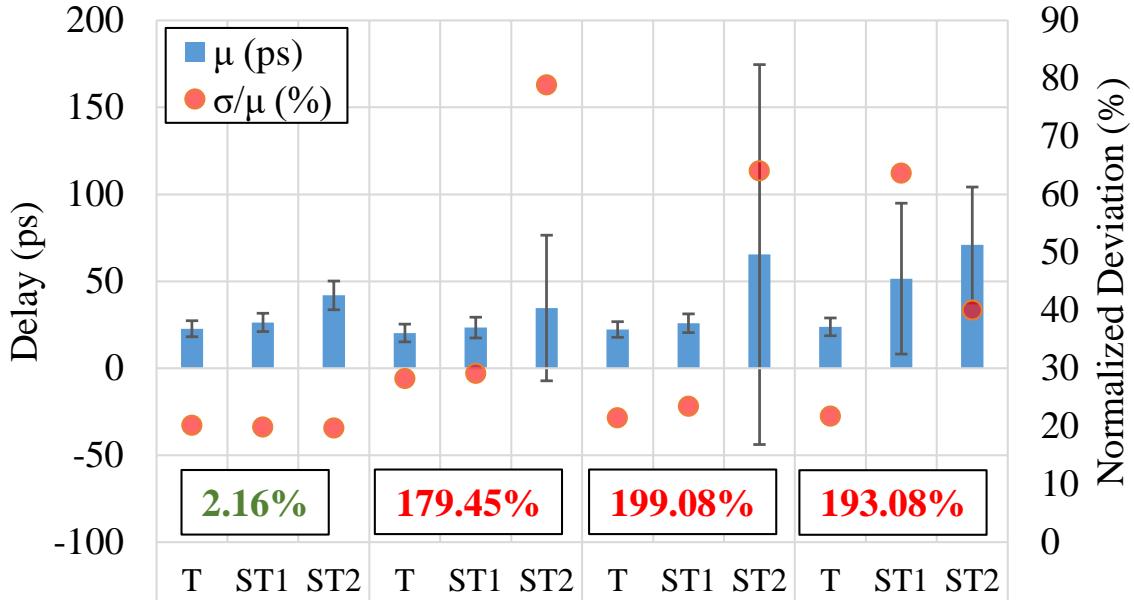


Figure 7.25: Average energy measures for nominal operation and their respective normalized deviation (variability sensitivity).

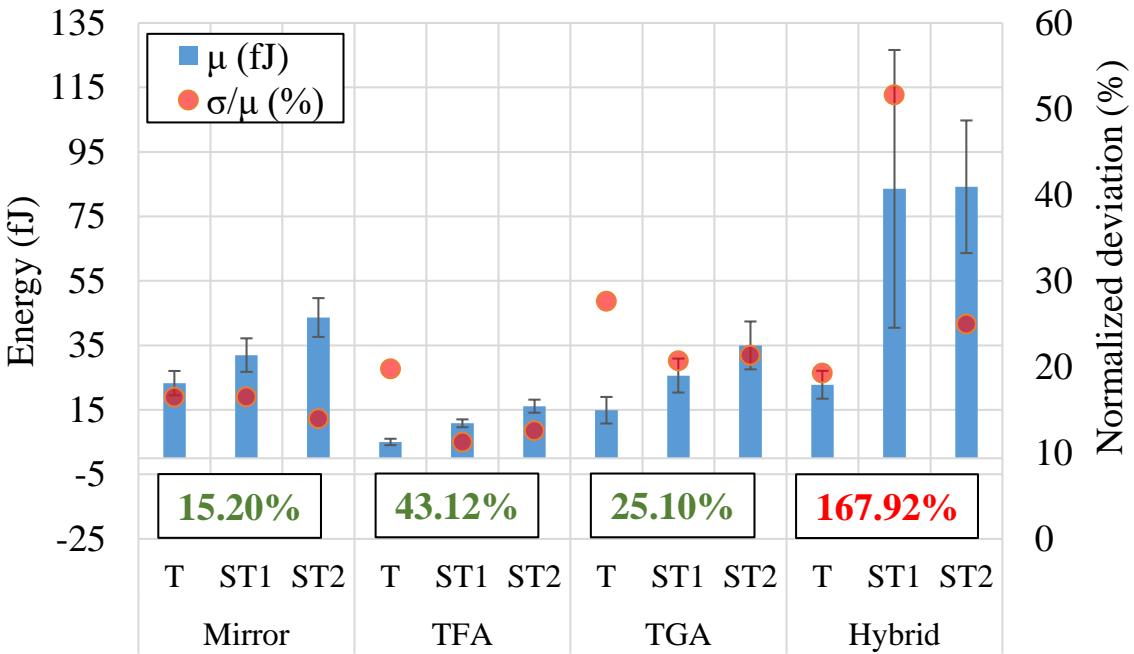


Figure 7.26: Average delay measures for near-threshold operation and their respective normalized deviation (variability sensitivity).

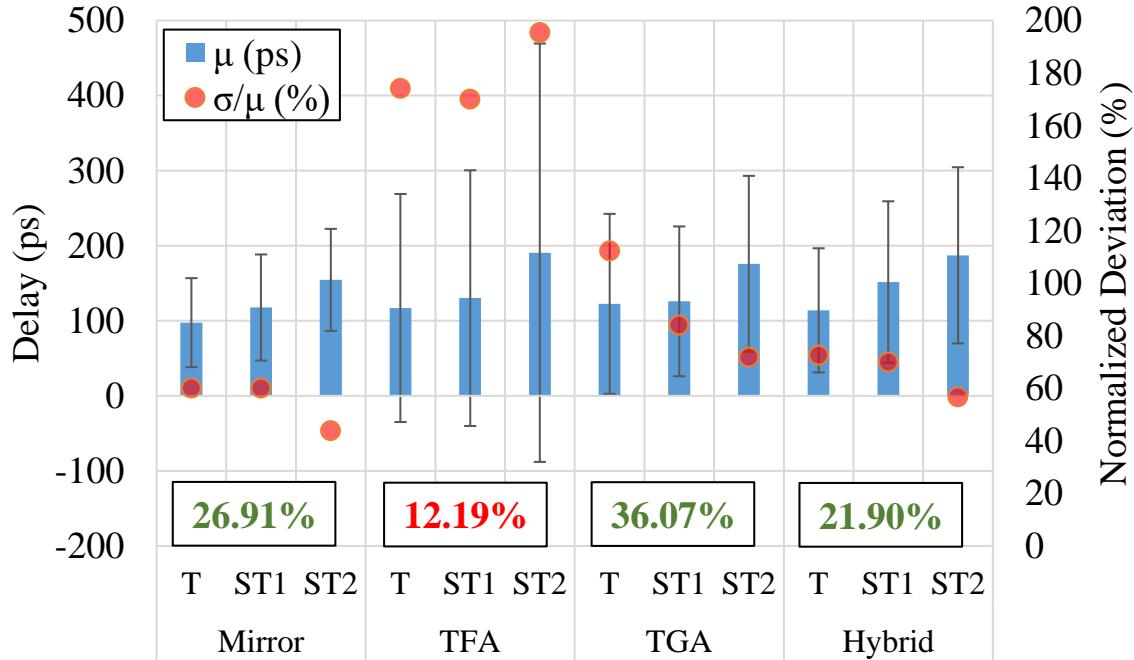
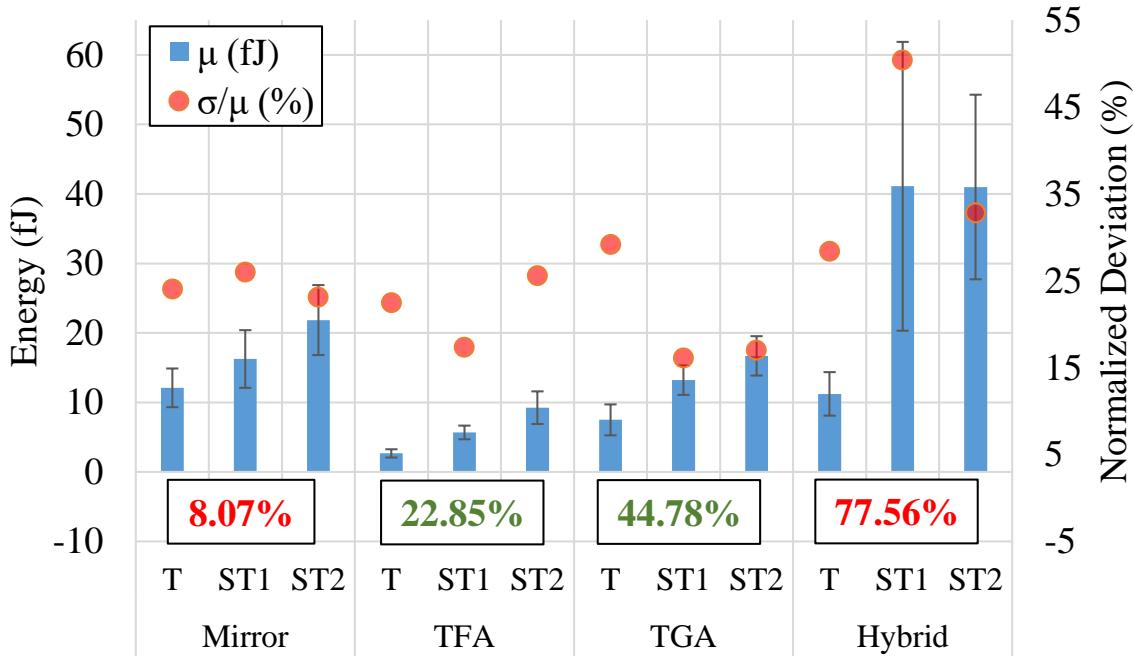


Figure 7.27: Average energy measures for near-threshold operation and their respective normalized deviation (variability sensitivity).



8 CONCLUSIONS

The ongoing trend of IoT devices was enabled by two key technology improvements: battery lifetime and capacity improvement, and node scaling. Although, for specific applications, battery maintenance and charging through the power grid is not possible. Given so, IoT devices have been constrained with tight energy consumption metrics, and adapted with self-sufficient mechanisms in order to produce energy through external sources.

The node scaling, that enabled IoT devices, comes not short of inherent challenges, with process variability being the major one. New transistor technologies have been proposed such as FinFETs, although even such devices, at deep submicron nodes (e.g. 7-nm), present considerable deviation in its metrics. Such deviations are not appropriate for such sensible devices working at narrow constraints (with energy consumption being a priority).

Given so, an analysis over multiple scenarios considering several levels of process variability, supply voltages, and transistor sizing was performed in order to identify the adequate fin number and supply voltage for various kinds of applications prioritizing energy consumption and the minimization of deviations.

Performance maior desempenho perda de frequencia maior robustez nos delays

Energia menor consumo de energia menor desvios

Correntes Ganhos Histerese Margens de ruído Area

REFERENCES

- ABBAS, Z. et al. Optimal nbti degradation and pvt variation resistant device sizing in a full adder cell. In: **IEEE. Reliability, Infocom Technologies and Optimization (ICRITO)(Trends and Future Directions), 2015 4th International Conference on.** [S.I.], 2015. p. 1–6.
- AHMAD, S. et al. Single-ended schmitt-trigger-based robust low-power sram cell. In: . [S.I.]: IEEE, 2016. v. 24, n. 8, p. 2634–2642.
- AHMADI, M.; ALIZADEH, B.; FOROUZANDEH, B. A hybrid time borrowing technique to improve the performance of digital circuits in the presence of variations. In: . [S.I.]: IEEE, 2017. v. 64, n. 1, p. 100–110.
- AL-SARAWI, S. Low power schmitt trigger circuit. **Electronics letters**, IET, v. 38, n. 18, p. 1009–1010, 2002.
- ALIOTO, M.; CONSOLI, E.; PALUMBO, G. Variations in nanometer cmos flip-flops part ii: Energy variability and impact of other sources of variations. In: . [S.I.: s.n.], 2015. v. 62, n. 3, p. 835–843.
- ALIOTO, M.; CONSOLI, E.; PALUMBO, G. Variations in nanometer cmos flip-flops: Part i—impact of process variations on timing. **IEEE Transactions on Circuits and Systems I: Regular Papers**, IEEE, v. 62, n. 8, p. 2035–2043, 2015.
- ALIOTO, M.; PALUMBO, G. Delay variability due to supply variations in transmission-gate full adders. In: **IEEE. Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on.** [S.I.], 2007. p. 3732–3735.
- AMES, S. O. et al. Investigating pvt variability effects on full adders. In: **IEEE. Power and Timing Modeling, Optimization and Simulation (PATMOS), 2016 26th International Workshop on.** [S.I.], 2016. p. 155–161.
- ASENOV, A. Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm mosfets: a statistical 3datomistic’simulation study. In: . [S.I.]: IOP Publishing, 1999. v. 10, n. 2, p. 153.
- ASENOV, A. et al. Simulation of intrinsic parameter fluctuations in decanometer and nanometer-scale mosfets. **IEEE transactions on electron devices**, IEEE, v. 50, n. 9, p. 1837–1852, 2003.
- AUSTIN, T. et al. Opportunities and challenges for better than worst-case design. In: **ACM. Proceedings of the 2005 Asia and South Pacific Design Automation Conference.** [S.I.], 2005. p. 2–7.
- BAI, X.; VISWESWARIAH, C.; STRENSKI, P. N. Uncertainty-aware circuit optimization. In: **ACM. Proceedings of the 39th annual Design Automation Conference.** [S.I.], 2002. p. 58–63.
- BECKETT, P. A fine-grained reconfigurable logic array based on double gate transistors. In: **IEEE. Field-Programmable Technology, 2002.(FPT). Proceedings. 2002 IEEE International Conference on.** [S.I.], 2002. p. 260–267.

- BERNSTEIN, K. et al. High-performance cmos variability in the 65-nm regime and beyond. **IBM journal of research and development**, IBM, v. 50, n. 4.5, p. 433–449, 2006.
- BHATTACHARYA, D.; JHA, N. K. Finfets: From devices to architectures. In: . [S.l.]: Hindawi, 2014. v. 2014.
- BLEITNER, A. et al. Comparison and optimization of the minimum supply voltage of schmitt trigger gates versus cmos gates under process variations. In: VDE. **ANALOG 2018; 16th GMM/ITG-Symposium**. [S.l.], 2018. p. 1–6.
- BORKAR, S. et al. Design and reliability challenges in nanometer technologies. In: ACM. **Proceedings of the 41st annual Design Automation Conference**. [S.l.], 2004. p. 75–75.
- BOSE, S.; JOHNSTON, M. L. A stacked-inverter ring oscillator for 50 mv fully-integrated cold-start of energy harvesters. In: IEEE. **2018 IEEE International Symposium on Circuits and Systems (ISCAS)**. [S.l.], 2018. p. 1–5.
- BROWN, A. R. et al. Impact of metal gate granularity on threshold voltage variability: A full-scale three-dimensional statistical simulation study. **IEEE Electron Device Letters**, IEEE, v. 31, n. 11, p. 1199–1201, 2010.
- BRUNNER, T. A. Why optical lithography will live forever. **Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena**, AVS, v. 21, n. 6, p. 2632–2637, 2003.
- CHANG, K.-L. et al. Synchronous-logic and asynchronous-logic 8051 microcontroller cores for realizing the internet of things: A comparative study on dynamic voltage scaling and variation effects. **IEEE journal on emerging and selected topics in circuits and systems**, IEEE, v. 3, n. 1, p. 23–34, 2013.
- CHAVA, B. et al. Standard cell design in n7: Euv vs. immersion. In: INTERNATIONAL SOCIETY FOR OPTICS AND PHOTONICS. **Design-Process-Technology Co-optimization for Manufacturability IX**. [S.l.], 2015. v. 9427, p. 94270E.
- CLARK, L. T. et al. Asap7: A 7-nm finfet predictive process design kit. In: . [S.l.]: Elsevier, 2016. v. 53, p. 105–115.
- COLINGE, J.-P. et al. **FinFETs and other multi-gate transistors**. [S.l.]: Springer, 2008.
- DADGOUR, H.; DE, V.; BANERJEE, K. Statistical modeling of metal-gate work-function variability in emerging device technologies and implications for circuit design. In: IEEE. **2008 IEEE/ACM International Conference on Computer-Aided Design**. [S.l.], 2008. p. 270–277.
- DATTA, S. et al. High mobility si/sige strained channel mos transistors with hfo/sub 2//tin gate stack. In: IEEE. **IEEE International Electron Devices Meeting 2003**. [S.l.], 2003. p. 28–1.

DEVADAS, M.; KISHORE, K. L. Design topologies for low power cmos full adder. In: **IEEE. Inventive Systems and Control (ICISC), 2017 International Conference on.** [S.I.], 2017. p. 1–4.

DIGHE, S. et al. Within-die variation-aware dynamic-voltage-frequency-scaling with optimal core allocation and thread hopping for the 80-core teraflops processor. **IEEE Journal of Solid-State Circuits**, IEEE, v. 46, n. 1, p. 184–193, 2011.

DOKANIA, V.; IMRAN, A.; ISLAM, A. Investigation of robust full adder cell in 16-nm cmos technology node. In: **IEEE. Multimedia, Signal Processing and Communication Technologies (IMPACT), 2013 International Conference on.** [S.I.], 2013. p. 207–211.

DOKANIA, V.; ISLAM, A. Circuit-level design technique to mitigate impact of process, voltage and temperature variations in complementary metal-oxide semiconductor full adder cells. In: . [S.I.]: IET, 2015. v. 9, n. 3, p. 204–212.

DOKI, B. L. Cmos schmitt triggers. In: **IET. IEE Proceedings G-Electronic Circuits and Systems.** [S.I.], 1984. v. 131, n. 5, p. 197–202.

DRESLINSKI, R. G. et al. Near-threshold computing: Reclaiming moore's law through energy efficient integrated circuits. **Proceedings of the IEEE**, IEEE, v. 98, n. 2, p. 253–266, 2010.

FARKHANI, H. et al. Comparative study of finfets versus 22nm bulk cmos technologies: Sram design perspective. In: **IEEE. 2014 27th IEEE International System-on-Chip Conference (SOCC).** [S.I.], 2014. p. 449–454.

FEDERSPIEL, X. et al. 28nm node bulk vs fdsoi reliability comparison. In: **IEEE. Reliability Physics Symposium (IRPS), 2012 IEEE International.** [S.I.], 2012. p. 3B–1.

FERNANDES, T. **CMOS Amplifiers and Schmitt Triggers for Ultra-Low-Voltage Applications.** [S.I.: s.n.], 2019.

FOJTIK, M. et al. A millimeter-scale energy-autonomous sensor system with stacked battery and solar cells. **IEEE Journal of Solid-State Circuits**, IEEE, v. 48, n. 3, p. 801–813, 2013.

FRANK, D. J. et al. Device scaling limits of si mosfets and their application dependencies. **Proceedings of the IEEE**, IEEE, v. 89, n. 3, p. 259–288, 2001.

FRANK, D. J.; WONG, H.-S. Simulation of stochastic doping effects in si mosfets. In: **IEEE. 7th International Workshop on Computational Electronics. Book of Abstracts. IWCE (Cat. No. 00EX427).** [S.I.], 2000. p. 2–3.

GUDURI, M.; ISLAM, A. Design of hybrid full adder in deep subthreshold region for ultralow power applications. In: **IEEE. Signal Processing and Integrated Networks (SPIN), 2015 2nd International Conference on.** [S.I.], 2015. p. 931–935.

GUSEV, E. et al. Ultrathin high-k gate stacks for advanced cmos devices. In: **IEEE. International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224).** [S.I.], 2001. p. 20–1.

- GUSEV, E. P.; NARAYANAN, V.; FRANK, M. M. Advanced high- κ dielectric stacks with polysilicon and metal gates: Recent progress and current challenges. **IBM Journal of Research and Development**, IBM, v. 50, n. 4.5, p. 387–410, 2006.
- HARRINGTON, R. C. et al. Effect of transistor variants on single-event transients at the 14/16nm bulk finfet technology generation. In: . [S.l.: s.n.], 2018. p. 1–1.
- HAYS, K. I. A 62 mv 0.13 um cmos standard-cell-based design technique using schmitt-trigger logic. 2012.
- HENZLER, S. **Power management of digital circuits in deep sub-micron CMOS technologies**. [S.l.]: Springer Science & Business Media, 2006.
- HOBBS, C. C. et al. Fermi-level pinning at the polysilicon/metal-oxide interface-part ii. **IEEE Transactions on Electron Devices**, IEEE, v. 51, n. 6, p. 978–984, 2004.
- ISLAM, A. et al. Design and analysis of robust dual threshold cmos full adder circuit in 32nm technology. In: **IEEE. Advances in Recent Technologies in Communication and Computing (ARTCom), 2010 International Conference on**. [S.l.], 2010. p. 418–420.
- ISLAM, A.; AKRAM, M. W.; HASAN, M. Variability immune finfet-based full adder design in subthreshold region. In: **IEEE. Devices and Communications (ICDeCom), 2011 International Conference on**. [S.l.], 2011. p. 1–5.
- ISLAM, A.; HASAN, M. Design and analysis of power and variability aware digital summing circuit. In: . [S.l.: s.n.], 2011. v. 2, n. 2, p. 6–14.
- JEON, D. et al. Design methodology for voltage-overscaled ultra-low-power systems. **IEEE Transactions on Circuits and Systems II: Express Briefs**, IEEE, v. 59, n. 12, p. 952–956, 2012.
- JEONG, K.; KAHNG, A. B.; SAMADI, K. Impact of guardband reduction on design outcomes: A quantitative approach. **IEEE Transactions on Semiconductor Manufacturing**, IEEE, v. 22, n. 4, p. 552–565, 2009.
- KAHNG, A. B. et al. Slack redistribution for graceful degradation under voltage overscaling. In: **IEEE. 2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC)**. [S.l.], 2010. p. 825–831.
- KAKOEE, M. R.; LOI, I.; BENINI, L. Variation-tolerant architecture for ultra low power shared-11 processor clusters. **IEEE Transactions on Circuits and Systems II: Express Briefs**, IEEE, v. 59, n. 12, p. 927–931, 2012.
- KHAN, S.; DAHIYA, R. S.; LORENZELLI, L. Flexible thermoelectric generator based on transfer printed si microwires. In: **IEEE. 2014 44th European Solid State Device Research Conference (ESSDERC)**. [S.l.], 2014. p. 86–89.
- KIM, D.; KIH, J.; KIM, W. A new waveform-reshaping circuit: an alternative approach to schmitt trigger. **IEEE journal of solid-state circuits**, IEEE, v. 28, n. 2, p. 162–164, 1993.
- KING, T.-J. Finfets for nanoscale cmos digital integrated circuits. In: **ICCAD-2005. IEEE/ACM International Conference on Computer-Aided Design, 2005**. [S.l.: s.n.], 2005. p. 207–210.

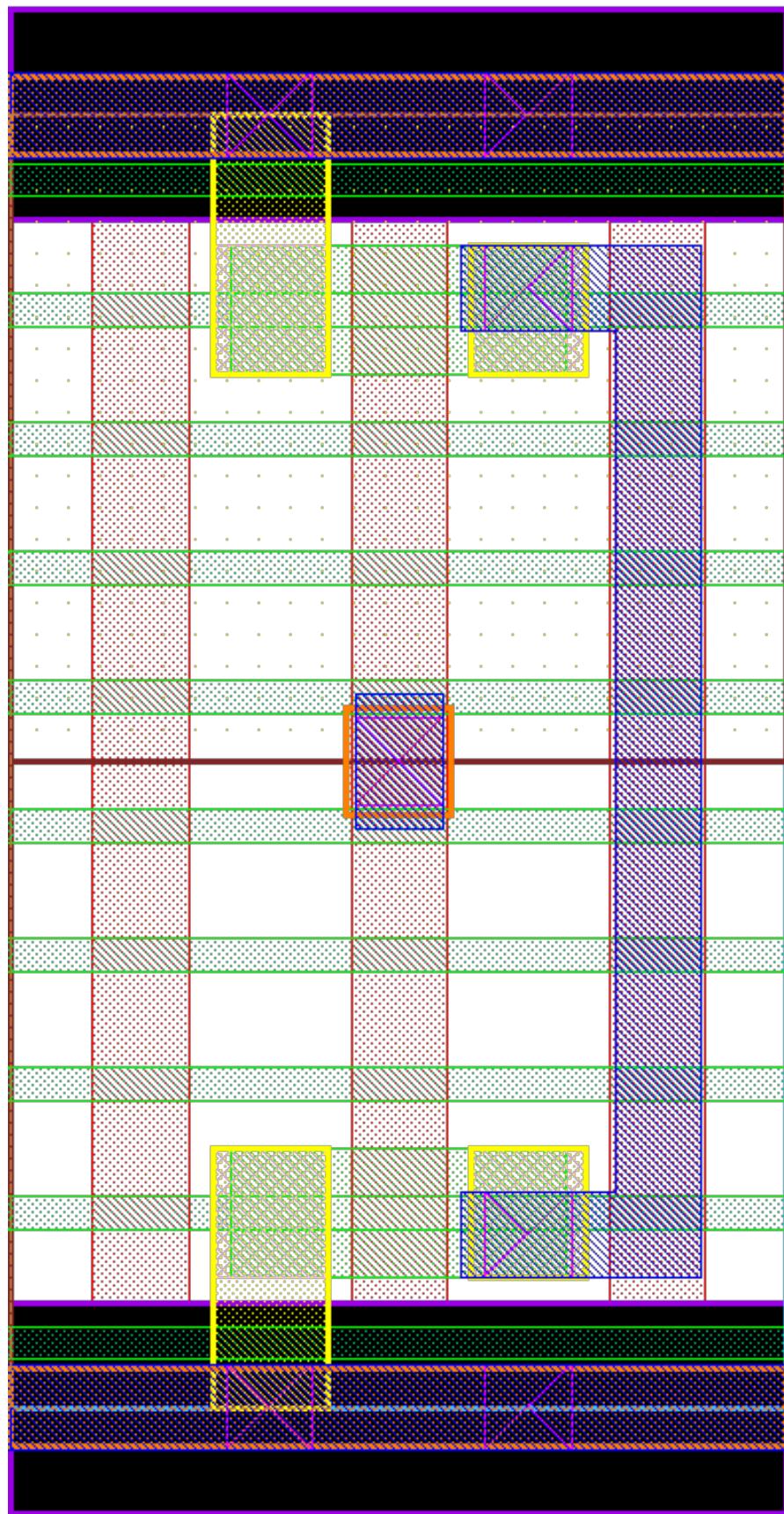
- KULKARNI, J. P.; KIM, K.; ROY, K. A 160 mv robust schmitt trigger based subthreshold sram. **IEEE Journal of Solid-State Circuits**, IEEE, v. 42, n. 10, p. 2303–2313, 2007.
- LIAO, W. et al. Investigation of reliability characteristics in nmos and pmos finfets. In: . [S.I.]: IEEE, 2008. v. 29, n. 7, p. 788–790.
- LOMBARDO, S. et al. Dielectric breakdown mechanisms in gate oxides. **Journal of applied physics**, AIP, v. 98, n. 12, p. 12, 2005.
- LOTZE, N.; MANOLI, Y. Ultra-sub-threshold operation of always-on digital circuits for iot applications by use of schmitt trigger gates. **IEEE Transactions on Circuits and Systems I: Regular Papers**, IEEE, v. 64, n. 11, p. 2920–2933, 2017.
- LUO, Z. et al. A sub-10 mv power converter with fully integrated self-start, mppt, and zcs control for thermoelectric energy harvesting. **IEEE Transactions on Circuits and Systems I: Regular Papers**, IEEE, v. 65, n. 5, p. 1744–1757, 2017.
- MANOJ, C. R. et al. Device optimization of bulk finfets and its comparison with soi finfets. In: **2007 International Workshop on Physics of Semiconductor Devices**. [S.I.: s.n.], 2007. p. 134–137.
- MANOLI, Y. Energy harvesting—from devices to systems. In: **IEEE. 2010 Proceedings of ESSCIRC**. [S.I.], 2010. p. 27–36.
- MEINHARDT, C.; ZIMPECK, A. L.; REIS, R. Impact of gate workfunction fluctuation on finfet standard cells. In: **IEEE. Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on**. [S.I.], 2014. p. 574–577.
- MELEK, L. et al. Analysis and design of the classical cmos schmitt trigger in subthreshold operation. In: . [S.I.]: IEEE, 2017. v. 64, n. 4, p. 869–878.
- MIORANDI, D. et al. Internet of things: Vision, applications and research challenges. **Ad hoc networks**, Elsevier, v. 10, n. 7, p. 1497–1516, 2012.
- MOGHADDAM, M.; MOAIYERI, M. H.; ESHGHI, M. Design and evaluation of an efficient schmitt trigger-based hardened latch in cntfet technology. In: . [S.I.]: IEEE, 2017. v. 17, n. 1, p. 267–277.
- MORAES, L. B. d. et al. Evaluation of variability using schmitt trigger on full adders layout. **Microelectronics Reliability**, Elsevier, v. 88, p. 116–121, 2018.
- MUSTAFA, M.; BHAT, T. A.; BEIGH, M. Threshold voltage sensitivity to metal gate work-function based performance evaluation of double-gate n-finFET structures for lstp technology. Scientific Research Publishing, 2013.
- NASSIF, S. Process variability at the 65nm node and beyond. In: **IEEE. Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE**. [S.I.], 2008. p. 1–8.
- NASSIF, S. R. Within-chip variability analysis. In: **IEEE. International Electron Devices Meeting 1998. Technical Digest (Cat. No. 98CH36217)**. [S.I.], 1998. p. 283–286.
- NAVI, K. et al. A novel low-power full-adder cell for low voltage. In: . [S.I.]: Elsevier, 2009. v. 42, n. 4, p. 457–467.

- NAWAZ, S. M. et al. Comparison of random dopant and gate-metal workfunction variability between junctionless and conventional finfets. **IEEE electron device letters**, IEEE, v. 35, n. 6, p. 663–665, 2014.
- PAL, I.; ISLAM, A. Circuit-level technique to design variation-and noise-aware reliable dynamic logic gates. **IEEE Trans. on Device and Materials Reliability**, IEEE, v. 18, n. 2, p. 224–239, 2018.
- PAWLOWSKI, R. et al. A 530mv 10-lane simd processor with variation resiliency in 45nm soi. In: **IEEE. 2012 IEEE International Solid-State Circuits Conference**. [S.l.], 2012. p. 492–494.
- PEDRONI, V. Low-voltage high-speed schmitt trigger and compact window comparator. **Electronics Letters**, IET, v. 41, n. 22, p. 1213–1214, 2005.
- PFISTER, A. Novel cmos schmitt trigger with controllable hysteresis. **Electronics Letters**, IET, v. 28, n. 7, p. 639–641, 1992.
- RABAEY, J.; CHANDRAKASAN, A.; NIKOLIC, B. **Digital integrated circuits**. [S.l.]: Prentice hall Englewood Cliffs, 2002.
- RAHIMI, A.; BENINI, L.; GUPTA, R. K. Variability mitigation in nanometer cmos integrated systems: A survey of techniques from circuits to software. In: . [S.l.]: IEEE, 2016. v. 104, n. 7, p. 1410–1448.
- REN, P. et al. New insights into the hci degradation of pass-gate transistor in advanced finfet technology. In: **2018 IEEE International Reliability Physics Symposium (IRPS)**. [S.l.: s.n.], 2018. p. P-CR.3–1–P-CR.3–4.
- RITHE, R. et al. The effect of random dopant fluctuations on logic timing at low voltage. **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, IEEE, v. 20, n. 5, p. 911–924, 2011.
- SCHROM, G.; DE, V.; SELBERHERR, S. Vlsi performance metric based on minimum tcad simulations. In: **IEEE. SISPAD'97. 1997 International Conference on Simulation of Semiconductor Processes and Devices. Technical Digest**. [S.l.], 1997. p. 25–28.
- SHAMS, A. M.; BAYOUMI, M. A. A novel high-performance cmos 1-bit full-adder cell. In: . [S.l.]: IEEE, 2000. v. 47, n. 5, p. 478–481.
- STEYAERT, M.; SANSEN, W. Novel cmos schmitt trigger. **Electronics Letters**, IET, v. 22, n. 4, p. 203–204, 1986.
- STINE, B. E.; BONING, D. S.; CHUNG, J. E. Analysis and decomposition of spatial variation in integrated circuit processes and devices. **IEEE Transactions on Semiconductor Manufacturing**, IEEE, v. 10, n. 1, p. 24–41, 1997.
- TACHE, M. et al. Reliability and performance of optimised schmitt trigger gates. **The Journal of Engineering**, IET, v. 2018, n. 8, p. 735–744, 2018.
- TAKEDA, E.; SUZUKI, N. An empirical model for device degradation due to hot-carrier injection. **IEEE electron device letters**, IEEE, v. 4, n. 4, p. 111–113, 1983.

- TAUR, Y.; NING, T. H. **Fundamentals of modern VLSI devices.** [S.l.]: Cambridge university press, 2013.
- TOLEDO, S. P.; ZIMPECK, A. L.; MEINHARDT, C. Impact of schmitt trigger inverters on process variability robustness of 1-bit full adders. In: **IEEE Conference on Electronics, Circuits and Systems (ICECS).** [S.l.], 2016.
- TOLEDO, S. P. et al. Pros and cons of schmitt trigger inverters to mitigate pvt variability on full adders. In: **IEEE. 2018 IEEE International Symposium on Circuits and Systems (ISCAS).** [S.l.], 2018. p. 1–5.
- TSCHANZ, J. W. et al. Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage. **IEEE Journal of Solid-State Circuits**, IEEE, v. 37, n. 11, p. 1396–1402, 2002.
- WANG, W. et al. Statistical prediction of circuit aging under process variations. In: **IEEE. 2008 IEEE Custom Integrated Circuits Conference.** [S.l.], 2008. p. 13–16.
- WANG, X. et al. Statistical threshold-voltage variability in scaled decanometer bulk hkmg mosfets: A full-scale 3-d simulation scaling study. In: . [S.l.]: IEEE, 2011. v. 58, n. 8, p. 2293–2301.
- WESTE, N. H. E.; ESHRAGHIAN, K. **Principles of CMOS VLSI design.** [S.l.]: Addison-Wesley New York, 1985.
- WONG, H.-S. et al. Nanoscale cmos. **Proceedings of the IEEE**, IEEE, v. 87, n. 4, p. 537–570, 1999.
- XIONG, S.; BOKOR, J. Sensitivity of double-gate and finfetdevices to process variations. In: . [S.l.: s.n.], 2003. v. 50, n. 11, p. 2255–2261.
- YOUNG, D.; CHRISTOU, A. Failure mechanism models for electromigration. **IEEE Transactions on Reliability**, IEEE, v. 43, n. 2, p. 186–192, 1994.
- ZHANG, C.; SRIVASTAVA, A.; AJMERA, P. K. Low voltage cmos schmitt trigger circuits. In: . [S.l.]: IET, 2003. v. 39, n. 24, p. 1696–1698.
- ZHANG, R. et al. Modeling of the reliability degradation of a finfet-based sram due to bias temperature instability, hot carrier injection, and gate oxide breakdown. In: **2017 IEEE International Integrated Reliability Workshop (IIRW).** [S.l.: s.n.], 2017. p. 1–4.
- ZIMPECK, A. L. et al. Finfet cells with different transistor sizing techniques against pvt variations. In: **IEEE. Circuits and Systems (ISCAS), 2016 IEEE International Symposium on.** [S.l.], 2016. p. 45–48.

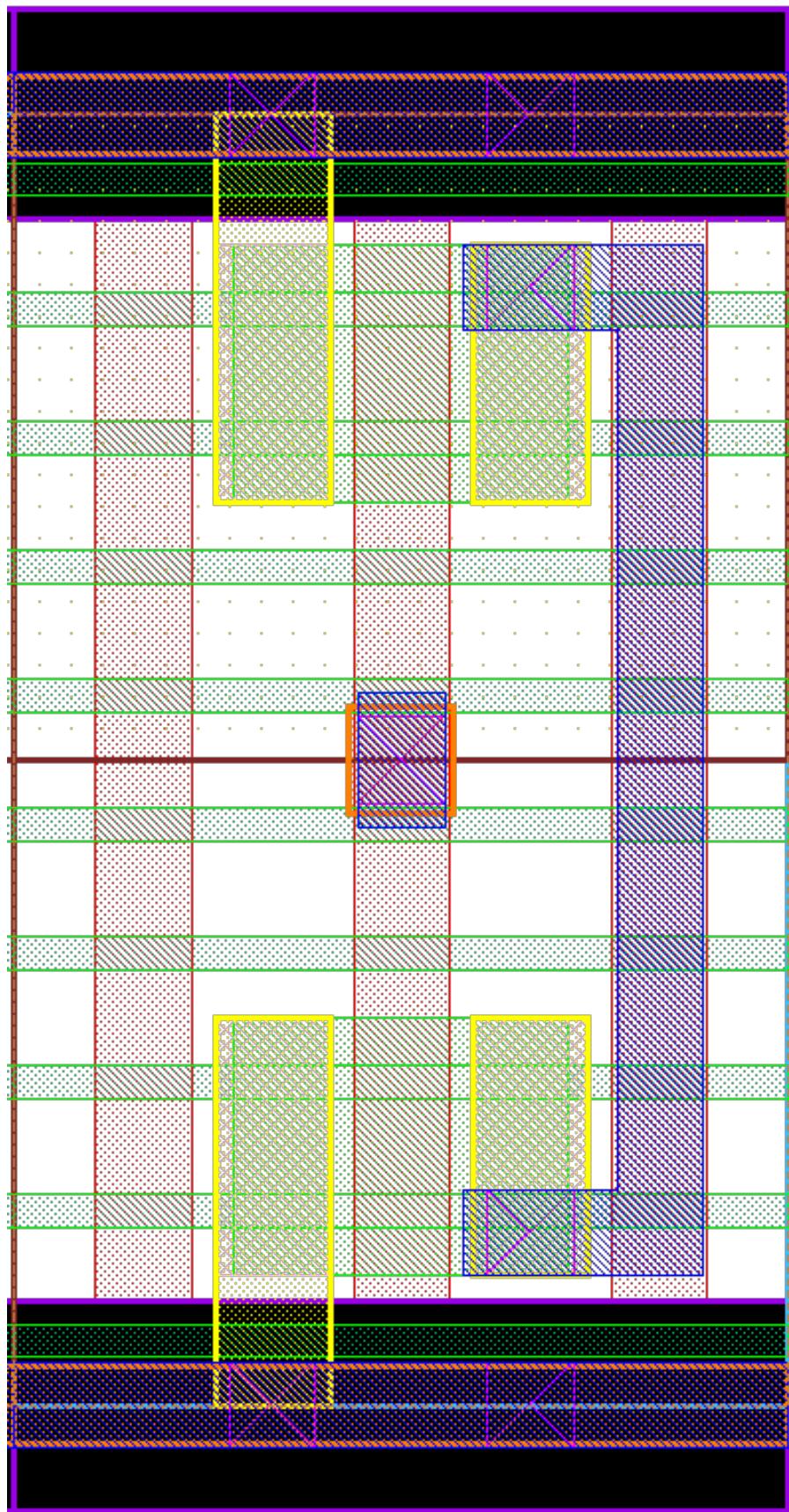
ANNEX A — INVERTER DESIGNS LAYOUTS

Figure A.1: 1 fin inverter layout.



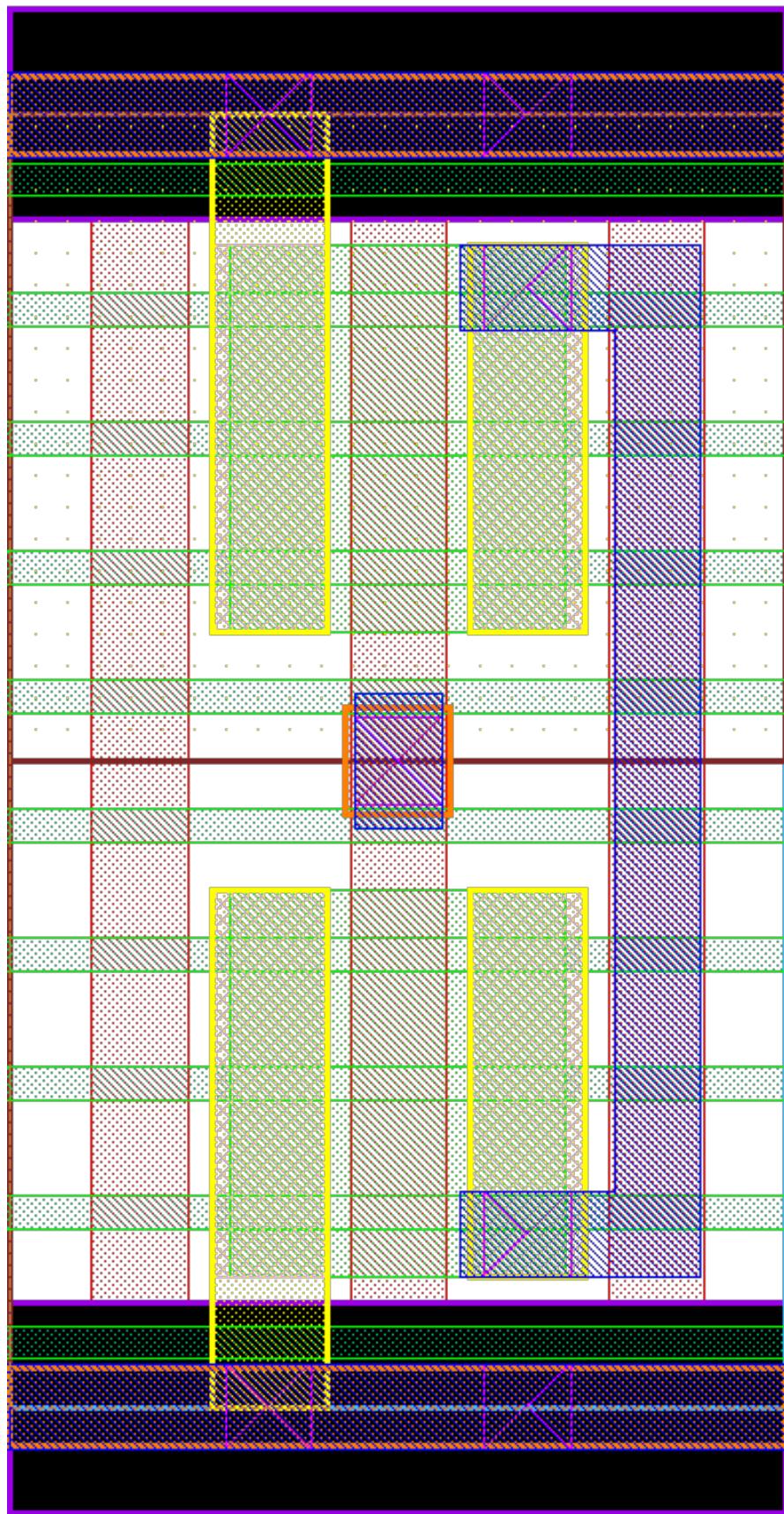
Source: From the author.

Figure A.2: 2 fins inverter layout.



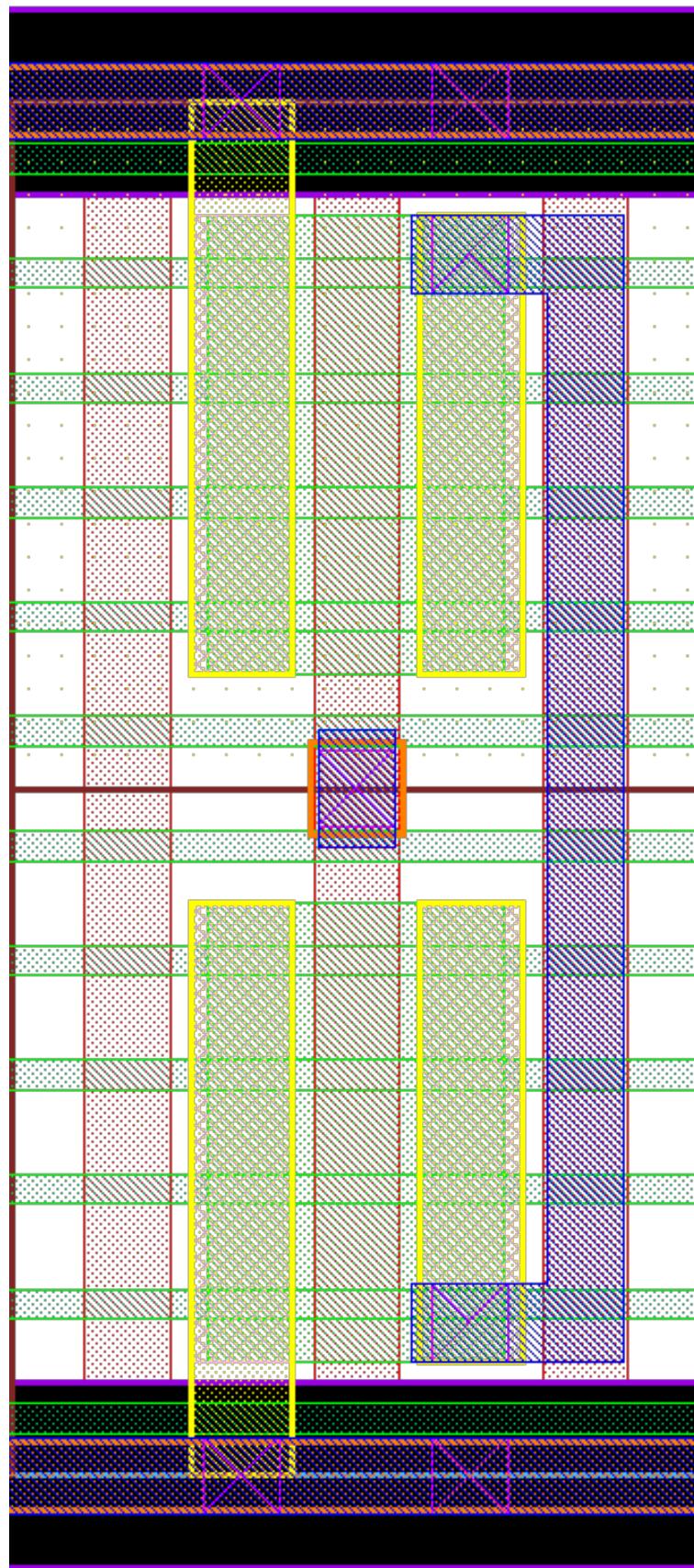
Source: From the author.

Figure A.3: 3 fins inverter layout.



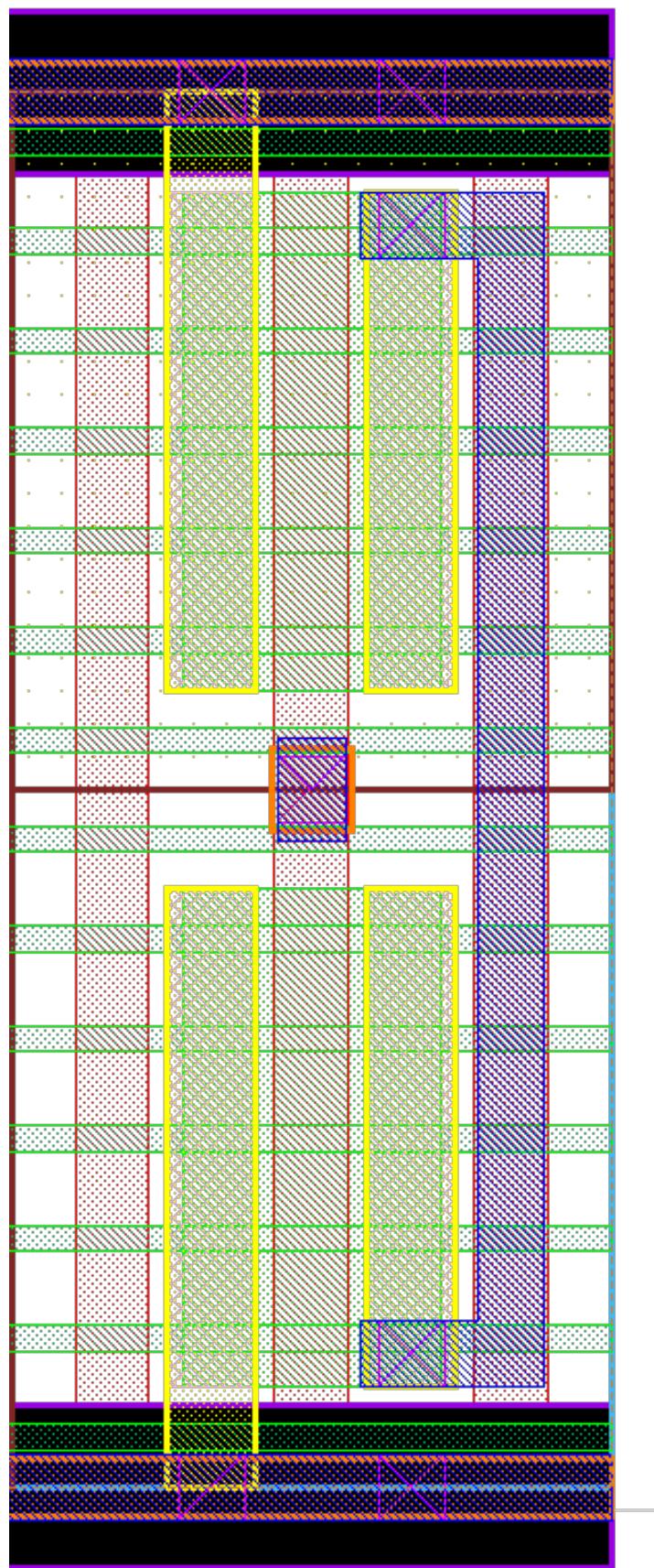
Source: From the author.

Figure A.4: 4 fins inverter layout.



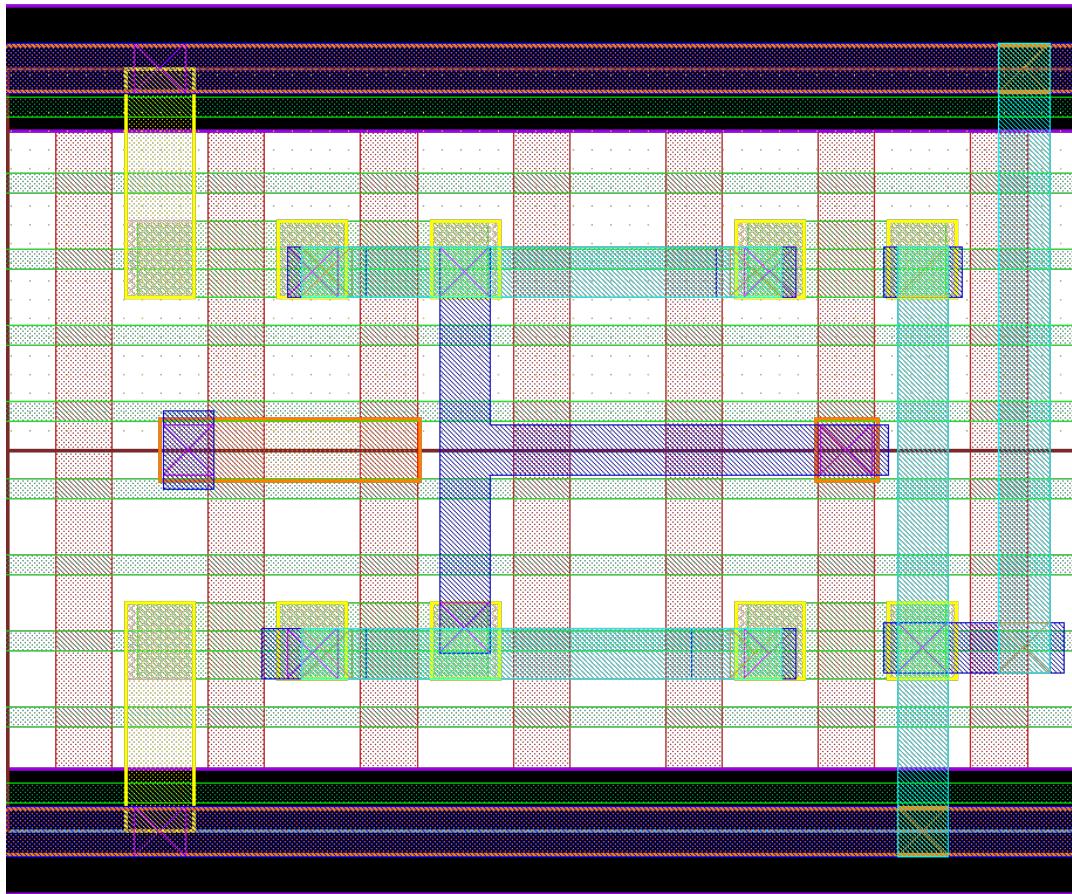
Source: From the author.

Figure A.5: 5 fins inverter layout.



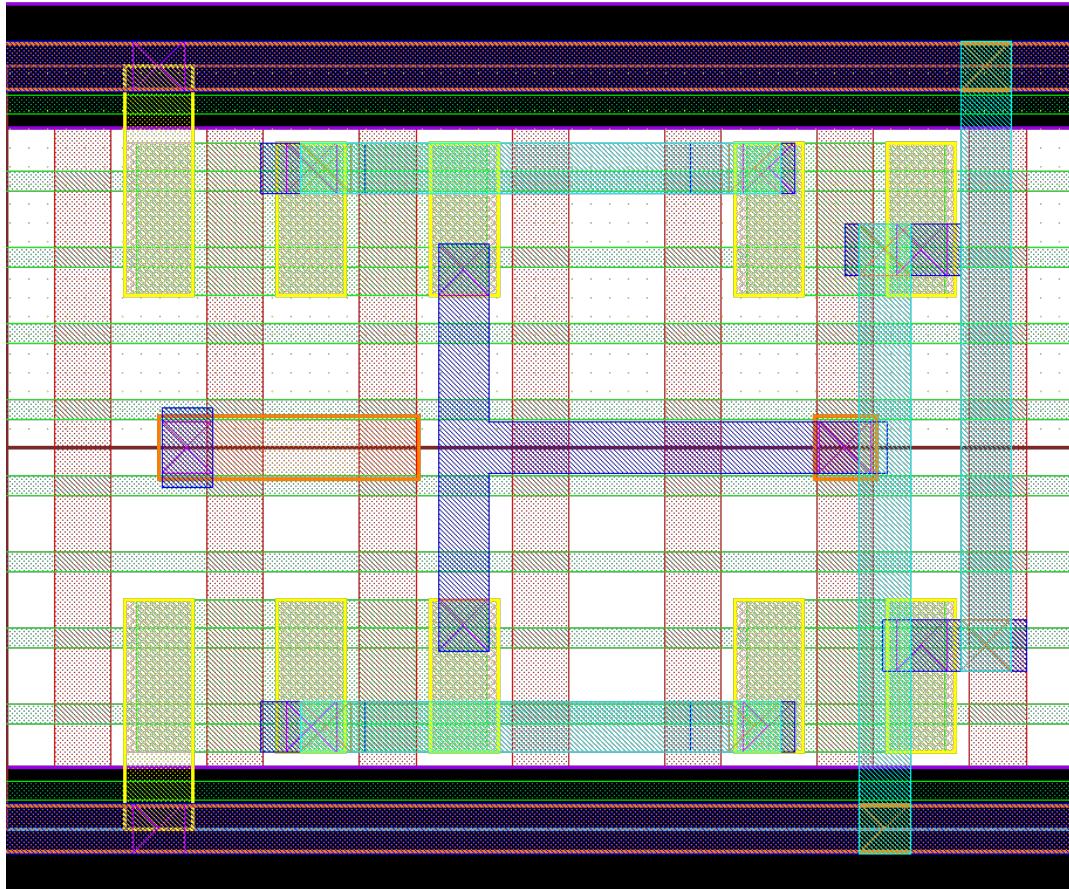
Source: From the author.

Figure A.6: 1 fin ST layout.



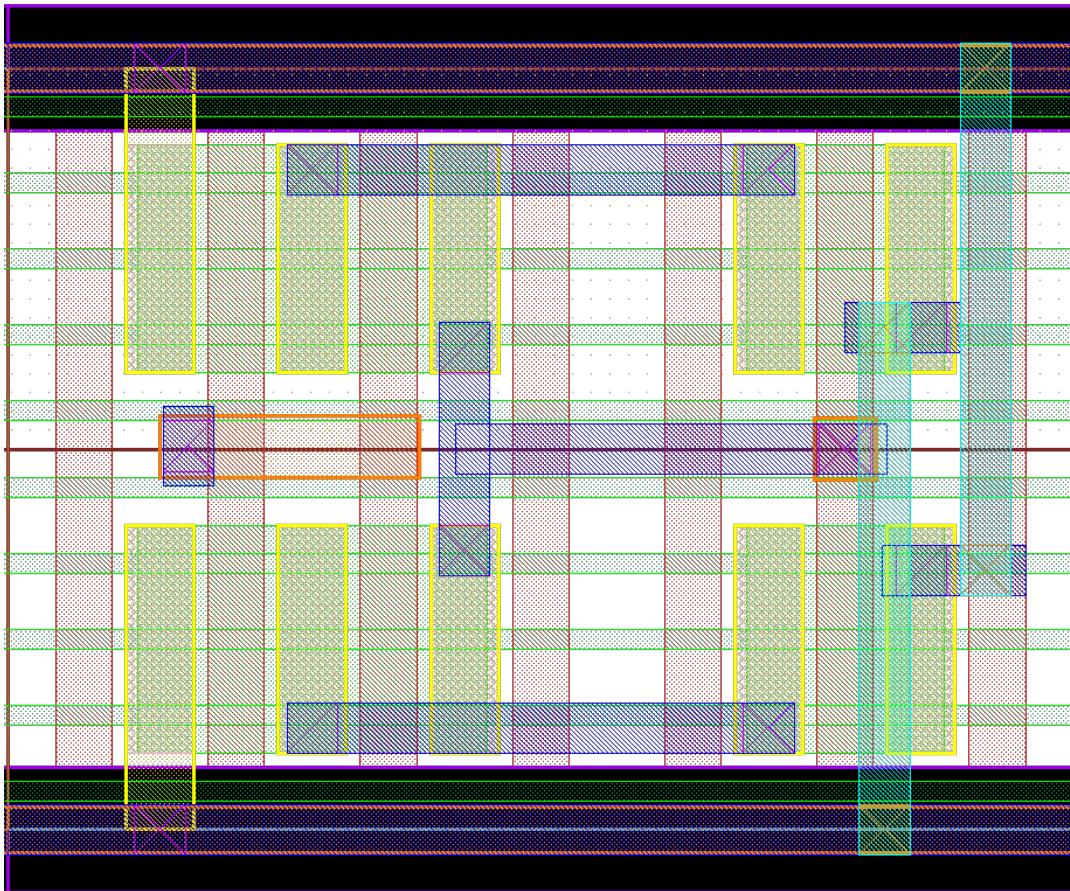
Source: From the author.

Figure A.7: 2 fins ST layout.



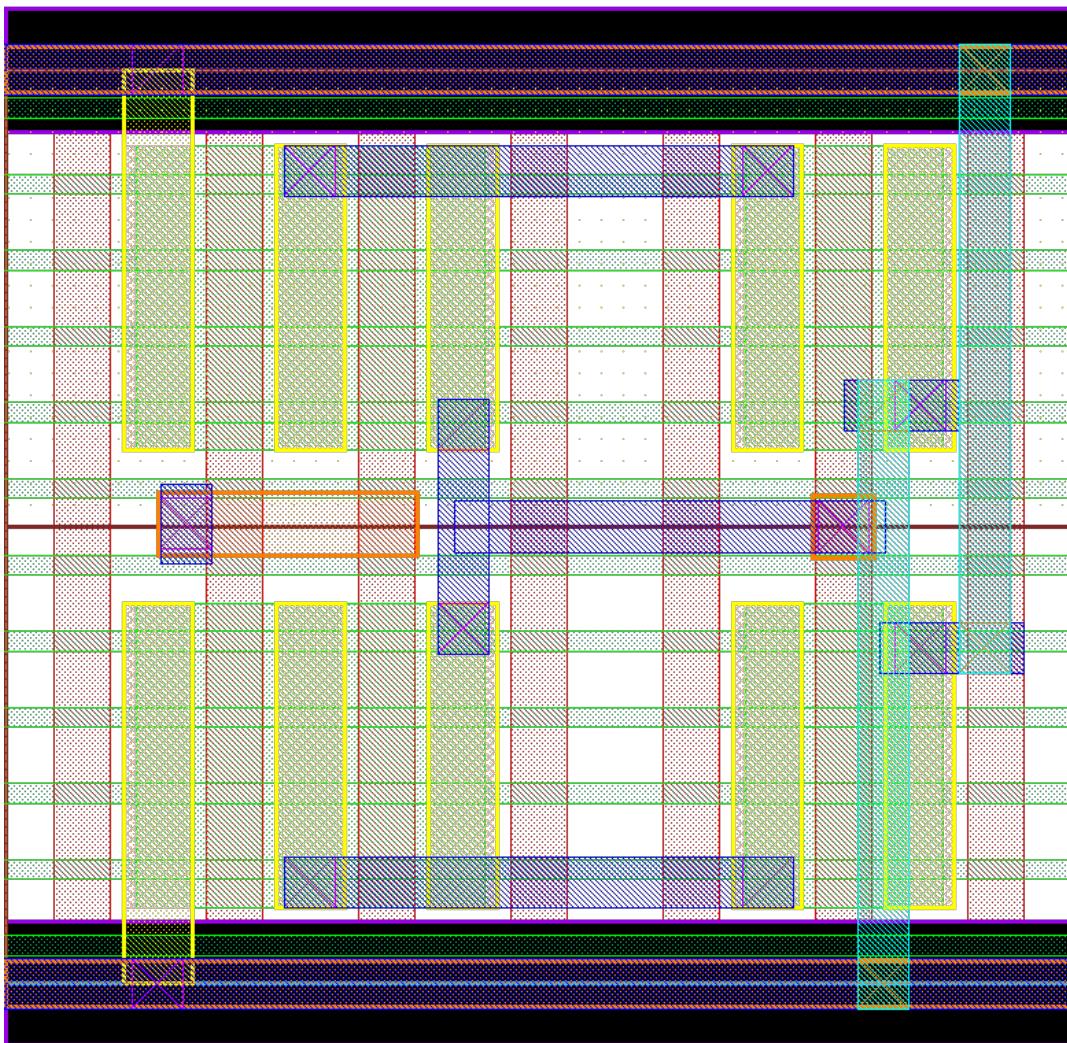
Source: From the author.

Figure A.8: 3 fins ST layout.



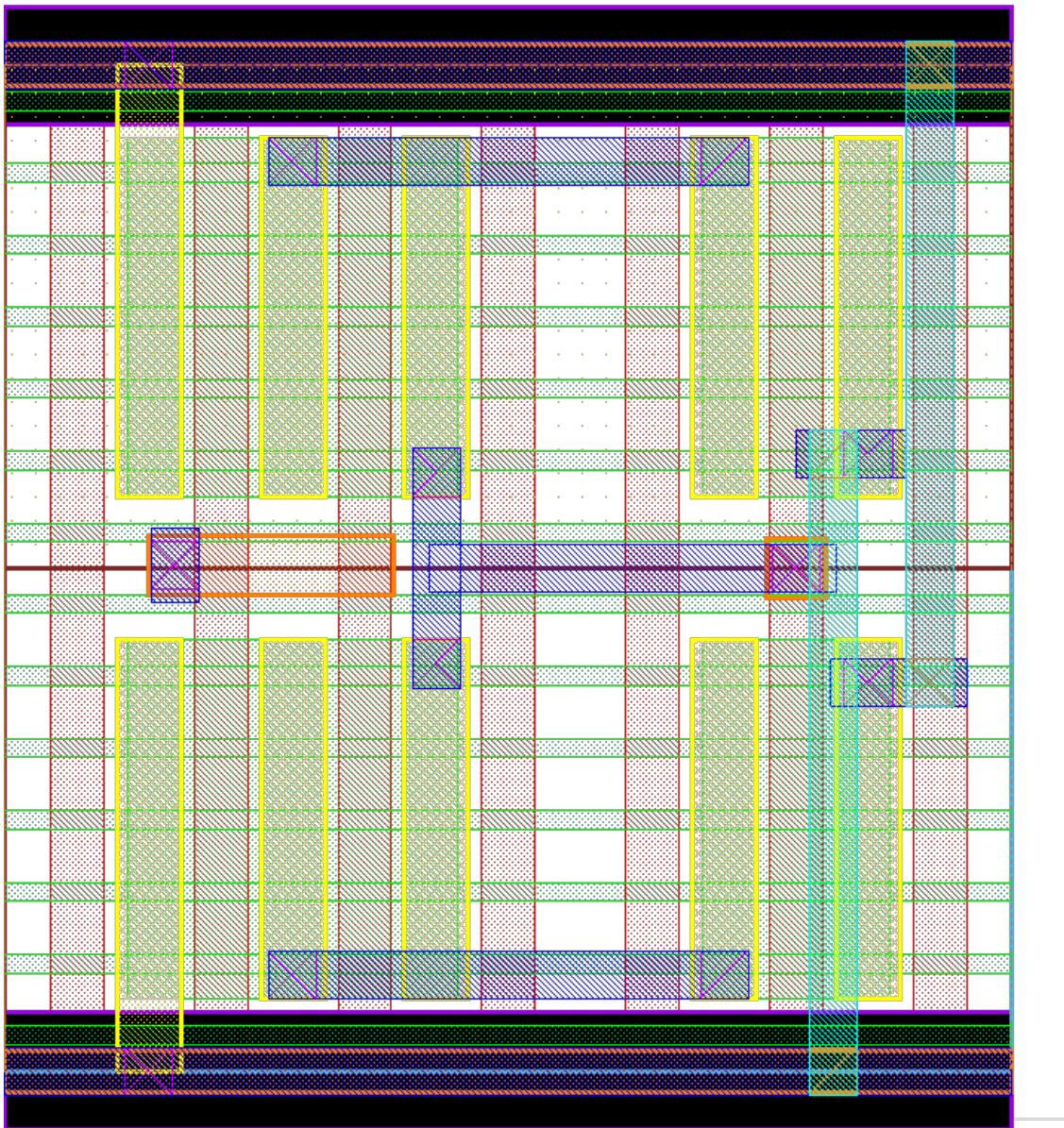
Source: From the author.

Figure A.9: 4 fins ST layout.



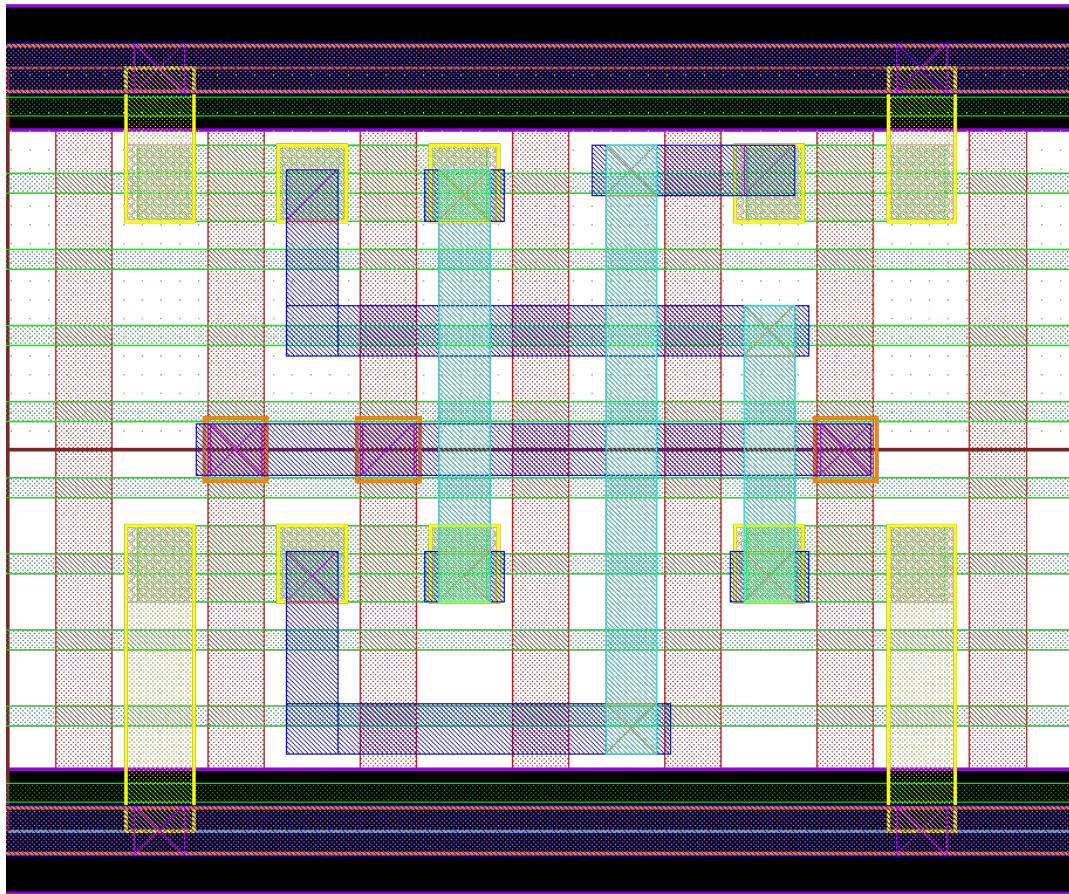
Source: From the author.

Figure A.10: 5 fins ST layout.



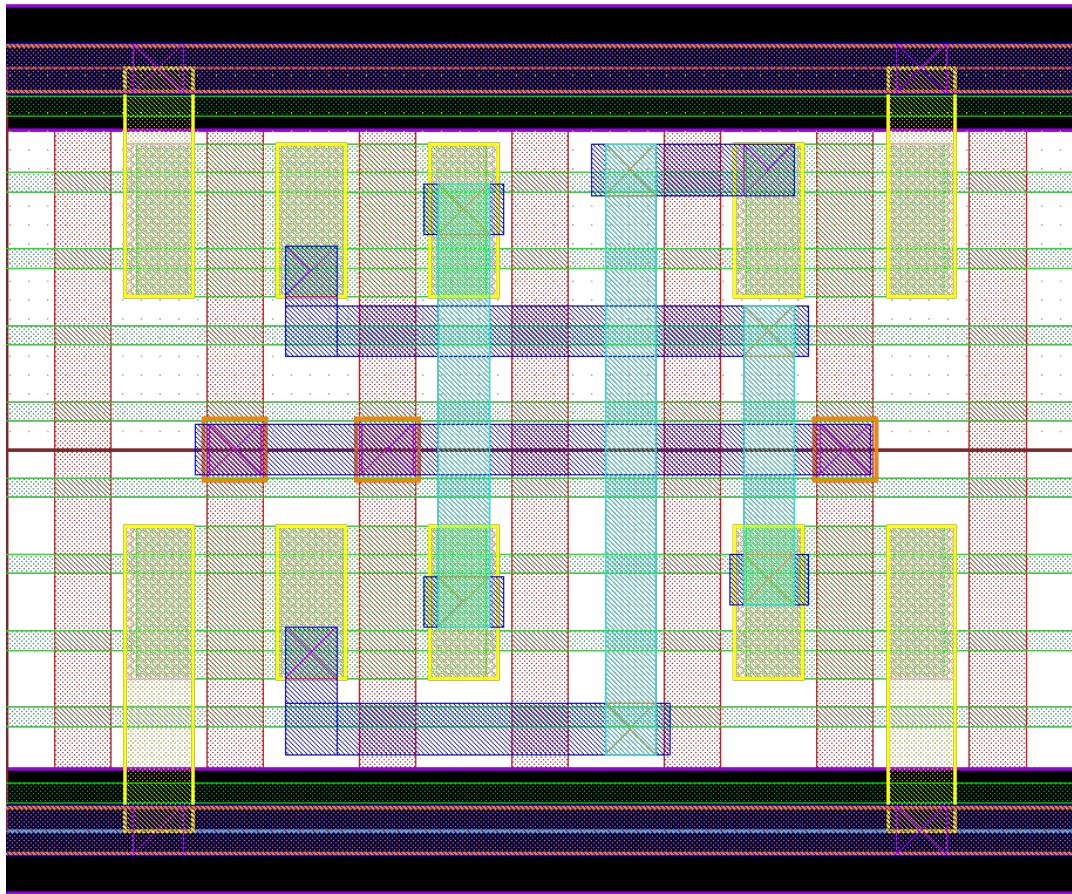
Source: From the author.

Figure A.11: 1 fin SIG layout.



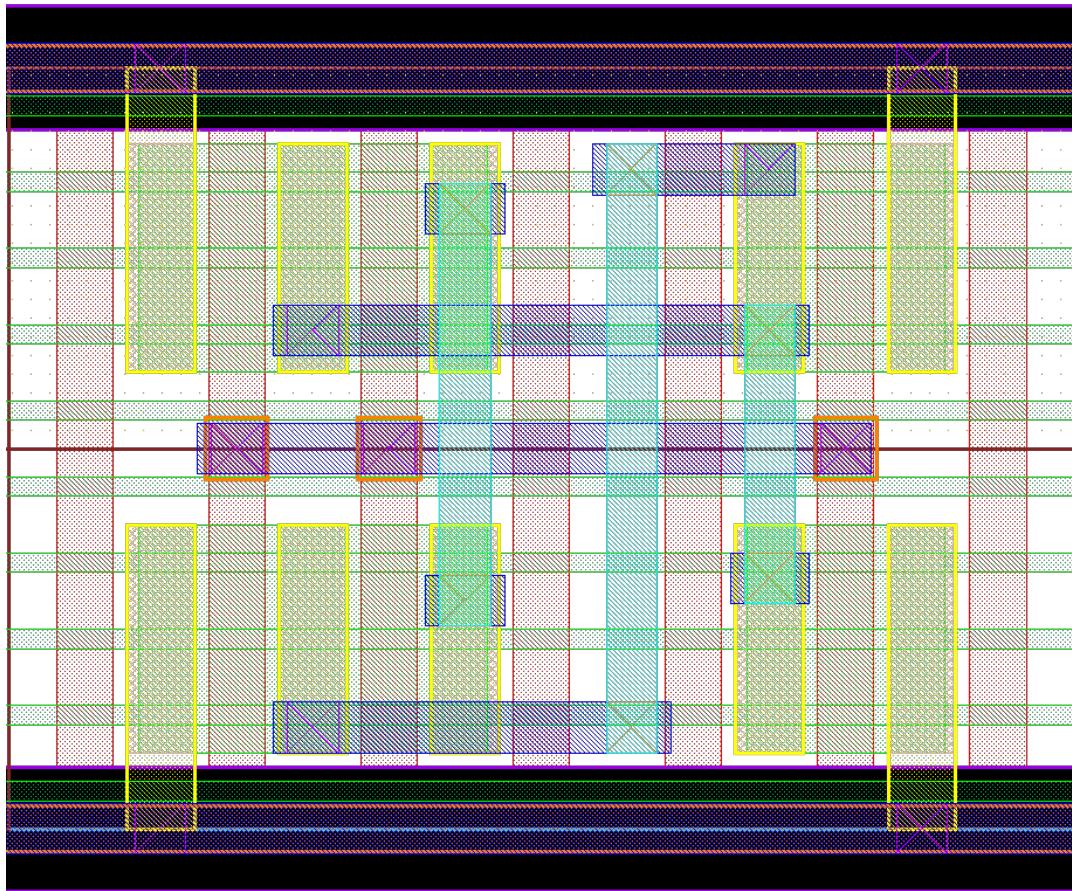
Source: From the author.

Figure A.12: 2 fins SIG layout.



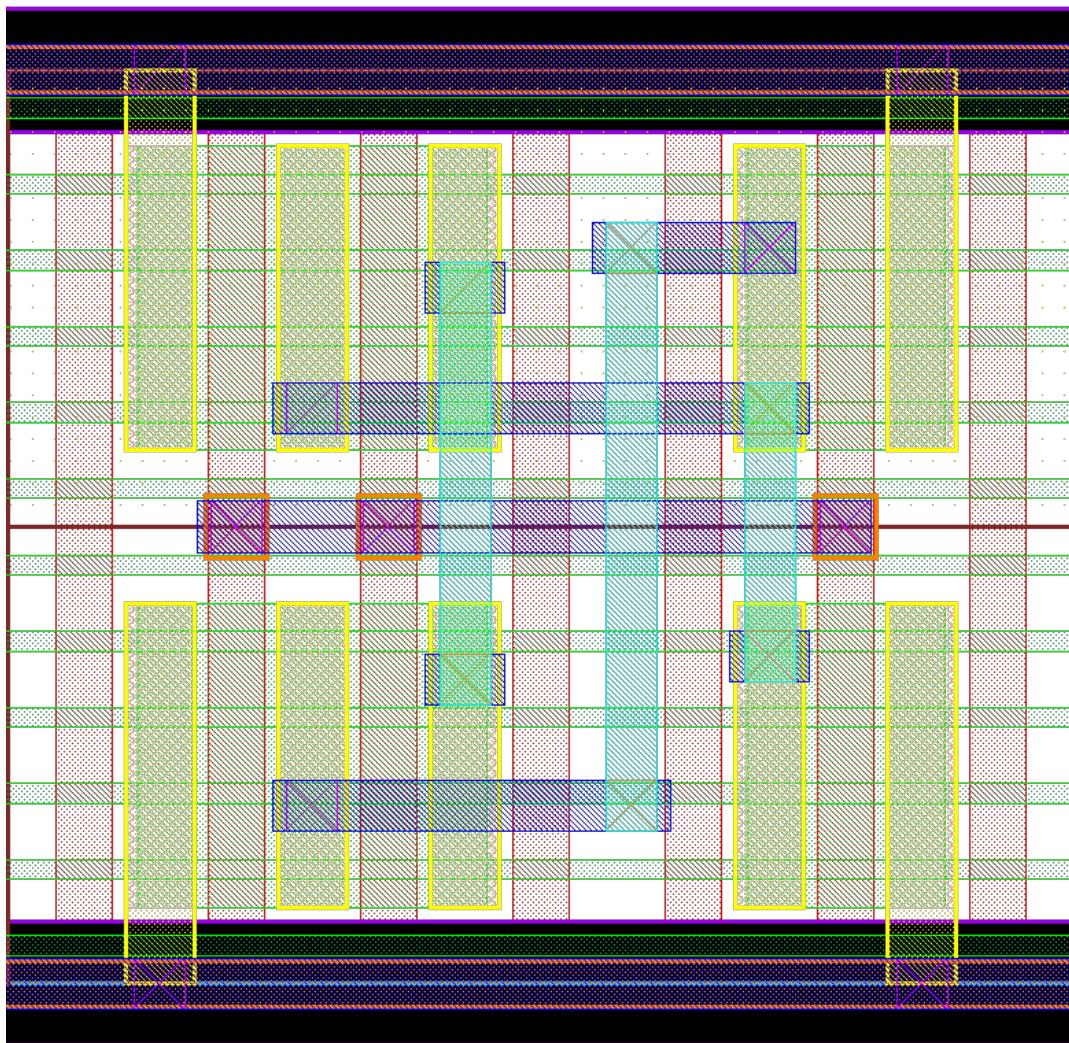
Source: From the author.

Figure A.13: 3 fins SIG layout.



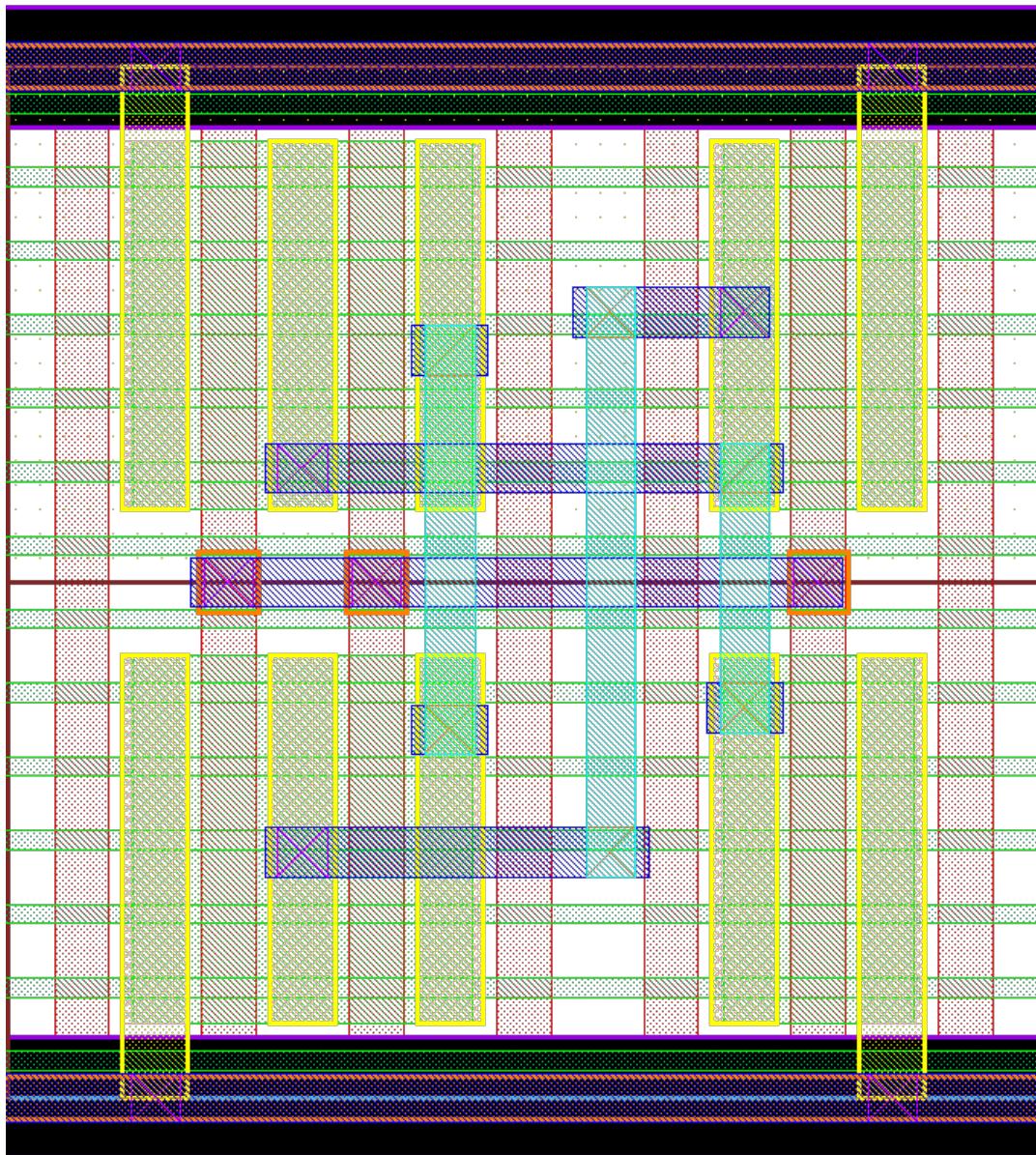
Source: From the author.

Figure A.14: 4 fins SIG layout.



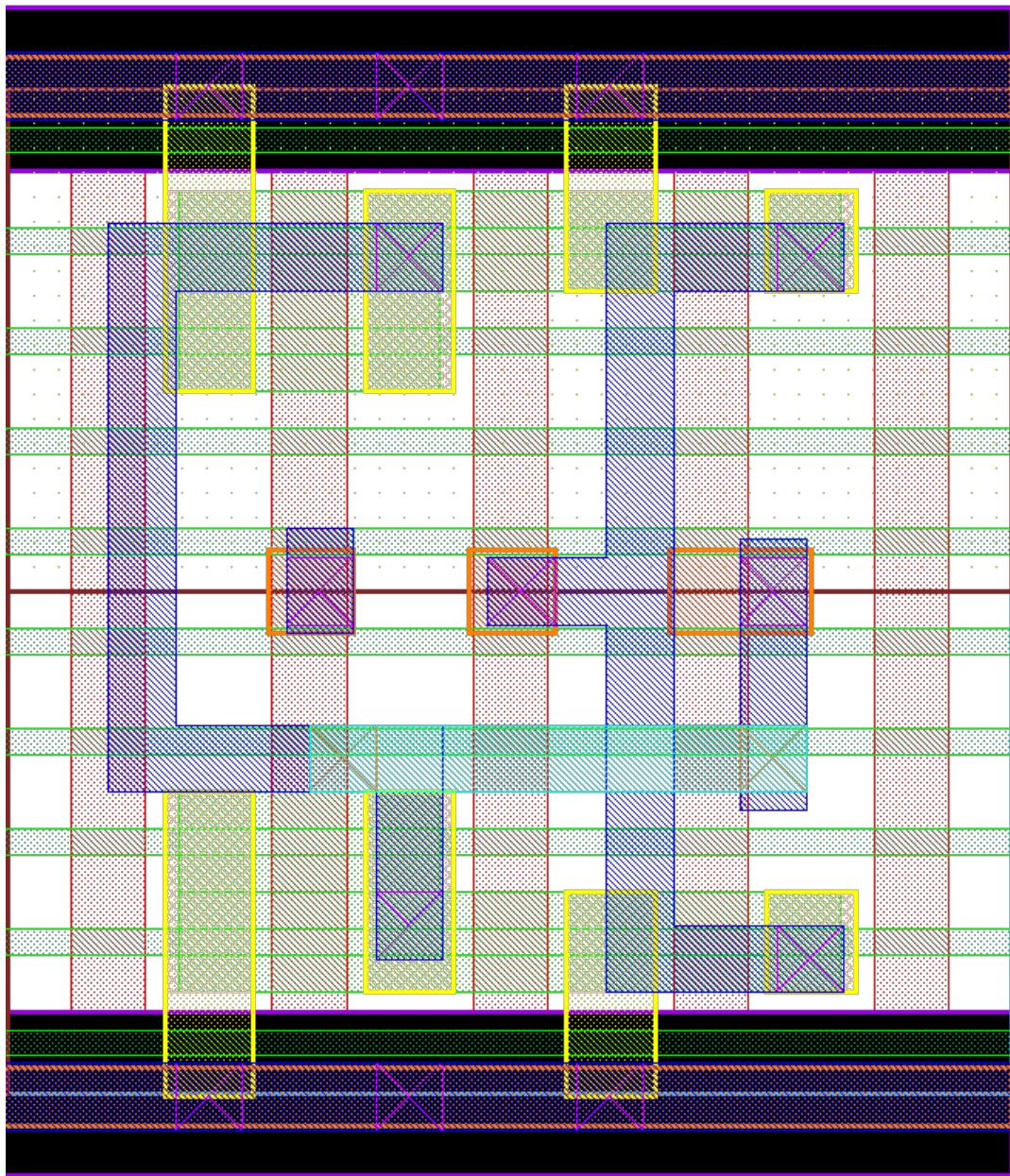
Source: From the author.

Figure A.15: 5 fins SIG layout.



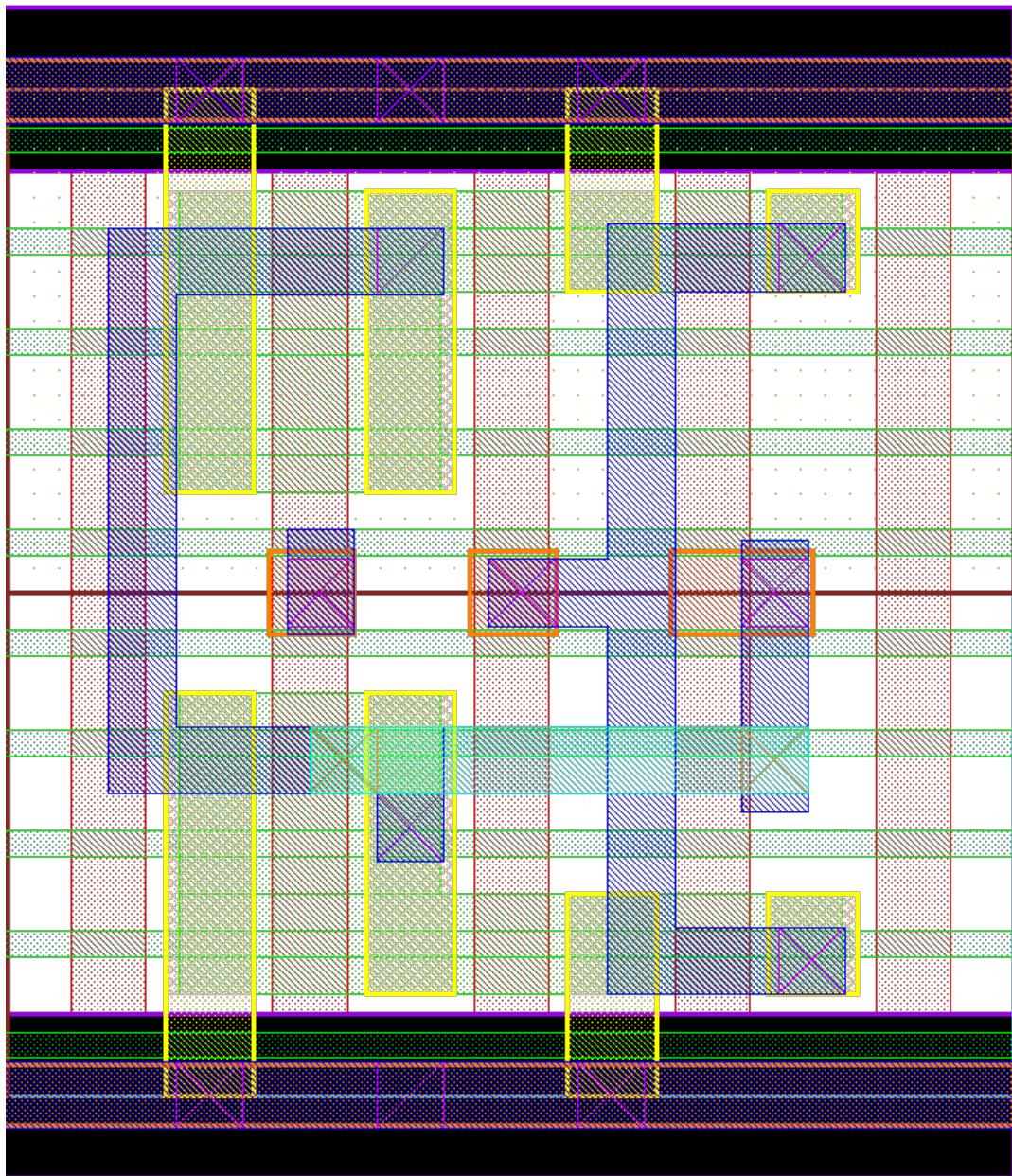
Source: From the author.

Figure A.16: 2 fin max., proportion 2:1 TIST layout.



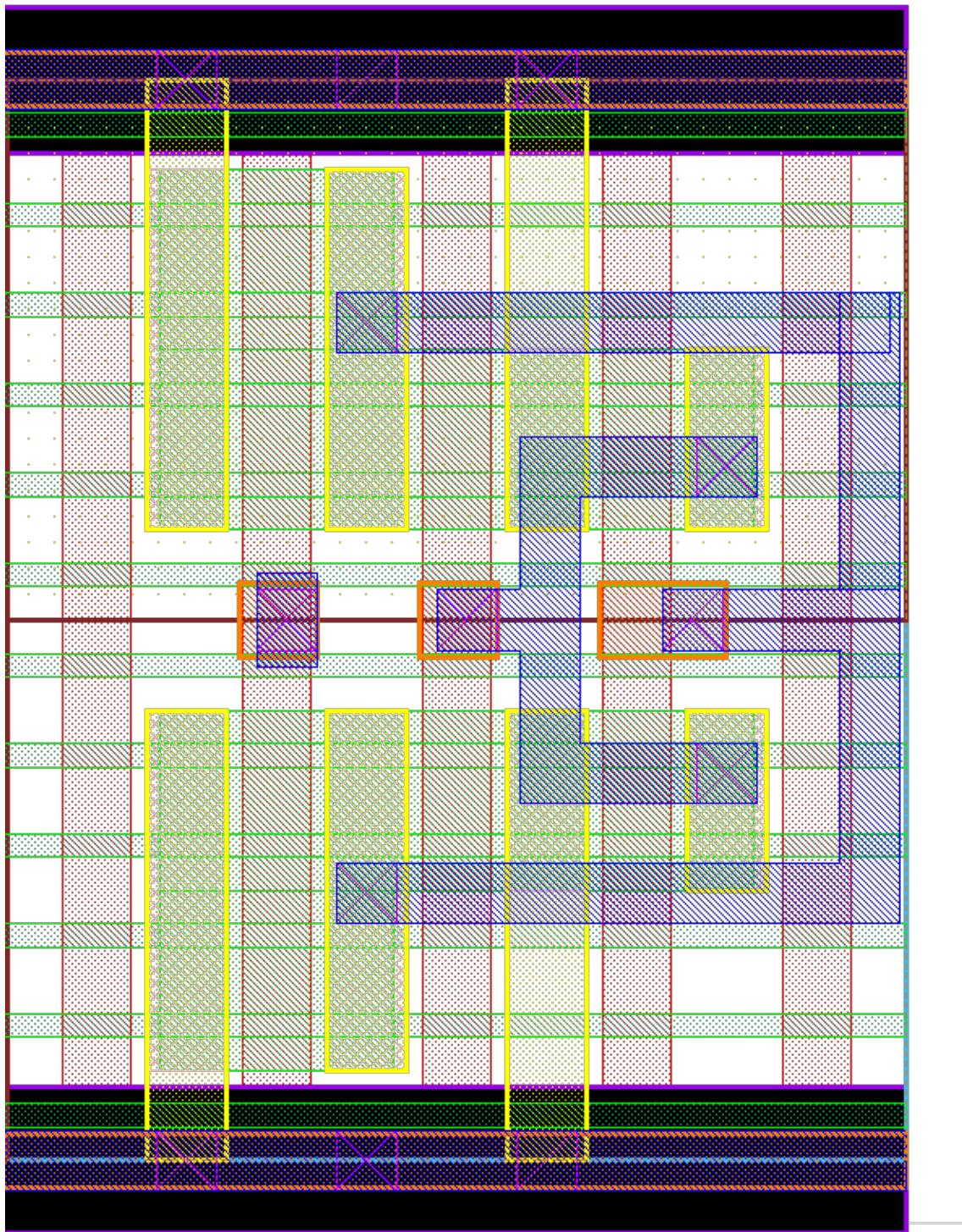
Source: From the author.

Figure A.17: 3 fin max., proportion 3:1 TIST layout.



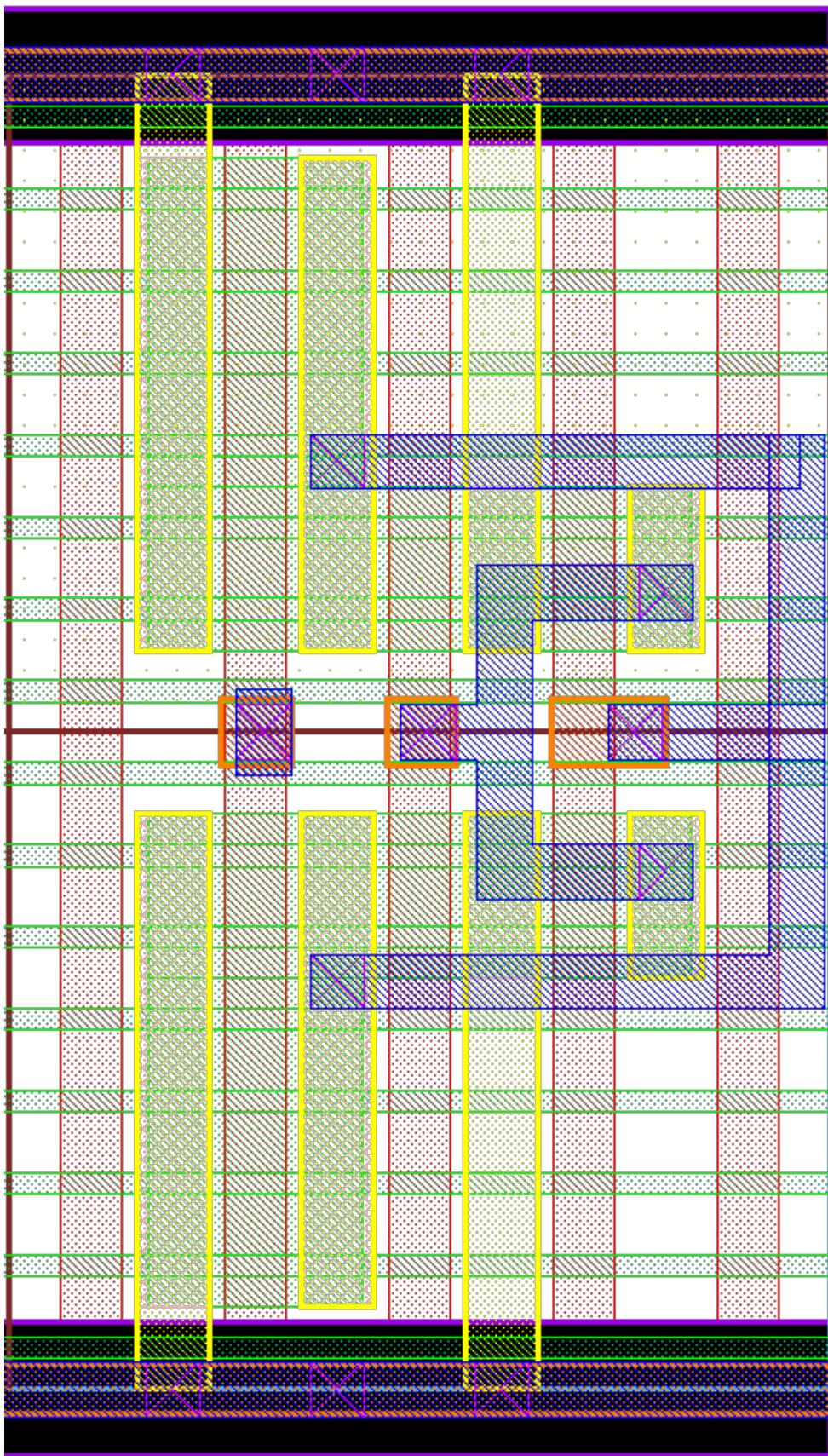
Source: From the author.

Figure A.18: 4 fin max., proportion 2:1 TIST layout.



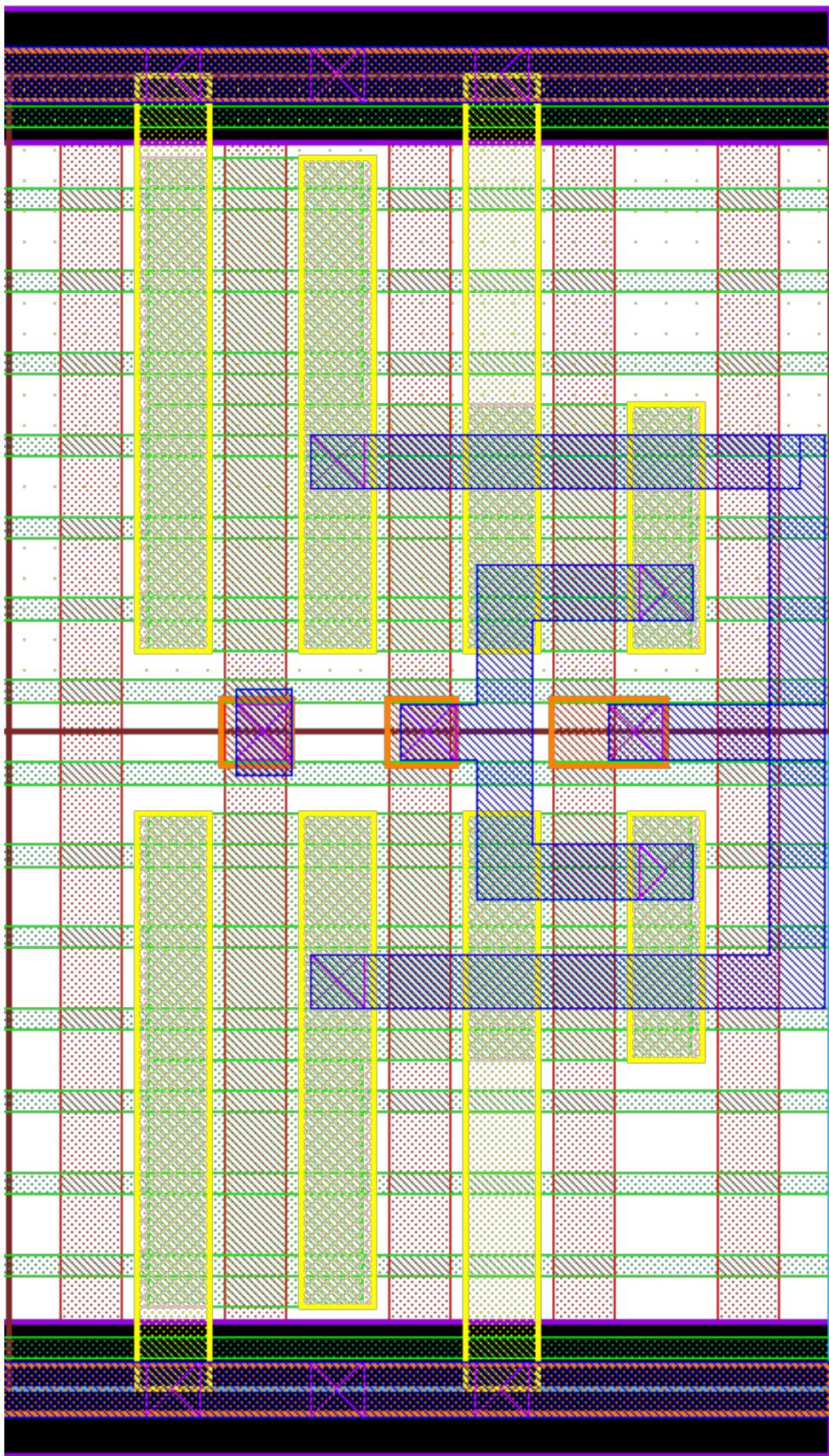
Source: From the author.

Figure A.19: 6 fin max., proportion 3:1 TIST layout.



Source: From the author.

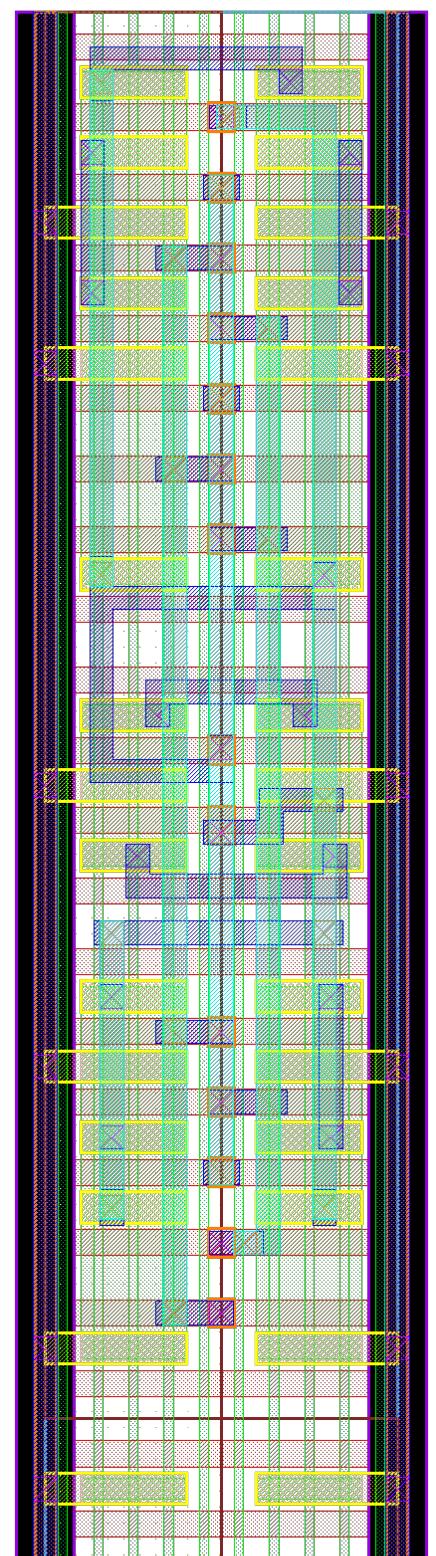
Figure A.20: 6 fin max., proportion 2:1 TIST layout.



Source: From the author.

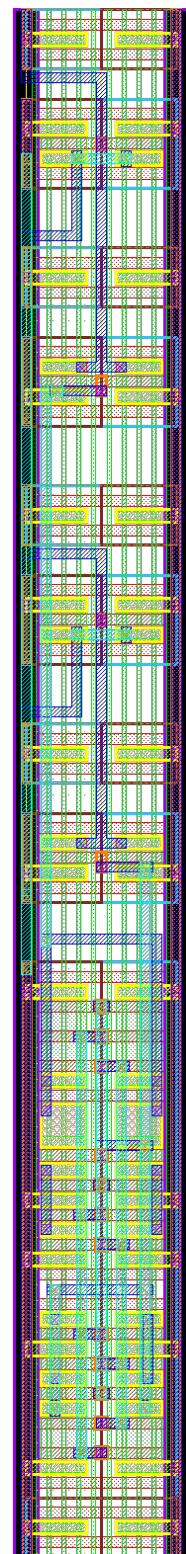
ANNEX B — FULL ADDERS

Figure B.1: Traditional Mirror Full Adder layout.



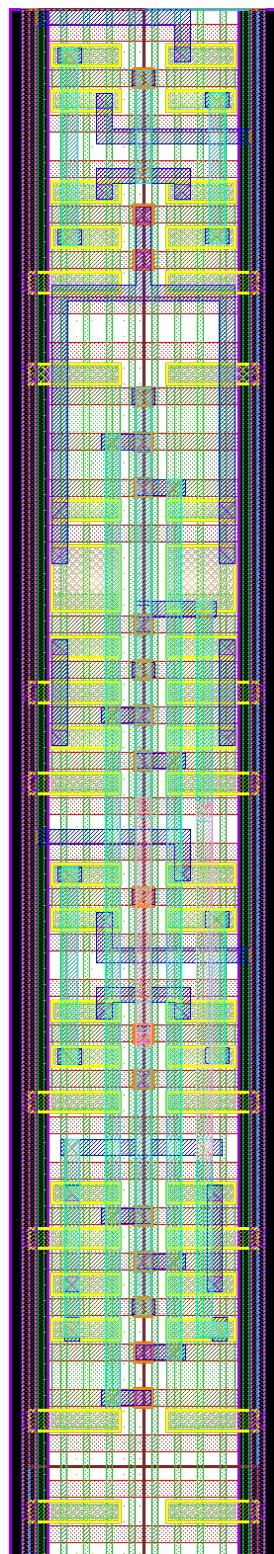
Source: From the author.

Figure B.2: Mirror Full Adder layout with internal inverters replaced by ST1.



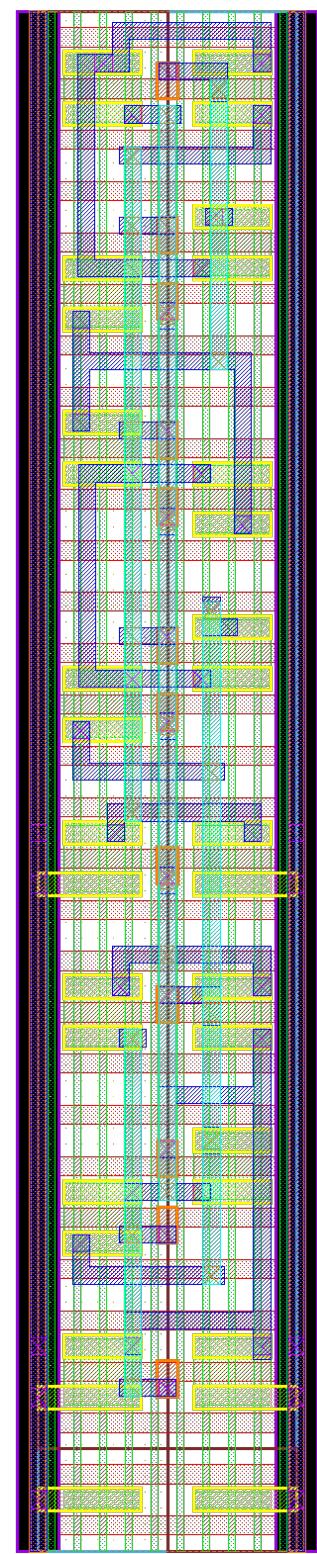
Source: From the author.

Figure B.3: Mirror Full Adder layout with internal inverters replaced by ST2.



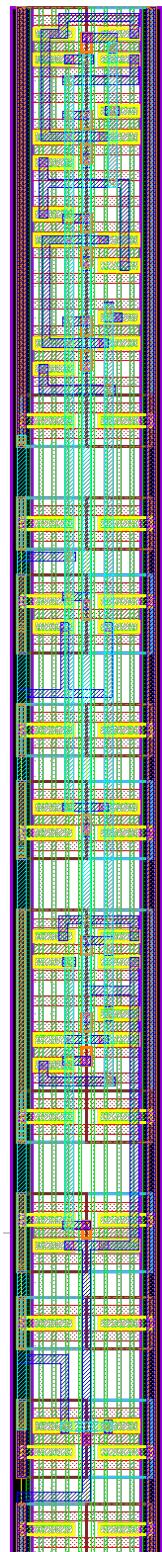
Source: From the author.

Figure B.4: Traditional Transmission Full Adder layout .



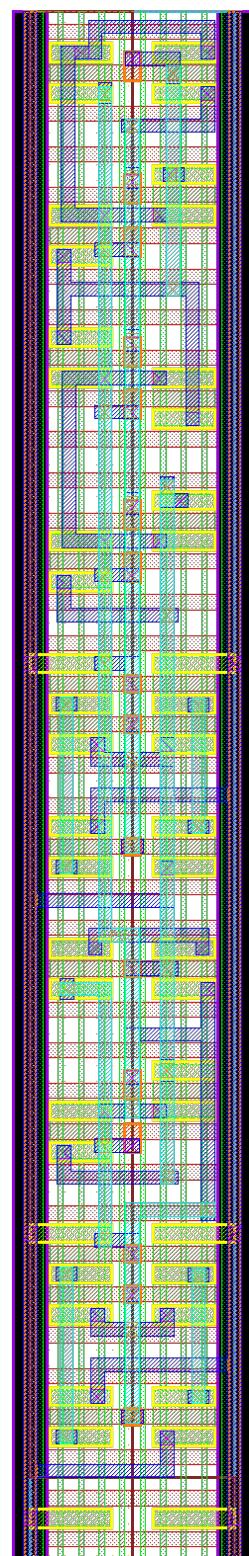
Source: From the author.

Figure B.5: Transmission Full Adder layout with internal inverters replaced by ST1.



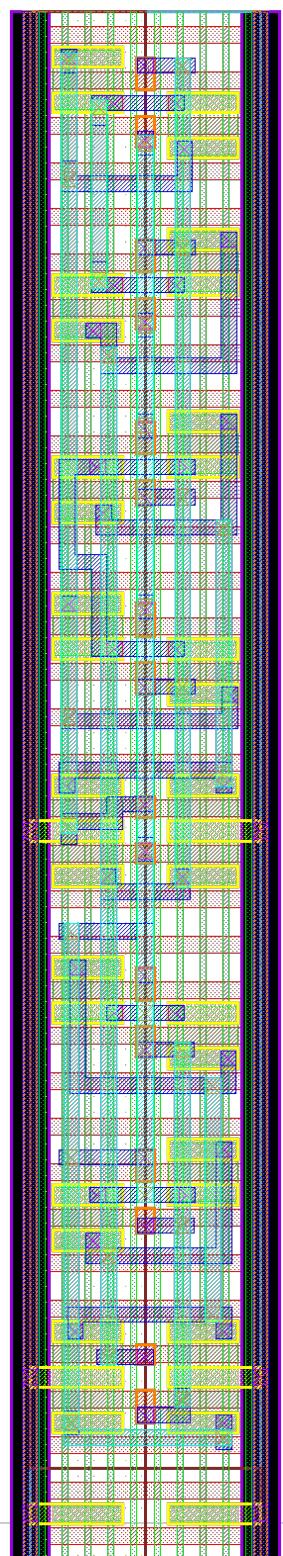
Source: From the author.

Figure B.6: Transmission Full Adder layout with internal inverters replaced by ST2.



Source: From the author.

Figure B.7: Traditional Transmission Gate Adder layout.



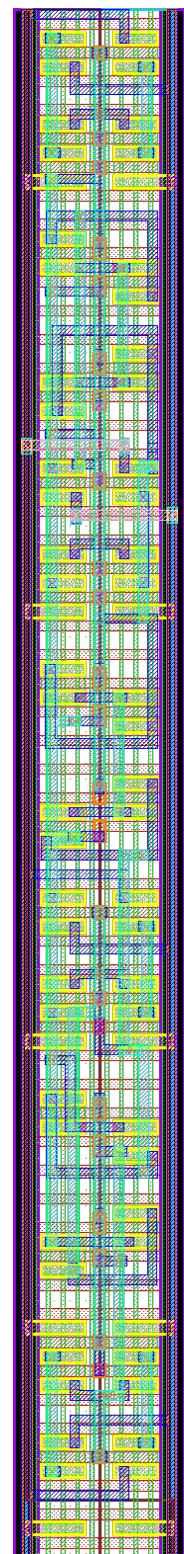
Source: From the author.

Figure B.8: Transmission Gate Adder layout with internal inverters replaced by ST1.



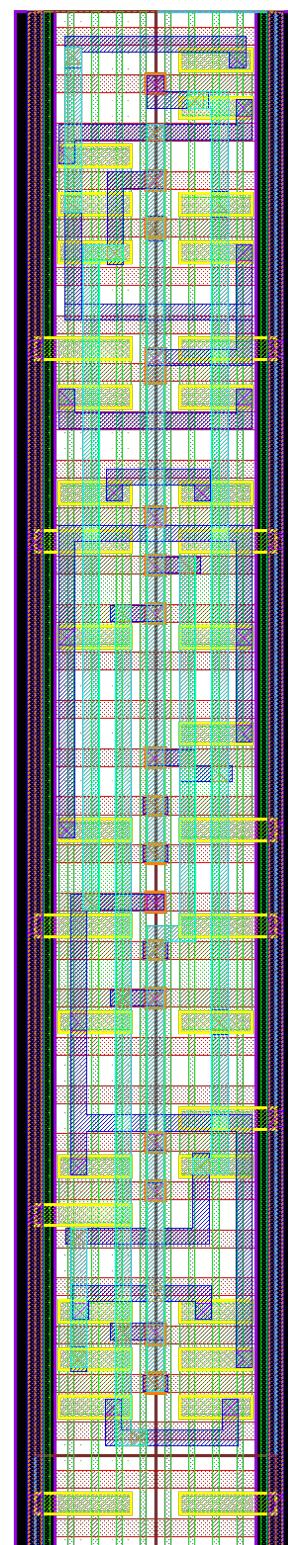
Source: From the author.

Figure B.9: Transmission Gate Adder layout with internal inverters replaced by ST2.



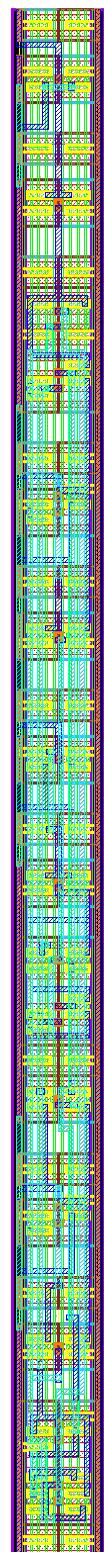
Source: From the author.

Figure B.10: Traditional Hybrid Full Adder layout.



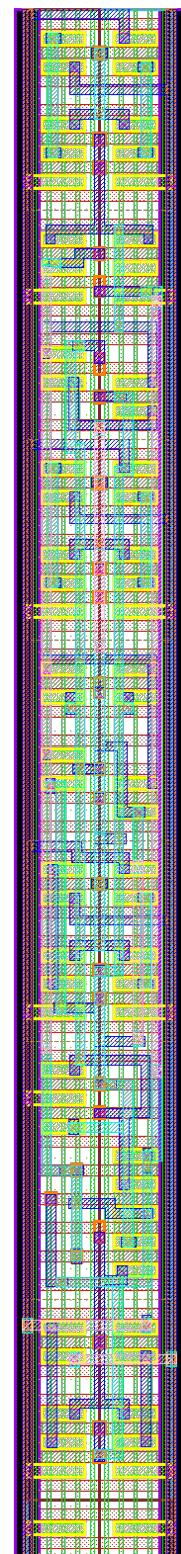
Source: From the author.

Figure B.11: Hybrid Full Adder layout with internal inverters replaced by ST1.



Source: From the author.

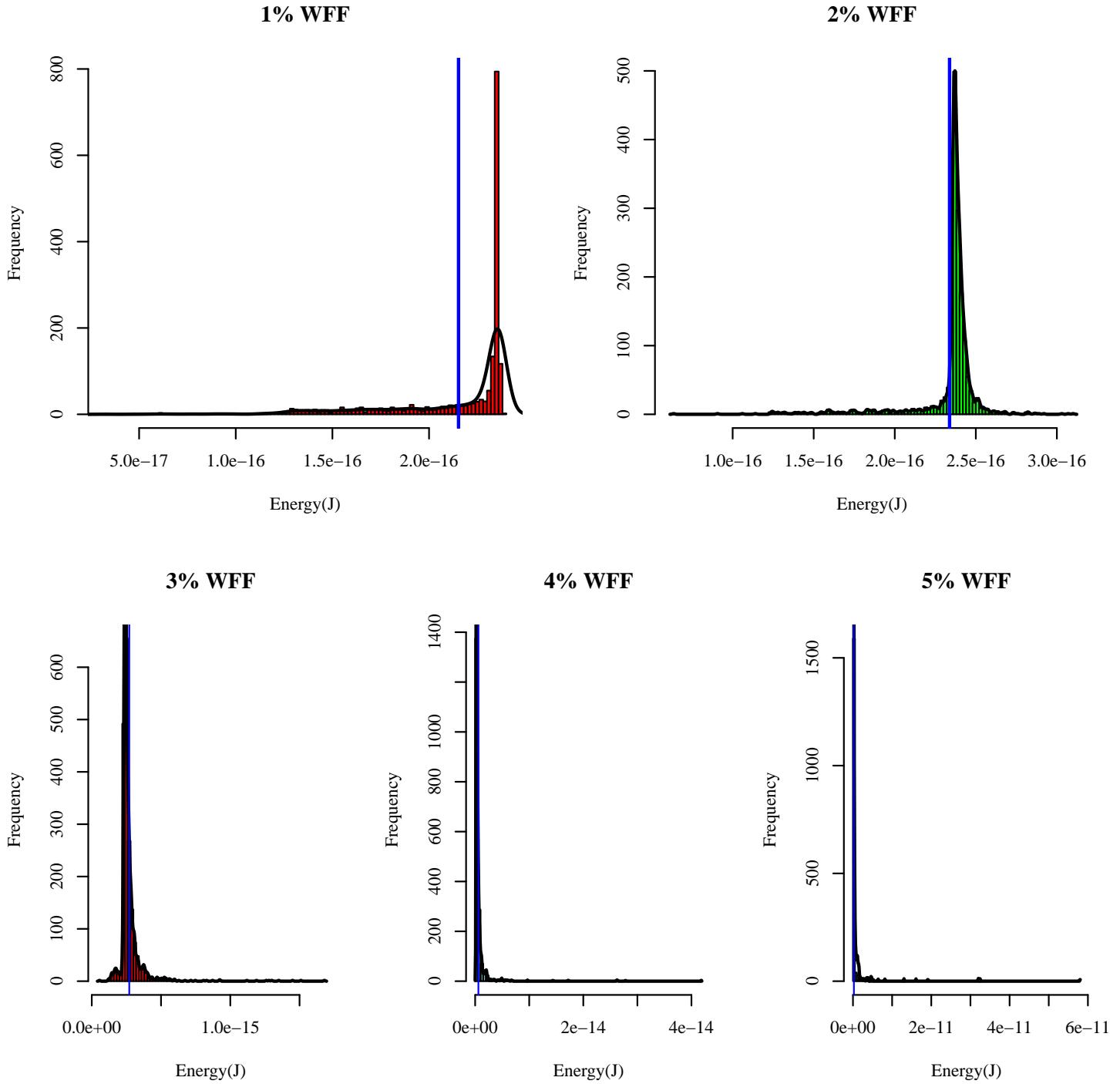
Figure B.12: Hybrid Full Adder layout with internal inverters replaced by ST2.



Source: From the author.

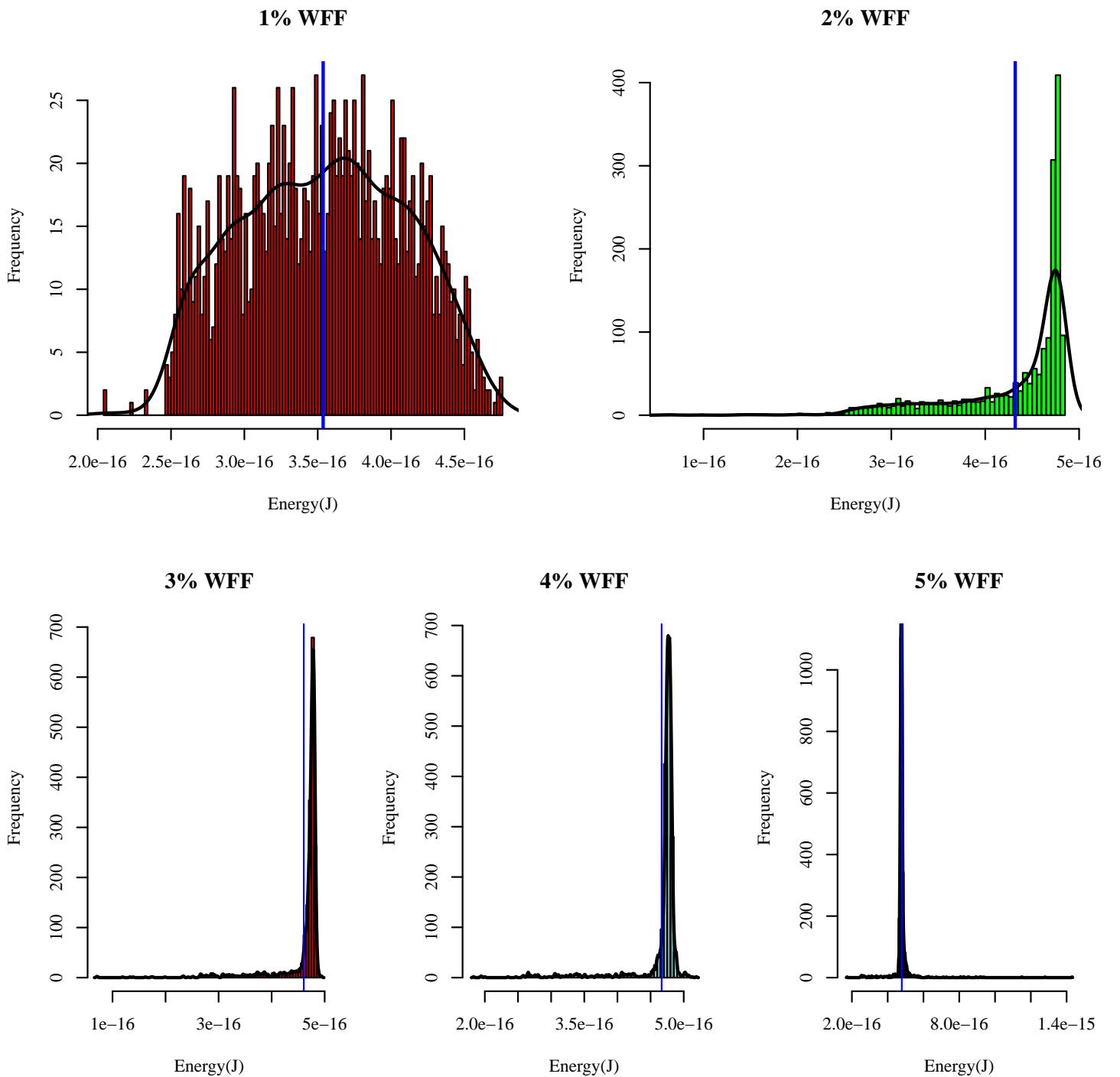
ANNEX C — ENERGY MEASURES DISTRIBUTIONS

Figure C.1: Inverter energy measures distribution operating at 0.2V.



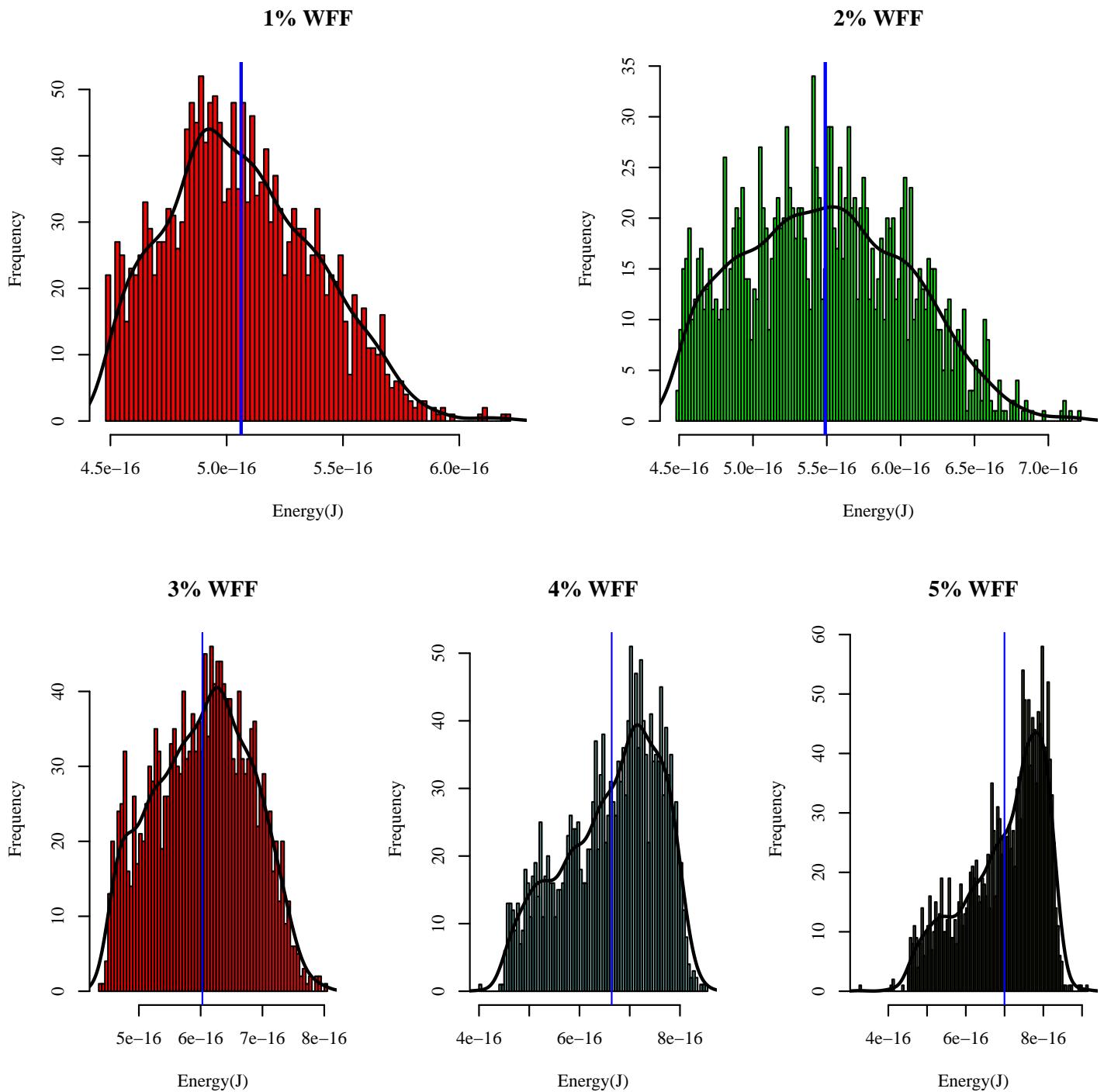
Source: From the author.

Figure C.2: Inverter energy measures distribution operating at 0.4V.



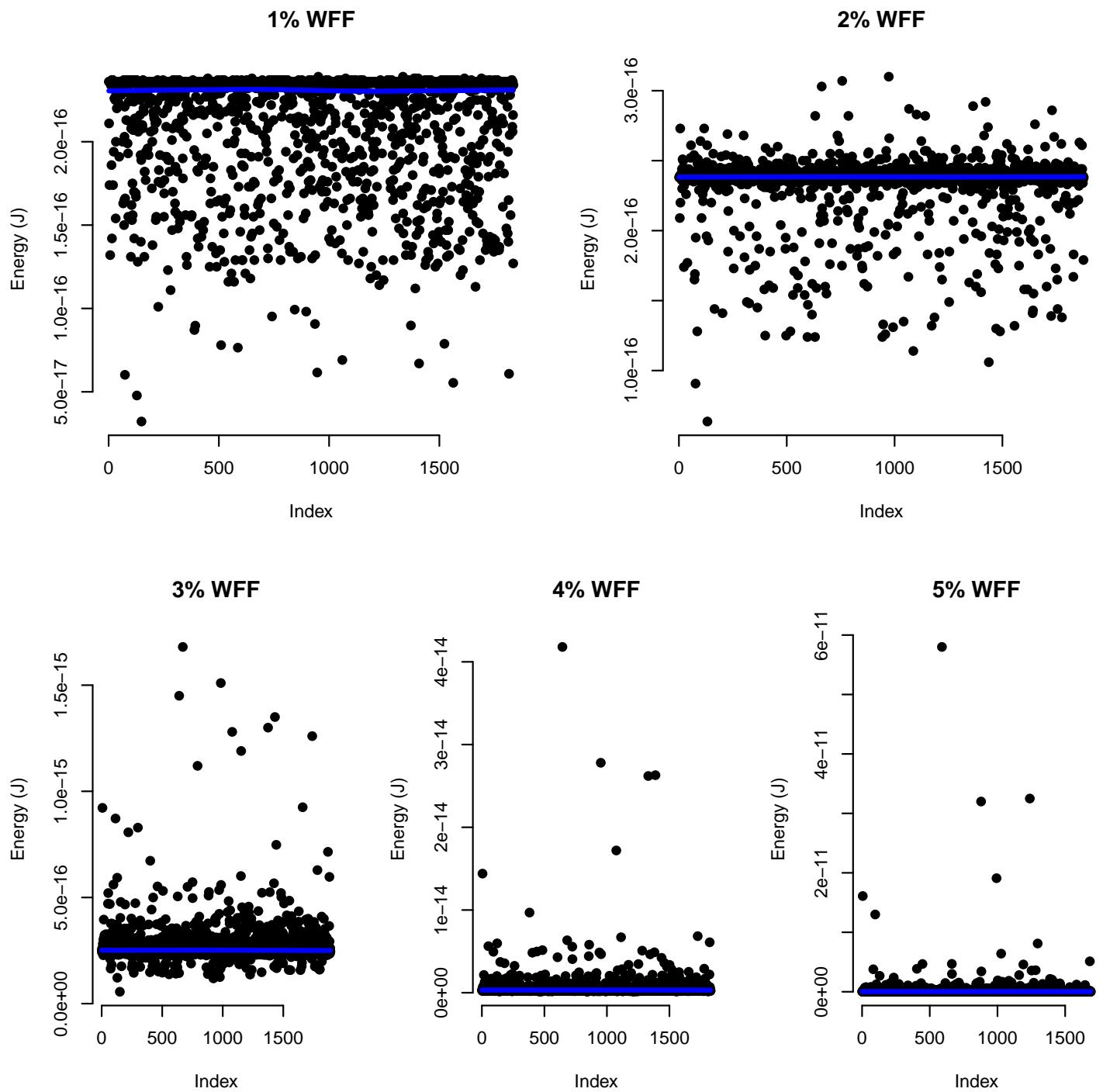
Source: From the author.

Figure C.3: Inverter energy measures distribution operating at 0.7V.



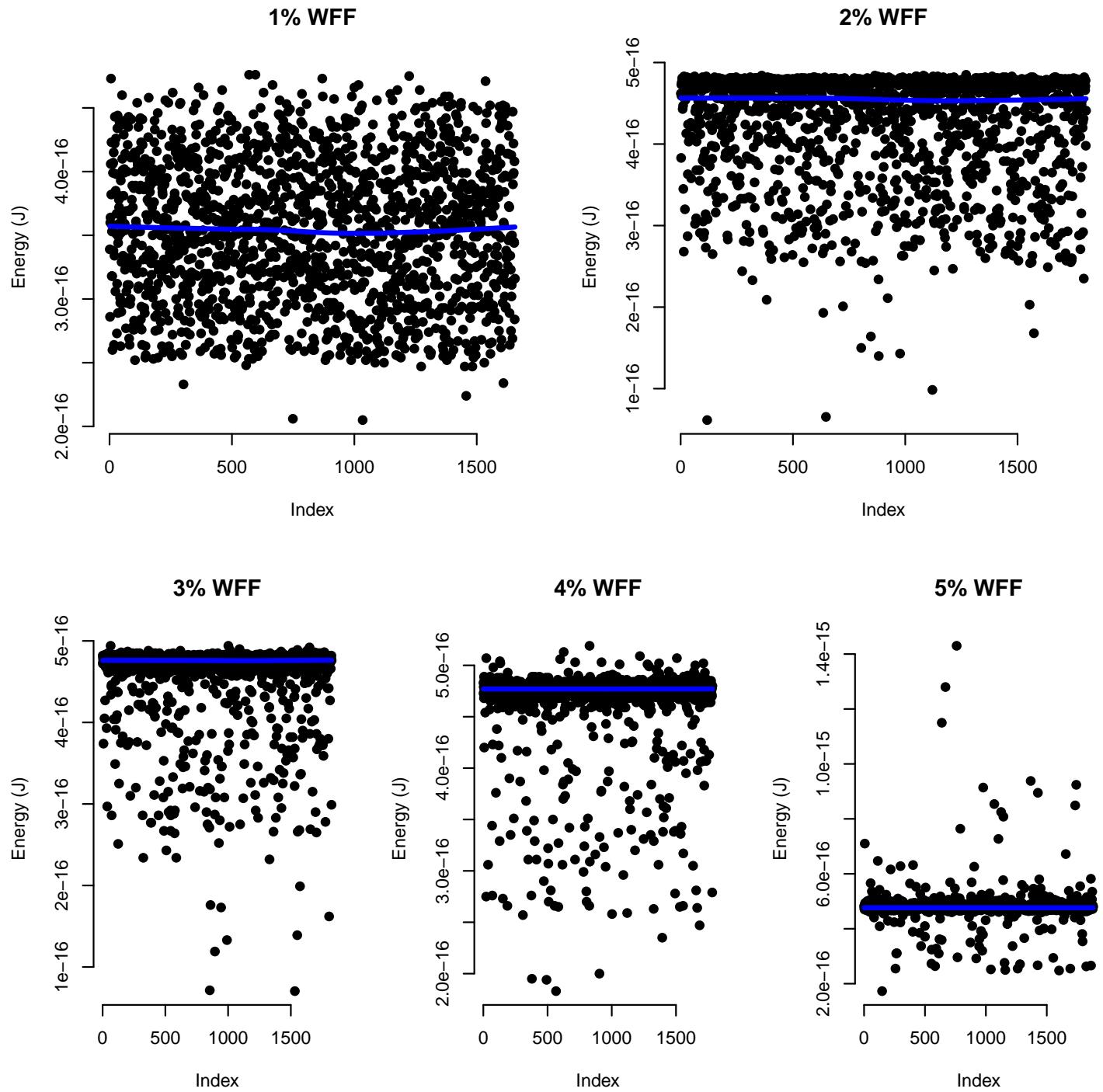
Source: From the author.

Figure C.4: Inverter energy measures dispersion operating at 0.2V.



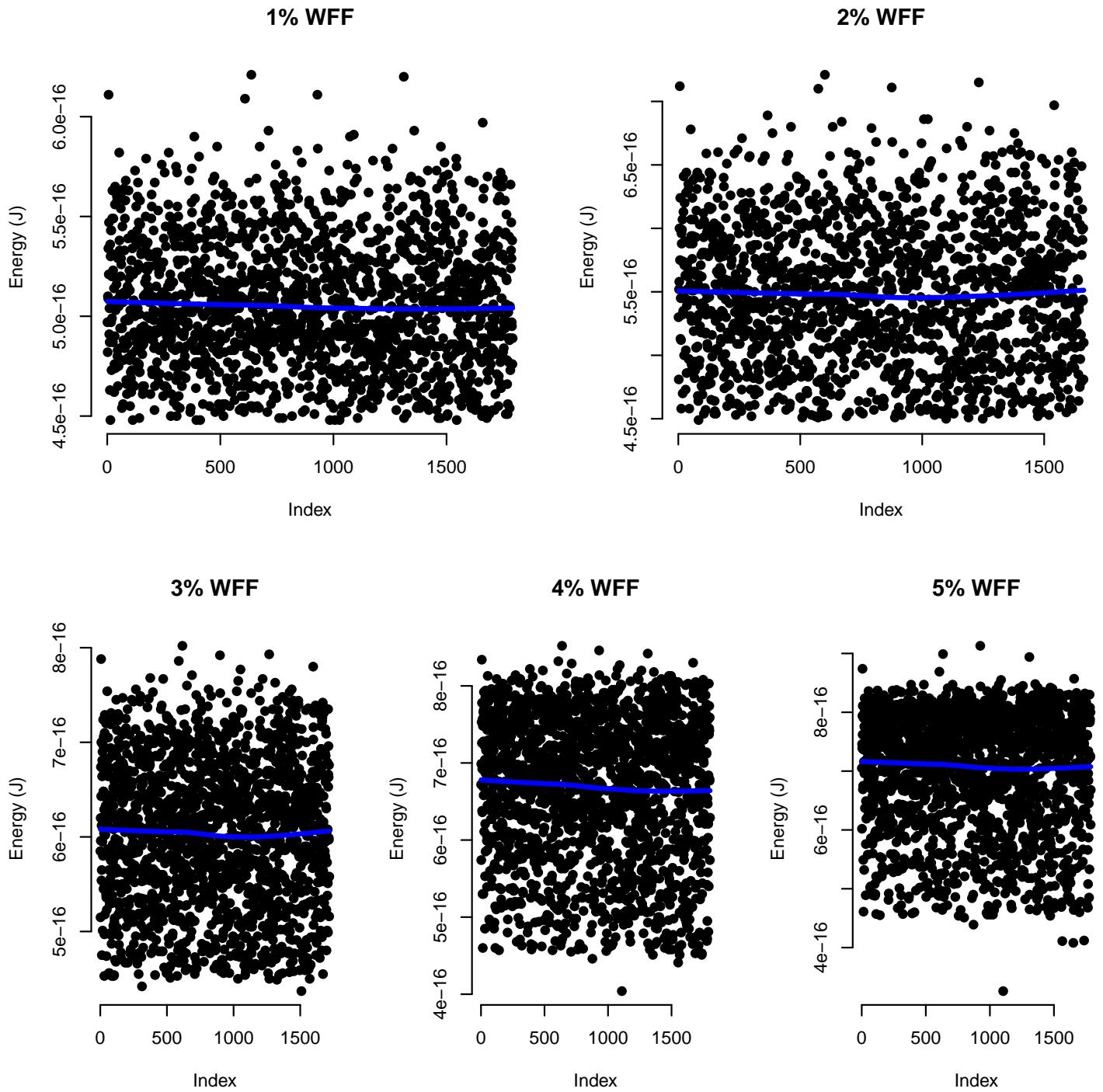
Source: From the author.

Figure C.5: Inverter energy measures dispersion operating at 0.4V.



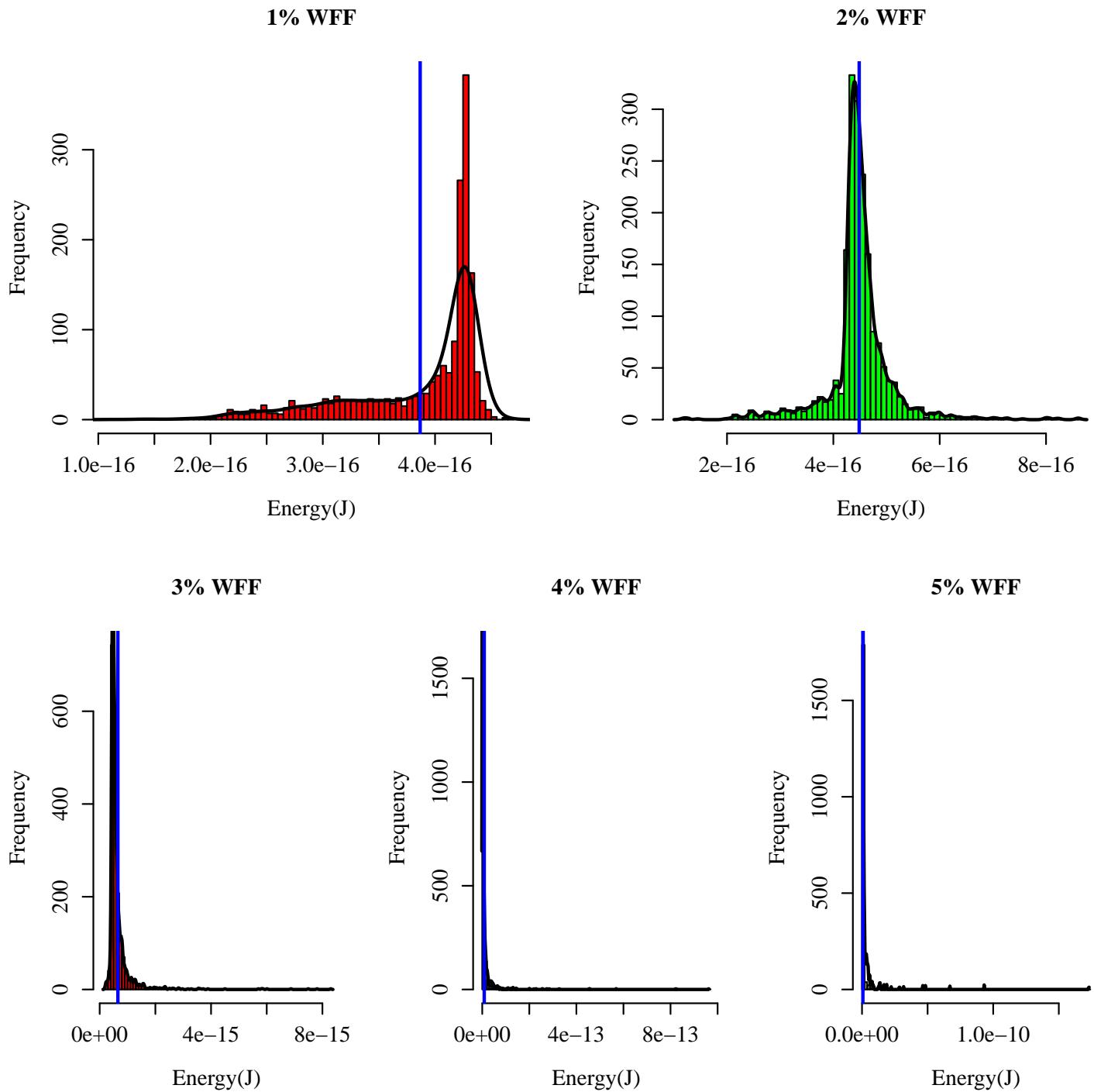
Source: From the author.

Figure C.6: Inverter energy measures dispersion operating at 0.7V.



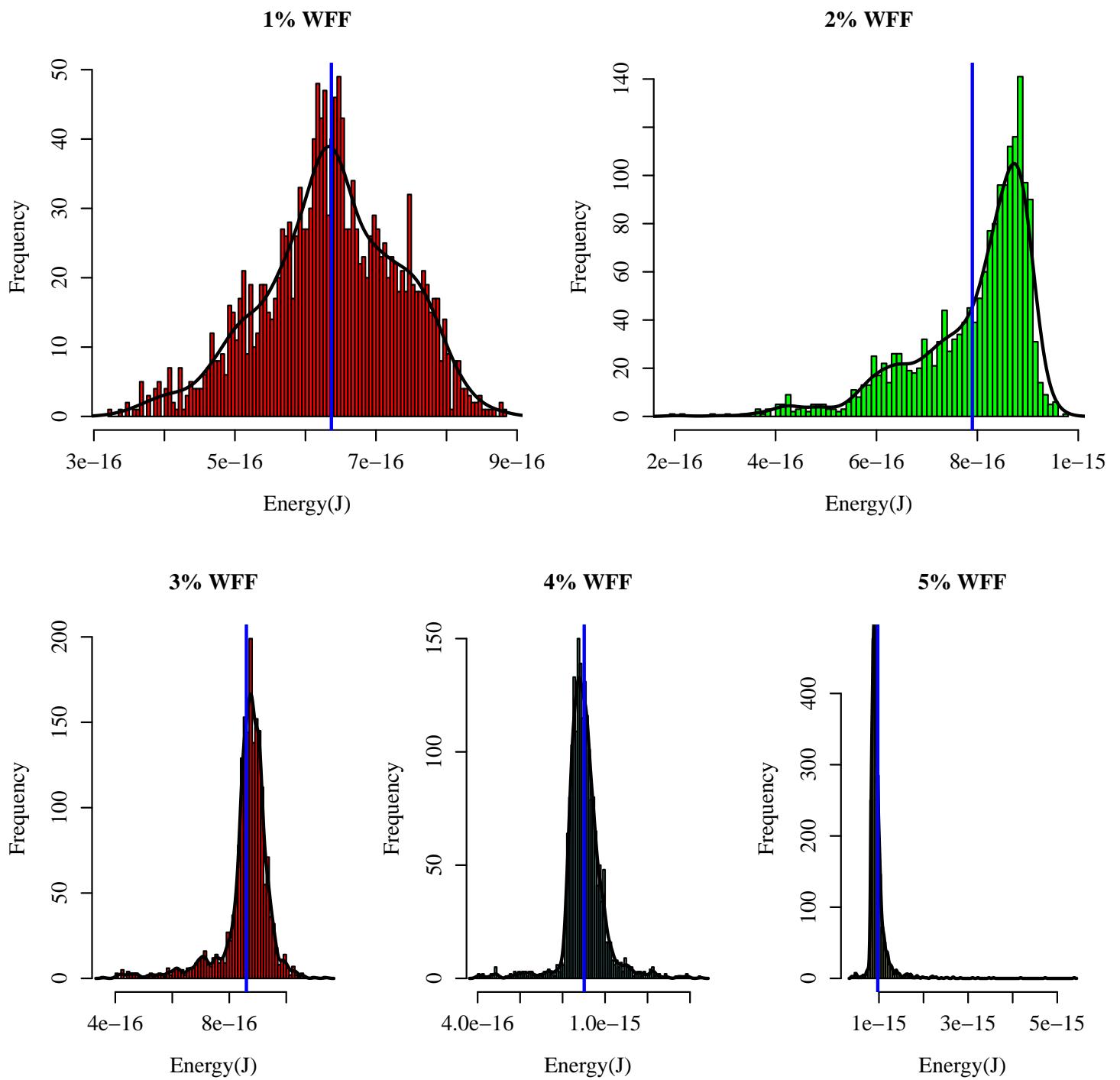
Source: From the author.

Figure C.7: ST energy measures distribution operating at 0.2V.



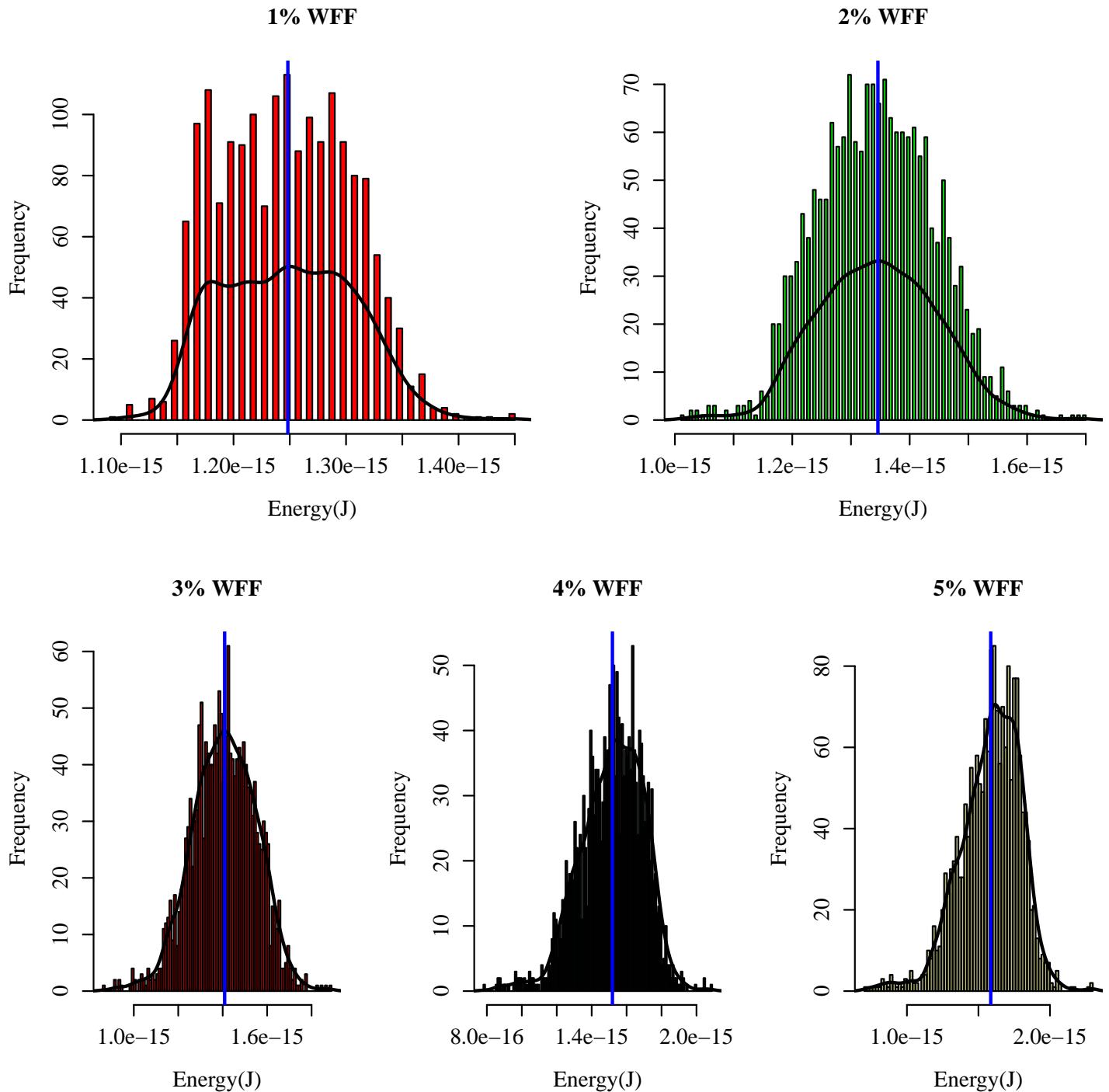
Source: From the author.

Figure C.8: ST energy measures distribution operating at 0.4V.



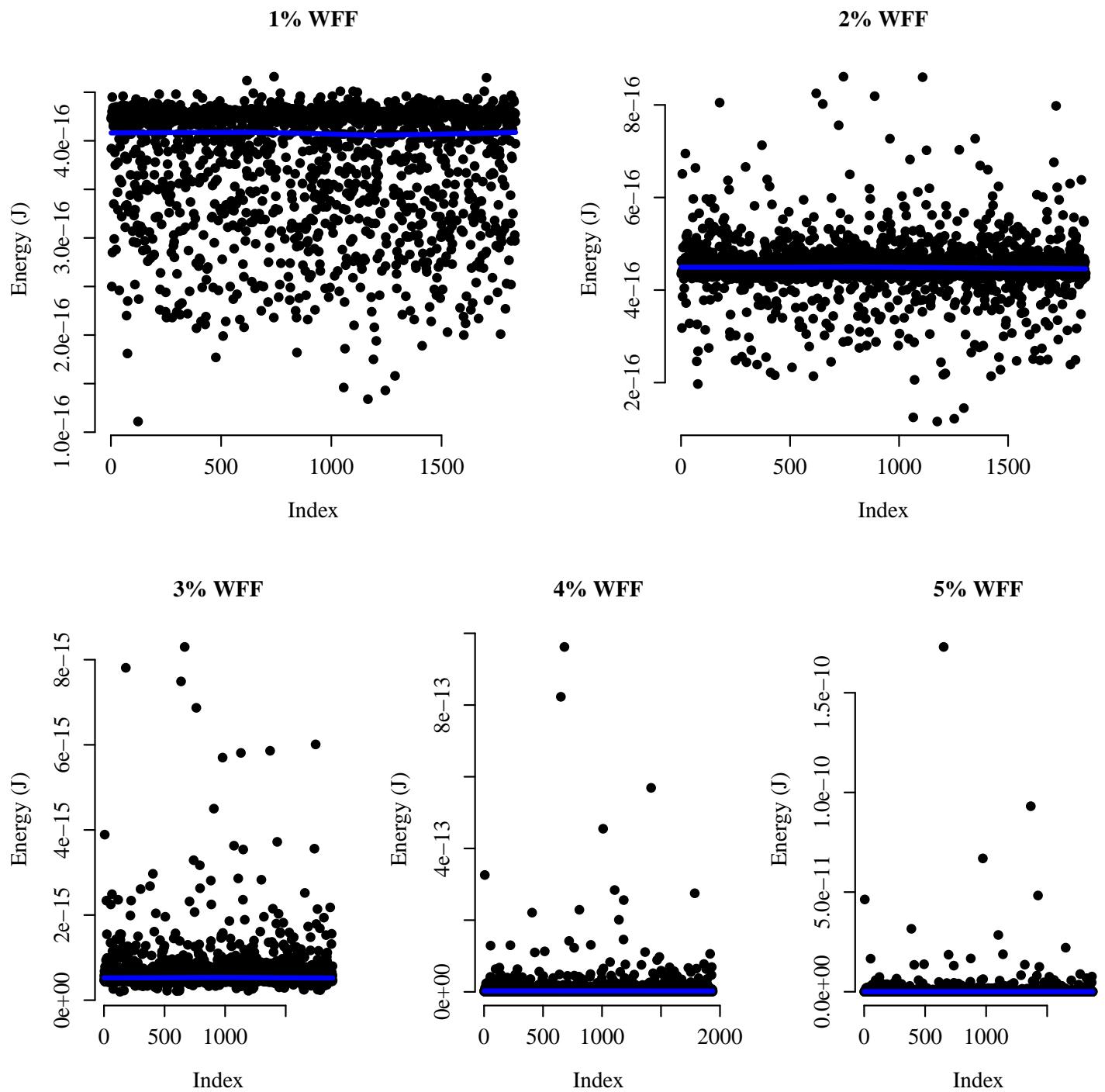
Source: From the author.

Figure C.9: ST energy measures distribution operating at 0.7V.



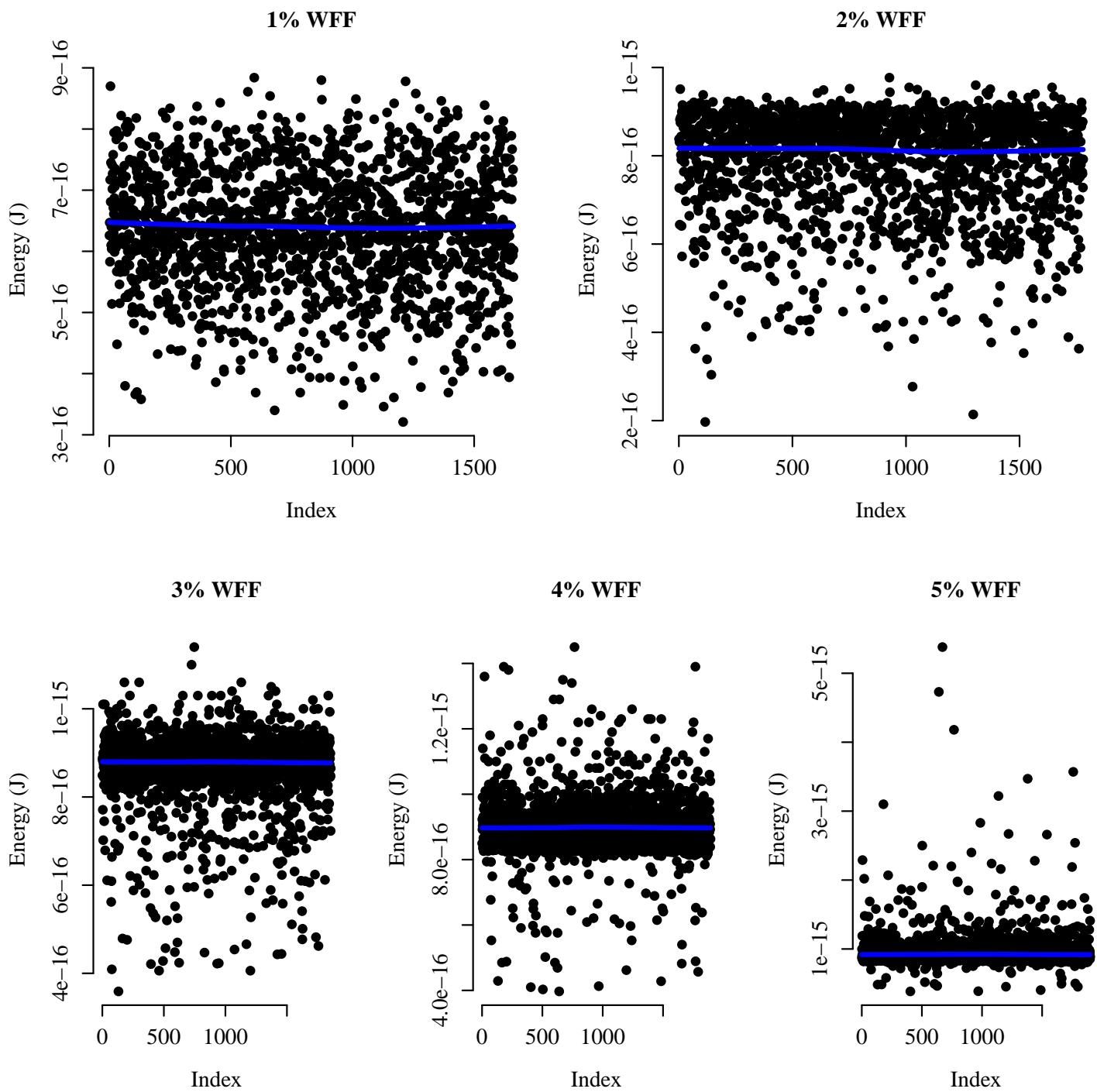
Source: From the author.

Figure C.10: ST energy measures dispersion operating at 0.2V.



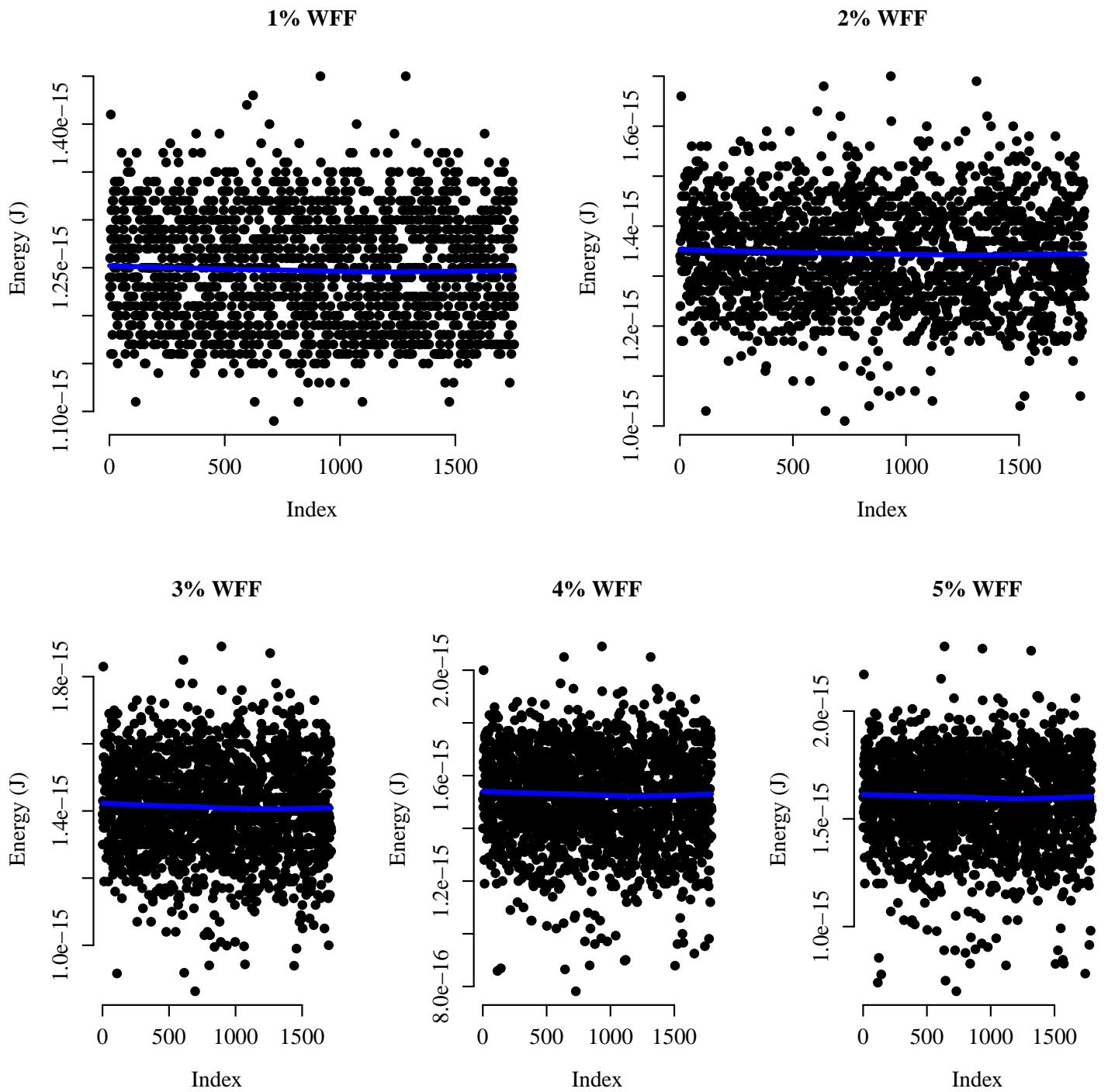
Source: From the author.

Figure C.11: ST energy measures dispersion operating at 0.4V.



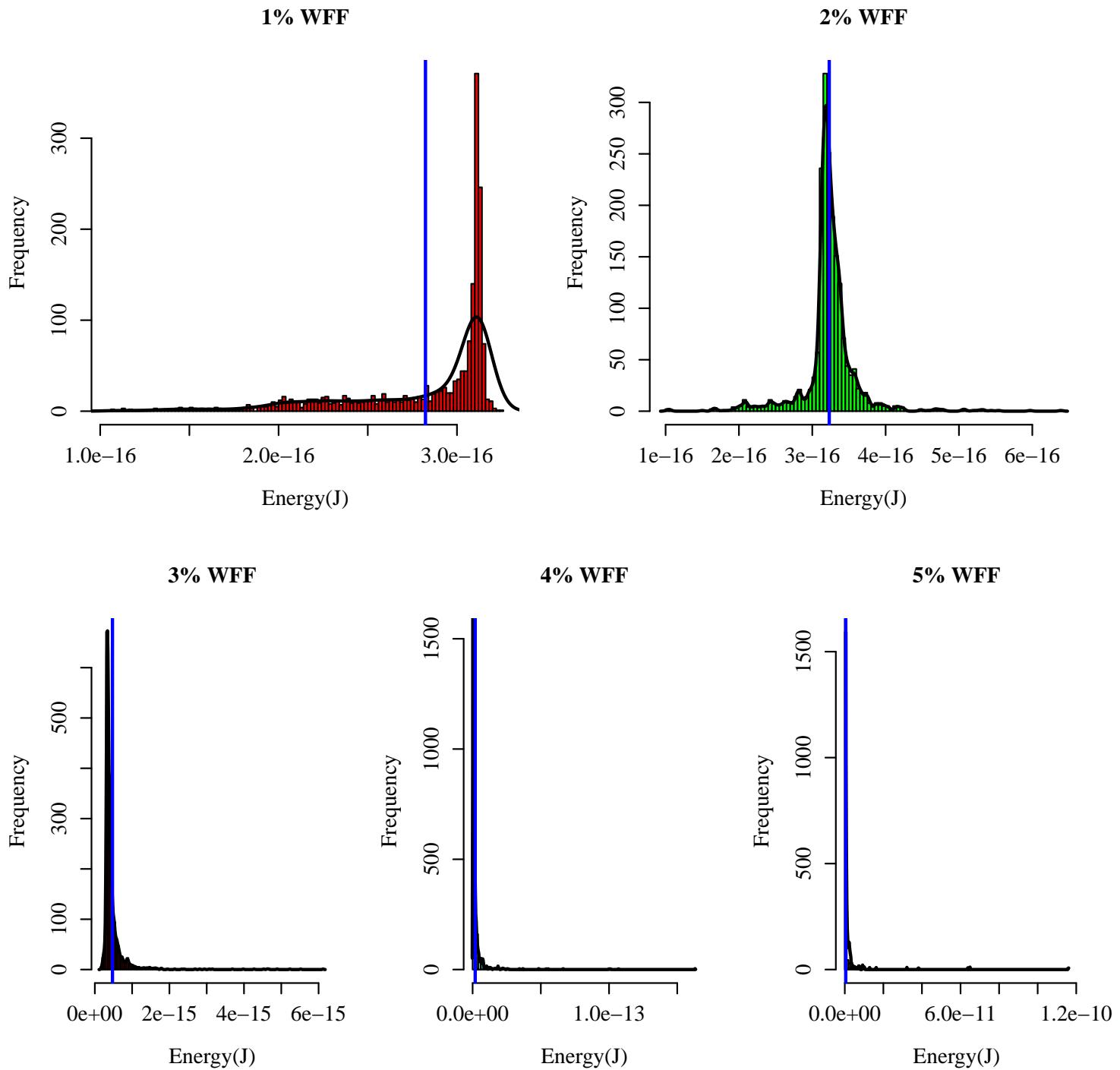
Source: From the author.

Figure C.12: ST energy measures dispersion operating at 0.7V.



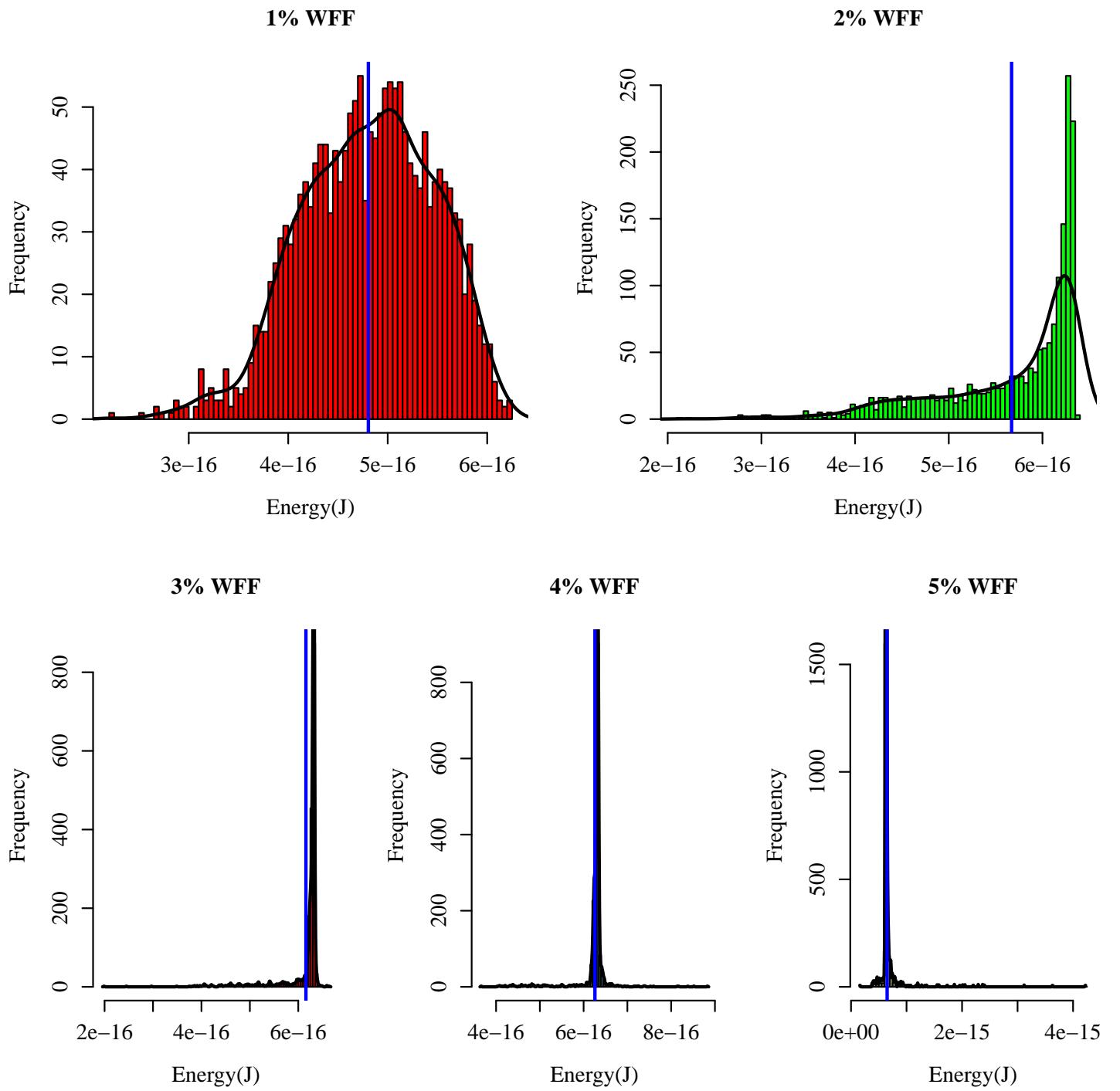
Source: From the author.

Figure C.13: SIG energy measures distribution operating at 0.2V.



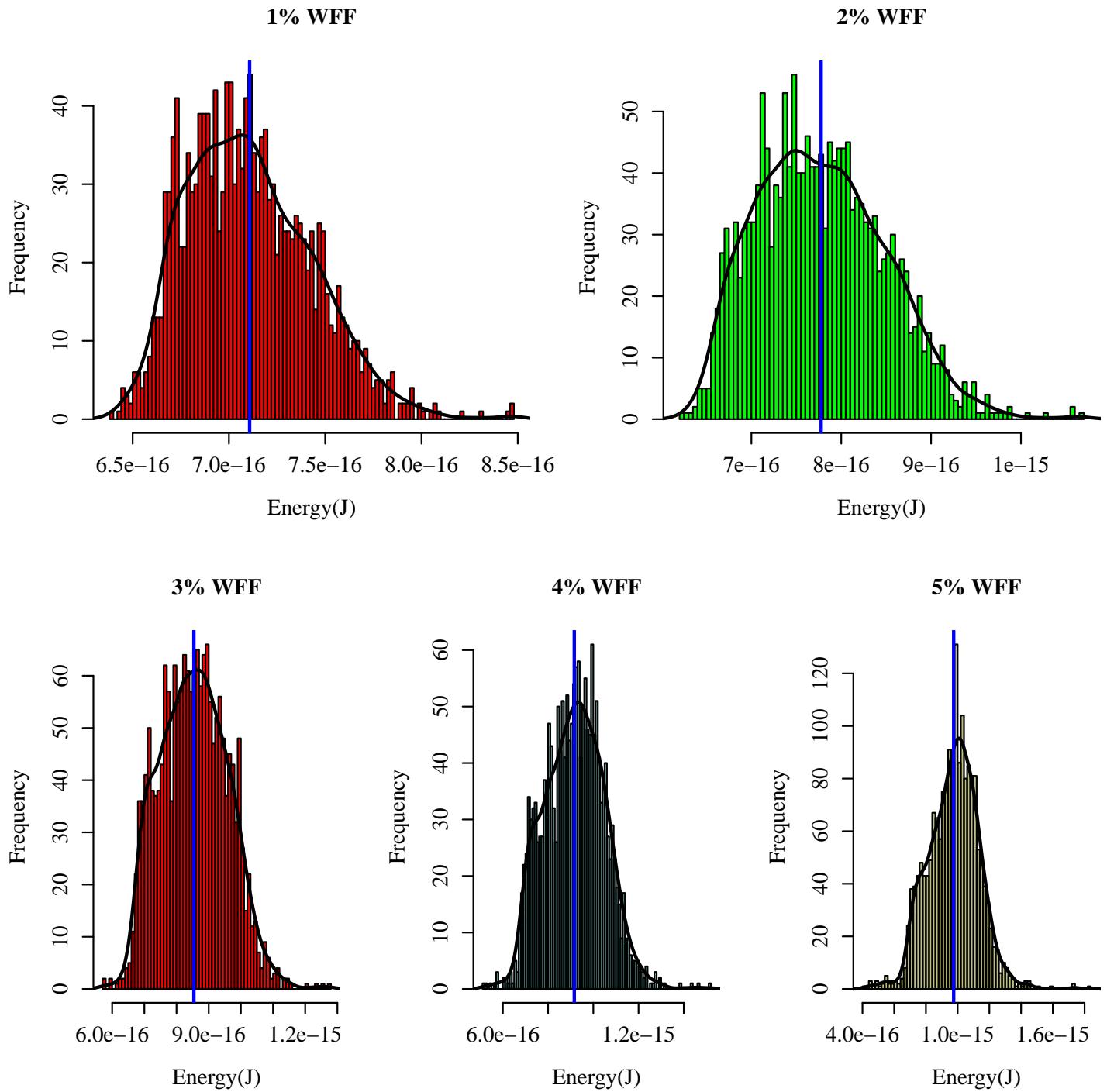
Source: From the author.

Figure C.14: SIG energy measures distribution operating at 0.4V.



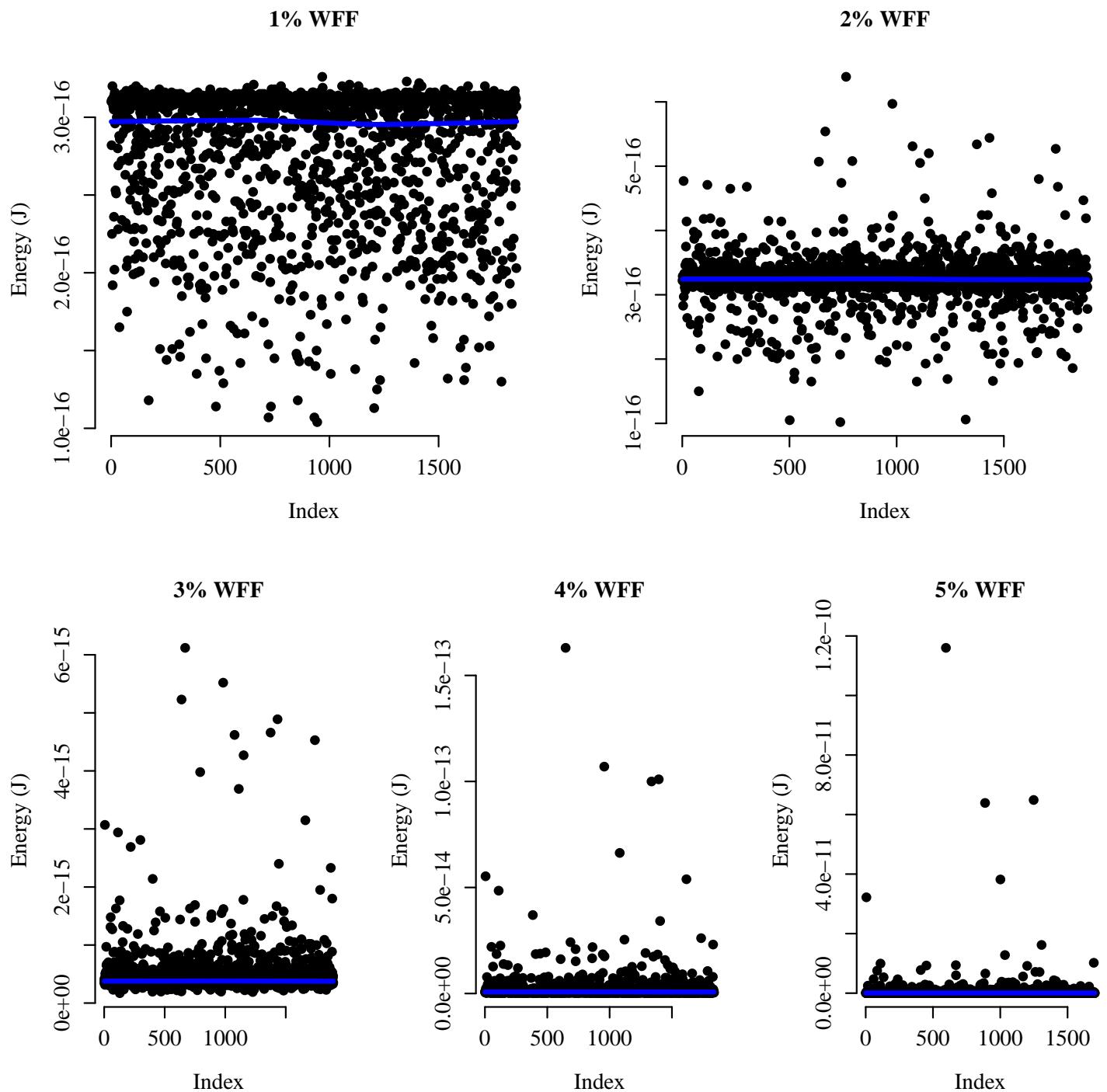
Source: From the author.

Figure C.15: SIG energy measures distribution operating at 0.7V.



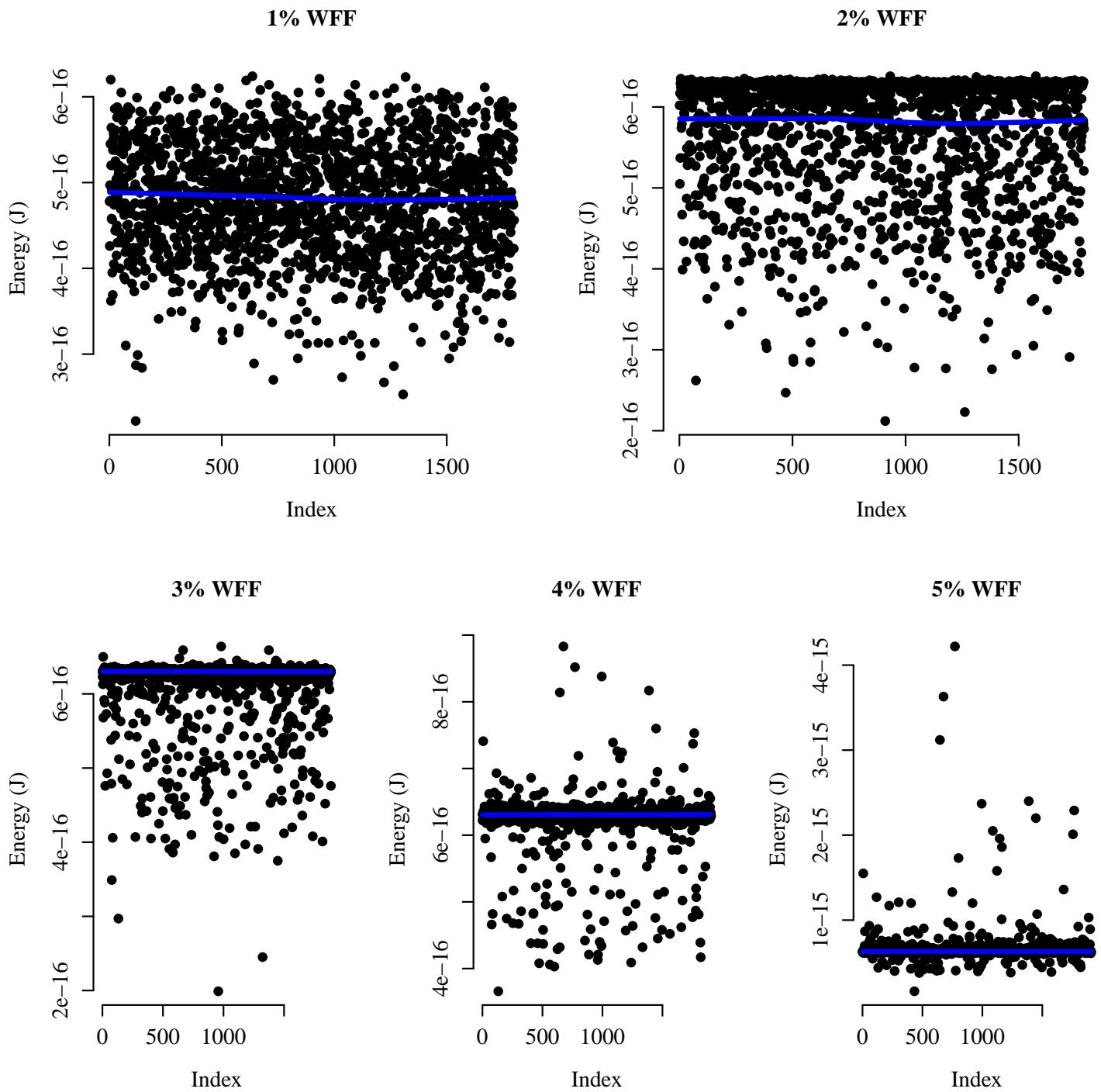
Source: From the author.

Figure C.16: SIG energy measures dispersion operating at 0.2V.



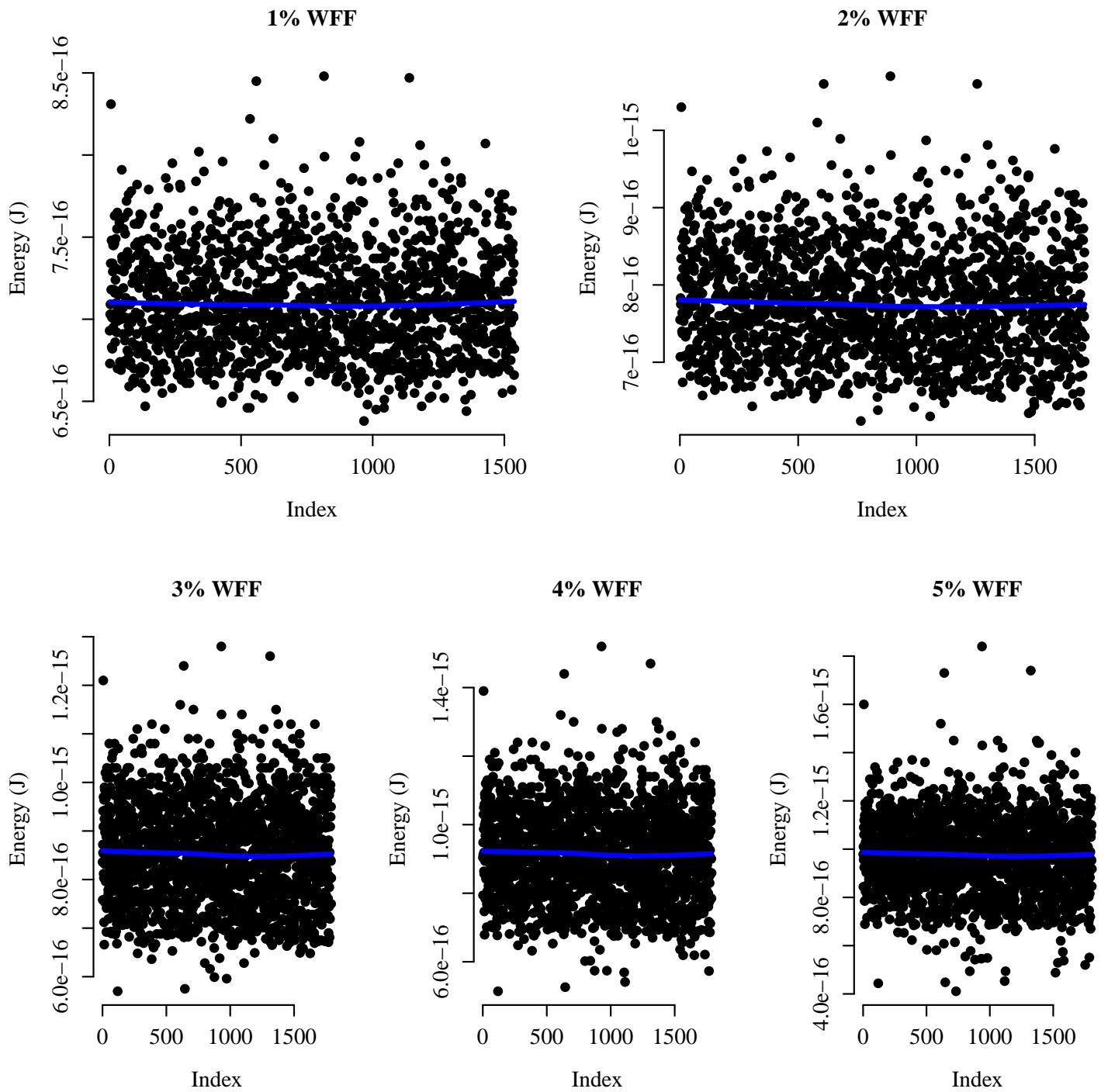
Source: From the author.

Figure C.17: SIG energy measures dispersion operating at 0.4V.



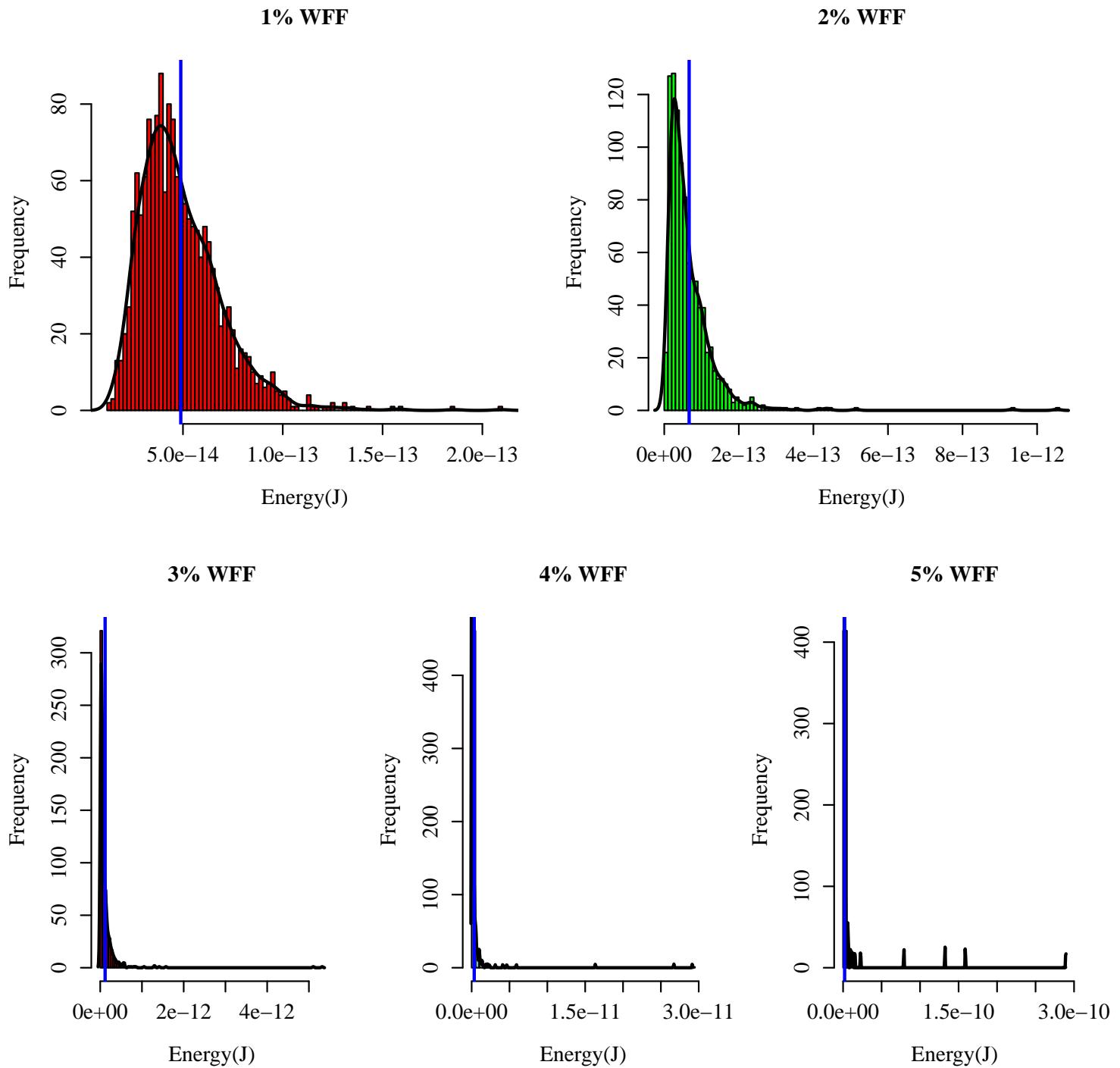
Source: From the author.

Figure C.18: SIG energy measures dispersion operating at 0.7V.



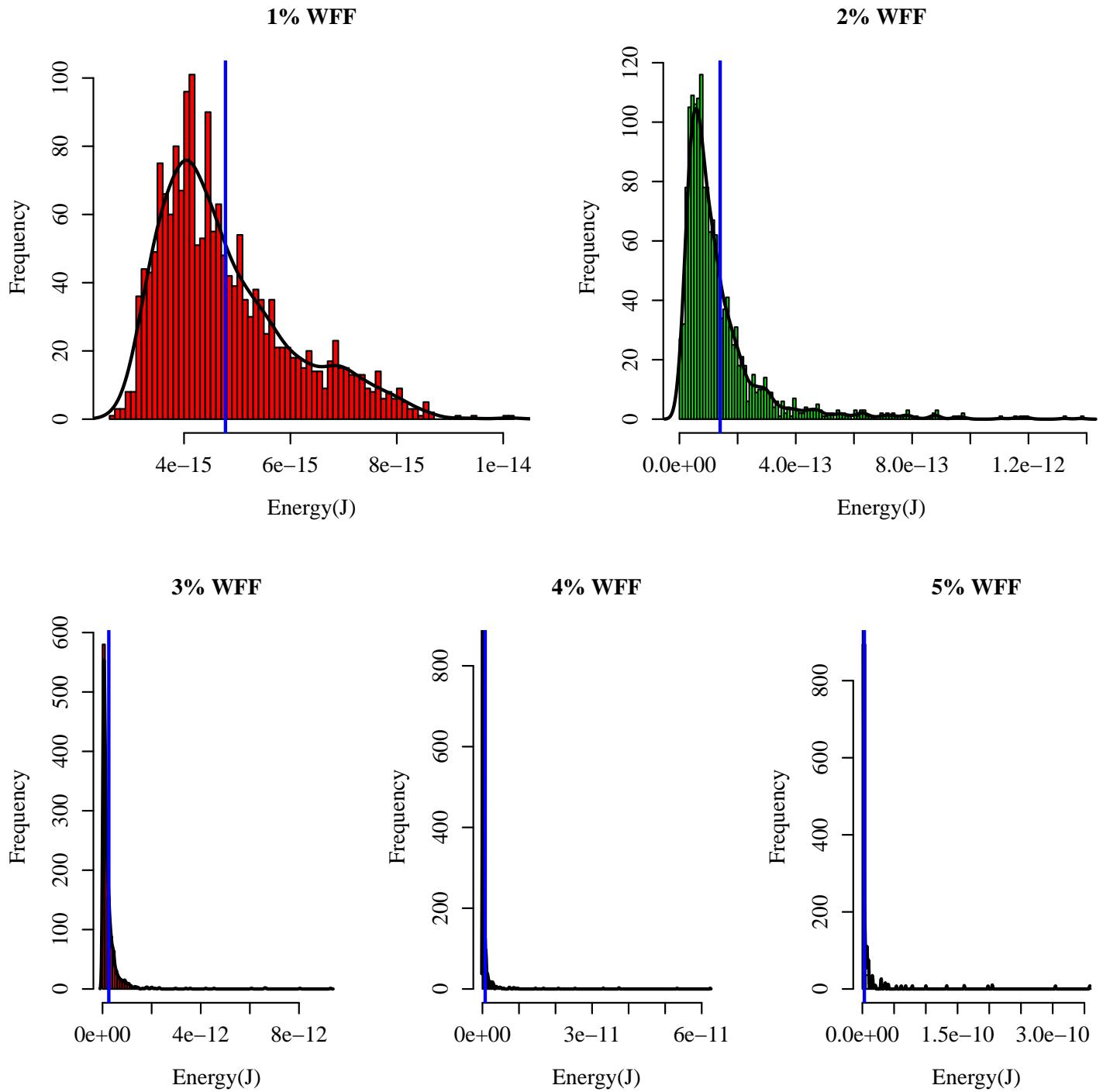
Source: From the author.

Figure C.19: TIST 2:1 energy measures distribution operating at 0.2V.



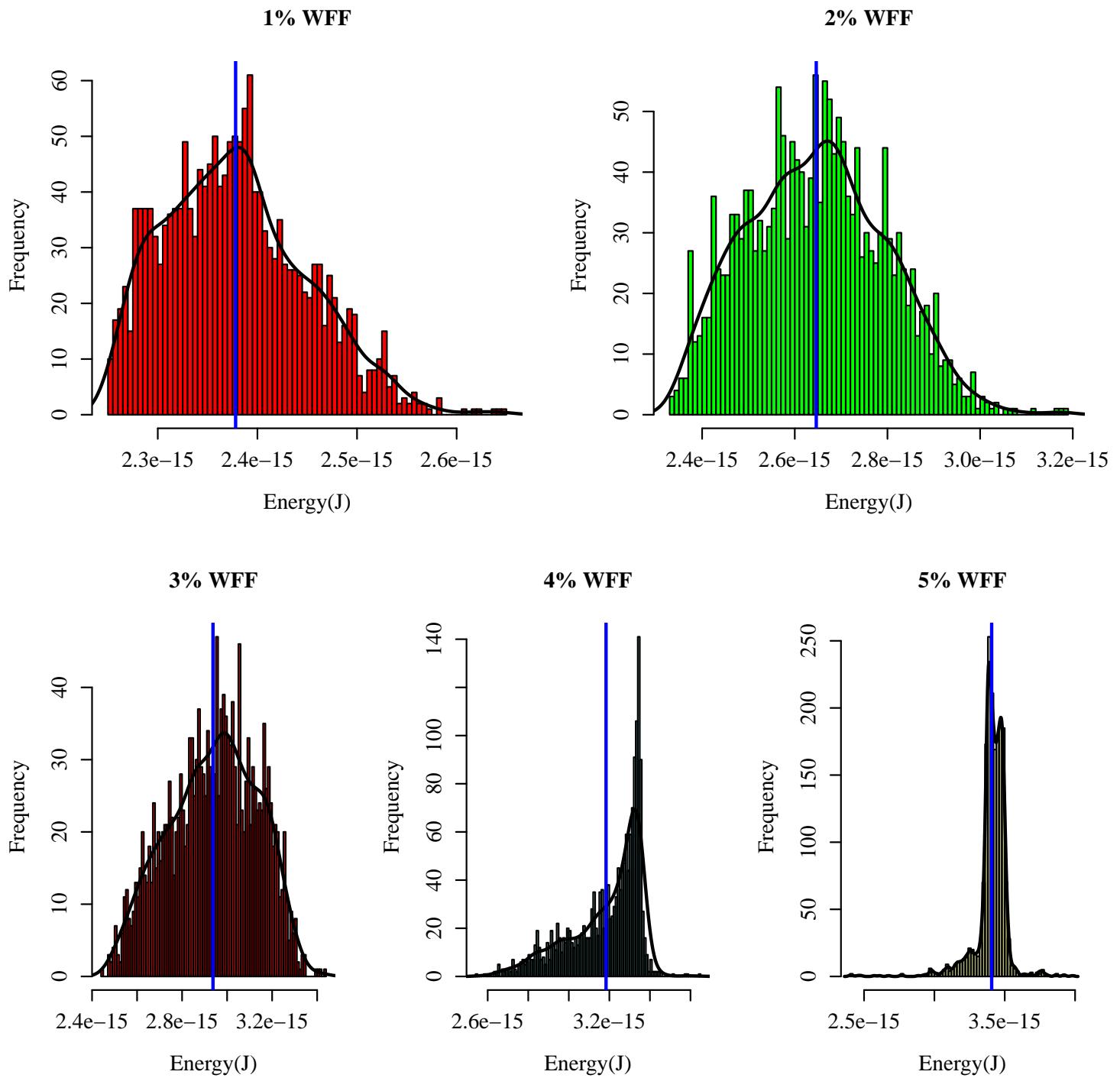
Source: From the author.

Figure C.20: TIST 2:1 energy measures distribution operating at 0.4V.



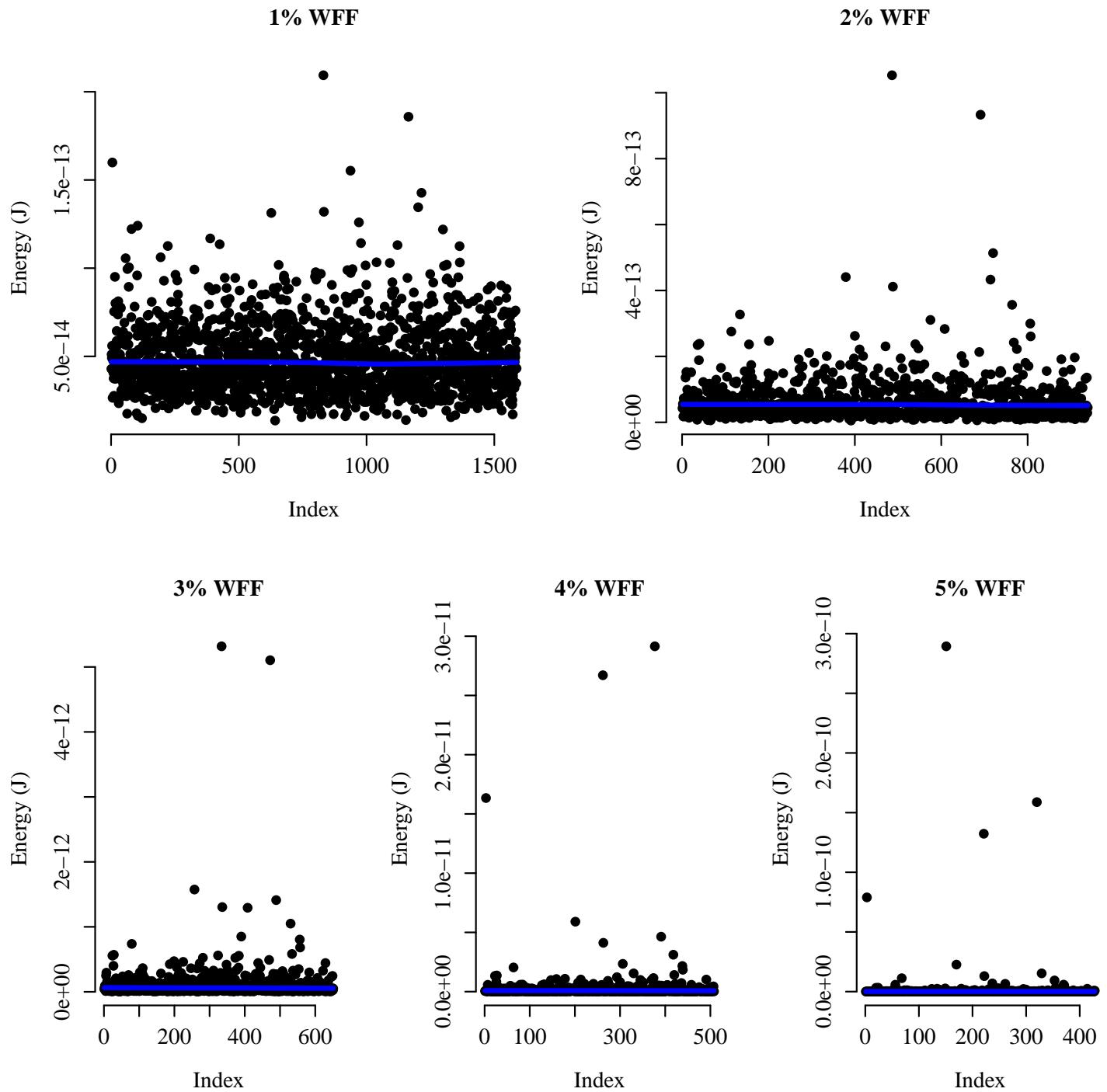
Source: From the author.

Figure C.21: TIST 2:1 energy measures distribution operating at 0.7V.



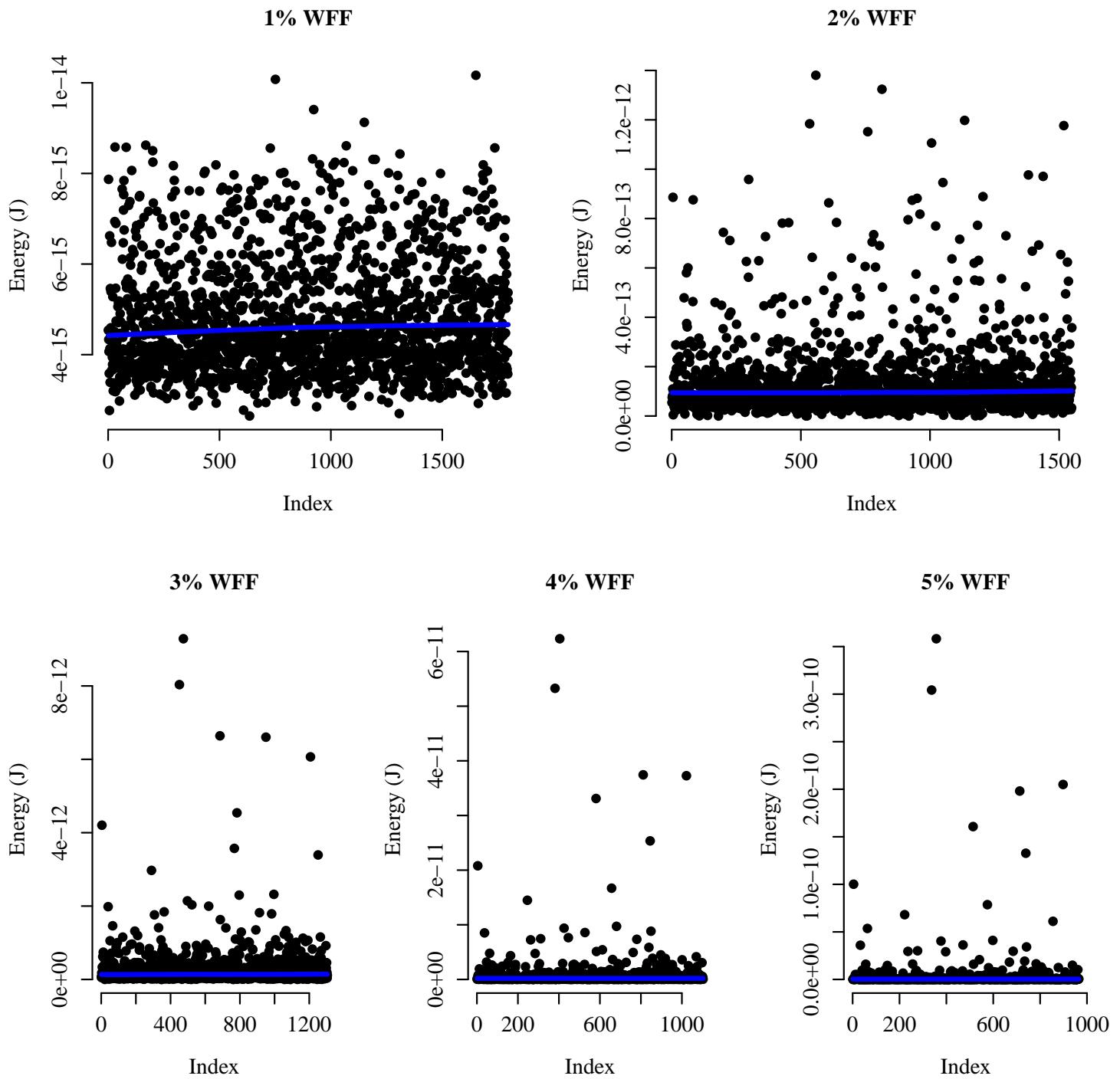
Source: From the author.

Figure C.22: TIST 2:1 energy measures dispersion operating at 0.2V.



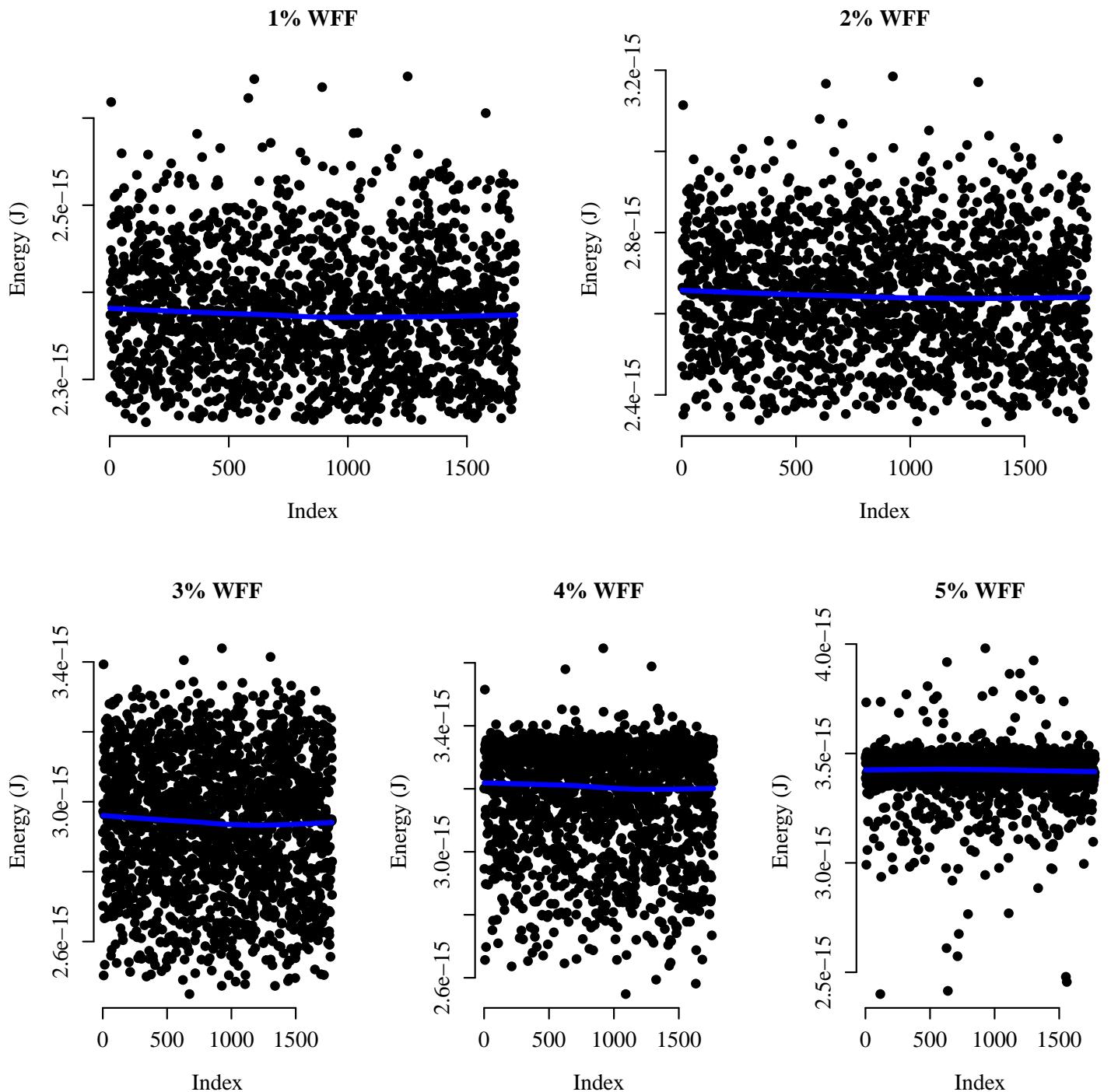
Source: From the author.

Figure C.23: TIST 2:1 energy measures dispersion operating at 0.4V.



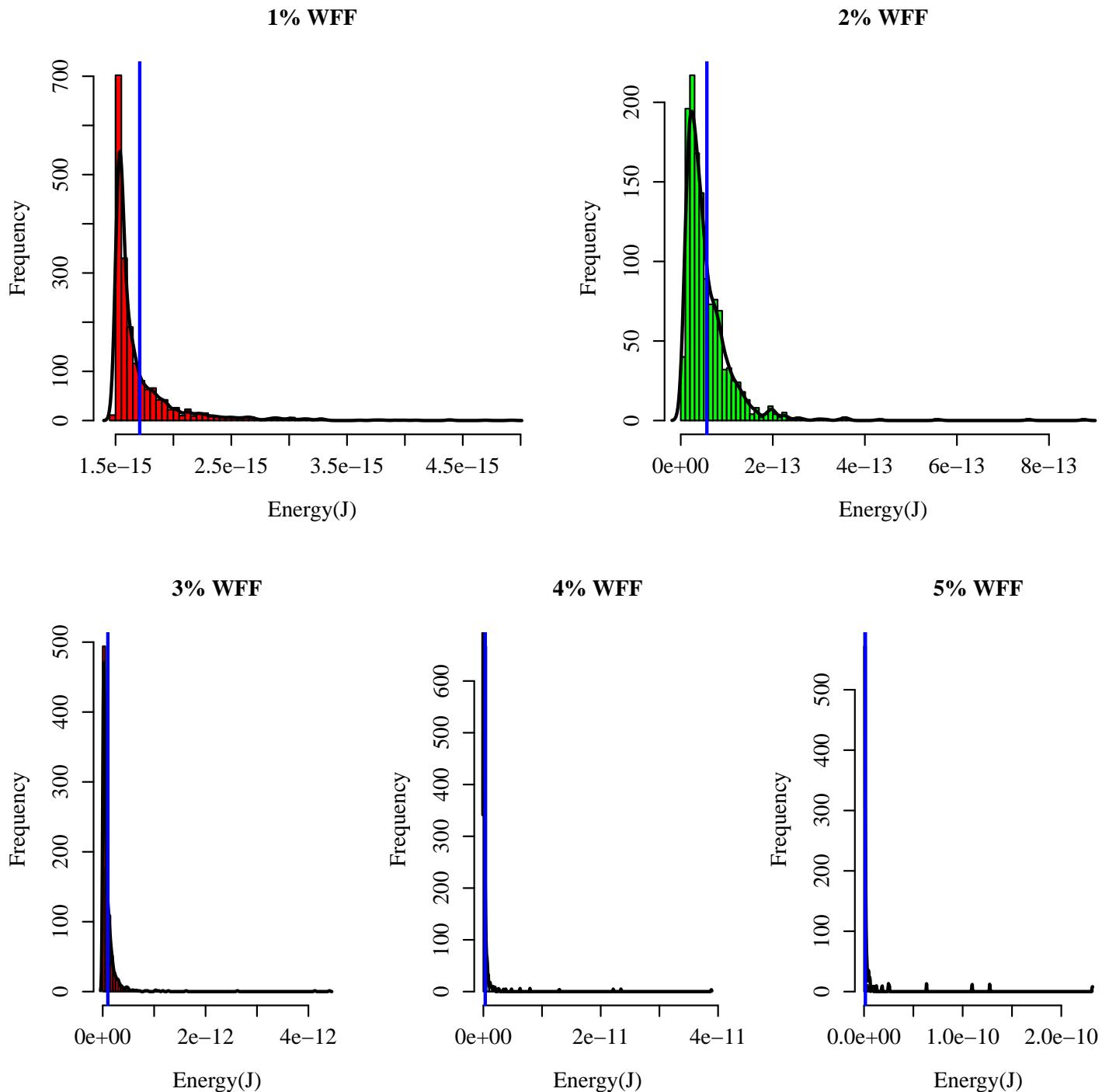
Source: From the author.

Figure C.24: TIST 2:1 energy measures dispersion operating at 0.7V.



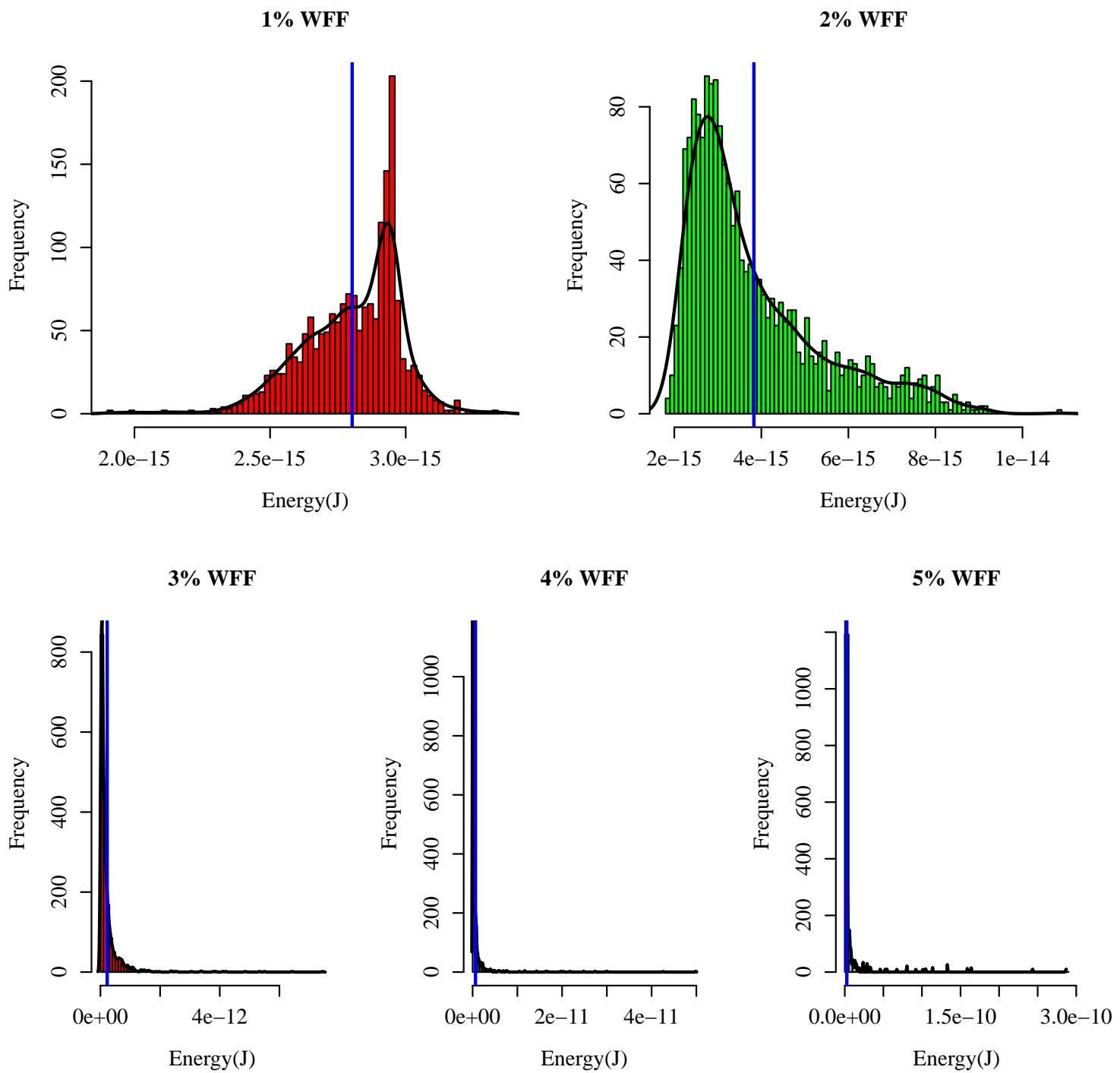
Source: From the author.

Figure C.25: TIST 3:1 energy measures distribution operating at 0.2V.



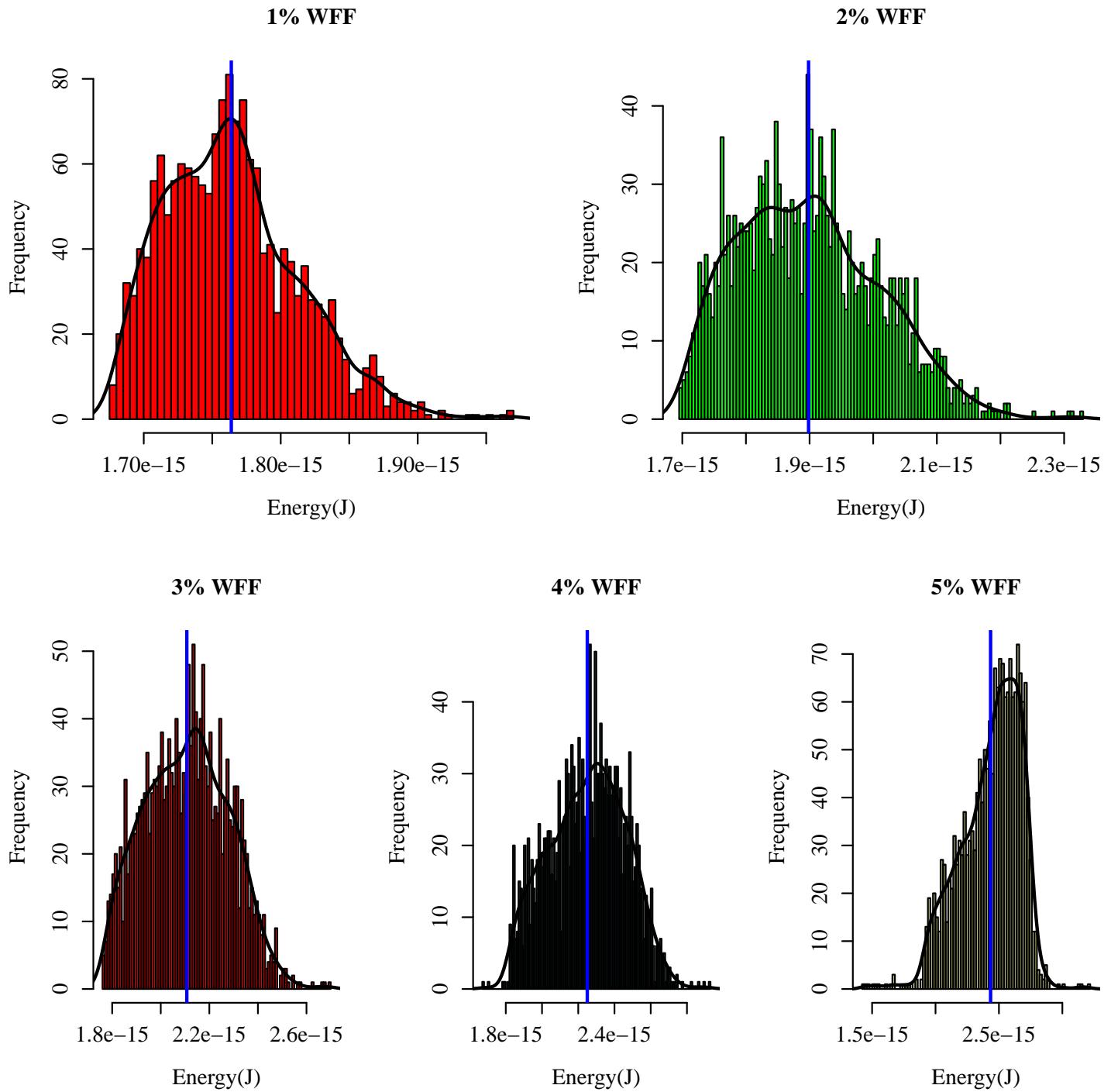
Source: From the author.

Figure C.26: TIST 3:1 energy measures distribution operating at 0.4V.



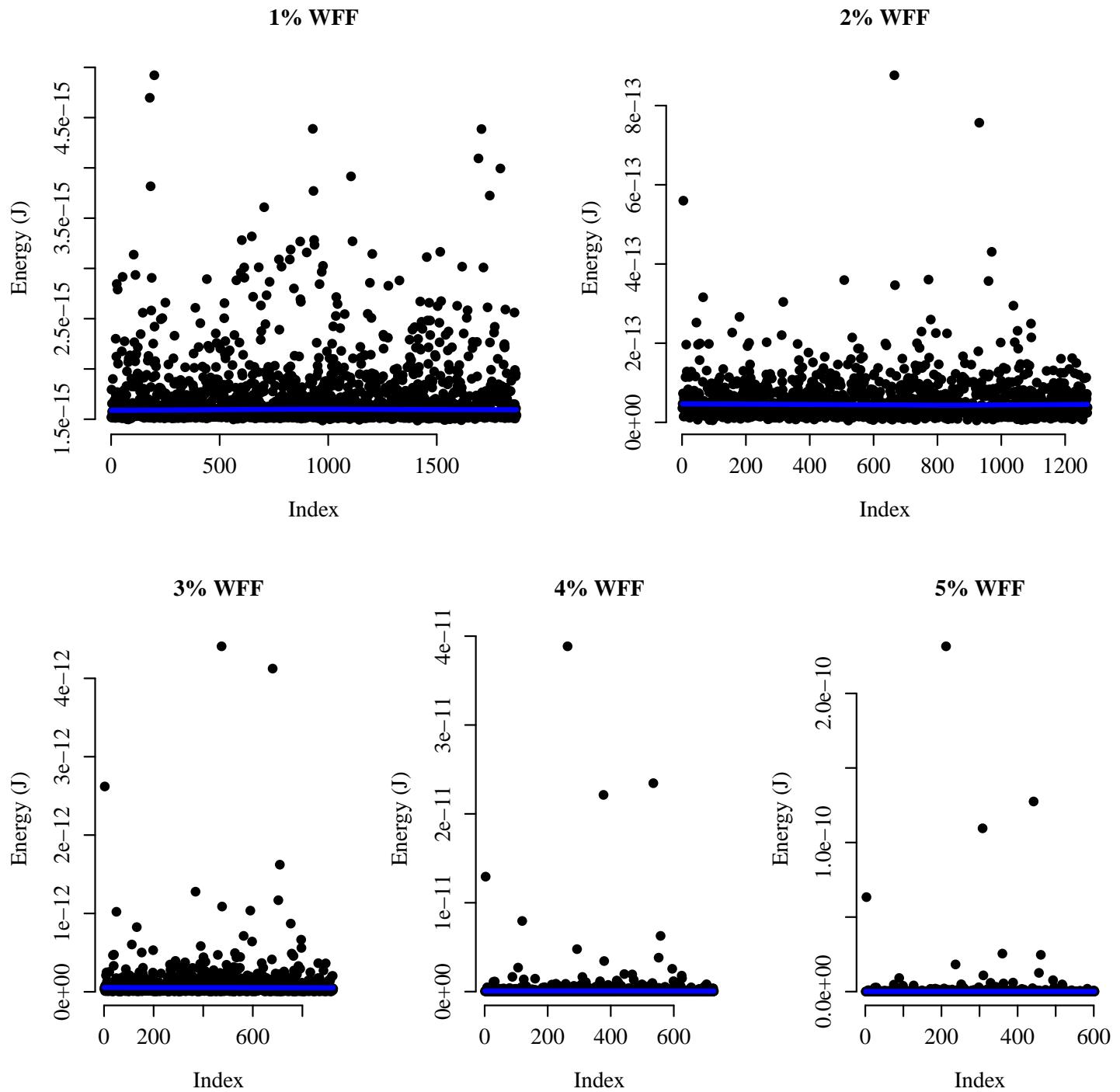
Source: From the author.

Figure C.27: TIST 3:1 energy measures distribution operating at 0.7V.



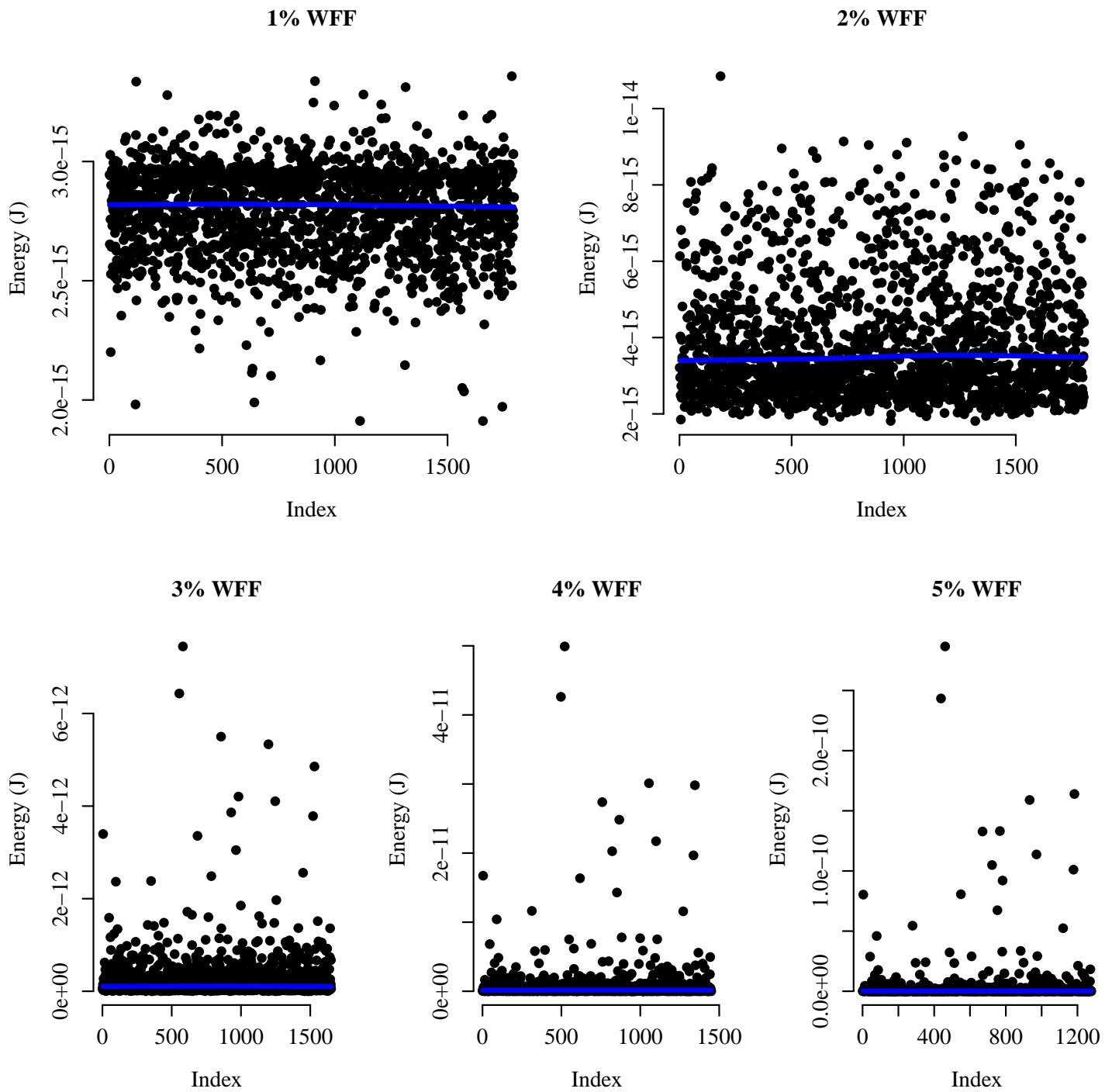
Source: From the author.

Figure C.28: TIST 3:1 energy measures dispersion operating at 0.2V.



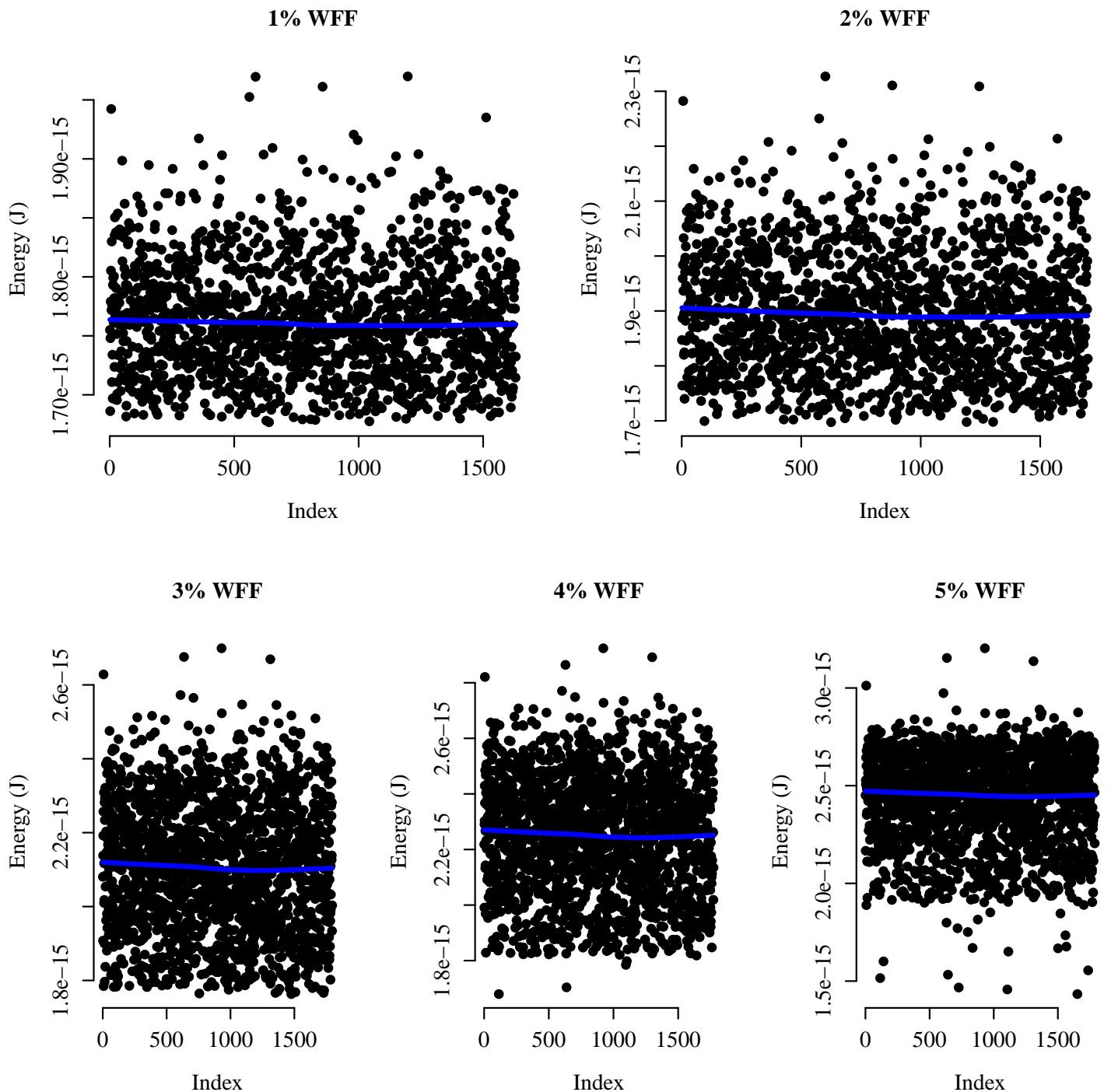
Source: From the author.

Figure C.29: TIST 3:1 energy measures dispersion operating at 0.4V.



Source: From the author.

Figure C.30: TIST 3:1 energy measures dispersion operating at 0.7V.



Source: From the author.

ANNEX D — EXTRACTED NETLISTS FROM LAYOUTS

Figure D.1: Inverter extracted netlist for all sizings.

Inverter 1 fin:	Inverter 2 fins:	Inverter 3 fins:	Inverter 4 fins:	Inverter 5 fins:
.subckt	.subckt	.subckt	.subckt	.subckt
PM_INV1F_GND 1 6 18 20 21 30 c10 30 0 0.00214761f c11 21 0 0.022629f c12 20 0 0.00975337f c13 6 0 0.0459004f r14 21 30 135 r15 20 21 2 r16 20 21 0.375 r17 18 20 2.85185 r18 14 18 4.48148 r19 14 30 2 r20 6 30 54.8065 r21 4 21 31.503 r22 1 4 22.2222 .ends	PM_INV2F_GND 1 6 18 20 21 30 c10 30 0 0.00224772f c11 21 0 0.0227237f c12 20 0 0.00975047f c13 6 0 0.0459004f r14 21 30 135 r15 20 21 2 r16 20 21 0.375 r17 18 20 2.85185 r18 14 18 4.48148 r19 14 30 2 r20 6 30 54.8065 r21 4 21 43.1548 r22 1 4 11.1111 .ends	PM_INV3F_GND 1 6 18 20 21 30 c11 30 0 0.00209582f c12 21 0 0.0227731f c13 20 0 0.00971704f c14 6 0 0.0459004f r15 21 30 135 r16 20 21 2 r17 20 21 0.375 r18 18 20 2.85185 r19 14 18 4.48148 r20 14 30 2 r21 6 30 54.8065 r22 4 21 54.8065 r23 1 4 7.40741 .ends	PM_INV4F_GND 1 6 18 20 21 30 c10 30 0 0.00364991f c11 21 0 0.0217095f c12 20 0 0.00954274f c13 6 0 0.0459004f r14 21 30 135 r15 20 21 2 r16 20 21 0.375 r17 18 20 2.85185 r18 14 18 4.48148 r19 14 30 2 r20 6 30 78.1101 r21 4 21 66.4583 r22 1 4 5.55556 .ends	PM_INV5F_GND 1 6 18 20 21 30 c9 30 0 0.00516145f c10 21 0 0.0216892f c11 20 0 0.00955738f c12 6 0 0.0459004f r13 21 30 135 r14 20 21 2 r15 20 21 0.375 r16 18 20 2.85185 r17 14 18 4.48148 r18 14 30 2 r19 6 30 101.414 r20 4 21 78.1101 r21 1 4 4.44444 .ends
.subckt	.subckt	.subckt	.subckt	.subckt
PM_INV1F_VDD 1 4 6 18 20 33 c13 33 0 0.0216828f c14 20 0 0.00973093f c15 6 0 0.0939485f c16 4 0 9.4283e-19 r17 30 33 135 r18 20 33 0.375 r19 20 33 2 r20 18 20 1.42593 r21 14 18 5.90741 r22 14 30 2 r23 6 30 54.375 r24 4 33 31.0714 r25 1 4 22.2222 .ends	PM_INV2F_VDD 1 4 6 18 20 33 c13 33 0 0.0216828f c14 20 0 0.00972803f c15 6 0 0.0940486f c16 4 0 0.00103752f r17 30 33 135 r18 20 33 0.375 r19 20 33 2 r20 18 20 1.42593 r21 14 18 5.90741 r22 14 30 2 r23 6 30 54.375 r24 4 33 42.7232 r25 1 4 11.1111 .ends	PM_INV3F_VDD 1 4 6 18 20 33 c13 33 0 0.0216828f c14 20 0 0.0096946f c15 6 0 0.0938967f c16 4 0 0.00108697f r17 30 33 135 r18 20 33 0.375 r19 20 33 2 r20 18 20 1.42593 r21 14 18 5.90741 r22 14 30 2 r23 6 30 54.375 r24 4 33 54.375 r25 1 4 7.40741 .ends	PM_INV4F_VDD 1 4 6 18 20 33 c12 33 0 0.0215991f c13 20 0 0.00954274f c14 6 0 0.0954508f c15 4 0 0.00111196f r16 30 33 135 r17 20 33 0.375 r18 20 33 2 r19 18 20 1.42593 r20 14 18 5.90741 r21 14 30 2 r22 6 30 77.6786 r23 4 33 66.0268 r24 1 4 5.55556 .ends	PM_INV5F_VDD 1 4 6 18 20 33 c11 33 0 0.0205975f c12 20 0 0.00955738f c13 6 0 0.0969623f c14 4 0 0.00109169f r15 30 33 135 r16 20 33 0.375 r17 20 33 2 r18 18 20 1.42593 r19 14 18 5.90741 r20 14 30 2 r21 6 30 100.982 r22 4 33 77.6786 r23 1 4 4.44444 .ends
.subckt PM_INV1F_IN 2 5 7 10 c11 10 0 7.73955e-19 c12 5 0 1.61129e-19 c13 2 0 0.0633249f r14 5 10 1 r15 5 7 354.044 r16 2 5 354.044 .ends	.subckt PM_INV2F_IN 2 5 7 10 c11 10 0 7.73955e-19 c12 5 0 1.61129e-19 c13 2 0 0.0633249f r14 5 10 1 r15 5 7 303.467 r16 2 5 303.467 .ends	.subckt PM_INV3F_IN 2 5 7 10 c11 10 0 7.73955e-19 c12 5 0 1.61129e-19 c13 2 0 0.0633249f r14 5 10 1 r15 5 7 252.889 r16 2 5 252.889 .ends	.subckt PM_INV4F_IN 2 5 7 10 c9 10 0 6.00013e-19 c10 5 0 7.20852e-23 c11 2 0 0.0574293f r12 5 10 1 r13 5 7 304.919 r14 2 5 304.919 .ends	.subckt PM_INV5F_IN 2 5 7 10 c7 10 0 9.64561e-19 c8 5 0 7.20852e-23 c9 2 0 0.0519474f r10 5 10 1 r11 5 7 356.303 r12 2 5 356.303 .ends
.subckt	.subckt	.subckt	.subckt	.subckt
PM_INV1F_OUT 1 4 6 9 14 15 21 28 c12 28 0 0.0011218f c13 21 0 0.0011218f c14 15 0 0.010793f c15 9 0 1.41975e-19 c16 4 0 1.41975e-19 r17 28 29 0.611111 r18 25 29 1.22222 r19 21 22 0.611111 r20 18 22 1.22222 r21 14 16 0.950617 r22 14 15 0.950617 r23 12 28 0.0734257 r24 12 16 5.16049 r25 11 21 0.0734257 r26 11 15 5.16049 r27 9 25 1 r28 6 9 22.2222 r29 4 18 1 r30 1 4 22.2222 .ends	PM_INV2F_OUT 1 4 6 9 14 15 21 28 c12 28 0 0.00107309f c13 21 0 0.00107309f c14 15 0 0.00937769f c15 9 0 2.79298e-19 c16 4 0 2.79298e-19 r17 28 29 0.611111 r18 25 29 1.22222 r19 21 22 0.611111 r20 18 22 1.22222 r21 14 16 0.950617 r22 14 15 0.950617 r23 12 28 0.0734257 r24 12 16 5.16049 r25 11 21 0.0734257 r26 11 15 5.16049 r27 9 25 1 r28 6 9 11.1111 r29 4 18 1 r30 1 4 11.1111 .ends	PM_INV3F_OUT 1 4 6 9 14 15 19 21 28 c13 28 0 0.001036f c14 21 0 0.001036f c15 19 0 1.64602e-19 c16 15 0 0.00796233f c17 9 0 1.64602e-19 r18 28 29 0.611111 r19 25 29 1.22222 r20 21 22 0.611111 r21 18 22 1.22222 r22 18 19 1 r23 14 16 0.950617 r24 14 15 0.950617 r25 12 28 0.0734257 r26 11 21 0.0734257 r27 11 21 5.16049 r28 11 15 5.16049 r29 9 25 1 r30 6 9 7.40741 r31 4 19 27.1875 r32 1 4 7.40741 .ends	PM_INV4F_OUT 1 4 6 9 14 15 19 21 28 c13 28 0 0.00119423f c14 21 0 0.00119423f c15 19 0 2.01812e-19 c16 15 0 0.0125505f c17 9 0 2.01812e-19 r18 28 29 0.611111 r19 25 29 1.22222 r20 21 22 0.611111 r21 18 22 1.22222 r22 18 19 1 r23 14 16 0.950617 r24 14 15 0.950617 r25 12 28 0.0734257 r26 11 21 0.0734257 r27 11 21 5.16049 r28 11 15 5.16049 r29 9 25 1 r30 6 9 5.55556 r31 4 19 38.8393 r32 1 4 5.55556 .ends	PM_INV5F_OUT 1 4 6 9 14 15 19 21 28 c13 28 0 0.00115276f c14 21 0 0.00115276f c15 19 0 2.39047e-19 c16 15 0 0.0125505f c17 9 0 2.39047e-19 r18 28 29 0.611111 r19 25 29 1.22222 r20 21 22 0.611111 r21 21 22 1.22222 r22 18 22 1.22222 r23 18 19 1 r24 14 16 0.950617 r25 14 15 0.950617 r26 12 28 0.0734257 r27 12 16 8.82716 r28 11 21 0.0734257 r29 11 15 8.82716 r30 9 26 50.4911 r31 6 9 4.44444 r32 4 19 50.4911 r33 1 4 4.44444 .ends

Source: From the author.