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LEONARDO BARLETTE MORAES

Schmitt Trigger Dimensioning Under Variability and Voltage Scaling for Minimum Energy Operation.

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Advisor: Prof. Dr. Ricardo Reis
Coadvisor: Profa. Dra. Cristina Meinhardt

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CONTENTS

LIST OF ABBREVIATIONS AND ACRONYMS

IoT	Internet of Things
CMOS	Complementary Metal Oxide Semiconductor
ULP	Ultra Low Power
FinFET	Fin Field Effect Transistor
SCE	Short Channel Effect
RDF	Random Dopant Fluctuation
ST	Schmitt Trigger
FA	Full Adder
V_T	Threshold Voltage
NBTI	Negative Bias Temperature Instability
HCI	Hot Carrier Injection
CMP	Chemical-Mechanical Polishing
LER	Line-Edge Roughness
WF	Work Function
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PVT	Process Voltage and Temperature
WID	Within-Die
SIMD	Single Instruction Multiple Data
PDP	Power Delay Product
TGA	Transmission Gate Adder
TFA	Transmission Function Adder
CPL	Complementary Pass Transistor Logic
CNFET	Carbon Nanotube Field Effect Transistor

FDSOI	Fully Depleted Silicon On Insulator
OTS	Optimal Transistor Sizing
L	Gate Length
W_{FIN}	Fin Width
H_{FIN}	Fin Height
T_{OX}	Oxide Thickness
SOI	Silicon On Insulator
WFF	Work Function Fluctuation
SRAM	Static Random Access Memory
GOBD	Gate Oxide Break Down
ECC	Error Correcting Code
SNM	Static Noise Margin
UDSM	Ultra-Deep Sub-Micron
VTC	Voltage Transfer Curve
DRC	Design Rule Checking
LVS	Layout Versus Schematic
EDA	Electronic Design Automation
PDK	Process Design Kit
ASAP	Arizona State Predictive PDK
FEOL	Front End Of Line
MOL	Middle End Of Line
BEOL	Back End Of Line
SDT	Source-Drain Trench
LIG	Local-Interconnect Gate
LISD	Local-Interconnect Source-Drain
V0	Via 0

M1	Metal 1
M2	Metal 2
MC	Monte Carlo
EDP	Energy Deviation Product
TIST	Triple-Inverter ST
SIG	Stacked-Inverter Gate

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ABSTRACT

The emergence of IoT alongside with the increased process variability impact in modern technology nodes, is the main reason to control variability impact over metrics. Given the large set of IoT devices working in battery-oriented environments, energy consumption should be minimal and the operation regime reliable. Schmitt Trigger inverters are traditionally used for noise immunity enhancement, and have been recently applied to mitigate radiation effects and process variability impact. However, Schmitt Trigger operation at the nominal voltage introduces high degradation on power consumption. Thus, this work main contribution is to identification of the relationship between transistor sizing, supply voltage, energy, and process variability robustness to get a minimal energy consumption circuit while keeping robustness. The results are extracted from 7-nm FinFET Schmitt Trigger layouts under different levels of process variability, supply voltages, and sizing. Also, a maximum frequency scaling under a failure threshold was performed. On average, the supply voltage decreases in layouts with a smaller number of fins, while maintaining acceptable robustness in high variability scenarios. Exploring voltage and transistor sizing made possible a reduction of about 24.84% of power consumption.

Keywords: Formatação eletrônica de documentos. LaTeX. ABNT. UFRGS.

Dimensionamento de Schmitt Trigger Sob Influência de Variabilidade e Escalonamento da Tensão de Alimentação para Operação com Consumo Mínimo de Energia

RESUMO

Palavras-chave: O surgimento da Internet das Coisas juntamente com o aumento do impacto da variabilidade de processo nos nós modernos de tecnologia é o principal motivo para controlar o impacto da variabilidade sobre as métricas. Dado o grande conjunto de dispositivos envolvidos na Internet das Coisas que funcionam em ambientes orientados para baterias, o consumo de energia dever ser o mínimo possível e o regime de operação confiável. Os inversores Schmitt Trigger na tensão nominal introduzem uma alta degradação no consumo de energia. Assim, a principal contribuição deste trabalho é a identificação da relação entre o dimensionamento do transistor, a tensão de alimentação, a energia e a robustez à variabilidade de processo para obter um circuito com consumo mínimo de energia, mantendo a robustez. Os resultados são extraídos de leiautes FinFET Schmitt Trigger de 7-nm sob diferentes níveis de variabilidade de processo, tensões de alimentação e dimensionamento. Além disso, foi executada uma calibração da frequência máxima sob um limiar de falha. Em média, a tensão de alimentação diminui em leiautes com um número menor de fins, mantendo robustez aceitável em cenários de alta variabilidade. A exploração da calibragem da tensão de alimentação e dimensionamento do transistor possibilitou uma redução de até 24.84% do consumo de energia. .

1 INTRODUCTION

The Internet of Things (IoT) has emerged to be one of the major mainstream trends, shaping technology development and the industry. The IoT concept englobes the shift from an internet which used to interconnect end-user devices to, nowadays, interconnect physical objects that communicate with each other and/or with humans (MIORANDI et al., 2012). The IoT rise alongside battery technology improvements has provided us with portable, powerful and useful equipment for our daily routine, with wireless communication making information available anytime and anywhere (MANOLI, 2010).

IoT devices have been applied in many different scenarios, from improving building maintenance, to sensoring remote areas for environmental observation and even in cars, for better safety and comfort. However, while many devices have to be connected to the power grid, sensor nodes are expected to be self-sufficient. Additionally, batteries, the traditional means of powering self-sufficient systems, need to be replaced and/or charged, which means maintenance must be frequently performed (BLEITNER et al., 2018). Given that, energy harvesting in combination with rechargeable batteries has become a viable way to alleviate the power source and consumption dilemma (MANOLI, 2010).

Energy harvesting makes use of readily available power sources in the vicinity as for example motion or vibration induced kinetic energy, solar and electromagnetic or temperature gradients. A number of viable solutions are already present on the market, like self powered wireless light switches and electro-magnetic generators, which converts vibrations available in industrial plants for powering wireless monitoring sensors (MANOLI, 2010) (BLEITNER et al., 2018). Although, regardless of the sensors power supply, it will be always restricted by its power budget, with devices which are able to perform their functionality under heavy power constraints being essential for IoT. In traditional Complementary Metal Oxide Semiconductor (CMOS) circuit design aimed at Ultra Low Power (ULP) applications, the ideal circuit is the one that performs a given task or functionality while consuming the least amount of energy. Such circuits are achieved under transistor sizing and supply voltage tuning, and are technology and application-dependent.

Nevertheless, the performance of a system operating in its minimum energy per operation point may exceed the power budget of a given application. For example, with an application such as presented in (FOJTIK et al., 2013), where the device is only active

once per hour, with 80% of its power consumption being due to standby power. In such a case, the minimization of energy-per-operation seems to be suboptimal in comparison to a idle power minimization kind-of solution. The minimization of supply voltage brings advantage for certain energy harvesting approaches such as thermo-electric. Such harvesting technique can result in DC voltage levels from tens to even hundreds of milivolts (KHAN; DAHIYA; LORENZELLI, 2014).

Technology scaling is a major factor in the ascendance of IoT, providing higher transistor densities and voltage scaling due to the miniaturization of gate dimensions, internal capacitances and resistances. These two parallel events contributed for the emergence of IoT (ISLAM et al., 2010). Alongside, with the advance of transistor technology, new challenges were introduced due to the scale down, as aging effects, high power consumption due to leakage current and an increase in the sensibility to transient faults due to radiation and variability (ABBAS et al., 2015).

The Fin Field Effect Transistor (FinFET) transistor technology has been adopted to overcome those challenges. FinFET devices present superior channel control due to the reduced Short Channel Effects (SCE) and low (if none) Random Dopant Fluctuation (RDF) effect due to the fully depleted channel (FARKHANI et al., 2014). Although, at deep technology nodes, variability is one of the most challenging factors, including on FinFET devices. Variability introduces behavior changing geometrical inconsistencies to the final manufactured product. Such variations influence the circuits metrics, hastening its degradation and deviating from its correct operation regime (ABBAS et al., 2015) (NASSIF, 2008).

Given the energy constraints of IoT applications and the variability impact on recent nodes, the Schmitt Trigger (ST) circuit has been pointed as an alternative. The classical ST has been employed as a key element for several ULP circuits (KULKARNI; KIM; ROY, 2007; HAYS, 2012; MELEK et al., 2017; LOTZE; MANOLI, 2017) and for variability mitigation, mainly attenuating the deviation on the power consumption. ST was applied replacing internal inverters of full adders (FAs) in (DOKANIA; ISLAM, 2015) where spreads in major metrics were successfully limited. Also, the same experiment was executed at electrical and layout levels considering FinFET technology, and showed a considerable decrease in overall variability impact on metrics (TOLEDO et al., 2018; MORAES et al., 2018). However, with a considerable increase in delay and power consumption. This work also evaluates two other circuits, the Stacked Inverter Gate (SIG) (BOSE; JOHNSTON, 2018) and Triple Inverter Schmitt Trigger (TI-ST) (LUO et al.,

2017).

This work is divided into five further sections: FinFET Technology, where its characteristics and major variability impact are explained, Variability Effects will show a theoretical foundation about variability. A section about the considered circuits will explain their functionality and applications. Objectives section, will lay the main objectives based on the beforehand laid concepts. The Methodology section will explain the experimental setup which will be employed to generate the results. A Results section is present, showing some preliminary results and analysis. Lastly, there are a Conclusions and Future Works sections.

2 VARIABILITY EFFECTS AND MITIGATION TECHNIQUES

As process technology scaling advanced, decreasing the transistor dimensions, the ratio between device size and atom-size have been decreasing as well. Multiple techniques have been developed to reduce the loss of precision due to the manufacturing process at different end-of-lines. However, as the quantum-mechanical limit approaches, manufacturing-induced imprecision impact rises (ASENOV, 1999).

Variability consists of characteristic deviations, internal or external to the circuit, which can determine its operational features and can be divided by three types concerning its sources:

Environmental Factors or use-induced variation is mostly external to the circuit, it englobes variations in the power supply voltage and temperature. Voltage drops mainly occur due to abrupt changes in the switching activity, inducing large current transients in the system both locally or globally across the due. Local temperature within the die can cause variations in the device mobility and threshold voltages (V_T), and wire resistance. It is highly design dependent with timing constants similar to clock frequency (NASSIF, 2008) (BERNSTEIN et al., 2006).

Reliability Factors are related to the aging process of the circuit. Circuit aging is defined by numerous phenomena: Negative Bias Temperature Instability (NBTI) which mines the performance of p-channel due to the weakening of Si-H bonds in the oxide generating of interface states and trapping positive charges while the device is operating (WANG et al., 2008), electromigration due to high enough current densities causing the gradual movement of metal ions due to the electron-ion momentum transfer (YOUNG; CHRISTOU, 1994), time dependent dielectric breakdown due to current flowing through gate oxides (LOMBARDO et al., 2005) and Hot Carrier Injection (HCI) trapping electrons on oxide which degrades n-MOSFET on-current (TAKEDA; SUZUKI, 1983) (NASSIF, 2008) (BERNSTEIN et al., 2006).

Physical Factors are caused by the manufacturing process, consequence of imprecisions in the manufacturing process, resulting in characteristic deviations of active and passive components. Those variations can be:

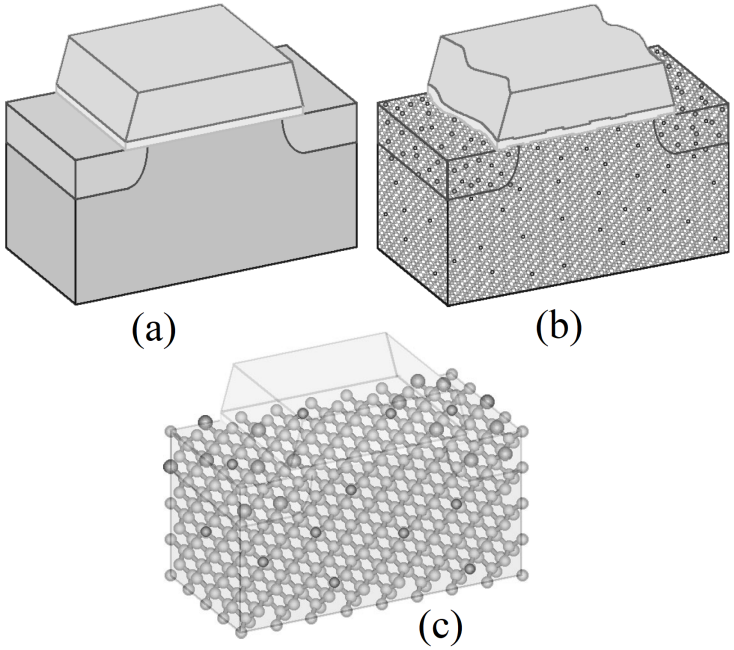
- Systematic or extrinsic: is related to unintentional imprecisions in the manufacturing process, not associated with fundamental atom-related problems. Extrinsic variability can present itself in multiple ways, from different lots, from different wafers within a lot, across wafers and even from chip to chip. The main contrib-

utor for extrinsic variation is the chip to chip variability, with its sources being both by-wafer and by-reticle process steps. By-wafer variability is caused by three manufacturing steps: rapid thermal anneal - with a uneven temperature distribution across the wafer, photoresist development and etching and by-reticle variability can contribute due to changes in the focus as the mask is stepped across the wafer in the photolithography process. The focus can suffer deviations due to exposure tool lens astigmatisms or by wafer nonplanarity. Additionally, the within-chip variability can be divided into two types. The similar-structure variability, consists of across-wafer and across-reticle variations that each chip ends up intercepting, and the dissimilar-structure which consists of variations caused by processing steps that differ by structure and layout variations of structure (difference of orientation for the same structures in the layout as well as variations in polygon densities) (BERNSTEIN et al., 2006).

- Design dependent: variations related to the placement can results in changes in the electrical parameters of active and passive devices. The sources of such type of variability include manufacturing related deviations. Manufacturing variability may be systematic, having a well-known relationship between design or layout and the final electrical parameters values. Chemical-Mechanical Polishing (CMP) relationship between the thickness of the metal and the layout feature density (STINE; BONING; CHUNG, 1997). The main difference between systematic and random variability is the way it is treated at design time. Systematic variability can be modeled and anticipated, allowing the designer to tune the layout or timing for mitigation. Random variations, however, require the designer to add time margins in order to guard against the worst timing possible (NASSIF, 1998).
- Random or intrinsic: consists of atomic-level deviations between devices (even when they are identical in layout and geometry). These deviations appear in dopant profiles, thickness variations, and Line-Edge Roughness (LER). Dopant fluctuations are the main cause to V_T variations (ASENOV et al., 2003), with the removal of doping from the channel contributing for the V_T variation reduction, introducing the necessity to set the V_T by gate-metal Work Function (WF) or by biased back gate (FRANK et al., 2001; WONG et al., 1999). Fluctuations in doping levels and device features cause variations in the source/drain regions, which affects the overlap capacitance and the source resistance (FRANK; WONG, 2000). LER arises from variations in the total number of incident photons during lithography. Such

roughness introduction into the polygons geometry may determine the effective gate width as one moves along the x axis of a Field Effect Transistor (FET) (BRUNNER, 2003). Another source of intrinsic device variability rises from the atomic-scale oxide thickness variation. It can introduce variations in the V_T (ASENOV et al., 2003), in the oxide tunneling current, and may cause mobility degradation due to the potential variation across the Metal Oxide Semiconductor FET (MOSFET) channel (BERNSTEIN et al., 2006). Fig. 2.1, depicts the transistor intrinsic variability.

Figure 2.1: Levels of abstraction from a ideal transistor concept towards a realistic and "atomistic" device concept. (a) Depicts a the current approach of semiconductor device simulation, with continuous dopant charge and smooth boundaries. (b) Depicts a 20-nm MOSFET, with less than 50 Si atoms along the channel. RDF, interface roughness and LER introduce considerable intrinsic parameter fluctuation. (c) Depicts a 4-nm MOSFET, with less than 10 Si atoms along the channel.



Source: Asenov et al. (2003)

Table 2.1: Impact of variability on performance and power.

Property	**Ease of measuring**	**Variability**	**Effects of variability**	**Effect of missing specification**
Performance	Medium	Medium: up to 60%	L, W, R, C, V_T, μ	Slower product, yield, timing error
Leakage Power	Easy	Large: up to 148%	L, V_T, μ, t_{ox}	Shorter battery life, yield, heat
Dynamic Power	Difficult	Workload dependent	C, α	Shorter battery life, heat

Source: Rahimi, Benini and Gupta (2016)

Table 2.1 illustrates the variations impact on performance and power. As a way to handle timing errors due to variations in the path delay, circuit designers commonly

add safety timing margins to the voltage and/or the clock frequency (guardband). Such practice leads to overly conservative designs due to the guardband overlapping and accumulation in the ever increasing multi-corner analysis (AUSTIN et al., 2005).

In (JEONG; KAHNG; SAMADI, 2009) the impact of each individual variability source: Process, Voltage and Temperature (PVT) is quantified concerning a standard inverter cell through SPICE simulations. A 1.8x delay variations was observed, with 1.46x, 1.25x and 0.97x coming from the process, voltage and temperature variations, respectively. Under the same operation conditions smaller supply voltages for a 80-core Intel processor, it was observed a normalized deviation of 5.93%, 6.37% and 8.64% for 1.2 (nominal), 0.9, and 0.8V, respectively. The lowering from 1.2 to 0.8V increases the critical path variability up to 45% (DIGHE et al., 2011).

Near-threshold operation has become a popular technique to achieve energy-efficient digital circuits. Although, operating at low voltages exacerbates the effects of delay variations (JEON et al., 2012; DRESLINSKI et al., 2010; RITHE et al., 2011; KAKOEE; LOI; BENINI, 2012; PAWLOWSKI et al., 2012). The measurement of Within-Die (WID) delay was performed for a 45nm Single Instruction Multiple Data (SIMD) processor, showing that reducing V_{DD} from 1.0 to 0.53 V increases delay variation by 6x (PAWLOWSKI et al., 2012).

Given the increase in performance variation, there is the need for mitigation methods to make the design resilient to timing errors, especially for circuits at low voltage operation regimes. There are several approaches to how and when errors should be manipulated as well as their abstraction levels. Among the steps there are: Predicting and Preventing, Detecting and Correcting, and Accepting. And among the abstraction levels there are Application Algorithm, Software, Architecture and Circuit. Since this work aims to investigate variability impact at layout level, some circuit-level techniques will explained next with higher level techniques being thoroughly explained at (RAHIMI; BENINI; GUPTA, 2016).

Tuning CMOS knobs consists of several approaches to tune electrical characteristics (e.g., power and delay) of circuit by interfering with the body bias supply voltage and clock frequency, for example. Forward body biasing reduces the V_T (improving performance and increasing leakage power) while reverse body bias increases the V_T (reducing performance and leakage power). Given so, a slow circuit block can have its performance improved upon forward body biasing while a leaky circuit can be reverse body biased. Additionally, voltage and/or the circuit's frequency can be tuned to compensate variations

(DIGHE et al., 2011; TSCHANZ et al., 2002; BORKAR et al., 2004).

There are topology changes employed during design time CAD optimizations in order to enhance the circuit resiliency against timing errors. Due to the general presence of clusters of critical paths in circuits some approaches focus on uncertainty-aware circuit optimizations (BAI; VISWESWARIAH; STRENSKI, 2002). Optimization such as upsizing and downsizing of gates, use of multiple V_T cells, and restructuration of the path delay distribution (KAHNG et al., 2010).

Lastly, asynchronous circuits have been proposed since there is no need for a clock signal to determine a starting time for computation. In (CHANG et al., 2013) both versions (synchronous and asynchronous) of 8051 microcontroller are designed. When PVT and workload variations are introduced, the synchronous version required 4x, 1.5x, and 2x delay margins while the asynchronous version operated at nominal performance.

In order to mitigate variability impact, many works try to indicate the most robust design for a given type of circuit. For example, in (DOKANIA; IMRAN; ISLAM, 2013) twelve different FA topologies are analyzed considering delay, power and Power-Delay-Product (PDP) variability. It is used a 16nm bulk CMOS technology node in SPICE simulations with PVT variability being considered and Monte Carlo simulations performed. The authors concluded that Cell A, CLRCL and Cell B FAs presented the best results for all three metrics (Delay, Power and PDP).

In (AMES et al., 2016) the effects of PVT variability in different FA designs are investigated. The simulations are performed in HSPICE with the bulk CMOS 32nm node technology. With Transmission Gate Adder (TGA) and Transmission Function Adder (TFA) architectures showing acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested FAs - 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) FA.

In (ISLAM; HASAN, 2011) various popular 1-bit digital summing circuits functionality and robustness are analyzed in light of PVT variations with the best FA being simulated in Carbon Nanotube Field Effect Transistor (CNFET) technology for comparison with the bulk CMOS version. The simulations are carried at the 22nm bulk CMOS and CNFET technology node in HSPICE. Its results show that the TGA has the strongest PVT variability robustness and its CNFET version provides over 3x, 1.14x and 1.1x less propagation delay, power dissipation and energy delay product (EDP) variations, respectively. This work does not consider the total power consumption of each FA separately.

Some articles analyze the adoption of new technologies: (GUDURI; ISLAM,

2015) proposes a hybrid of bulk CMOS and CNFET FA at 16nm in deep subthreshold operation region for ULP applications simulated in SPICE which showed some improvement over its bulk CMOS FA counterpart achieving 5% and 1% improvement in power, power-delay and energy-delay products and their variability, respectively. In (ISLAM; AKRAM; HASAN, 2011) a new subthreshold-FinFET FA is proposed and compared over multiple FAs showing huge metric improvements provided by the FinFET technology up to 2.22x improvement in power variability. It was simulated in 32nm predictive technology model on HSPICE.

It is notable that none of these works consider a layout approach for its simulations and do not address any novel general technique which can be applied to a range of different types of circuits. Although, some works introduce novel designs.

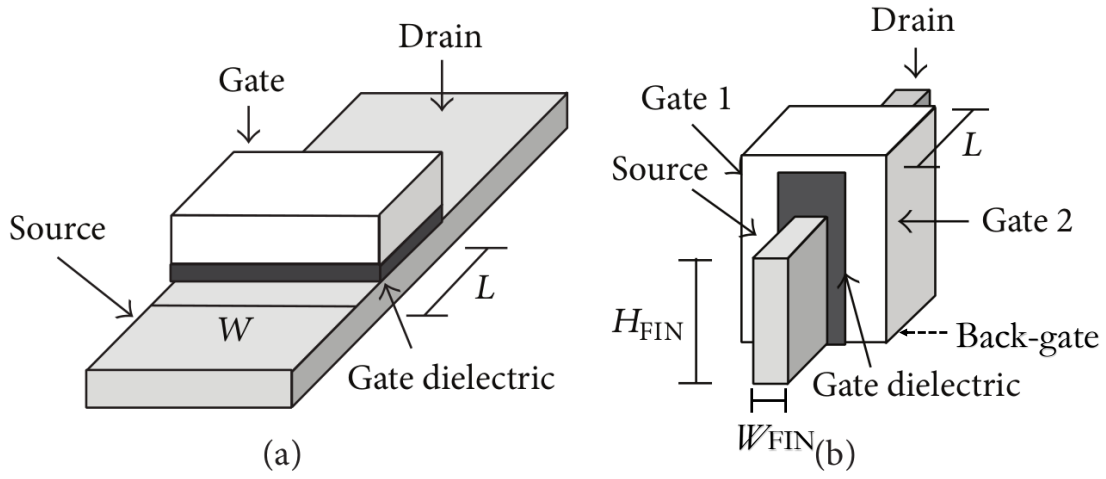
(FEDERSPIEL et al., 2012) presents reliability comparison between 28nm bulk CMOS and Fully Depleted Silicon On Insulator (FDSOI) technologies at layout level, with FDSOI showing 32% improved performance, 40% reduced power consumption and improved matching, with its intrinsic reliability behavior similar to 28nm bulk at the device level. (ALIOTO; PALUMBO, 2007) presents a study about the delay variability caused by supply variations in the TGA. The experiments were performed at 90nm and 180nm bulk CMOS Technology in Spectre at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TGA presenting worse results 15% (25%) for the 90 nm (180 nm) in comparison to static logic.

Some works focus on evaluating techniques: In (ZIMPECK et al., 2016) three transistor sizing techniques are applied on a set of cells and their impact on variability robustness is analyzed. The simulations were performed considering a 14nm FinFET technology using HSPICE tool. The authors concluded that the Optimized Transistor Sizing (OTS) technique has the best ratio between nominal PDP and PDP under process variability. (AHMADI; ALIZADEH; FOROUZANDEH, 2017) introduces a new technique to improve the performance of digital circuits in the presence of variations. It consists of a hybrid of two former methods to prevent errors due to delay variations. The simulations were performed with a 45nm predictive technology using HSPICE and applied on ITC'99 and ISCAS'89 benchmarks circuits. The results show that the hybrid technique can tolerate process variations up to 27.3% better than previous state-of-the-art techniques.

3 FINFET TECHNOLOGY AND VARIABILITY IMPACT

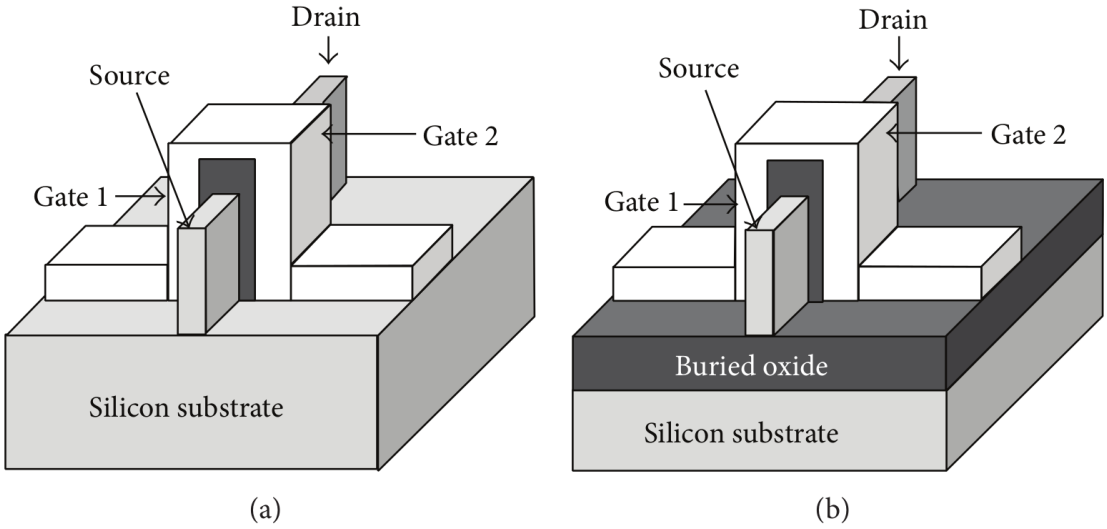
New commercial technologies have been developed for mitigation of variability impact. The Fin Field Effect Transistor (FinFET) remains as one promising new technology for variability mitigation while maintaining technology scaling. The FinFET main geometric parameters are the gate length (L or L_G), fin width (W_{FIN}, T_{FIN} or T_{SI}), fin height (H_{FIN}) and Oxide Thickness (T_{OX}). FinFET transistors can be built on a traditional bulk or on a Silicon on Insulator (SOI) substrate with a conducting channel that rises above the level of the insulator, creating a thin silicon structure, the gate, as shown in Figures 3.1 and 3.2. FinFET devices can be shorted-gate (3 gate nodes) or independent-gate (4 gate nodes). The shorted gate model is similar to the traditional MOSFET given that the front-gate and back-gate are connected and controlled by the gate signal. The independent gate has 4 nodes, making possible to connect the front and back gate to different voltage values.

Figure 3.1: Structural comparison between (a) planar MOSFET and (b) FinFET transistors.



Source: Bhattacharya and Jha (2014)

Figure 3.2: Structural comparison between (a) bulk and (b) SOI FinFETs.



Source: Bhattacharya and Jha (2014)

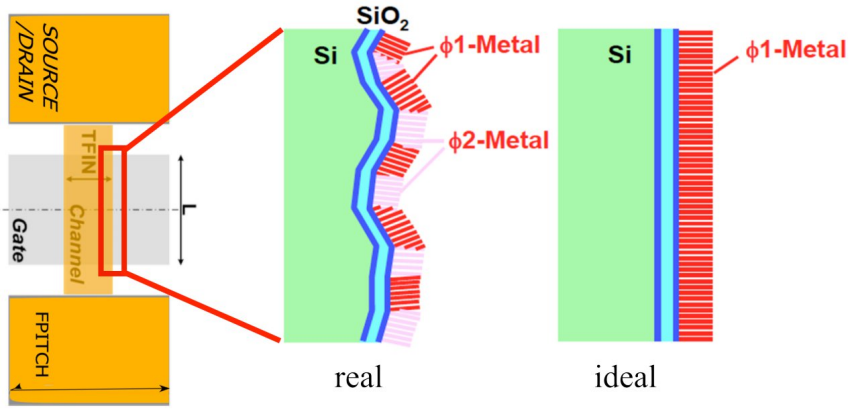
The channel being surrounded from three dimensions by the gate results in a superior control, reduced SCE and RDF effect due to the fully depleted channel that causes less sensitivity to process variations (TAUR; NING, 2013). FinFETs also present relative immunity to gate LER, a major source of variability in planar nanoscale FETs (KING, 2005). The disadvantage over MOSFETs is the harder manufacturing process due to difficulty in the lithography steps as it is increasingly difficult to print small patterns, the increased variability impact due to the further miniaturization of dimensions, in comparison to MOSFET and a more costly manufacturing process due to the need of techniques to address the manufacturing imprecision and, in the case of SOI FinFET, to change the CMOS substrate process to support a SOI substrate manufacturing process (KING, 2005) (MANOJ et al., 2007).

Given the elevated levels of gate leakage due to the scaling down of the gate oxide, insulating materials with higher dielectric constant (high-k) have been introduced. Although, with the high-k dielectric adoption, challenges such as Fermi level pinning (HOBBS et al., 2004) and phonon scattering (GUSEV; NARAYANAN; FRANK, 2006) rised, being necessary the replacement of the traditional polysilicon gate electrode by a metal gate electrode (GUSEV et al., 2001; DATTA et al., 2003).

Metals exist *in natura* in the form of crystals where each atom has several bonds with adjacent atoms. Although, due to defects and disorientations, several crystals are formed, with "grain boundaries" between regions of regularity (crystal grains) in the metal (DADGOUR; DE; BANERJEE, 2008), as shown in Fig. 3.3. The electrostatic potential

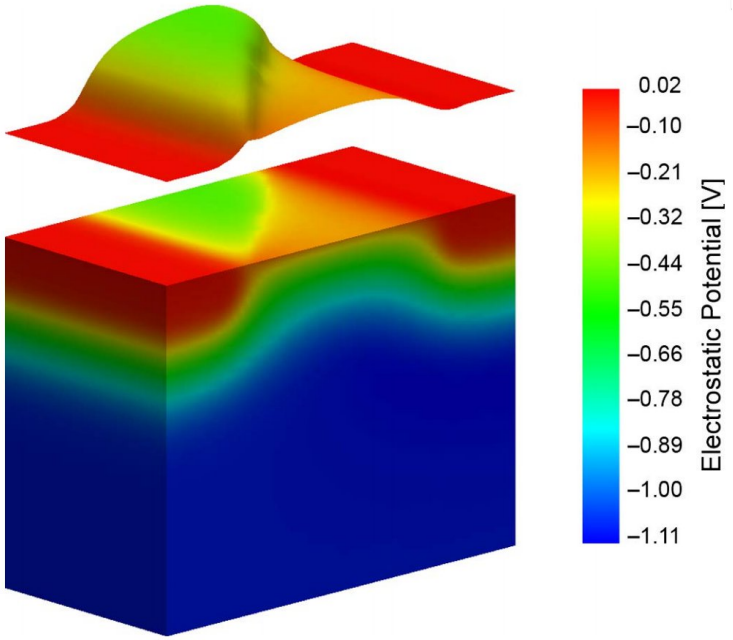
(e.g. V_T) varies depending on each grain boundary, as shown in Fig. 3.4. At Table 3.1 a example of possible orientation, probability and WF is given. Between several technology nodes - FD-SOI, Bulk and FinFET - the latter showed the lowest V_T variation due to the much larger gate area (DADGOUR; DE; BANERJEE, 2008).

Figure 3.3: Metal fabrication ideal and real aspects.



Source: Meinhardt, Zimpeck and Reis (2014)

Figure 3.4: Electrostatic potential in a generic 30-nm MOSFET with the surface potential shown below. The metal gate has two grains with the grain boundary diagonally across the channel.



Source: Brown et al. (2010)

Table 3.1

Orientation	Probability	Work Function
<200>	60%	4.6 eV
<111>	40%	4.4 eV

Source: Brown et al. (2010)

Several works analyze the FinFET reliability. It is shown in (MEINHARDT; ZIMPECK; REIS, 2014) the major influence that WF Fluctuations (WFF) exercise over V_T variations of several standard cells. In addition, in (WANG et al., 2011) it was shown the high correlation between the I_{ON} and I_{OFF} currents and V_T fluctuations due to the granularity of the metal gate.

In (HARRINGTON et al., 2018) it is shown, at 14/16nm fabricated bulk FinFET technology, that for high energy charged particles, the drive current is the dominant factor to the transient fault pulse width and cross-section. And low energy particles have a grater dependence on secondary transistor and circuit design factors (number of fins, transistor arrangement, etc).

In (REN et al., 2018) the HCI effect is analyzed in pass-gate FinFET transistors. The tests were executed using commercial FinFET technology showing a 50% chance of errors due to HCI in pass-gate transistors. In (XIONG; BOKOR, 2003) a analysis of the sensitivity of double-gate and FinFET devices to process variations is shown. It is concluded that for 20nm FinFET devices large channel doping concentration is necessary to obtain suitable values of V_T if heavily doped polysilicon gates are used. Due to the small volume of the channel the channel doping will bring unacceptable V_T fluctuations. Given that, heavily doped polysilicon may not be a viable choice with the work function adjustment being a better approach.

In (ZHANG et al., 2017) the modeling of the reliability degradation of a FinFET-based Static Random Access Memory (SRAM) is shown. It is concluded that the probability of failure due to NBTI and Gate Oxide Break Down (GOBD) is relatively lower in comparison to HCI-induced failures. They also shown the improvement of lifetime due to Error-Correcting Code (ECC) memory. In (LIAO et al., 2008) a investigation on reliability characteristics of NMOS and PMOS FinFETs is conducted. Based on fabricated FinFETs transistor with 17-27 nm width, it was shown that the life time of FinFET is very dependable of its dimensions. The predicted lifetime for a 50nm gate length NMOS FinFET was 133 years, for the first HCI event. While a 27nm fin-width PMOS FinFET

showed 26.84 years of lifetime wich is reduced to 2.76 years when reducing its fin-width from 27 to 17 nm for a NBTI event, showing the huge reliability challenge introduced by technology scaling.

4 SCHMITT TRIGGER

STs circuits present a hysteresis characteristic. This hysteresis exists in the presence of two switching V_T. If the input level is within the hysteresis region, the ST shall not switch. Such characteristic gives a higher static noise margin (SNM) in comparison to traditional inverters, ensuring a high noise immunity.

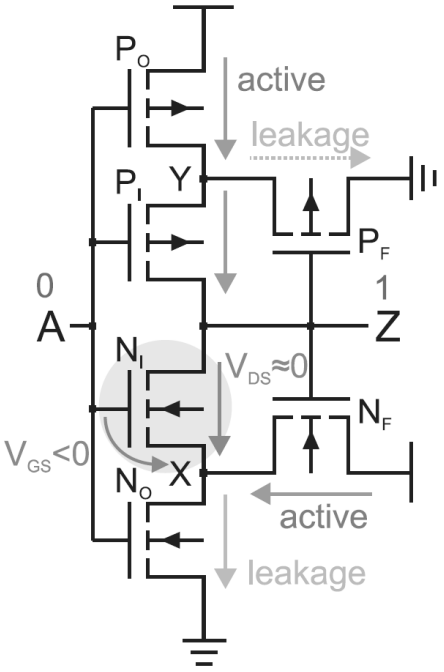
Variations in physical parameters became alarming at ultra-deep sub-micron (UDSM) nodes because the node scaling was accompanied by a supply voltage scaling, making the circuits more susceptible to noise and electromagnetic interference due to the deterioration in SNM (PAL; ISLAM, 2018). Given that, this work explores a set of STs.

4.1 6T Traditional ST

The first is the 6T traditional ST where the main difference from the most common versions is the presence of P_F and N_F devices as shown in Fig. 4.1 (DOKI, 1984). These transistors are responsible for a feedback system. For example, if the output is in a high level, the N_F is on, pulling the node X to a high potential, and forcing the drain-source voltage of transistor N_I almost zero and its gate-source voltage into the negative region. This kind of arrangement reduces the leakage current N_I exponentially, increasing the on-to-off current ratio, and minimizing the output degradation (LOTZE; MANOLI, 2017).

The main effect of process variability is a shift on the voltage transfer curve (VTC) due to the threshold voltage variation. Usually, the input voltage, where a device starts delivering current, is directly dependent on the V_T. Thus, the variability impact on VTC is reduced in the ST as a result of the high influence of the gate-source voltage of the inner transistor (N_I and P_I) over its switching point (LOTZE; MANOLI, 2017).

Figure 4.1: ST inverter leakage suppression (LOTZE; MANOLI, 2017).



A variety of CMOS STs have been proposed and implemented over the years based on different requirements. A higher performance ST is proposed in (STEYAERT; SANSEN, 1986) where, by a different design, a smaller load capacitor value is achieved, decreasing the slew rate of the ST internal node. In (PFISTER, 1992) a ST with a programmable hysteresis is proposed. The programmable hysteresis is achieved by adding a P and N transistors in series with the 6T ST P_F and N_F transistors, respectively, both receiving the same gate signal. (KIM; KIH; KIM, 1993) proposes a 10T ST which its hysteresis interval does not depend on transistors width/length ratios being, consequently, more robust to process variations.

A low-power ST is proposed at (AL-SARAWI, 2002) with low short circuit current achieved by the presence of only one path to each power rail, being recommended for low power, very low frequency applications. In (ZHANG; SRIVASTAVA; AJMERA, 2003) a low-power ST is proposed as well by forward body biasing, decreasing the V_T, improving performance and decreasing the short circuit current. Additionally, (PEDRONI, 2005) proposes a low-power ST by having only one transistor transmitting (at stable output values), considerably reducing power consumption. STs can be optimised by adequate dimensioning as well as stated in (TACHE et al., 2018) where the OTS technique presented the best metrics for low power applications, in accordance to (ZIMPECK et al., 2016).

In (DOKANIA; ISLAM, 2015) a novel technique based on the replacement of

FA's internal inverters with low voltage STs for PVT variability robustness improvement is originally introduced and applied on seven different FA designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in PDP. Although, the improvements occur at the cost of an increase in the area and power dissipation of each design.

Alongside, in (TOLEDO; ZIMPECK; MEINHARDT, 2016) the ST technique is applied on four FAs. It presented promising results regarding the power deviation due to the process variability with a decrease up to 79% with a drawback of a significant increase in average energy consumption. The simulations were performed with the 16nm technology predictive technology model in NGSPICE.

This technique is tested in several works: In (AHMAD et al., 2016) it is presented a novel Schmitt-trigger-based single-ended 11 Transistor SRAM cell. It analyses its performance against seven different SRAM topologies. The novel cell showed the least energy consumption per operation with the smallest leakage power and a 6.9x higher I_{ON}/I_{OFF} ratio. Further PVT variability simulations confirmed the robustness of the design regarding read and write operation. The simulations were carried in 22nm predictive technology using HSPICE. (MOGHADDAM; MOAIYERI; ESHGHI, 2017) presents a ST buffer using CNFET. It was evaluated against other two buffers and showed, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain considering PVT variability robustness. The simulations were carried in 16nm Stanford CNFET model using HSPICE.

In previous work (MORAES et al., 2018) the ST technique is evaluated considering 4 different FAs layouts at 7nm FinFET. 64.74% and 66.6% reduction in delay and power deviation was achieved.

STs are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. On a typical input (non-ST), its binary value will switch at the same point on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit causing a shift in the threshold voltage.

If the threshold shifts, it will cross the input causing it to switch again. It can go indefinitely causing oscillation. The same thing can happen if there is noise on the input. STs are applied in these cases to filter noise introducing superior and inferior threshold

voltages.

5 OBJECTIVES

Given the laid concepts, this work objective is to identify a appropriate layout, considering the number of fins, and supply voltage in order to achieve a minimum energy device. The considered circuit will be a traditional Schmitt Trigger.

Multiple levels of process variability will be considered. Therefore, depending on manufacturability quality, different recommended layouts and supply voltages can arise.

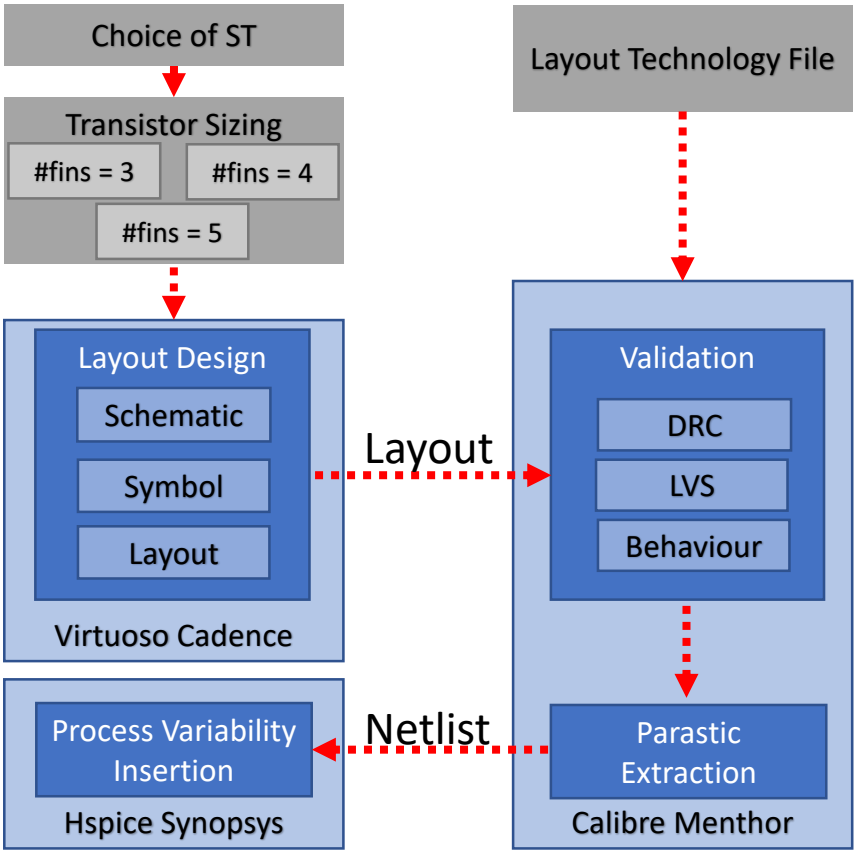
There will be considered the means, standard deviations and normalized standard deviations for each metric, energy and delays, respectively.

6 METHODOLOGY

To provide an extensive exploration of the process variability effects on the ST characteristics, this work will evaluate: 1) ST circuits operating at multiple combinations of supply voltages; 2) the impact of different levels of process variability; 3) the influence of the transistor sizing exploring devices from 1 to 5 fins, in one-by-one fin steps; and 4) the impact of these parameters on the maximum achievable frequency within a failure threshold.

The project was divided into two main steps: the layouts designing and electrical simulations. After finishing the layout design process, each layout passed through validation which consisted of a Design Rule Checking (DRC) to detect if the layout obeys the technology geometry restrictions and layer rules, Layout Versus Schematic (LVS) where layout and schematic are compared to detect their equivalence (same nodes and nets) and a Behavioral test, in order to observe if the circuit works as expected. The design flow is shown at Figure 6.1.

Figure 6.1: Design flow of the experiments.



Source: From the author.

6.1 Layout Design

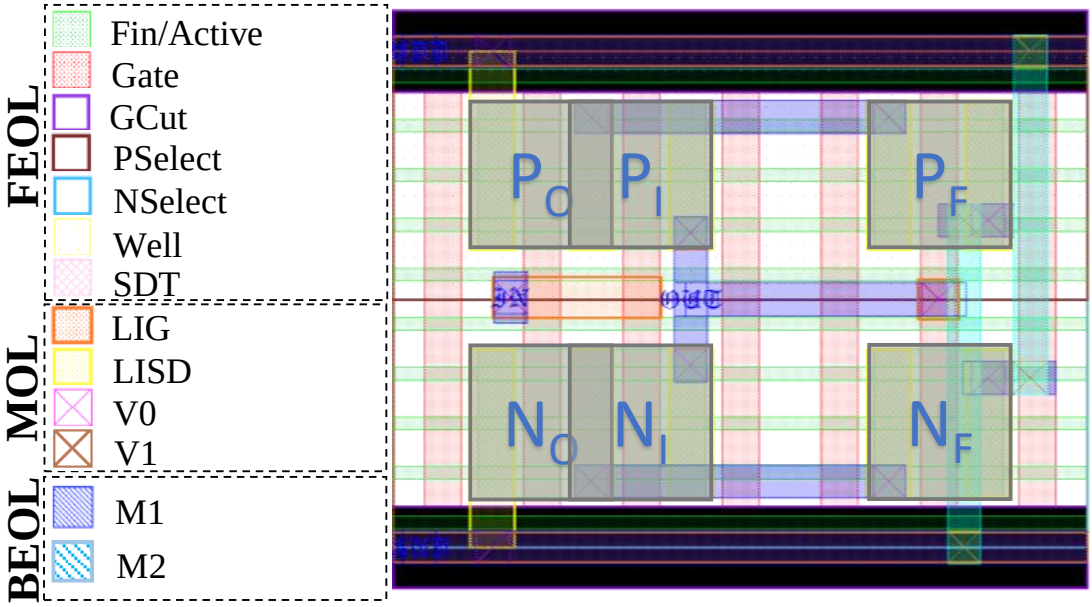
All STs will be designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence®with the process design kit (PDK) of 7-nm FinFET of Arizona State Predictive PDK (ASAP7) from the Arizona State University in partnership with ARM (CLARK et al., 2016). It is the only available 7-nm PDK for academic use. This PDK was chosen due to realistic design conjecture regarding the current design competencies. FinFET tehcnologies present the width quantization aspect (ALIOTO; CONSOLI; PALUMBO, 2015a). With a 27nm fin pitch, high-density layout is achieved with 3-fins transistors. Otherwise, for a higher fin count, there is a lower density and routing complexity (CHAVA et al., 2015). The main PDK rules and lithography assumptions considered in this work are shown in Table I. To exemplify the PDK layers, the 3-fins transistors ST is shown in Fig. 6.2.

Table 6.1: Key layer lithography assumptions, widths and pitches

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

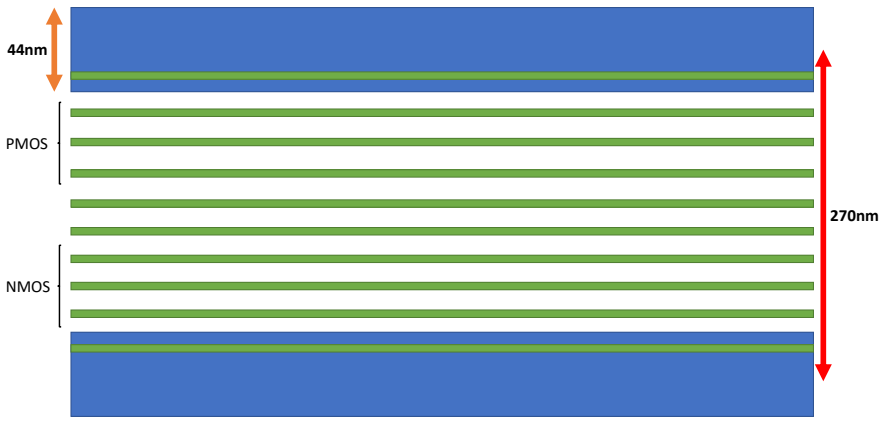
Source: Clark et al. (2016)

Figure 6.2: Technology layers and 3-fins transistors 6T ST layout



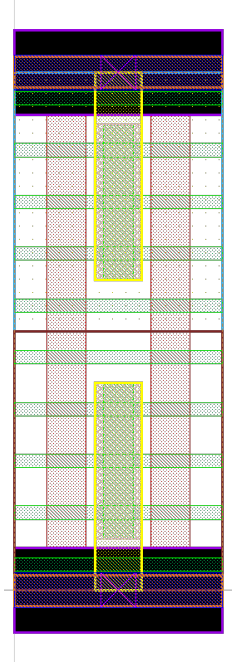
Source: From the author.

Figure 6.3: Transistor height and number of fins.



Source: From the author.

Figure 6.4: TAP-Cell Layout.



Source: From the author.

The ASAP7 PDK contains the manufacturing process composed by front end of line (FEOL), middle of line (MOL) and back end of line (BEOL). The layouts were developed in a continuous diffusion layer with every gate surrounding another gate in the horizontal axis. The Source-Drain Trench (SDT) connects the active area to the LISD layer. The Local-Interconnect Gate (LIG) is applied to connect the gate terminal, and Local-Interconnect Source-Drain (LISD) is used to connect the source and drain of the transistors. The function of Via 0 (V0) is to join the LIG and LISD to the BEOL layers. The Metal 1 (M1) is used for intra-cell routing and short connections. The Metal 2 (M2) was applied to connect the PF and NF drains to ground and source, respectively. To make the back-gate connections it is necessary a TAP-Cell. It is responsible to connect the NMOS and PMOS back-gates to supply/ground, respectively, being possible to connect the PMOS back-gates to another node. It is a PDK restriction needed for the proper function of the circuit.

6.2 Electrical Simulation

The simulations will be carried out in HSPICE (https://www.synopsys.com/) using the netlist obtained after the physical verification flow and the parasitic capacitances extraction. The deviation on the device geometry impacts the electrical parameter WF caus-

ing high fluctuations (ZIMPECK et al., 2016). It happens due to the orientation of metal grains randomly aligned in FinFET manufacturing process. In this way, WFF represents the most significant variation beyond the other parameters (MEINHARDT; ZIMPECK; REIS, 2014). The process variability evaluation will be taken through 2000 Monte Carlo (MC) simulations (ALIOTO; CONSOLI; PALUMBO, 2015b) varying the WF of devices according to a Gaussian distribution considering a 3σ deviation and variations from 1% up to 5% with 1% steps on nominal values. For each step on WF variation, all simulations will be carried from 0.1V to 0.7V supply voltage, with 0.1V steps.

For all experiments, it will be observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: hysteresis interval, delay, energy, and on and off currents where σ/μ represents the sensibility of the cell to process variability.

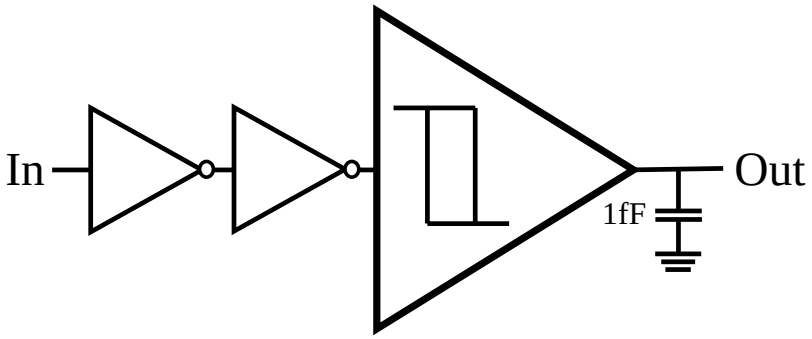
The reference values from ASAP7 technology for electrical simulations are shown in Table 6.2. For a more realistic test bench, it will be considered a scenario where the ST receives the signal passing through two inverters in series and having a 1fF output capacitance, as shown in Fig. 6.5. It is essential to consider some details such as: the same supply voltage is applied in the entire testbench, only the ST suffers from variability, the inverters are the same (3-fins transistors) for all experiments, and they are, like the ST, simulated from the extracted layout.

Table 6.2: Parameters applied in the electrical simulations

Parameter		**7nm**
Nominal Supply Voltage		0.7 V
Gate Length (LG)		21nm
Fin Width (WFIN)		6.5nm
Fin Height (HFIN)		32nm
Oxide Thickness (TOX)		2.1nm
Channel Doping		1x$10^{22}m^{-3}$
Source/Drain Doping		2x$10^{22}m^{-3}$
Work Function (eV)	NFET	4.372
	PFET	4.8108

Source: Clark et al. (2016)

Figure 6.5: Test Bench.



Source: From the author.

7 RESULTS

This section is divided into several parts due to the high volume of data. First, a discussion concerning energy consumption and robustness analysis followed by the performance (delays and maximum frequencies) and after, the variability effects on the hysteresis interval are presented.

7.1 Energy Consumption

For each level of process variability, there is a different ideal scenario for each kind of application and/or priority. As shown in Table 7.1, considering the lowest absolute energy consumption observed, the 1-fin layout showed, in all cases, the lowest energy consumption. It is due to its smaller driving capability, resulting in smaller currents. The supply voltages recommended for each scenario increase almost linearly in relation to the level of WFF variability. The fact that the 0.1V regime did not prevail as the best option across all scenarios, shows the dependency of energy consumption with propagation times. Fig. 7.1 shows an average between all variability scenarios, showing a steep increase in energy consumption below 0.3V.

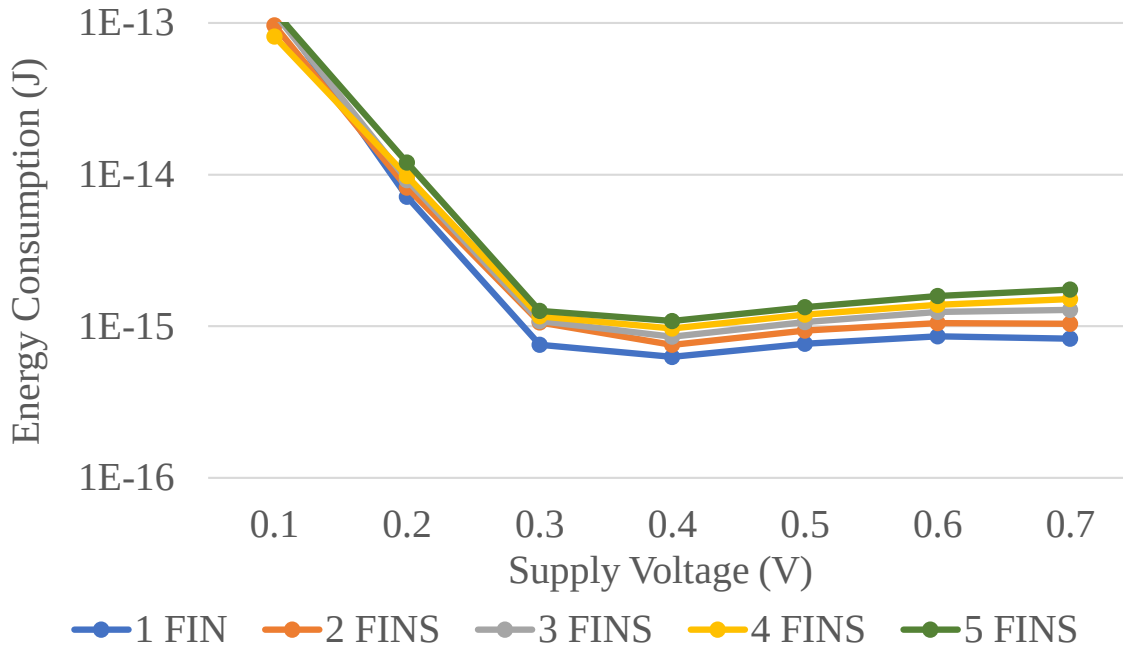
Table 7.1: Recommended setup by each specific scenario

WFF	**Lowest Energy**		**Most Robust**		**Cost-Benefit**	
	# Fins	**Supply (V)**	**# Fins**	**Supply (V)**	**# Fins**	**Supply (V)**
1%	1	0.1	1	0.7	1	0.7
2%	1	0.2	1	0.7	1	0.7-0.2
3%	1	0.2	5	0.3	1	0.3
4%	1	0.3	5	0.4	1	0.4
5%	1	0.4	5	0.5	1	0.5

If variation sensibility is a priority, for each variability scenario, the setup recommended is at 1 fin layout and 0.7V for 1% and 2% WFF. Then, for all layouts, from 0.7V to 0.4V, normalized deviations are below 16%, favoring small to average supply scaling. At 3% of WFF deviation, the recommended supply voltage decreases to 0.3V rising linearly afterwards.

The energy robustness is mainly determined by variations in the on-current and in the time necessary for the circuit charging/discharging. At nominal supply voltages, the on-current falls into the saturation region with an exponential dependence over the threshold voltage. Given that, variations on the threshold voltage will result in exponential

Figure 7.1: Average energy consumption over supply voltage scaling.



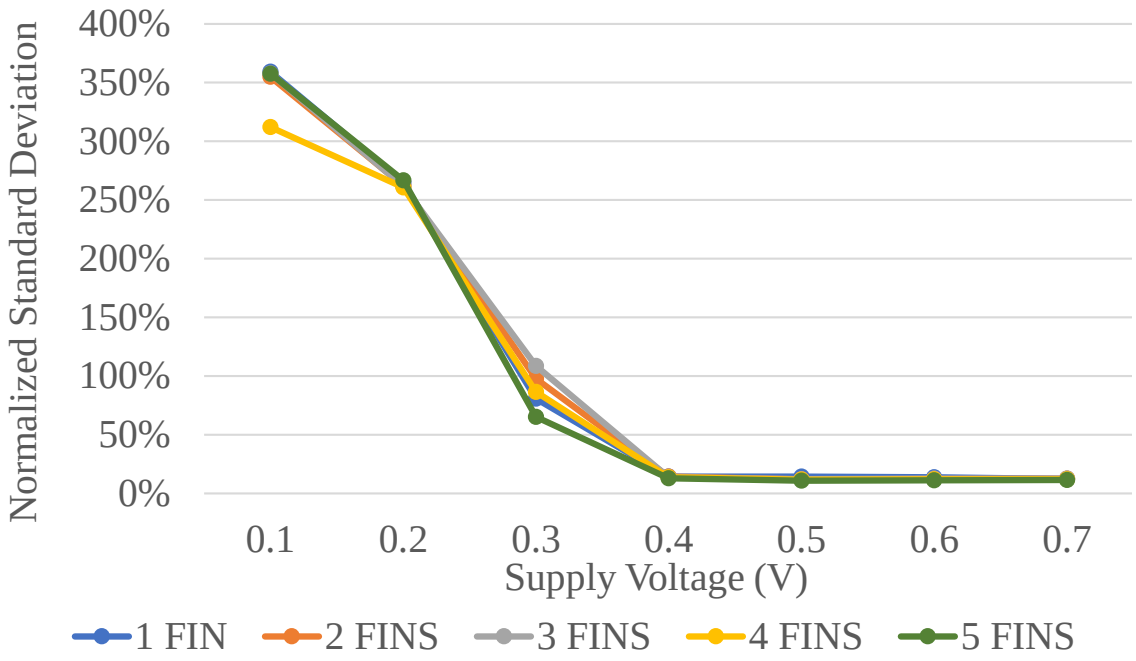
variations in nature. With the supply voltage scaling, the on-current and variations fall into the linear region.

Thus, at low variability scenarios, close-to-nominal supply voltages will not suffer from the exponential threshold voltage dependence, diminishing its effect with high current peaks, small signal slopes overcharging and discharging and higher noise immunity. As variability rises, the linearity from the threshold voltage will gain an advantage, favoring smaller supply voltages. However, as variability rises again, the rise and variation in propagation times will start to determine the adequate supply voltage. Fig. 7.2, shows the average scaling on the impact of process variability on energy consumption.

For the sake of comparison, Figs. 7.3 and 7.4 show the difference in energy consumption and energy consumption variation in relation to the layouts with the lowest of each one, respectively, and compares to the traditional 3-fin layout at the same supply voltage and variability scenario. The highest difference was 27.85% and 14.44% for energy consumption and variability, respectively.

Considering a cost-benefit scenario, the best choice was defined by the lowest value given by the energy consumption and the normalized deviation product (EDP). A comparison between the layouts with the lowest energy consumption, energy variability, and the best cost-benefit are shown in Figs. 7.5 and 7.6 in relation to energy consumption and energy variability, respectively. The energy variability of the lowest energy layout at 3% WFF is one example of why a cost-benefit analysis should be made since it shows an

Figure 7.2: Average energy consumption sensibility scaling over supply voltage.



11.5% lower energy consumption with a 582.47% higher sensibility.

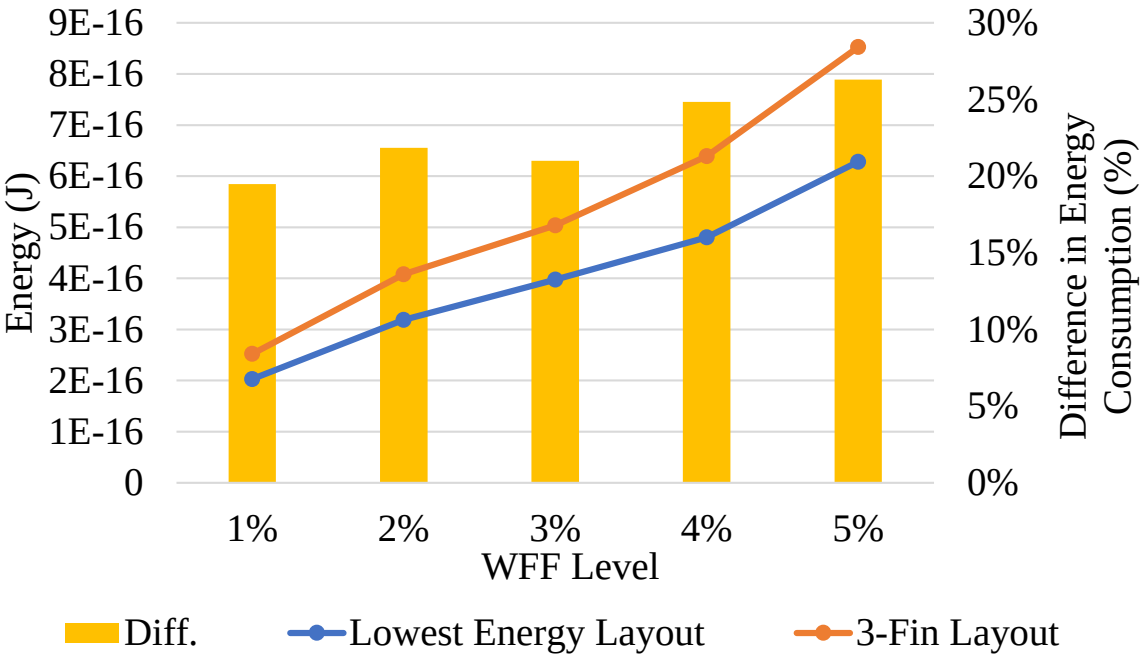
7.2 Delays

At performance scaling it can be observed a worsening on propagation times over the lowering of the supply voltage and fin count. The transistor driving capability is proportional to the fin count, given that with more fins there is a larger active area passing current. Fastening the charging/discharging process. Given the area penalty, which will be discussed, the 4-fins layout only gives a 10% penalty on propagation times, being a good choice over area constraints in comparison to the 5-fins layout. The 3, 2 and 1 fins layouts bring a 42%, 92% and 268% delay increase on average, respectively.

In comparison to the traditional 3-fins layout, the 5 and 4-fins variants bring 20% and 13.612% decrease on propagation times while the 2-fins and 1-fin variants bring 27.24% and 107% delay increase, respectively.

For variability impact, it can be observed a tendency of lower sensibility over higher fin count at higher supply voltages. As supply voltage scales down, a lower number of fins starts to keep up with the variability robustness, as shown in Fig. 7.7. It can be concluded that due to the exponential relation of drain current with gate-to-source voltage, the higher fin count is capable of providing the necessary current drive at higher supply voltages. At lower supply voltages, with the drain current decreasing exponentially, the

Figure 7.3: Energy consumption comparison between the layout with the lowest energy consumption and the traditional 3-fins layout at the same supply voltage.



fin count impact on variability robustness is diminished.

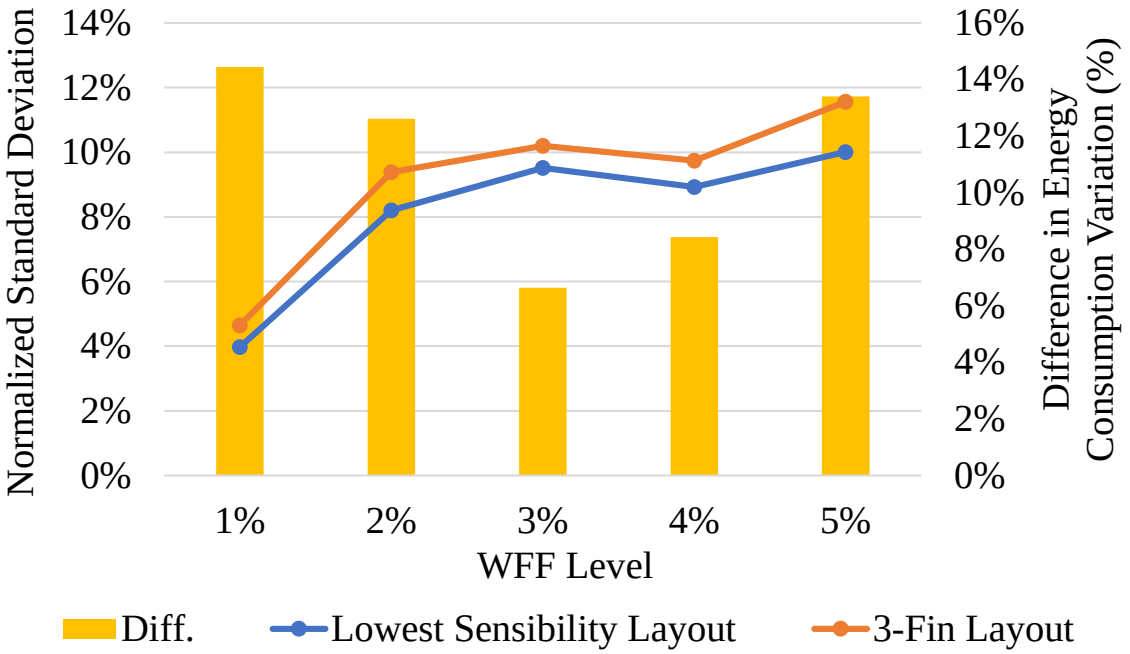
7.3 Maximum Frequency

The maximum frequency is proportional to the supply voltage and fin count. The higher fin count allows faster charging and discharging due to a bigger active area driving current. On average, the 5 and 4-fins layouts were able to present 16% and 10.34% higher frequencies while the 2 and 1-fin variants showed 19.18% and 44.65% lower frequencies, in comparison to the 3-fins variant.

7.4 Hysteresis Interval

Hysteresis is one of the major characteristics concerning the circuit ability to filter noise. A higher hysteresis interval brings more robustness to the circuit. As a priority, the ratio between its value and the supply voltage should be as high as possible. The ST, at nominal operation (nominal supply voltage and no process variability), presented a maximum hysteresis interval of approximately 0.45V. Given that, considering the average absolute values of the hysteresis interval, it can be observed a difference below than 5%

Figure 7.4: Energy variability comparison between the layout with the lowest sensibility and the traditional 3-fins layout at the same supply voltage.



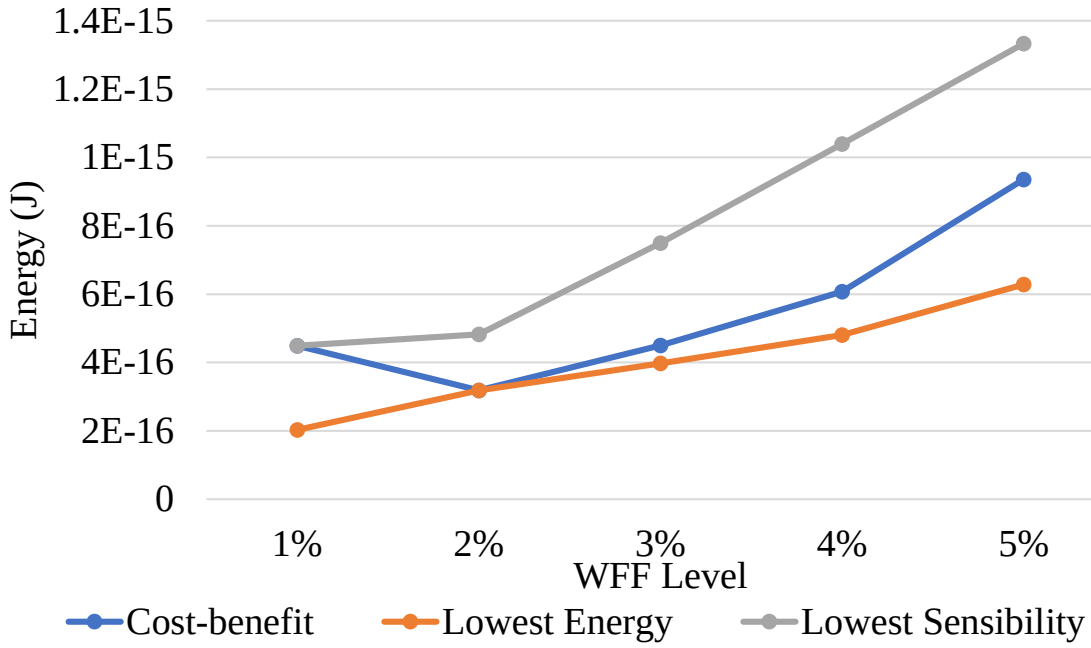
between the best and worst cases, considering different fin counts.

At higher supply voltages of 0.6V and 0.7V, the difference widens up reaching up to 10.76% and 25.26% between the 5-fins and 1-fin layout, respectively. Such results come from the faster charging/discharging, which decreases the signal slopes widening the circuit hysteresis interval. At lower supply voltages, a decreased number of fins is sufficient to keep the slopes low enough, presenting high hysteresis to supply voltage ratios while at higher supply voltages a lower number of fins will increase the signal slopes.

Although, there is a hysteresis interval improvement, as shown in Fig. 7.8, over the WFF increase as well. Such behavior happens due to the hysteresis interval dependency over the PFET and NFET threshold voltages (DOKI, 1984). This means that lower WF decreases the NFET threshold, while higher WF will increase the NFET threshold, and vice-versa for PFET devices. Therefore, the ideal scenario would be with negative WFF for the PFET devices and positive WFF for the NFET devices. Though, the NFET term also depends on the β-ratio (ratio between the transistor emitter and base current) of the PFET and NFET transistors. Giving an estimate based on saturation and off-currents from (CLARK et al., 2016), the NFET threshold voltage influence on the final hysteresis interval is almost 40% higher, in comparison to its counterpart.

As shown in Table 7.2, the only cases with considerable hysteresis worsening hap-

Figure 7.5: Energy consumption comparison among the layouts with the best cost-benefit, lowest energy consumption and lowest variability sensibility.



pens when the NFET WF is above 2%, while the subset showing improvements includes most of the possible scenarios. And since the hysteresis voltage will never be higher than the supply voltage, the average tends to the supply voltage value.

Figure 7.6: Energy variability comparison among the layouts with the best cost-benefit, lowest energy consumption and lowest variability sensibility.

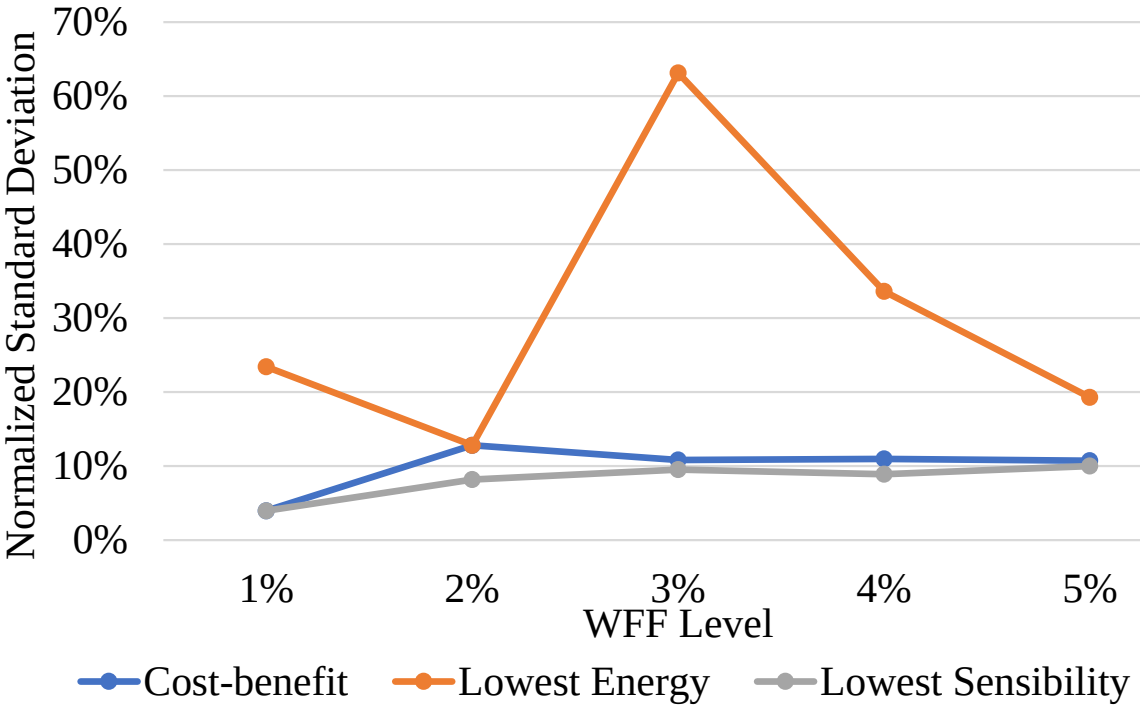


Figure 7.7: Delay sensibility ratio between layouts.

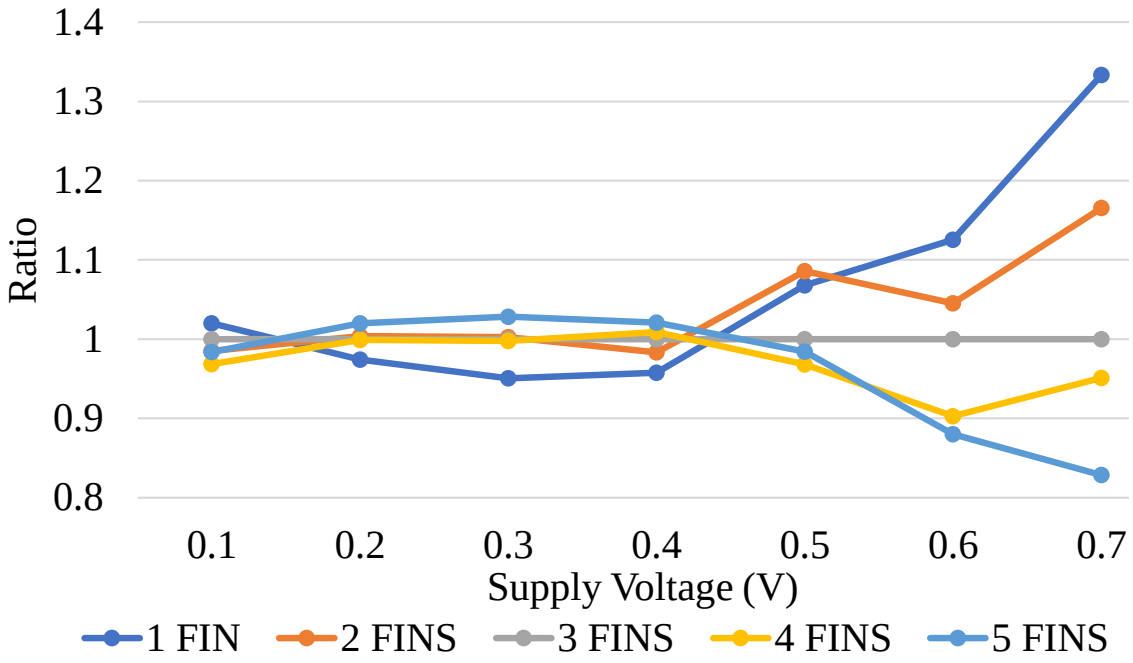


Figure 7.8: Average of hysteresis interval increase over WFF scaling.

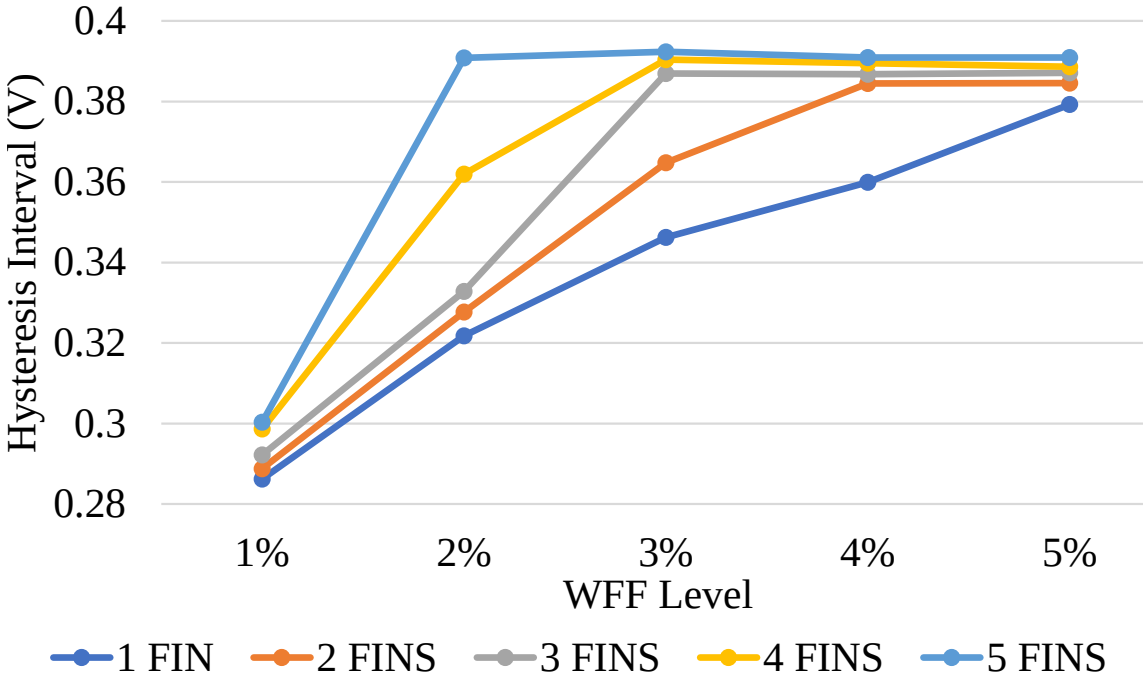


Table 7.2: Hysteresis interval ratio dependency over NFET and PFET workfunction

NFETPFET	5%	4%	3%	2%	1%	0%	-1%	-2%	-3%	-4%	-5%
5%	**0.30**	**0.28**	**0.28**	**0.27**	**0.26**	**0.25**	**0.26**	**0.27**	**0.28**	**0.30**	**0.32**
4%	**0.46**	**0.46**	**0.55**	**0.54**	**0.54**	**0.54**	**0.55**	**0.56**	**0.57**	**0.59**	**0.61**
3%	**0.76**	**0.76**	**0.76**	**0.78**	**0.80**	**0.81**	**0.83**	**0.84**	**0.86**	**0.87**	**0.89**
2%	**0.88**	0.90	0.92	0.92	0.95	0.97	0.99	1.00	1.00	1.00	1.00
1%	0.93	0.94	0.97	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00
0%	0.95	0.96	0.97	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
-1%	0.95	0.96	0.99	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00
-2%	0.96	0.97	0.99	1.00	1.00	0.99	0.99	0.99	0.99	0.98	0.98
-3%	0.95	0.97	0.99	0.99	0.99	0.99	0.98	0.98	0.98	0.97	0.97
-4%	0.93	0.94	0.97	0.97	0.96	0.96	0.96	0.95	0.95	0.95	0.94
-5%	0.93	0.94	0.96	0.96	0.96	0.95	0.95	0.94	0.94	0.94	0.93

8 CONCLUSIONS

The ongoing trend of IoT devices was enabled by two key technology improvements: battery lifetime and capacity improvement, and node scaling. Although, for specific applications, battery maintenance and charging through the power grid is not possible. Given so, IoT devices have been constrained with tight energy consumption metrics, and adapted with self-sufficient mechanisms in order to produce energy through external sources.

The node scaling, that enabled IoT devices, comes not short of inherent challenges, with process variability being the major one. New transistor technologies have been proposed such as FinFETs, although even such devices, at deep submicron nodes (e.g. 7-nm), present considerable deviation in its metrics. Such deviations are not appropriate for such sensible devices working at narrow constraints (with energy consumption being a priority).

Given so, an analysis over multiple scenarios considering several levels of process variability, supply voltages, and transistor sizing was performed in order to identify the adequate fin number and supply voltage for various kinds of applications prioritizing energy consumption and the minimization of deviations. ST is a promising circuit for variability effects mitigation and enhancement of noise immunity being fairly applied on critical applications with tight reliability constraints.

The results show that fewer fins can enable considerable energy reduction. On the contrary, for the ST robustness, a higher fin count will bring an increase in the on-current, bringing noise immunity improvements. In performance results, it could be observed up to 16% and 44.65% maximum average increase and decrease in frequency, respectively, with differences between variability impact in the layouts rising alongside the supply voltage value. The hysteresis intervals showed clear advantages over higher fin count and supply voltages with 10.76% and 25.26% better hysteresis.

Lastly, considering energy consumption and variability, it was possible to achieve 24.84% and 14.44% decreases, respectively, in comparison to a traditional transistor sizing. A cost-benefit analysis was made as well, giving an additional option in order to achieve acceptable energy consumption and variability robustness.

9 FUTURE WORKS AND CRONOGRAM

For future works it is expect the same analysis presented in the results section to be made over two additional ST designs: the Triple-Inverter ST (TIST), Stacked-Inverter Gate (SIG) and, for the sake of comparison, a classical inverter. Both TIST and SIG designs are shown in Figs. 9.1 and 9.2, respectively. Additionally, the analysis will be expanded by considering the SNMs, VTC and, I_{ON} and I_{OFF} currents under variability.

Figure 9.1: TIST schematic (RABAEY; CHANDRAKASAN; NIKOLIC, 2002)

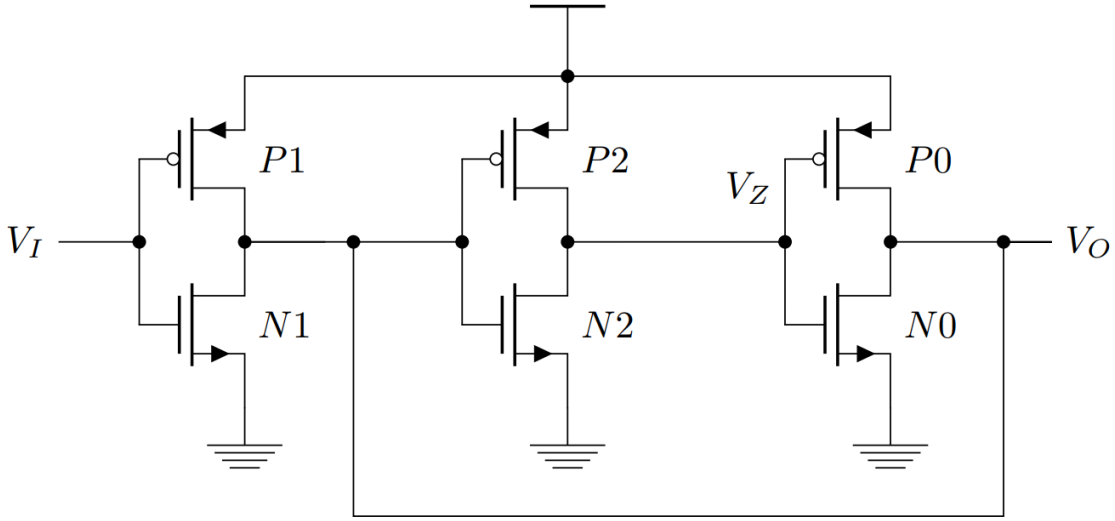


Figure 9.2: SIG schematic (BOSE; JOHNSTON, 2018)

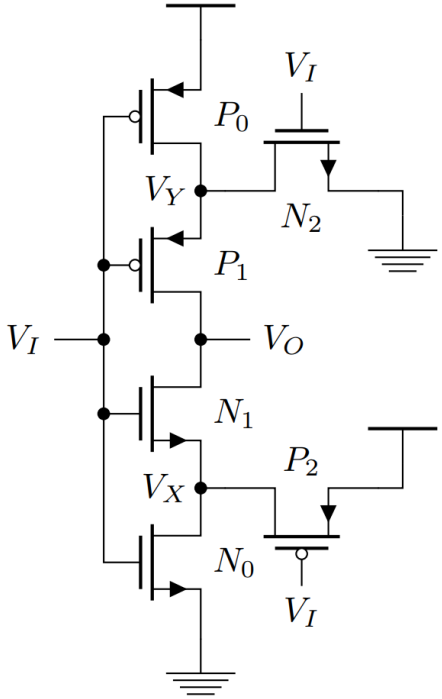


Table 9.1, shows the expected cronogram for the dissertation:

Table 9.1: Dissertation Cronogram

	Simulations	Writing	Event	Publication	Revision
July	X				
August	X	X		X	
September		X		X	X
October				X	X

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