

LEONARDO **MORAES**

Masters Student on Microelectronics



2016 – 2018

SCIENTIFIC INITIATION FELLOW

Universidade Federal do Rio Grande do Sul (UFRGS)

Porto Alegre, RS

Research project focused on the analysis of layout robustness over process variability.

2018 -Present

MASTER IN MICROELECTRONICS

Universidade Federal do Rio Grande do Sul (UFRGS) @ PGMICRO

Porto Alegre, RS

Research project focused on enabling the application of robustness enhancing circuitry on Low Power IoT devices at FinFET technology node.



2012 -2018

COMPUTER ENGINEERING DEGREE

Universidade Federal do Rio Grande do Sul (UFRGS)

Porto Alegre, RS

Publications:

Moraes, Leonardo Barlette de, et al. "Evaluation of variability using Schmitt trigger on full adders layout." Microelectronics Reliability 88 (2018): 116-121.

https://doi.org/10.1016/j.microrel.2018.07.061

Moraes, L. B., et al. "Exploring Schmitt Trigger Circuits for Process Variability Mitigation." 2019 17th IEEE International New Circuits and **Systems** Conference (NEWCAS). IEEE. 2019. https://doi.org/10.1109/NEWCAS44328.2019.8961235

Moraes, L. B., et al. "Minimum Energy FinFET Schmitt Trigger Design Considering Process Variability." 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC). IEEE, 2019. https://doi.org/10.1109/VLSI-SoC.2019.8920297

ABOUT ME

am Masters student in Microelectronics and look for internships in areas compatible with my specialization. I hope to learn new skills, work on a team and solve problems. I am punctual, responsible and proactive.



Apart from skills developed during my BS, involving programming, circuit analysis, and basic knowledge. During my academic experience I mostly work on Virtuoso® designing layouts on different PDKs, SPICE for electrical simulations, and overall scripting/programming (Shell script, Python and C/C++, mostly). For more general skills, I have plenty of experience working on Linux, officerelated programs and Latex.

本 LANGUAGES

Portuguese Native/Fluent English Advanced Spanish Basic



Research Gate

ORCID

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CONTACTS

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