Computer Organization 2024
Online Examination

Goal

In this online exam, you will modify the processor you have designed for Programming HW#3 to add the support of two new instructions. Note that these are **not** standard MIPS instructions. The register $t0, $t1, and $t2 have the IDs 8, 9, and 10, respectively. The exam is divided into two parts:

Part I (50%): implementation of a saturation instruction "**`sat $rt, $rs, imm`**" that truncates the value of a register to [0, upper_bound]. This instruction uses the I-format, with opcode = 6'b100000, and the operation is defined by:

R[rt] (R[rs] > 0)? ((R[rs] < upper_bound)? R[rs] : upper_bound) : 0,

where R[] is the register file, and upper_bound = R[rs] + { 16'b0, imm }.

Note that the 16-bit *imm value* is an unsigned value and R[rs] is a signed number.

Part II (50%): implementation of a branch upon odd value instruction "**`bodd $rs, imm`**". This instruction

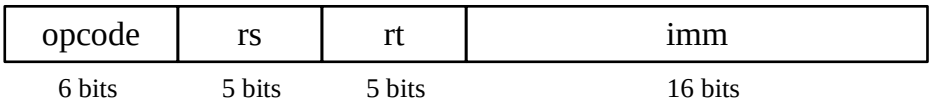
uses the I-format, with opcode = 6'b000111, and the operation is:

if (R[rs] is odd) PC = PC + 4 + { $SignExt_{30}$(imm), 2'b0 },

where R[] is the register file and $SignExt_{30}$() is the sign extension to 30 bits.

Note that the rt field is not used and is set to zero.

The I-format of instruction is as follows:



To test your CPU, you can put the following code in the instruction memory of your testbench:

```
00000000: 20080111 ;     addi $t0, $zero,
273
00000004: 800900FA ;     sat  $t1, $t0, 250
00000008: 1D200001 ;     bodd $t1, bye
0000000c: 21290001 ;     addi $t1, $t1, 1
00000010: <bye>     ; bye:
00000010: ac090000 ;     sw      $t1,
0($zero)
00000014: 08000004 ;     j    bye
```

Exam Regulations

[1] You are not allowed to use your mobile phone, browse the internet for any references, and talk to any other classmates. If you have any questions, please raise your hand and the TA will talk to you.

[2] You are allowed **2 hours** for this online exam.

[3] You can download the exam workspace, your previous homework code, or the Power Point slides from E3 to the test computer between 10:10 ~ 12:10. Any downloading behavior outside this period will be regarded as cheating.

[4] After your circuit is completed and verified, please upload all your **modified** Verilog files to E3. You

have to leave the computer classroom immediately afterwards.