ASMEDIA TECHNOLOGY INC

ASM3074C Data Sheet

USB 3.2 Gen2x2 HUB Controller

Office:
ASMedia Technology, Inc.
6F, No.115, Minquan Rd., Xindian Dist., New Taipei City 231, Taiwan, R.O.C.
http://www.asmedia.com.tw
Tel: +886-2-2219-6088
Fax: +886-2-2219-6080

Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	Jan 06, 2023	Initial Release
0.2	Apr 12,2023	Top Marking Update. Power On Sequence Update

Table of Contents

List of Figures

This page is intentionally left blank.

1. General Description

The ASM3074C is a USB 3.2 compliant hub with ASMedia's legacy, innovative, and self-designed PHY technology perfectly integrated into it. The ASM3074C DSPs supports one USB 3.2 Gen2x2 port and two USB3.2 Gen2x1 ports , and offers a low-power and cost-effective solution for a variety of USB applications. The ASM3074C is fully compliant with USB 3.2 Specification Revision 1.0 and USB Battery Charging Specification Revision 1.2.

2. Features

USB 3.2 HUB Features

- Compliant with USB 3.2 Specification Rev. 1.0
- Upstream Port supports USB 3.2 Gen2x2 (20Gbps), High-Speed and Full-Speed Connections
- Each of the four Downstream Ports supports USB 3.2 Gen2, High-Speed, Full-Speed and Low-Speed Connections ASM3074C supports one USB 3.2 Gen2x2 port , two USB3.2 Gen2x1 ports and one USB2.0 port
- Implements USB 3.0 power management function
    - SuperSpeed Link Power Management support
    - USB 2.0 Link Power Management support
- Compliant with USB Attached SCSI Protocol (UASP) Rev. 1.0
- Multiple Transaction Translator support
- Supports external Port Power Switching and Over-Current Protection per port control
- Individual and Gang mode selectable via strapping
- Marked as removable or permanently attached

Battery Charging Features

- Supports portable devices such as iPad and cellphones
- Dedicated Charge Port (DCP) support
- Battery Charge Rev. 1.2 specification Compliance
- Supports automatic Battery Charger Detection
- Charging Downstream Ports support USB-C 5V/3A with an external CC logic chip
- Supports charging while the system enters the active or suspended state

General Feature

- Integrated 8-bit microprocessor
- SPI flash support for customized firmware
- I2C EEPROM support for customized configuration
- Uploadable Firmware & configuration via upstream port
- Integrated 5V to 3.3V LDO
- Supports self-powered and bus-powered modes
- Automatic power type detection and dynamic power type switch
- Supports 25 MHz X'tal as clock source
- Multiple GPIOs for LED applications
- Two Power Supply domains
    - IO power supply with 3.3V+/-0.3V and 2.5V +/-0.2V
    - Core power supply 1.05V+/-0.05V
- Green Package with RoHs compliance

Package Type

◇ QFN 88L (10x10 mm^2)

3. Functional Block Diagram

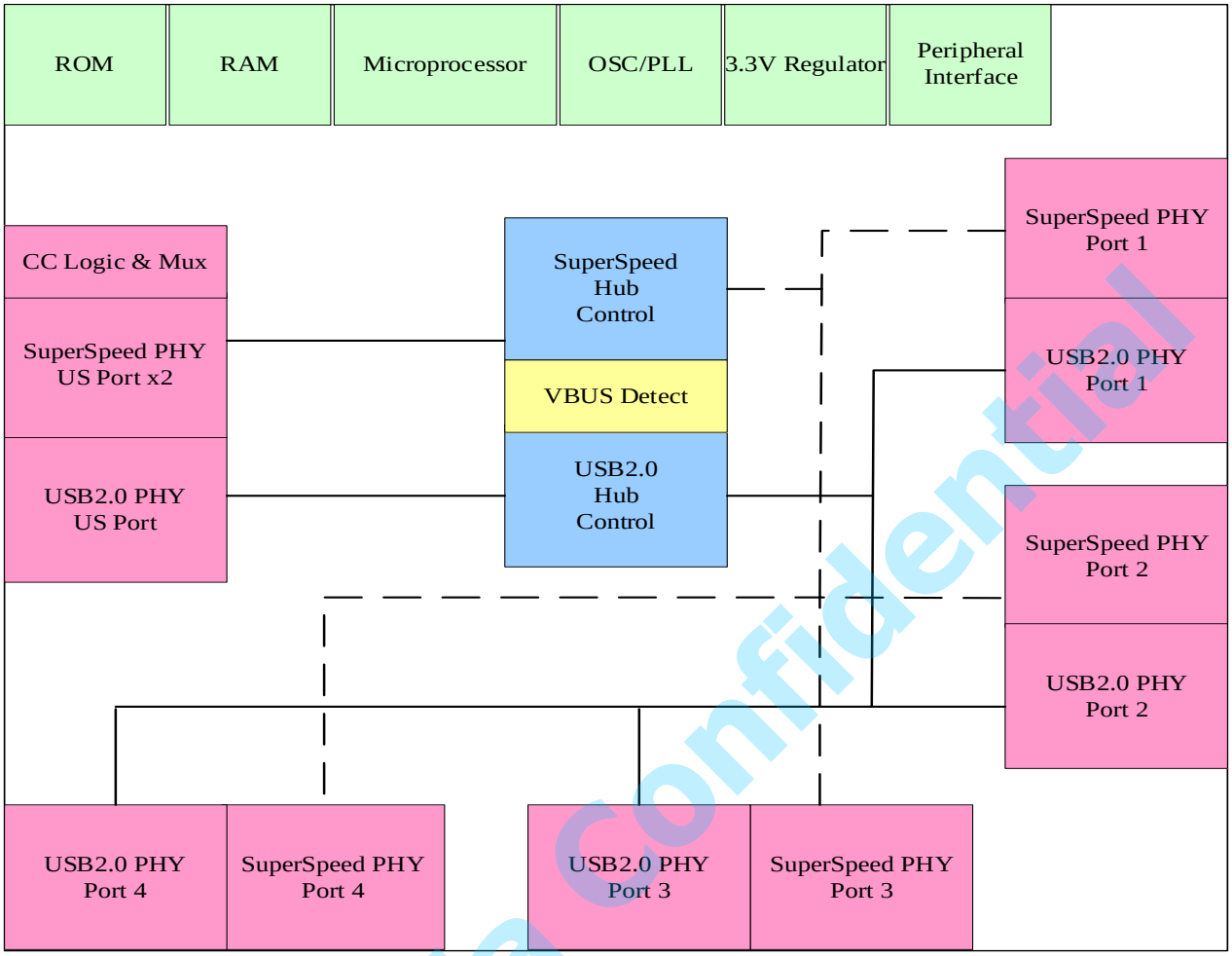


Figure 1: ASM3074C Functional Block Diagram

4. Pin Diagram

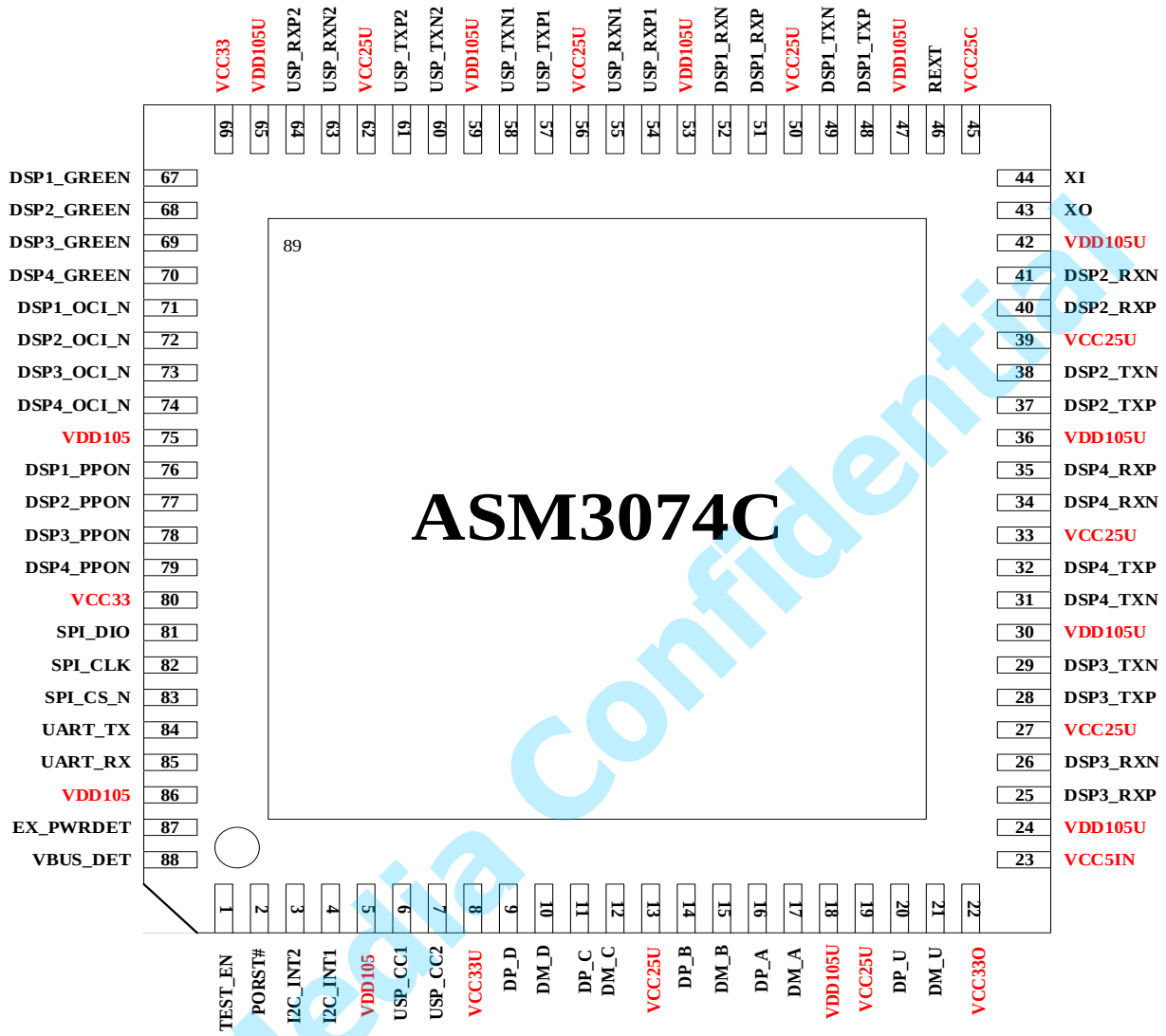


Figure 2: ASM3074C Pinout

5. Pin Descriptions

The following table lists the descriptions of each type of signal.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

USB 3.2 Interface

Pin No.	Name	Type	Description
25	RXP_3	DiI	USB 3.2 Downstream Port 3 Differential Receive Data +
26	RXN_3	DiI	USB 3.2 Downstream Port 3 Differential Receive Data -
28	TXP_3	DiO	USB 3.2 Downstream Port 3 Differential Transmit Data +
29	TXN_3	DiO	USB 3.2 Downstream Port 3 Differential Transmit Data -
31	TXN_4	DiO	USB 3.2 Downstream Port 4 Differential Transmit Data -
32	TXP_4	DiO	USB 3.2 Downstream Port 4 Differential Transmit Data +
34	RXN_4	DiI	USB 3.2 Downstream Port 4 Differential Receive Data -
35	RXP_4	DiI	USB 3.2 Downstream Port 4 Differential Receive Data +
37	TXP_2	DiO	USB 3.2 Downstream Port 2 Differential Transmit Data +
38	TXN_2	DiO	USB 3.2 Downstream Port 2 Differential Transmit Data -
40	RXP_2	DiI	USB 3.2 Downstream Port 2 Differential Receive Data +
41	RXN_2	DiI	USB 3.2 Downstream Port 2 Differential Receive Data -
48	TXP_1	DiO	USB 3.2 Downstream Port 1 Differential Transmit Data +
49	TXN_1	DiO	USB 3.2 Downstream Port 1Differential Transmit Data -
51	RXP_1	DiI	USB 3.2 Downstream Port 1 Differential Receive Data +
52	RXN_1	DiI	USB 3.2 Downstream Port 1 Differential Receive Data -
54	RXP1_U	DiI	USB 3.2 Upstream Port Side 1 Differential Receive Data +
55	RXN1_U	DiI	USB 3.2 Upstream Port Side 1Differential Receive Data -
57	TXP1_U	DiO	USB 3.2 Upstream Port Side1 Differential Transmit Data +
58	TXN1_U	DiO	USB 3.2 Upstream Port Side 1 Differential Transmit Data -
60	TXN2_U	DiO	USB 3.2 Upstream Port Side 2 Differential Transmit Data -
61	TXP2_U	DiO	USB 3.2 Upstream Port Side 2 Differential Transmit Data +
63	RXN2_U	DiI	USB 3.2 Upstream Port Side 2 Differential Receive Data -
64	RXP2_U	DiI	USB 3.2 Upstream Port Side 2 Differential Receive Data +
6	USP_CC1	IO	Upstream Port Configuration Channel for Side1
7	USP_CC2	IO	Upstream Port Configurartion Channel for Side2

USB 2.0 Interface

Pin No.	Name	Type	Description
9	DP_D	DiB	USB 2.0 Downstream Port 4 Bus Data +
10	DM_D	DiB	USB 2.0 Downstream Port 4 Bus Data -
11	DP_C	DiB	USB 2.0 Downstream Port 3 Bus Data +
12	DM_C	DiB	USB 2.0 Downstream Port 3 Bus Data -
14	DP_B	DiB	USB 2.0 Downstream Port 2 Bus Data +
15	DM_B	DiB	USB 2.0 Downstream Port 2 Bus Data -
16	DP_A	DiB	USB 2.0 Downstream Port 1 Bus Data +
17	DM_A	DiB	USB 2.0 Downstream Port 1 Bus Data -
20	DP_U	DiB	USB 2.0 Upstream Port Bus Data +
21	DM_U	DiB	USB 2.0 Upstream Port Bus Data -

MISC Interface

Pin No.	Name	Type	Description
1	TEST_EN	I	Test Enable Pin. 0: Normal mode, 1:ATE Test mode
88	VBUS_DET	I	VBUS Detection
76	PRON1	O	Port 1 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
77	PRON2	O	Port 2 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
78	PRON3	O	Port 3 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
79	PRON4	O	Port 4 Power Switch Enable Internal ~40Kohm resistance Pull Down during chip reset
71	OC_N1	I	Port 1 Over Current Indicator
72	OC_N2	I	Port 2 Over Current Indicator
73	OC_N3	I	Port 3 Over Current Indicator
74	OC_N4	I	Port 4 Over Current Indicator
2	POR_N	I	Power On Reset
46	REXT	I	External Reference Resistor 12.1Kohm +/-0.1%
87	EX_PWRDET	I	External Power Detect 1: Self-powered mode 0: Bus-powered mode
44	XI	I	Crystal Input or Clock input
43	XO	O	Crystal Output
81	SPI_DIO	IO	SPI Data IO
82	SPI_CLK	O	SPI Clock Bus Output
83	SPI_CS	O	SPI Chip Select for External SPI Flash, internal pull high
84	UART_TX	O	UART DATA Transmit Internal ~40Kohm resistance Pull Down during chip reset
85	UART_RX	I	UART DATA Receive
3	I2C_INT2	IO	I2C_INT2 or GPIO
4	I2C_INT1	IO	I2C_INT1 / CC_IND
67	GRN_LED1	IO	I2C_CLK1 / STATUS_IND1
68	GRN_LED2	IO	I2C_DAT1/ STATUS_IND2
69	GRN_LED3	IO	I2C_CLK2
70	GRN_LED4	IO	I2C_DAT2

Power and Ground Signals

Pin No.	Name	Type	Description
89	GND	**G**	Common Ground
23	VCC5IN	**P**	VCC 3.3V regulator 5V input
22	VCCO	**P**	LDO Reulator 3.3V Output
8, 66, 80	VCCH	**P**	High voltage VCC 3.3V IO Power
13, 19, 27, 33, 39, 45, 50, 56, 62	VCCL	**P**	Low voltage VCC 2.5V IO Power
5, 18, 24, 30, 36, 42, 47, 53, 59, 65, 75, 86	VDD	**P**	1.05V Core Power

Strapping Table

Pin	Function	Description
I2C_INT2	Individual/Gang mode selection	0: Individual mode (Default) 1: Gang mode
I2C_INT1	CC_IND	0: CC1 1: CC2

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. It is recommended to use a clamp circuit to protect the device against abnormal voltage spikes when the power is switched on or off.

Parameter	Range	Unit
Power Supply	-0.5 ~ VCC+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
V_{CCH}	High voltage VCC power supply	3.0	3.3	3.6	V	
V_{CCHO}	High voltage VCC power supply	3.0	3.3	3.6	V	
V_{CCL}	Low voltage VCC power supply	2.3	2.5	2.7	V	
V_{CCLU}	Low voltage VCC power supply for USB	2.3	2.5	2.7	V	
V_{DD}	Core power supply	1.00	1.05	1.1	V	
T_C	Operating Case Temperature	0		85	ºC	
T_J	Silicon Junction Temperature	0	25	120	ºC	
HBM	Human Body mode		TBD		KV	
MM	Machine mode		TBD		V	

6.2.1 Chip Temperature (T_J, T_C) Calculation

Symbol	Parameter	How to get?
T_A	Ambient temperature	Measure temperature around chip
T_J	Operating junction temperature	$T_J = \Theta_{JA}$ * Power + T_A
T_C	Operating case temperature	$T_C = T_J - \Psi_{JT}$ * Power
R_{JA}	Junction-to-ambient thermal resistance	TBD (data from package vender)
R_{JC}	Junction-to-case thermal resistance	TBD (data from package vender)
Ψ_{JT}	Junction-to-top thermal characterization	TBD (data from package vender)
Power	Chip power consumption	Measure chip power consumption

- For thermal test board standards, please refer to JEDEC JESD51-5.
- For thermal test method environmental conditions, please refer to JESD51-2.
- Example: TBD

6.3 AC/DC Characteristics

6.3.1 USB 3.2 Electrical Specification

(Refer to Universal Serial Bus 3.2 Specification Rev. 1.0)

6.3.2 USB 2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

6.3.3 DC Electrical Characteristics for digital pins

(Including VBUS, PERST, I2C, UART, HDDPC and GPIOs)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Input Hysteresis	0.32	0.37	0.4	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.4	1.6	1.8	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1	1.23	1.4	V
V_{OH}	High-Level Output Voltage	2.4			V
V_{OL}	Low-Level Output Voltage			0.4	V
I_{OH}	Output Driving Current while V_{OH}	12			mA
I_{OL}	Output Driving Current while V_{OL}	12			mA
R_{UP}	Internal Pull-up resistance while Vin=0V	65	96	140	KΩ
	Internal Pull-up resistance while Vin=VCC/2 V	38	56	81	KΩ
R_{DN}	Internal Pull-down resistance while Vin=VCC	59	96	142	KΩ
	Internal Pull-down resistance while Vin=VCC/2 V	35	55	79	KΩ
I_{IL-UP}	Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=0	21	34.4	56	uA
	Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=VCC/2	18	29.4	47	uA
I_{IL-DN}	Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC	21	34.5	60	uA
	Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC/2	18	30	50	uA

6.3.4 DC Electrical Characteristics for POR_N pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-Level Input Voltage	2.6			V
V_{IL}	Low-Level Input Voltage			1.4	V
V_{HYS}	Input Hysteresis	0.21	0.23	0.25	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.9	2.2	2.55	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.65	1.97	2.35	V
Input	Input leakage current while Vin=0V			1	uA

6.3.5 External Crystal Electrical Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{XTAL}	Frequency		25		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 25 °C)	-30		30	ppm
t_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

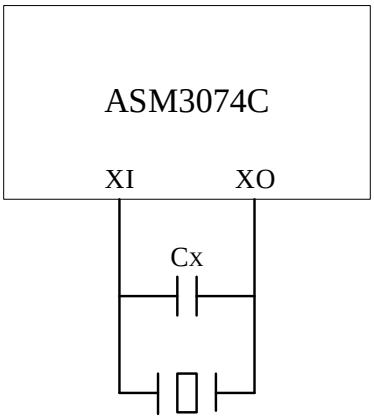


Figure 3: Differential Crystal Design

6.3.6 Differential Clock Oscillator Electrical Specification

Note: The table describes the specification of clock with external 25MHz crystal.

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{XTAL}	Frequency		25		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 25 °C)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		10		pF
C_{TATAL}	Total external equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	pF
R_{TOTAL}	Total external equivalent Series Resistance from XI pin to XO pin (Differential mode)			60	Ω

6.3.7 Internal Linear Regulator Electrical Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage Range	4.0	5.0	5.5	V
V_{OUT}	Output Voltage Range	3.0	3.3	3.6	V
I_{MAX}	Maximum capacity of current			90	mA

Total Power Consumption

TBD

7. Timing Diagram

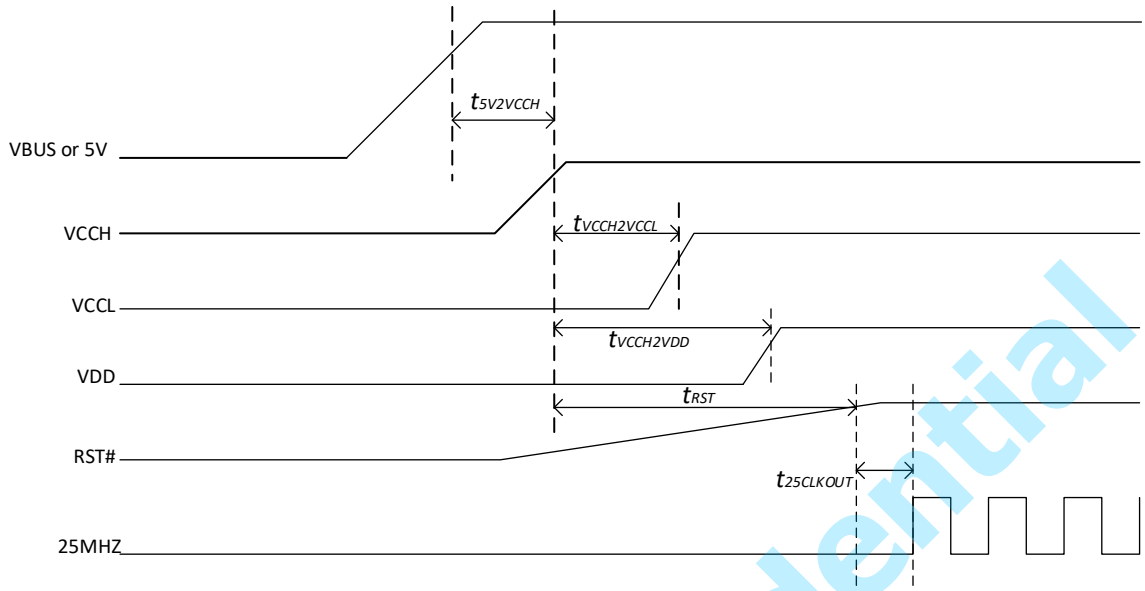
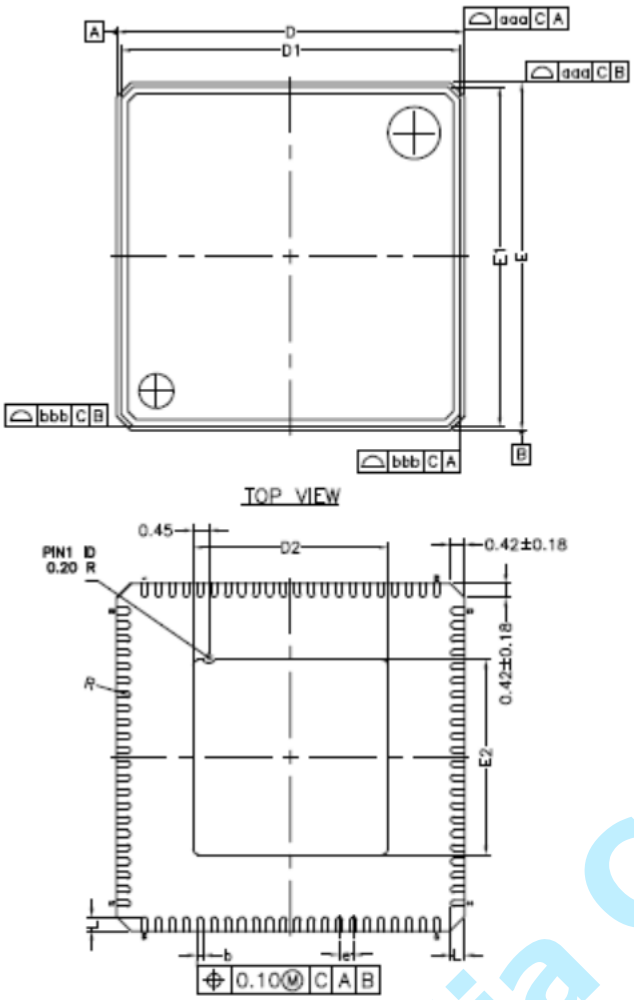


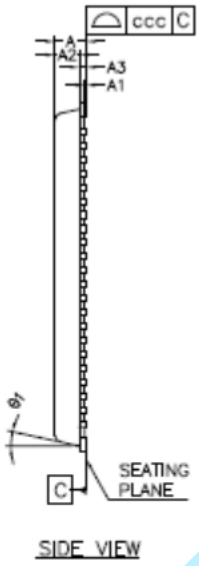
Figure 4: Power on Sequence

Power on Sequence Timing Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
$t_{5V2VCCH}$	V_{CCH} (90%) available after 5V or VBUS (90%) available		3	10	ms
$t_{VCCH2VCCL}$	V_{CCL} (90%) available after V_{CCH} (90%) available	0	5	10	ms
$t_{VCCH2VDD}$	V_{DD} (90%) available after V_{CCH} (90%) available			90	ms
t_{RST}	RST (90%) ready after V_{CCH} (90%) available	0			ms
$t_{25CLKOUT}$	25MHz clock available after RST#(90%) assertion			10	ms

8. Package Information



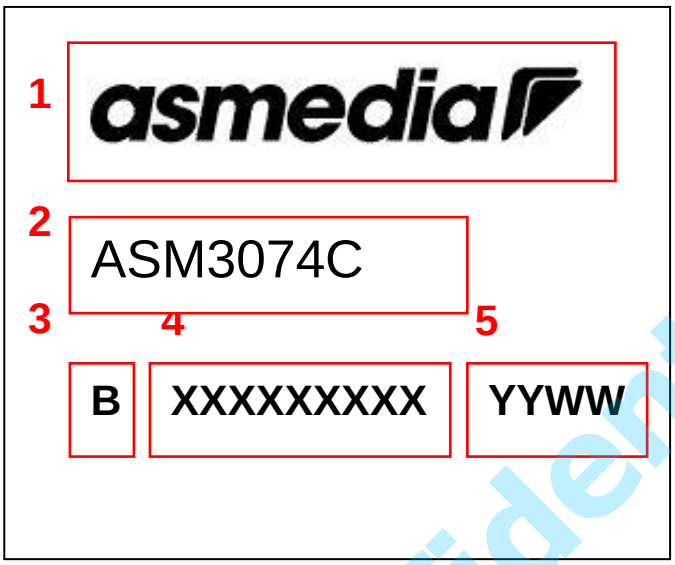


* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.13	0.18	0.23	0.005	0.007	0.009
D	10.00 bsc			0.394 bsc		
D1	9.75 bsc			0.384 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	10.00 bsc			0.394 bsc		
E1	9.75 bsc			0.384 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.065	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.13 AND 0.23 mm FROM TERMINALTIP.(REFER TO SPEC "b")
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING. (TIN PLATING)
9.APPLIED ONLY TO TERMINALS.(TIN PLATING)
10.PACKAGE CORNERS UNLESS
OTHERWISE SPECIFIED
ARE R0.175±0.025 mm.

9. Top Marking Information



1. asmedia: ASMedia Logo
2. ASM3074C: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code