1. Basic configuration

The PWM is configured using the following registers:

1. Power: In the PCONP register (Table 4–63), set bit PCPWM0/1.

   Remark: On reset, the both PWMs are enabled (PCPWM0/1 = 1).
2. Peripheral clock: In the PCLK_SEL0 register (Table 4–56), select PCLK_PWM0/1.
3. Pins: Select PWM pins and pin modes in registers PINSELn and PINMODEn (see Section 9–5).
4. Interrupts: See register PWM0/1MCR (Table 25–560) and PWM0/1CCR (Table 25–561) for match and capture events. Interrupts are enabled in the VIC using the VICIntEnable register (Table 7–106).

2. Features

- Two PWMs with the same operational features. The PWMs may be operated in a synchronized fashion by setting them both up to run at the same rate, then enabling both simultaneously. PWM0 acts as the Master and PWM1 as the slave for this use.
- Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must "release" new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32 bit Timer/Counter with a programmable 32 bit Prescaler.
- Three 32 bit capture channels take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.

3. Description

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the microcontroller. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

Figure 25–132 shows the block diagram of the PWM. The portions that have been added to the standard timer block are on the right hand side and at the top of the diagram. At the lower left of the diagram may be found the Master Enable output from the Timer Control register that allows the Master PWM (PWM0) to enable both itself and the Salve PWM (PWM1) at the same time, if desired. The Master Enable output from PWM0 is connected to the external enable input of both PWM blocks.

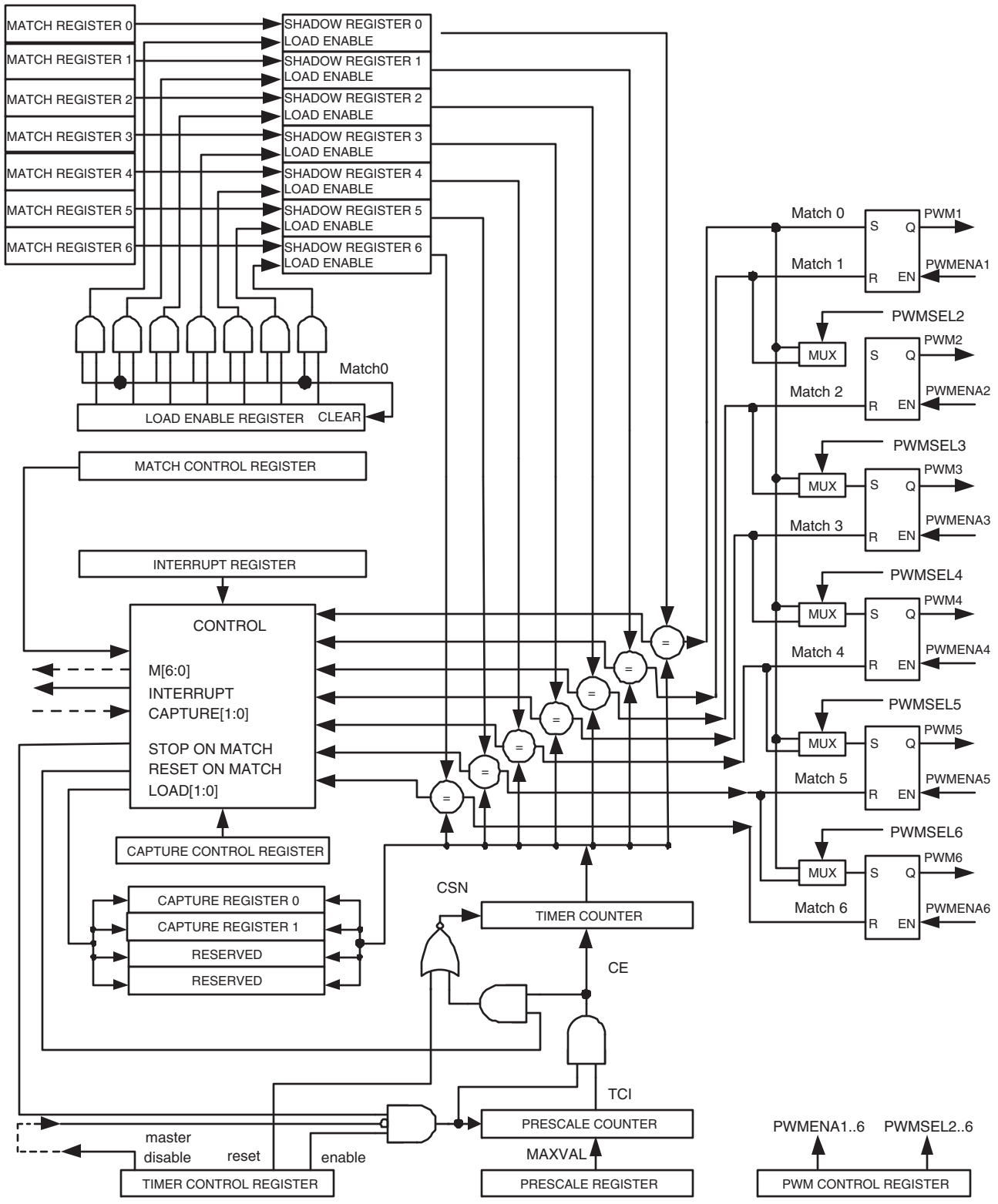


Fig 132. PWM block diagram

3.1 Rules for single edge controlled PWM outputs

1. All single edge controlled PWM outputs go high at the beginning of a PWM cycle unless their match value is equal to 0.
2. Each PWM output will go low when its match value is reached. If no match occurs (i.e. the match value is greater than the PWM rate), the PWM output remains continuously high.

3.2 Rules for double edge controlled PWM outputs

Five rules are used to determine the next value of a PWM output when a new cycle is about to begin:

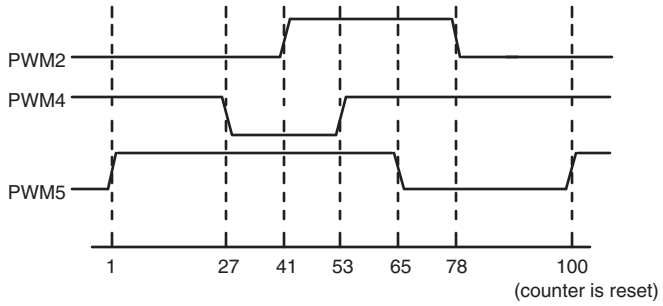
1. The match values for the **next** PWM cycle are used at the end of a PWM cycle (a time point which is coincident with the beginning of the next PWM cycle), except as noted in rule 3.
2. A match value equal to 0 or the current PWM rate (the same as the Match channel 0 value) have the same effect, except as noted in rule 3. For example, a request for a falling edge at the beginning of the PWM cycle has the same effect as a request for a falling edge at the end of a PWM cycle.
3. When match values are changing, if one of the "old" match values is equal to the PWM rate, it is used again once if the neither of the new match values are equal to 0 or the PWM rate, and there was no old match value equal to 0.
4. If both a set and a clear of a PWM output are requested at the same time, clear takes precedence. This can occur when the set and clear match values are the same as in, or when the set or clear value equals 0 and the other value equals the PWM rate.
5. If a match value is out of range (i.e. greater than the PWM rate value), no match event occurs and that match channel has no effect on the output. This means that the PWM output will remain always in one state, allowing always low, always high, or "no change" outputs.

3.3 Summary of differences from the standard timer block

1. A synchronizing register (shadow register) is added to each match register to allow changes to take effect only when requested by software, and only at the transition between PWM cycles.
2. A new Load Enable Register (LER) is added to allow software to control Match register updates. The LER contains one bit for each Match register. When a bit in the LER is written with a one, the shadow register contents for the corresponding Match channel are loaded into the actual Match register when the counter is reset (when Match 0 occurs). LER bits are reset automatically when the counter is reset.
3. A single PWM mode bit is added to the TCR register. The PWM mode enables loading the actual match registers from the shadow registers under software/hardware control as described above. When PWM mode is not enabled, the match value shadow registers are either transparent or bypassed.
4. A Master Enable bit is added to the TCR register, the value of which is brought out of the PWM block. An external enable input is added to the PWM block, that is connected to the Master Enable output of the Master PWM block.

5. The maximum number of match registers is increased to 7 in order to allow support for up to 3 double edge PWM channels. This includes the necessary match outputs, control bits, etc. for each match register:
   - Three new Match registers are added, creating Match channels 4 through 6.
   - Three additional sets of stop (S), reset (R), and interrupt (I) bits are added to the MCR register (3 per additional match register).
6. Add PWM outputs to the timer that connect a functional equivalent of an RS Flip-Flop to two match outputs. A 2-to-1 mux on each PWM output allows selection of either a single or a double edged PWM. A new register (PCR) is added to hold the control bits for the muxes (PWMSEL bits).
7. Three interrupt bits are added to the IR register.

A sample of how PWM values relate to waveform outputs is shown in Figure 25–133. PWM output logic is shown in Figure 25–132 that allows selection of either single or double edge controlled PWM outputs via the muxes controlled by the PWMSELn bits. The match register selections for various PWM outputs is shown in Table 25–554. This implementation of the PWM module supports up to N-1 single edge PWM outputs or (N-1)/2 double edge PWM outputs, where N is the number of match registers that are implemented. PWM types can be mixed if desired.For LPC2400 devices N = 7 which gives up to 6 single edge PWM outputs or up to 3 double edge PWM outputs available at the same time



The waveforms below show a single PWM cycle and demonstrate PWM outputs under the following conditions:

The timer is configured for PWM mode (counter resets to one).

Match 0 is configured to reset the timer/counter when a match event occurs.

Control bits PWMSEL2 and PWMSEL4 are set.

The Match register values are as follows:

MR0 = 100 (PWM rate)

MR1 = 41, MR2 = 78 (PWM2 output)

MR3 = 53, MR4 = 27 (PWM4 output)

MR5 = 65 (PWM5 output)

Fig 133. Sample PWM waveforms

Table 554. Set and reset inputs for PWM flip-flops

PWM Channel	Single Edge PWM (PWMSELn = 0)		Double Edge PWM (PWMSELn = 1)	
	Set by	Reset by	Set by	Reset by
1	Match 0	Match 1	Match 0[1]	Match 1[1]
2	Match 0	Match 2	Match 1	Match 2
3	Match 0	Match 3	Match 2[2]	Match 3[2]
4	Match 0	Match 4	Match 3	Match 4
5	Match 0	Match 5	Match 4[2]	Match 5[2]
6	Match 0	Match 6	Match 5	Match 6

[1] Identical to single edge mode in this case since Match 0 is the neighboring match register. Essentially, PWM1 cannot be a double edged output.

[2] It is generally not advantageous to use PWM channels 3 and 5 for double edge PWM outputs because it would reduce the number of double edge PWM outputs that are possible. Using PWM 2, PWM4, and PWM6 for double edge PWM outputs provides the most pairings.

4. Pin description

Table 25–555 gives a brief summary of each of PWM related pins.

Table 555. Pin summary

Pin	Type	Description
PWM0/1[1]	Output	Output from PWM channel 1.
PWM0/1[2]	Output	Output from PWM channel 2.
PWM0/1[3]	Output	Output from PWM channel 3.
PWM0/1[4]	Output	Output from PWM channel 4.
PWM0/1[5]	Output	Output from PWM channel 5.
PWM0/1[6]	Output	Output from PWM channel 6.
PCAP0[0] PCAP1[1:0]	Input	Capture Inputs. A transition on a capture pin can be configured to load the corresponding Capture register with the value of the Timer Counter and optionally generate an interrupt. PWM0 brings out one capture input, PWM1 brings out 2 capture inputs.

5. PWM base addresses

Table 556: Addresses for PWM 0 and 1

PWM	Base addresses
0	0xE001 4000
1	0xE001 8000

6. Register description

The PWM0 and PWM1 function adds new registers and registers bits as shown in Table 25–557 below.

Table 557. PWM0 and PWM1 register map

Generic Name	Description	Access	Reset Value[1]	PWM0 Address & Name	PWM1 Address & Name
IR	Interrupt Register. The IR can be written to clear interrupts. The IR can be read to identify which of eight possible interrupt sources are pending.	R/W	0	0xE001 4000 PWM0IR	0xE001 8000 PWM1IR
TCR	Timer Control Register. The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	R/W	0	0xE001 4004 PWM0TCR	0xE001 8004 PWM1TCR
TC	Timer Counter. The 32 bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	R/W	0	0xE001 4008 PWM0TC	0xE001 8008 PWM1TC
PR	Prescale Register. The TC is incremented every PR+1 cycles of PCLK.	R/W	0	0xE001 400C PWM0PR	0xE001 800C PWM1PR
PC	Prescale Counter. The 32 bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented. The PC is observable and controllable through the bus interface.	R/W	0	0xE000 4010 PWM0PC	0xE001 8010 PWM1PC
MCR	Match Control Register. The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	R/W	0	0xE001 4014 PWM0MCR	0xE001 8014 PWM0MCR
MR0	Match Register 0. MR0 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC sets any PWM output that is in single-edge mode, and sets PWM1 if it's in double-edge mode.	R/W	0	0xE001 4018 PWM0MR0	0xE001 8018 PWM1MR0
MR1	Match Register 1. MR1 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM1 in either edge mode, and sets PWM2 if it's in double-edge mode.	R/W	0	0xE001 401C PWM0MR1	0xE001 801C PWM1MR1
MR2	Match Register 2. MR2 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM2 in either edge mode, and sets PWM3 if it's in double-edge mode.	R/W	0	0xE001 4020 PWM0MR2	0xE001 8020 PWM1MR2
MR3	Match Register 3. MR3 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM3 in either edge mode, and sets PWM4 if it's in double-edge mode.	R/W	0	0xE001 4024 PWM0MR3	0xE001 8024 PWM1MR3
CCR	Capture Control Register. The CCR controls which edges of the capture inputs are used to load the Capture Registers and whether or not an interrupt is generated when a capture takes place.	R/W	0	0xE001 4028 PWM0CCR	0xE001 8028 PWM1CCR
CR0	Capture Register 0. PWMn CR0 is loaded with the value of the TC when there is an event on the CAPn.0 input.	RO	0	0xE001 402C PWM0CR0	-
CR1	Capture Register 1. See CR0 description.	RO	0	0xE001 4030 PWM0CR1	0xE001 8030 PWM1CR1

Table 557. PWM0 and PWM1 register map

Generic Name	Description	Access	Reset Value[1]	PWM0 Address & Name	PWM1 Address & Name
MR4	Match Register 4. MR4 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM4 in either edge mode, and sets PWM5 if it's in double-edge mode.	R/W	0	0xE001 4040 PWM0MR	0xE001 8040 PWM1MR
MR5	Match Register 5. MR5 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM5 in either edge mode, and sets PWM6 if it's in double-edge mode.	R/W	0	0xE001 4044 PWM0MR	0xE001 8044 PWM1MR
MR6	Match Register 6. MR6 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM6 in either edge mode.	R/W	0	0xE001 4048 PWM0MR	0xE001 8048 PWM1MR
PCR	PWM Control Register. Enables PWM outputs and selects PWM channel types as either single edge or double edge controlled.	R/W	0	0xE001 404C PWM0PCR	0xE001 804C PWM1PCR
LER	Load Enable Register. Enables use of new PWM match values.	R/W	0	0xE001 4050 PWM0LER	0xE001 8050 PWM1LER
CTCR	Count Control Register. The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	R/W	0	0xE001 4070 PWM0CTCR	0xE001 8070 PWM1CTCR

[1] Reset Value relects the data stored in used bits only. It does not include reserved bits content.

6.1 PWM Interrupt Register (PWM0IR - 0xE001 4000 and PWM1IR 0xE001 8000)

The PWM Interrupt register consists of eleven bits (Table 25–558), seven for the match interrupts and four reserved. If an interrupt is generated then the corresponding bit in the PWMIR will be high. Otherwise, the bit will be low. Writing a logic one to the corresponding IR bit will reset the interrupt. Writing a zero has no effect.

Table 558: PWM Interrupt Register (PWM0IR - address 0xE001 4000 and PWM1IR address 0xE001 8000) bit description

Bit	Symbol	Description	Reset Value
0	PWMMR0 Interrupt	Interrupt flag for PWM match channel 0.	0
1	PWMMR1 Interrupt	Interrupt flag for PWM match channel 1.	0
2	PWMMR2 Interrupt	Interrupt flag for PWM match channel 2.	0
3	PWMMR3 Interrupt	Interrupt flag for PWM match channel 3.	0
4	PWMCAP0 Interrupt	Interrupt flag for capture input 0	0
5	PWMCAP1 Interrupt	Interrupt flag for capture input 1 (available in PWM1IR only; this bit is reserved in PWM0IR).	0
7:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
8	PWMMR4 Interrupt	Interrupt flag for PWM match channel 4.	0

Table 558: PWM Interrupt Register (PWM0IR - address 0xE001 4000 and PWM1IR address 0xE001 8000) bit description

Bit	Symbol	Description	Reset Value
9	PWMMR5 Interrupt	Interrupt flag for PWM match channel 5.	0
10	PWMMR6 Interrupt	Interrupt flag for PWM match channel 6.	0
15:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

6.2 PWM Timer Control Register (PWM0TCR - 0xE001 4004 and PWM1TCR 0xE001 8004)

The PWM Timer Control Register (PWMTCR) is used to control the operation of the PWM Timer Counter. The function of each of the bits is shown in Table 25–559.

Table 559: PWM Timer Control Register (PWM0TCR - address 0xE001 4004 PWM1TCR address 0xE001 8004) bit description

Bit	Symbol	Value	Description	Reset Value
0	Counter Enable	1	The PWM Timer Counter and PWM Prescale Counter are enabled for counting.	0
		0	The counters are disabled.	
1	Counter Reset	1	The PWM Timer Counter and the PWM Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until this bit is returned to zero.	0
		0	Clear reset.	
2	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
3	PWM Enable	1	PWM mode is enabled (counter resets to 1). PWM mode causes the shadow registers to operate in connection with the Match registers. A program write to a Match register will not have an effect on the Match result until the corresponding bit in PWMLER has been set, followed by the occurrence of a PWM Match 0 event. Note that the PWM Match register that determines the PWM rate (PWM Match Register 0 - MR0) must be set up prior to the PWM being enabled. Otherwise a Match event will not occur to cause shadow register contents to become effective.	0
		0	Timer mode is enabled (counter resets to 0).	
4	Master Disable (PWM0 only)		The two PWMs may be synchronized using the Master Disable control bit. The Master disable bit of the Master PWM (PWM0 module) controls a secondary enable input to both PWMs, as shown in Figure 25–132. This bit has no function in the Slave PWM (PWM1).	0
		1	PWM0 is the master, and both PWMs are enabled for counting.	
		0	The PWM's are used independently, and the individual Counter Enable bits are used to control the PWM's.	
7:5	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

6.3 PWM Count Control Register (PWM0CTCR - 0xE001 4070 and PWM1CTCR 0xE001 8070)

The Count Control Register (CTCR) is used to select between Timer and Counter mode, and in Counter mode to select the pin and edge(s) for counting. The function of each of the bits is shown in Table 25–560.

Table 560: PWM Count control Register (PWM0TCR - address 0xE001 4004 and PWM1CTCR address 0xE001 8004) bit description

Bit	Symbol	Description	Reset Value
1:0	Counter/ Timer Mode	00: Timer Mode: the TC is incremented when the Prescale Counter matches the Prescale register. 01: Counter Mode: the TC is incremented on rising edges of the PCAP input selected by bits 3:2. 10: Counter Mode: the TC is incremented on falling edges of the PCAP input selected by bits 3:2. 11: Counter Mode: the TC is incremented on both edges of the PCAP input selected by bits 3:2.	00
3:2	Count Input Select	When bits 1:0 are not 00, these bits select which PCAP pin carries the signal used to increment the TC. For PWM0: 00 = PCAP0.0 (Other combinations are reserved) For PWM1: 00 = PCAP1.0, 01 = PCAP1.1(Other combinations are reserved)	00
7:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

[1] PCAP input signal frequency must not exceed PCLK/4. When the PWM clock is supplied via the PCAP pin, at no time high(low) level of the signal on this pin can last less than 1/(2×PCLK).

6.4 PWM Match Control Register (PWM0MCR - 0xE001 4014 and PWM1MCR 0xE001 8014)

The PWM Match Control registers are used to control what operations are performed when one of the PWM Match registers matches the PWM Timer Counter. The function of each of the bits is shown in Table 25–561.

Table 561: Match Control Register (PWM0MCR - address 0xE000 4014 and PWM1MCR - address 0xE000 8014) bit description

Bit	Symbol	Value	Description	Reset Value
0	PWMMR0I	1	Interrupt on PWMMR0: an interrupt is generated when PWMMR0 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
1	PWMMR0R	1	Reset on PWMMR0: the PWMTC will be reset if PWMMR0 matches it.	0
		0	This feature is disabled.	
2	PWMMR0S	1	Stop on PWMMR0: the PWMTC and PWMPC will be stopped and PWMTCR bt 0 will be set to 0 if PWMMR0 matches the PWMTC.	0
		0	This feature is disabled	

Table 561: Match Control Register (PWM0MCR - address 0xE000 4014 and PWM1MCR - address 0xE000 8014) bit description

Bit	Symbol	Value	Description	Reset Value
3	PWMMR1I	1	Interrupt on PWMMR1: an interrupt is generated when PWMMR1 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
4	PWMMR1R	1	Reset on PWMMR1: the PWMTC will be reset if PWMMR1 matches it.	0
		0	This feature is disabled.	
5	PWMMR1S	1	Stop on PWMMR1: the PWMTC and PWMPC will be stopped and PWMTCR bit 0 will be set to 0 if PWMMR1 matches the PWMTC.	0
		0	This feature is disabled.	
6	PWMMR2I	1	Interrupt on PWMMR2: an interrupt is generated when PWMMR2 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
7	PWMMR2R	1	Reset on PWMMR2: the PWxMTC will be reset if PWMMR2 matches it.	0
		0	This feature is disabled.	
8	PWMMR2S	1	Stop on PWMMR2: the PWMTC and PWMPC will be stopped and PWMTCR bit 0 will be set to 0 if PWMMR2 matches the PWxMTC.	0
		0	This feature is disabled	
9	PWMMR3I	1	Interrupt on PWMMR3: an interrupt is generated when PWMMR3 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
10	PWMMR3R	1	Reset on PWMMR3: the PWMTC will be reset if PWMMR3 matches it.	0
		0	This feature is disabled	
11	PWMMR3S	1	Stop on PWMMR3: The PWMTC and PWMPC will be stopped and PWMTCR bit 0 will be set to 0 if PWMMR3 matches the PWMTC.	0
		0	This feature is disabled	
12	PWMMR4I	1	Interrupt on PWMMR4: An interrupt is generated when PWMMR4 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
13	PWMMR4R	1	Reset on PWMMR4: the PWMTC will be reset if PWMMR4 matches it.	0
		0	This feature is disabled.	
14	PWMMR4S	1	Stop on PWMMR4: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR4 matches the PWMTC.	0
		0	This feature is disabled	
15	PWMMR5I	1	Interrupt on PWMMR5: An interrupt is generated when PWMMR5 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	

Table 561: Match Control Register (PWM0MCR - address 0xE000 4014 and PWM1MCR - address 0xE000 8014) bit description

Bit	Symbol	Value	Description	Reset Value
16	PWMMR5R	1	Reset on PWMMR5: the PWMTC will be reset if PWMMR5 matches it.	0
		0	This feature is disabled.	
17	PWMMR5S	1	Stop on PWMMR5: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR5 matches the PWMTC.	0
		0	This feature is disabled	
18	PWMMR6I	1	Interrupt on PWMMR6: an interrupt is generated when PWMMR6 matches the value in the PWMTC.	0
		0	This interrupt is disabled.	
19	PWMMR6R	1	Reset on PWMMR6: the PWMTC will be reset if PWMMR6 matches it.	0
		0	This feature is disabled.	
20	PWMMR6S	1	Stop on PWMMR6: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR6 matches the PWMTC.	0
		0	This feature is disabled	
31:21	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

6.5 PWM Capture Control Register (PWM0CCR - 0xE001 4028 and PWM1CCR 0xE001 8028)

The Capture Control register is used to control whether any of the Capture registers is loaded with the value in the Timer Counter when a capture event occurs on PCAP0[0] or PCAP1[1:0], and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges. In the descriptions below, “n” represents the Timer number, 0 or 1.

Note: If Counter mode is selected for a particular PCAP input in the CTCR, the 3 bits for that input in this register should be programmed as 000, but capture and/or interrupt can be selected for the other two PCAP inputs.

Table 562: PWM Capture Control Register (PWM0CCR - address 0xE001 4028 and PWM1CCR address 0xE001 8028) bit description

Bit	Symbol	Value	Description	Reset Value
0	Capture on PCAPn.0 rising edge	0	This feature is disabled.	0
		1	A synchronously sampled rising edge on the PCAPn.0 input will cause CR0 to be loaded with the contents of the TC.	
1	Capture on PCAPn.0 falling edge	0	This feature is disabled.	0
		1	A synchronously sampled falling edge on PCAPn.0 will cause CR0 to be loaded with the contents of TC.	
2	Interrupt on PCAPn.0 event	0	This feature is disabled.	0
		1	A CR0 load due to a PCAPn.0 event will generate an interrupt.	

Table 562: PWM Capture Control Register (PWM0CCR - address 0xE001 4028 and PWM1CCR address 0xE001 8028) bit description

Bit	Symbol	Value	Description	Reset Value
3	Capture on PCAPn.1 rising edge[1]	0	This feature is disabled.	0
		1	A synchronously sampled rising edge on the PCAPn.1 input will cause CR1 to be loaded with the contents of the TC.	
4	Capture on PCAPn.1 falling edge[1]	0	This feature is disabled.	0
		1	A synchronously sampled falling edge on PCAPn.1 will cause CR1 to be loaded with the contents of TC.	
5	Interrupt on PCAPn.1 event[1]	0	This feature is disabled.	0
		1	A CR1 load due to a PCAPn.1 event will generate an interrupt.	
31:6	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

[1] Reserved for PWM0.

6.6 PWM Control Registers (PWM0PCR - 0xE001 404C and PWM1PCR 0xE001 804C)

The PWM Control registers are used to enable and select the type of each PWM channel. The function of each of the bits are shown in Table 25–563.

Table 563: PWM Control Registers (PWMPCR - address 0xE001 404C and PWM1PCR address 0xE001 804C) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	Unused		Unused, always zero.	NA
2	PWMSEL2		PWM2 output single/double edge mode control.	0
		1	Double edge controlled mode is selected.	
		0	Single edge controlled mode is selected.	
3	PWMSEL3	1	PWM3 output edge control. See PWMSEL2 for details.	0
4	PWMSEL4	1	PWM4 output edge control. See PWMSEL2 for details.	0
5	PWMSEL5	1	PWM5 output edge control. See PWMSEL2 for details.	0
6	PWMSEL6	1	PWM6 output edge control. See PWMSEL2 for details.	0
8:7	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
9	PWMENA1		The PWM1 output enable control.	0
		0	The PWM output is disabled.	
		1	The PWM output is enabled.	
10	PWMENA2		The PWM2 output enable control. See PWMENA1 for details.	0
11	PWMENA3		The PWM3 output enable control. See PWMENA1 for details.	0
12	PWMENA4		The PWM4 output enable control. See PWMENA1 for details.	0
13	PWMENA5		The PWM5 output enable control. See PWMENA1 for details.	0
14	PWMENA6		The PWM6 output enable control. See PWMENA1 for details.	0
31:15	Unused		Unused, always zero.	NA

6.7 PWM Latch Enable Register (PWM0LER - 0xE001 4050 and PWM1LER 0xE001 8050)

The PWM Latch Enable registers are used to control the update of the PWM Match registers when they are used for PWM generation. When software writes to the location of a PWM Match register while the Timer is in PWM mode, the value is actually held in a shadow register and not used immediately.

When a PWM Match 0 event occurs (normally also resetting the timer in PWM mode), the contents of shadow registers will be transferred to the actual Match registers if the corresponding bit in the Latch Enable register has been set. At that point, the new values will take effect and determine the course of the next PWM cycle. Once the transfer of new values has taken place, all bits of the LER are automatically cleared. Until the corresponding bit in the PWMLER is set and a PWM Match 0 event occurs, any value written to the PWM Match registers has no effect on PWM operation.

For example, if PWM is configured for double edge operation and is currently running, a typical sequence of events for changing the timing would be:

- Write a new value to the PWM Match1 register.
- Write a new value to the PWM Match2 register.
- Write to the PWMLER, setting bits 1 and 2 at the same time.
- The altered values will become effective at the next reset of the timer (when a PWM Match 0 event occurs).

The order of writing the two PWM Match registers is not important, since neither value will be used until after the write to PWMLER. This insures that both values go into effect at the same time, if that is required. A single value may be altered in the same way if needed.

The function of each of the bits in the PWMLER is shown in Table 25–564.

Table 564: PWM Latch Enable Register (PWM0LER - address 0xE001 4050 and PWM1LER address 0xE001 8050) bit description

Bit	Symbol	Description	Reset Value
0	Enable PWM Match 0 Latch	PWM MR0 register update control. Writing a one to this bit allows the last value written to the PWM Match Register 0 to be become effective when the timer is next reset by a PWM Match event. See Section 25–6.4 “PWM Match Control Register (PWM0MCR - 0xE001 4014 and PWM1MCR 0xE001 8014)”.	0
1	Enable PWM Match 1 Latch	PWM MR1 register update control. See bit 0 for details.	0
2	Enable PWM Match 2 Latch	PWM MR2 register update control. See bit 0 for details.	0
3	Enable PWM Match 3 Latch	PWM MR3 register update control. See bit 0 for details.	0
4	Enable PWM Match 4 Latch	PWM MR4 register update control. See bit 0 for details.	0

Table 564: PWM Latch Enable Register (PWM0LER - address 0xE001 4050 and PWM1LER address 0xE001 8050) bit description

Bit	Symbol	Description	Reset Value
5	Enable PWM Match 5 Latch	PWM MR5 register update control. See bit 0 for details.	0
6	Enable PWM Match 6 Latch	PWM MR6 register update control. See bit 0 for details.	0
7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA