System on Chip Design

Project Report

ANIK BARUA
UTU Student ID: 511580

Shift Register:

VHDL Code:

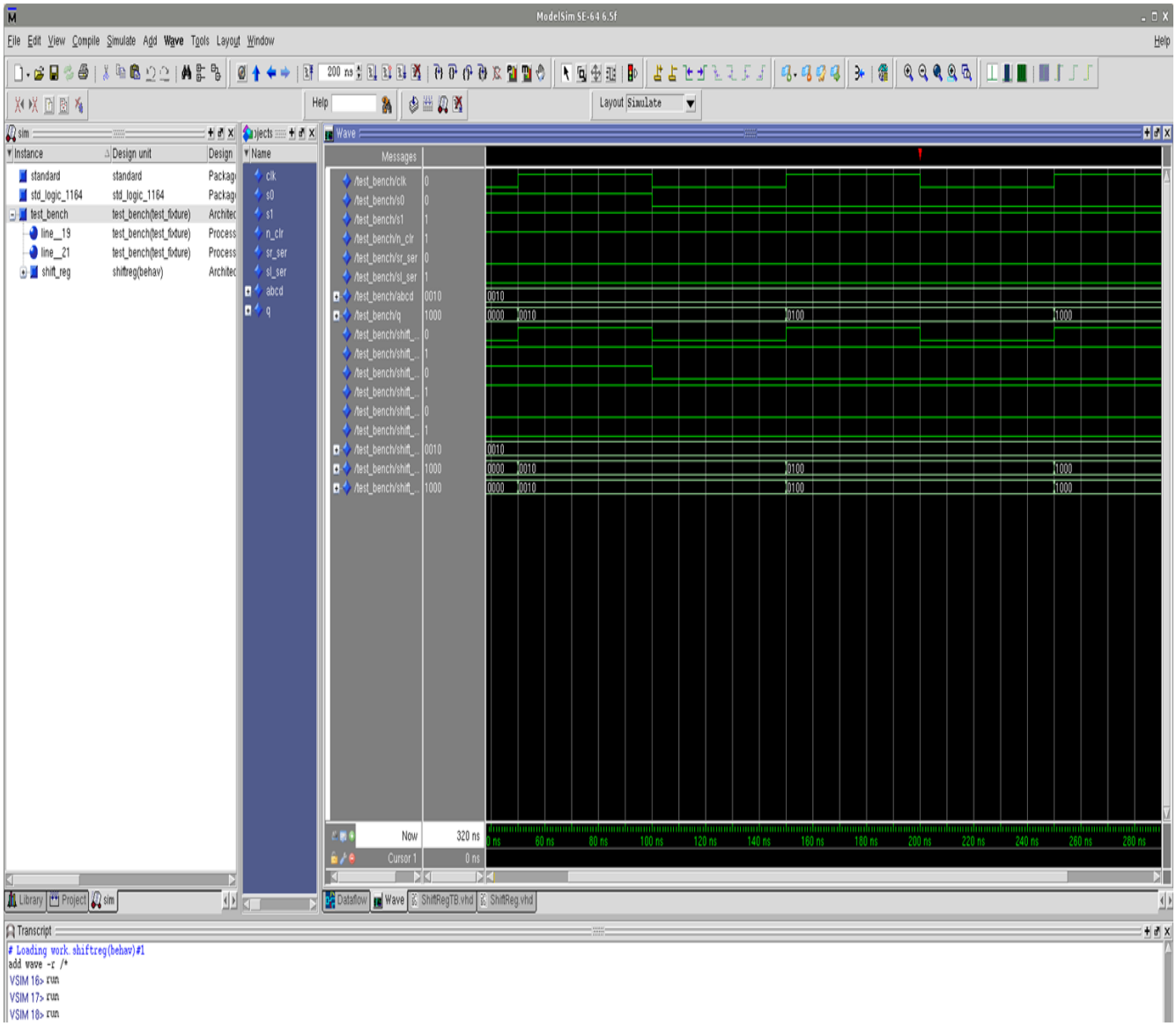
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY ShiftReg IS
PORT(clk, n_clr, s0, s1, sr_ser, sl_ser : IN std_logic;
abcd : IN std_logic_vector(3 DOWNTO 0);
q : OUT std_logic_vector(3 DOWNTO 0));
END ShiftReg;
ARCHITECTURE behav OF ShiftReg IS
SIGNAL temp : std_logic_vector(3 DOWNTO 0);
BEGIN
PROCESS(clk, n_clr)
BEGIN
If n_clr = '0' THEN -- asynchronous clear
temp <= "0000";
ELSIF clk'EVENT AND clk = '1' THEN
IF s0 = '1' AND s1 = '1' THEN -- synch load
temp <= abcd;
ELSIF s0 = '1' AND s1 = '0' THEN -- shift right
temp <= sr_ser & temp(3 DOWNTO 1);
ELSIF s0 = '0' AND s1 = '1' THEN -- shift left;
temp <= temp(2 DOWNTO 0) & sl_ser;
ELSE -- inhibit mode
temp <= temp;
END IF;
END IF;
END PROCESS;
q <= temp;
END behav;
```

VHDL Test bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY test_bench IS
END test_bench;
ARCHITECTURE test_fixture OF test_bench IS
COMPONENT ShiftReg
PORT(clk, n_clr, s0, s1, sr_ser, sl_ser : IN std_logic;
abcd : IN std_logic_vector(3 DOWNTO 0);
q : OUT std_logic_vector(3 DOWNTO 0));
END COMPONENT;
FOR all: ShiftReg USE ENTITY work.ShiftReg; -- configuration
-- define internal signals for connecting ShiftReg to driver
SIGNAL clk, s0, s1, n_clr, sr_ser, sl_ser : std_logic := '0';
SIGNAL abcd, q : std_logic_vector(3 DOWNTO 0);
BEGIN
-- instantiate ShiftReg shift register component
shift_reg:
ShiftReg PORT MAP(clk, n_clr, s0, s1, sr_ser, sl_ser, abcd, q);
clk <= NOT clk AFTER 50 ns; -- create system clock
PROCESS
BEGIN
WAIT FOR 10 ns;
ASSERT q = "0000"
REPORT "ERROR: clear failed"
SEVERITY error;
WAIT FOR 20 ns;
n_clr <= '1';
-- check synchronous load
```

```
s0 <= '1';
s1 <= '1';
abcd <= "0010";
WAIT UNTIl clk = '0'; -- first falling edge
ASSERT q = "0010"
REPORT "ERROR: load failed"
SEVERITY error;
-- now check shift left
s0 <= '0';
WAIT UNTIL clk = '0'; -- next falling clock edge
ASSERT q = "0011"
REPORT "ERROR: shift left failed"
SEVERITY error;
FOR i IN 0 TO 2 LOOP -- three more shift lefts
IF i = 1 THEN
sl_ser <= '1';
ELSE
sl_ser <= '0';
END IF;
WAIT UNTIL clk = '0';
END LOOP;
ASSERT q = "1010"
REPORT "ERROR: serial shift left failed"
SEVERITY error;
WAIT; -- suspend
END PROCESS;
END test_fixture;
```

Simulation of the Design:

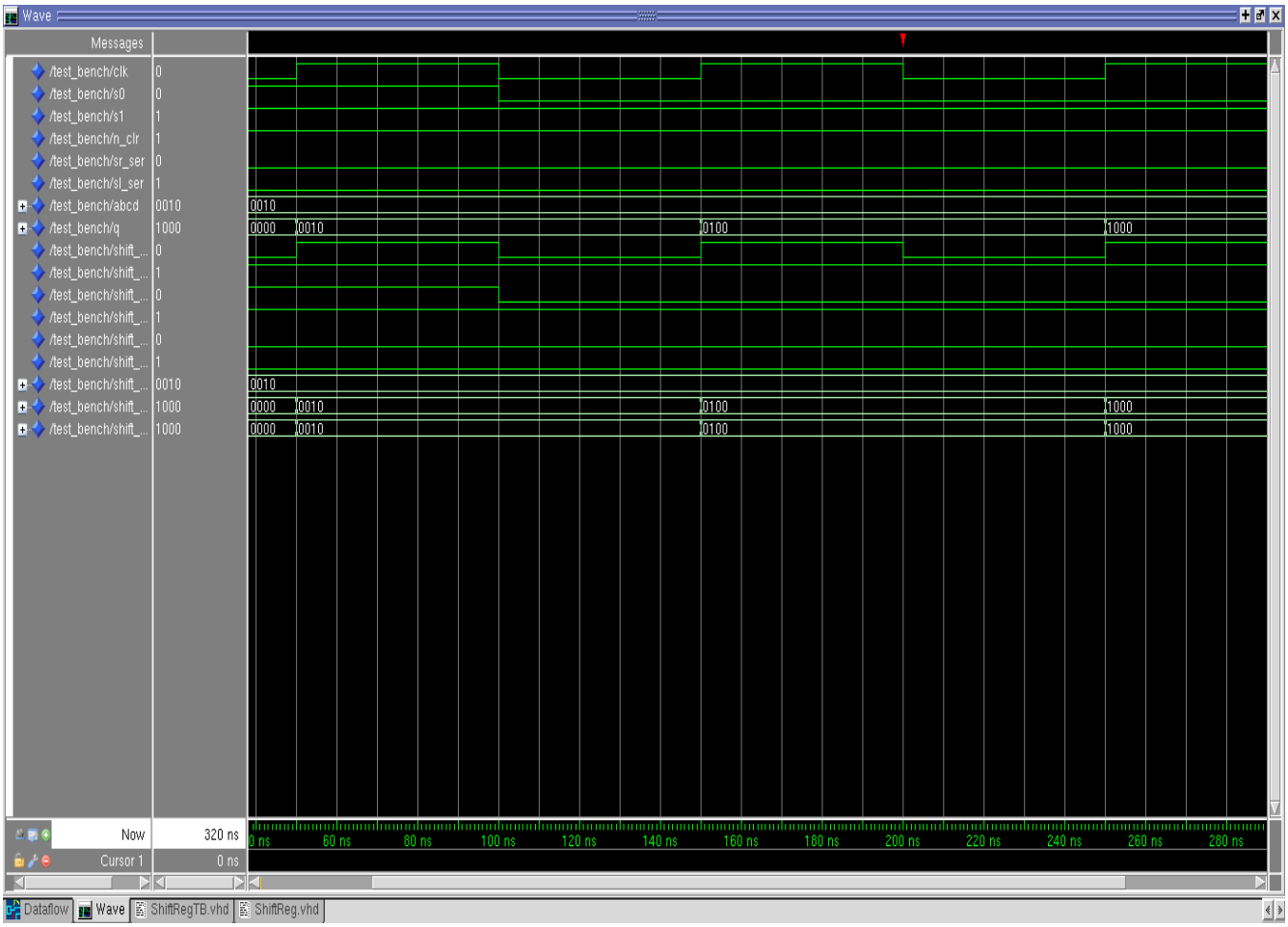


Synthesize - The extracted netlist:

```
// Generated by Cadence Encounter(R) RTL Compiler RC9.1.203 - v09.10-s242_1

module ShiftReg(clk, n_clr, s0, s1, sr_ser, sl_ser, abcd, q);
  input clk, n_clr, s0, s1, sr_ser, sl_ser;
  input [3:0] abcd;
  output [3:0] q;
  wire clk, n_clr, s0, s1, sr_ser, sl_ser;
  wire [3:0] abcd;
  wire [3:0] q;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
  QDFFRBX1 \temp_reg[0] (.RB (n_clr), .CK (clk), .D (n_13), .Q (q[0]));
  QDFFRBX1 \temp_reg[1] (.RB (n_clr), .CK (clk), .D (n_12), .Q (q[1]));
  QDFFRBX1 \temp_reg[2] (.RB (n_clr), .CK (clk), .D (n_14), .Q (q[2]));
  QDFFRBX1 \temp_reg[3] (.RB (n_clr), .CK (clk), .D (n_15), .Q (q[3]));
  ND2XLP g348(.I1 (n_11), .I2 (n_1), .O (n_15));
  ND2XLP g347(.I1 (n_2), .I2 (n_6), .O (n_14));
  ND2XLP g349(.I1 (n_5), .I2 (n_10), .O (n_13));
  ND2XLP g350(.I1 (n_0), .I2 (n_9), .O (n_12));
  AOI22XLP g357(.A1 (n_4), .A2 (q[3]), .B1 (n_3), .B2 (abcd[3]), .O
      (n_11));
  AOI22XLP g352(.A1 (n_7), .A2 (q[1]), .B1 (n_8), .B2 (sl_ser), .O
      (n_10));
  AOI22XLP g358(.A1 (n_8), .A2 (q[0]), .B1 (n_7), .B2 (q[2]), .O (n_9));
  AOI22XLP g353(.A1 (n_8), .A2 (q[1]), .B1 (n_7), .B2 (q[3]), .O (n_6));
  AOI22XLP g354(.A1 (n_4), .A2 (q[0]), .B1 (n_3), .B2 (abcd[0]), .O
      (n_5));
  AOI22XLP g355(.A1 (n_4), .A2 (q[2]), .B1 (n_3), .B2 (abcd[2]), .O
      (n_2));
```

```
  AOI22XLP g356(.A1 (n_8), .A2 (q[2]), .B1 (n_7), .B2 (sr_ser), .O
      (n_1));
  AOI22XLP g351(.A1 (n_4), .A2 (q[1]), .B1 (n_3), .B2 (abcd[1]), .O
      (n_0));
  AN2B1XLP g359(.I1 (s1), .B1 (s0), .O (n_8));
  AN2B1XLP g360(.I1 (s0), .B1 (s1), .O (n_7));
  NR2XLP g361(.I1 (s0), .I2 (s1), .O (n_4));
  AN2XLP g362(.I1 (s1), .I2 (s0), .O (n_3));
endmodule
```

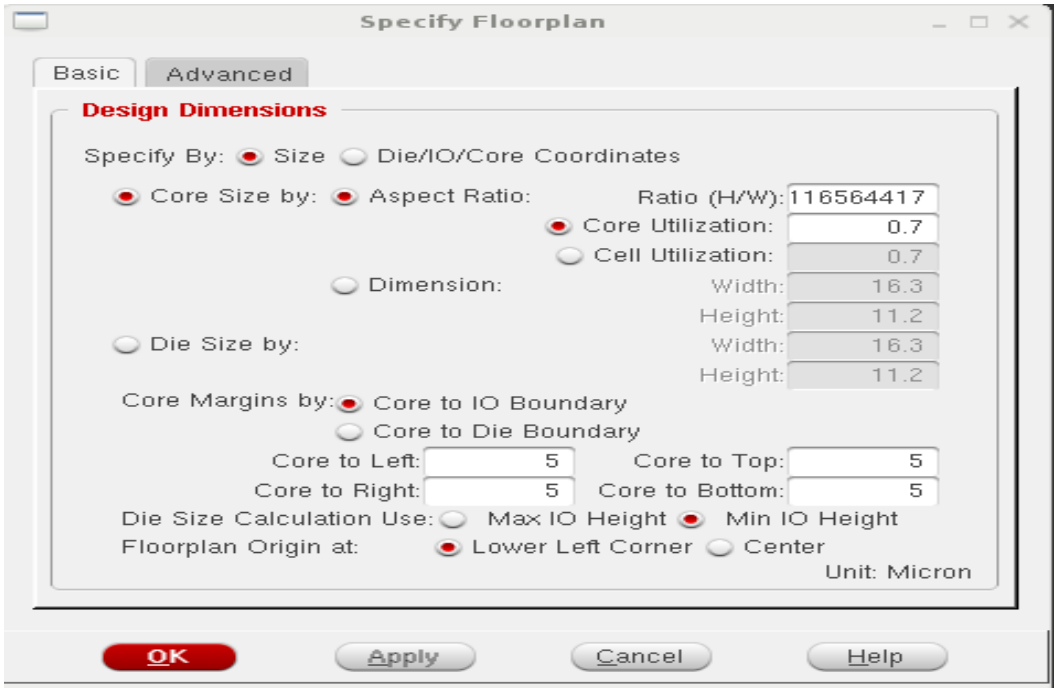
Post Synthesis Simulation waveform:

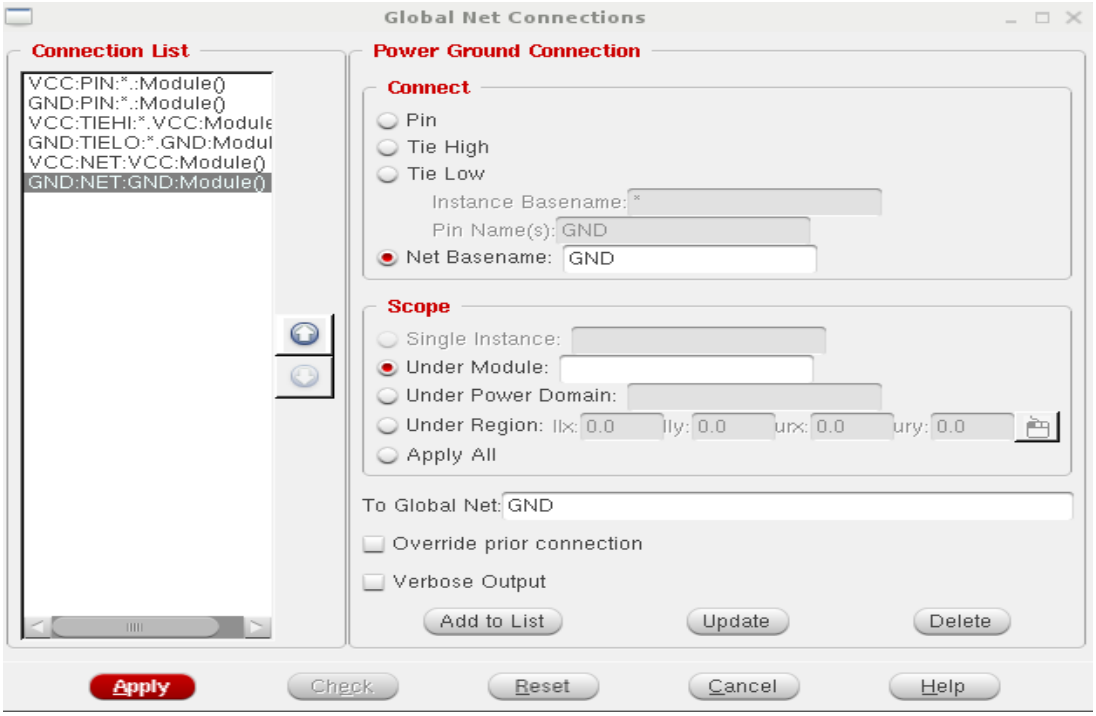


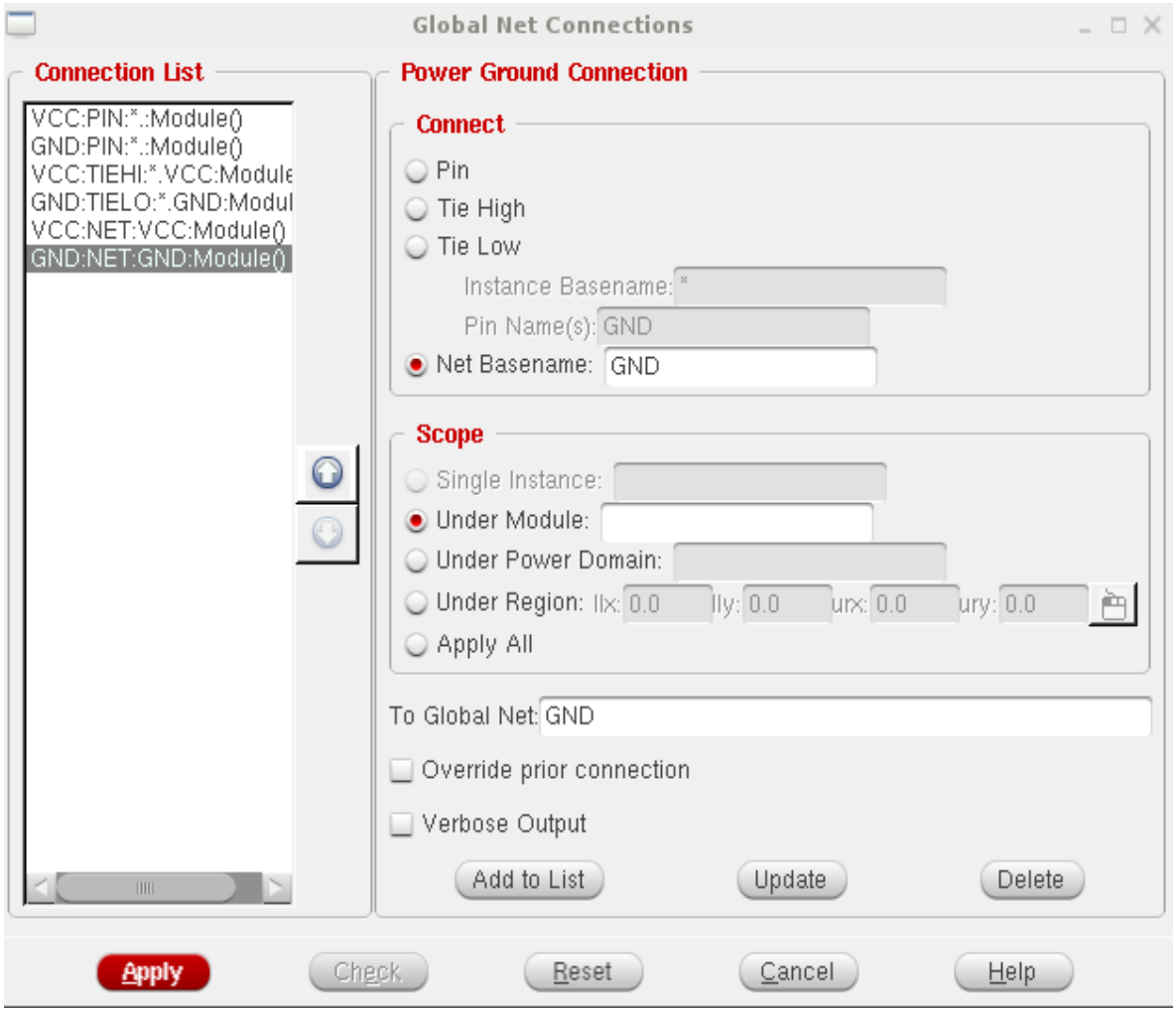
Area of the design:

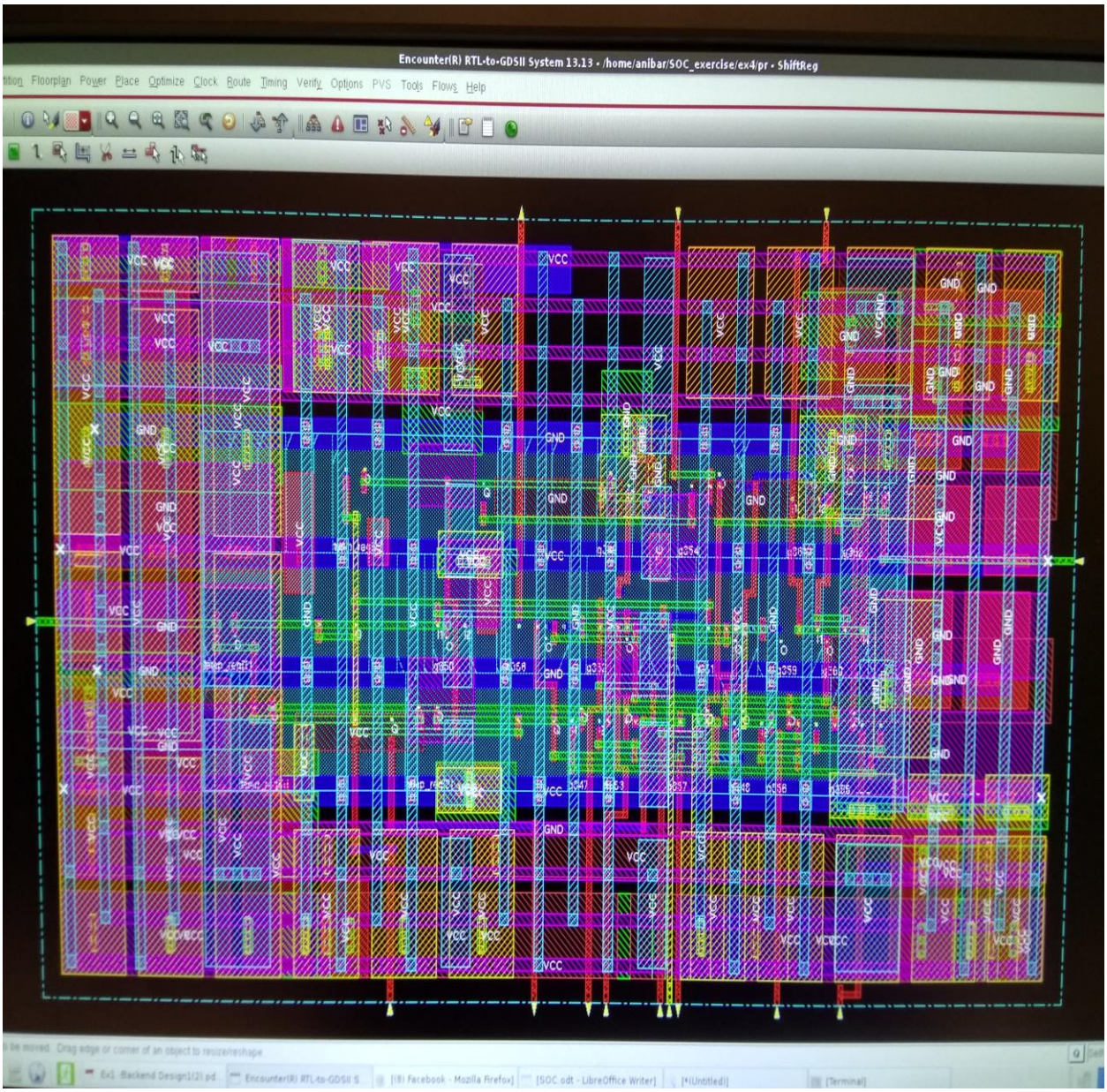
```
Global mapping status
=====================
                         Worst
                Total     Neg
Operation        Area    Slack  Worst Path
-------------------------------------------------------------------------------
 global_map       163        0  N/A

Global incremental target info
==============================
Cost Group 'default' target slack: Unconstrained


Global incremental optimization status
======================================
                         Worst
                Total     Neg
Operation        Area    Slack  Worst Path
-------------------------------------------------------------------------------
 global_inc       163        0  N/A
                         Worst  - - - - DRC Totals - - - -
                Total     Neg       Max       Max    Max
Operation        Area    Slack     Trans      Cap   Fanout
-------------------------------------------------------------------------------
 init_iopt        163        0         0        0        0

Incremental optimization status
===============================
                         Worst  - - - - DRC Totals - - - -
                Total     Neg       Max       Max    Max
Operation        Area    Slack     Trans      Cap   Fanout
-------------------------------------------------------------------------------
 init_delay       163        0         0        0        0
 init_drc         163        0         0        0        0
 init_area        163        0         0        0        0

Incremental optimization status
===============================
                         Worst  - - - - DRC Totals - - - -
                Total     Neg       Max       Max    Max
Operation        Area    Slack     Trans      Cap   Fanout
-------------------------------------------------------------------------------
 init_delay       163        0         0        0        0
 init_drc         163        0         0        0        0
 init_area        163        0         0        0        0

  Done mapping ShiftReg
  Synthesis succeeded.
rc:/> write_hdl > netlist_syn.v
rc:/> write_sdc > syn.sdc
```

Place and Route:

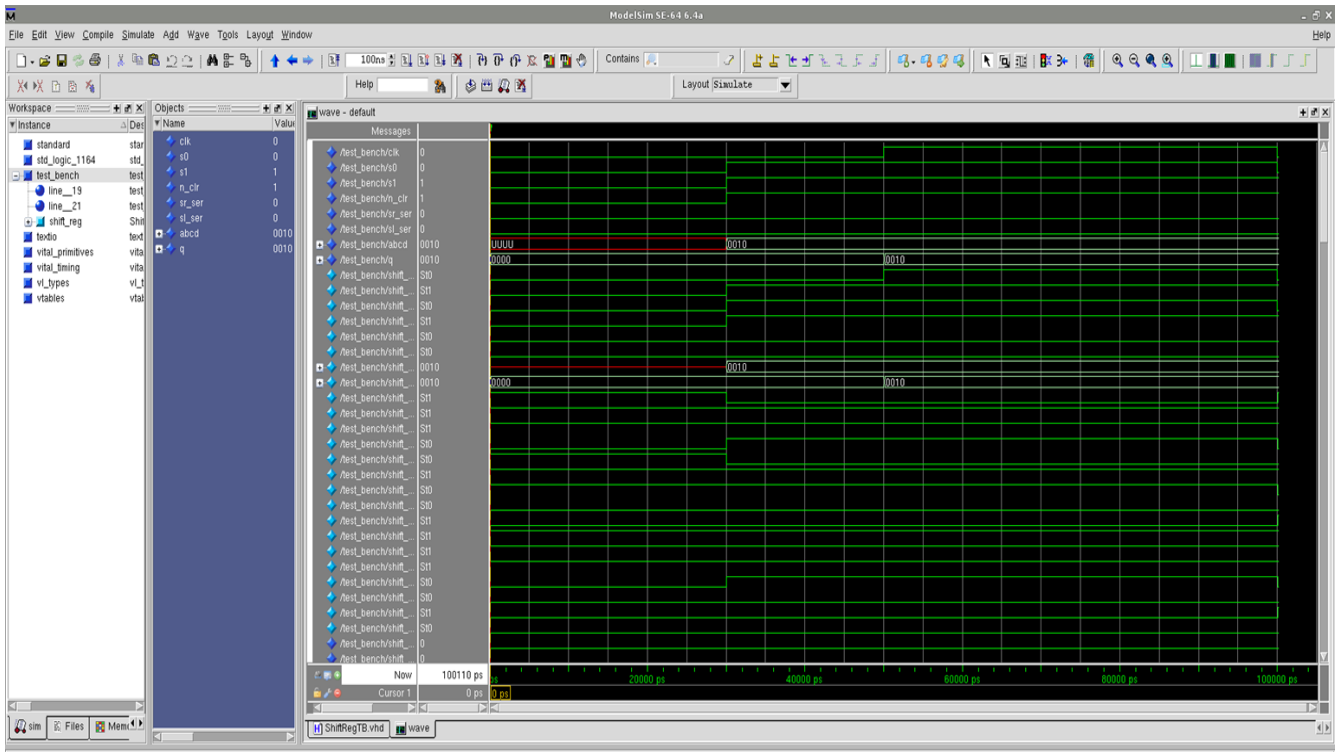


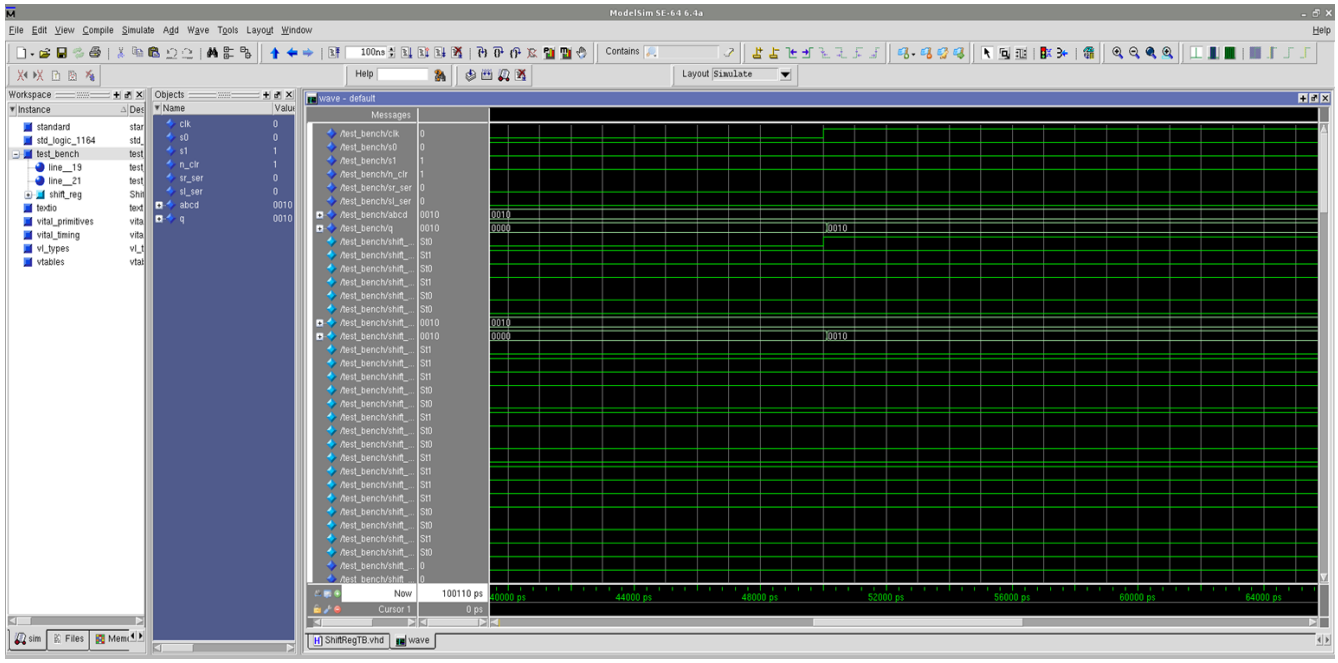



Global Net Connections
Connection List
VCC:PIN:*.:Module()
GND:PIN:*.:Module()
VCC:TIEHI:*.VCC:Module
GND:TIELO:*.GND:Modul
VCC:NET:VCC:Module()
GND:NET:GND:Module()
Power Ground Connection
Connect
Pin
Tie High
Tie Low
Instance Basename: *
Pin Name(s): GND
Net Basename: GND
Scope
Single Instance:
Under Module:
Under Power Domain:
Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
Apply All
To Global Net: GND
Override prior connection
Verbose Output
Add to List
Update
Delete
Apply
Check
Reset
Cancel
Help


Encounter(R) RTL-to-GDSII System 13.13 - /home/anibar/SOC_exercise/ex4/pr - ShiftReg
tition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help
VCC
GND

Post Synthesis Simulation:





Power Report using UMC 90 nm technology and 1.2v:

```
Information: Updating design information... (UID-85)
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
     -analysis_effort low
Design : LS194
Version: Y-2006.06
Date   : Thu Nov  3 17:27:45 2016
****************************************


Library(s) Used:

    fsd0a_a_generic_core_1d2vtc (File:
/tech/umc/faraday/Core/fsd0a_a/2007Q1v1.7/GENERIC_CORE_1D2V/FrontEnd/s
ynopsys/fsd0a_a_generic_core_1d2vtc.db)


Operating Conditions: TCCOM   Library: fsd0a_a_generic_core_1d2vtc
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
LS194                  enG5K             fsd0a_a_generic_core_1d2vtc


Global Operating Voltage = 1.2
Power-specific unit information:
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.0964 uW   (75%)
  Net Switching Power  = 367.8801 nW   (25%)
                         ---------
Total Dynamic Power    =   1.4643 uW  (100%)

Cell Leakage Power     = 321.4691 nW
```

Area Report:

```
****************************************
Report : area
Design : LS194
Version: Y-2006.06
Date   : Thu Nov  3 17:28:52 2016
****************************************

Library(s) Used:

    fsd0a_a_generic_core_1d2vtc (File:
/tech/umc/faraday/Core/fsd0a_a/2007Q1v1.7/GENERIC_CORE_1D2V/Fron
tEnd/synopsys/fsd0a_a_generic_core_1d2vtc.db)

Number of ports:               14
Number of nets:                23
Number of cells:               13
Number of references:           5

Combinational area:         70.000000
Noncombinational area:     100.000000
Net Interconnect area:      undefined  (Wire load has zero net
area)

Total cell area:           170.000000
Total area:                 undefined
```