Topic of the project:
Project name: "ASIC design with open source tools"

Developing of an low resolution ADC. As example an 4-Bit ADC with conversion of the thermometer code into binary code.

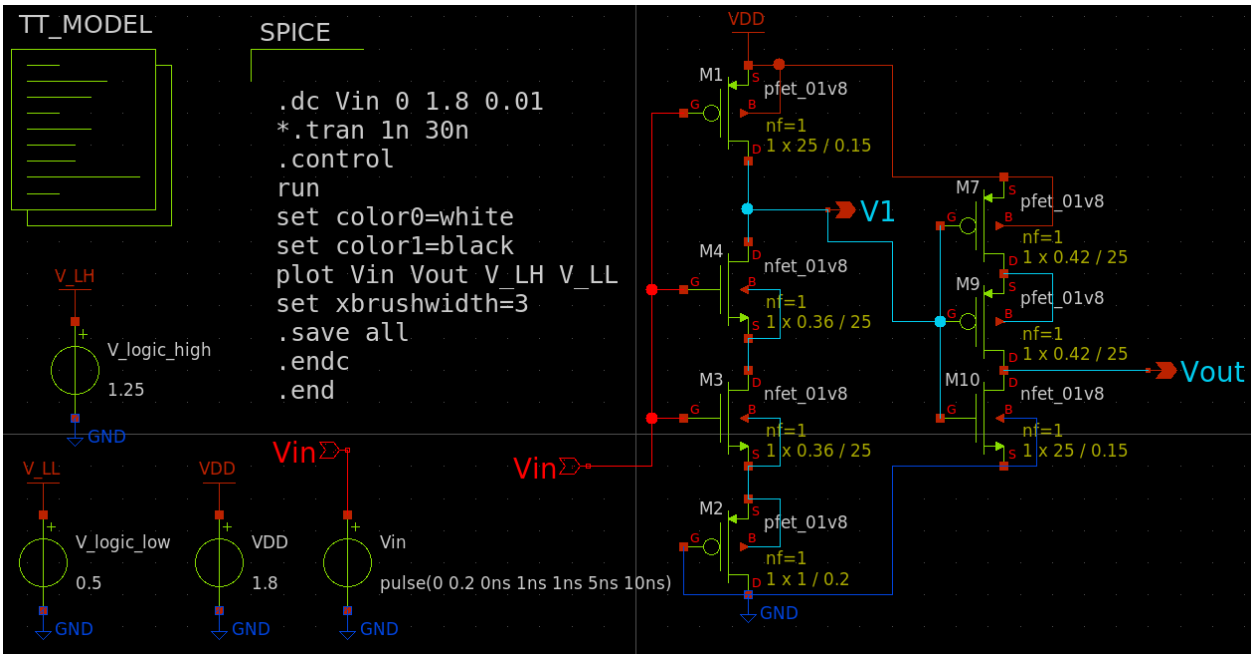
Steps:

A small CMOS inverter with xschem and the sky130a technology (PDK) and simulate the circuit with ngspice:

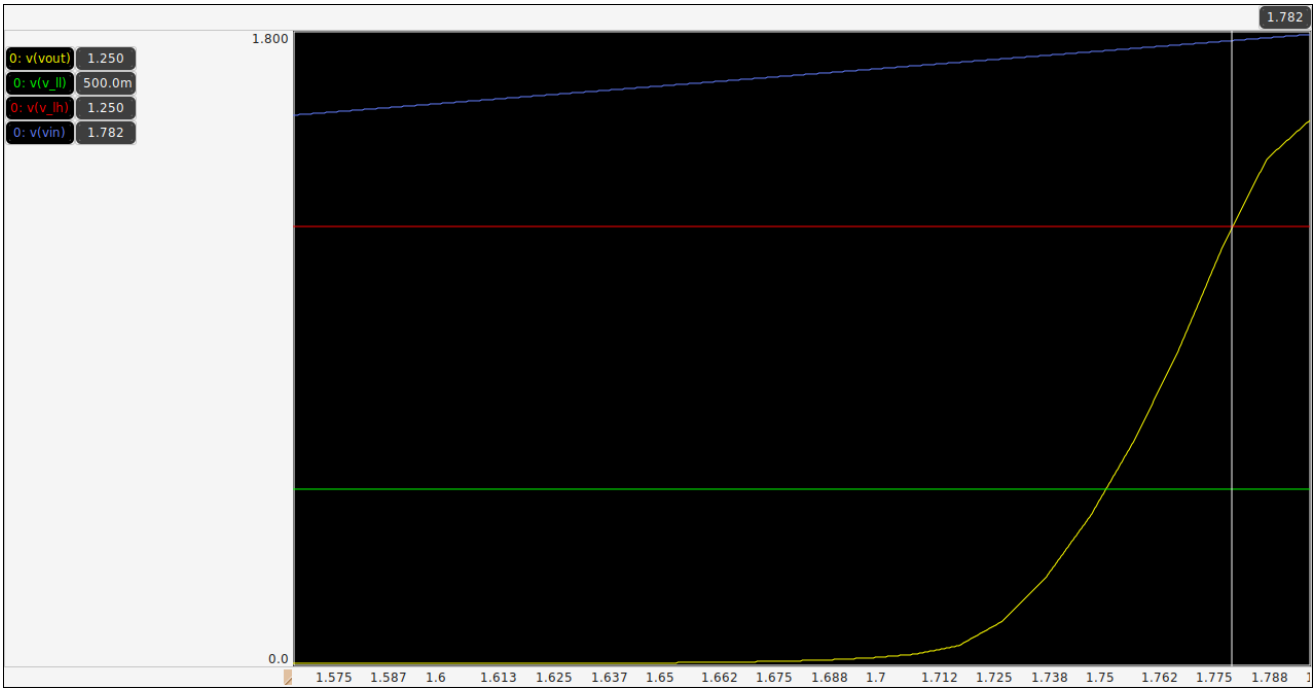
Binary Logic level assumption

https://en.wikipedia.org/wiki/Logic_level

Technology	L Voltage	H Voltage	note
CMOS	0 to 30% of Vdd	70% of Vdd to Vdd	Vdd = Supply voltage
	≈0.5 Volt	≈1.25 Volts	Vdd = 1.8 Volts



The above figure is the schematic for 15th threshold point of the analogue part of the ADC. The plot is as follows:



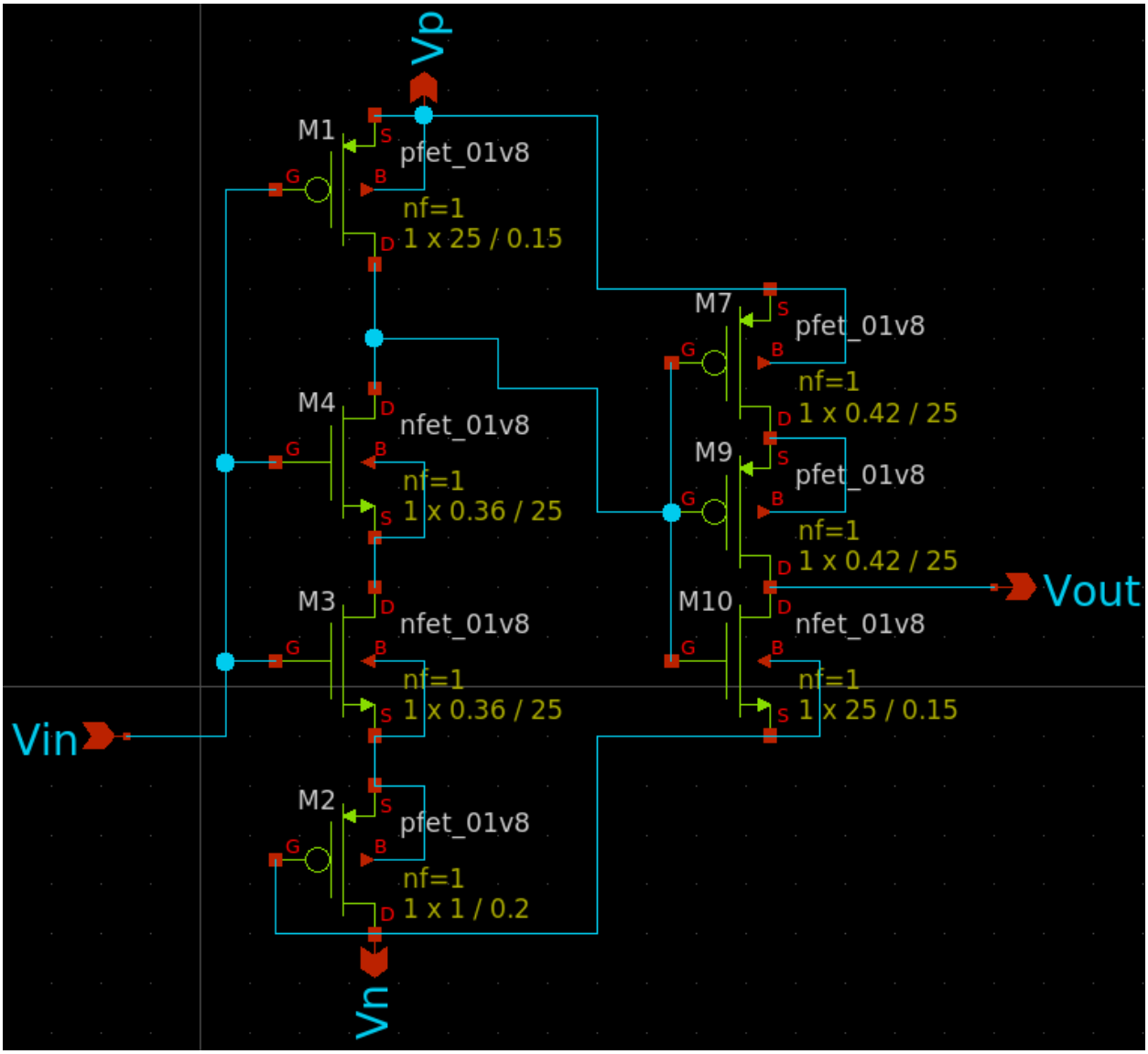
The inverter will switch from logic-low to logic-high when input voltage exceeds 1.782 volts. So, for this inverter the threshold is 1.782 volts.

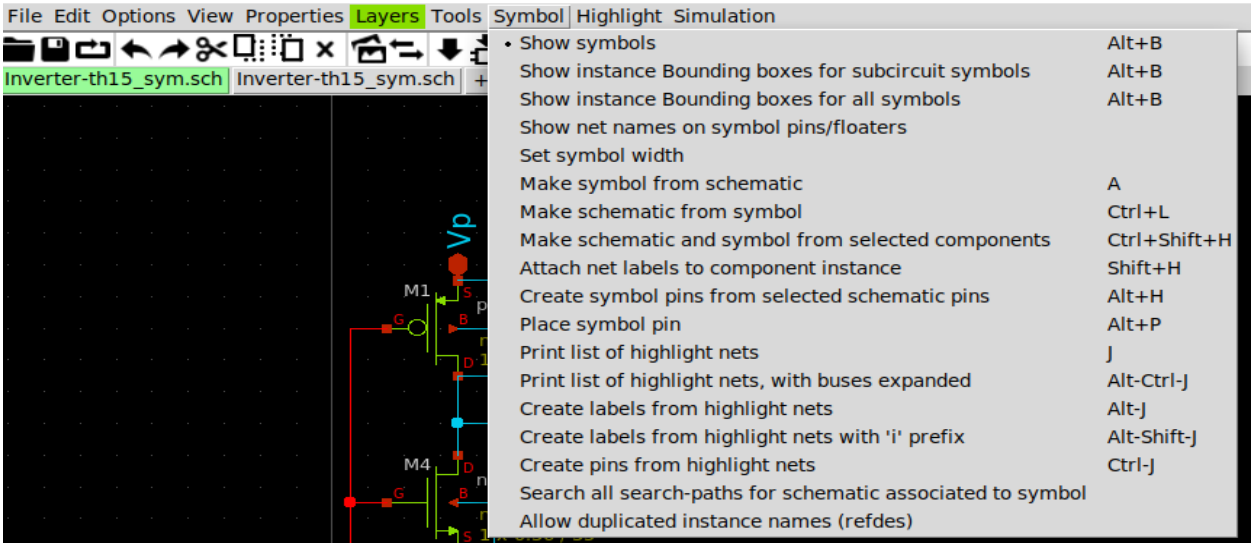
For a 4-bit ADC we need 16 voltage level including zero (0~1.782 volts). The quantization should be 1.782/15=0.1188 volts.

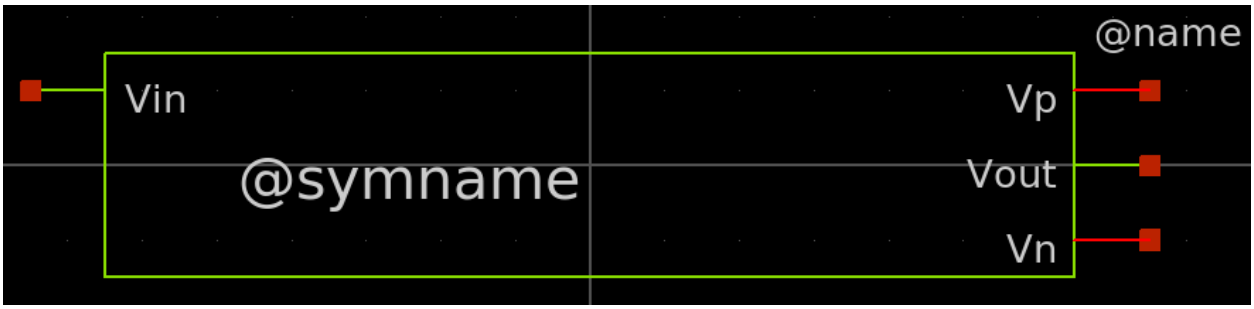
Vdd = 1.8 V

Th. 15: 1.782

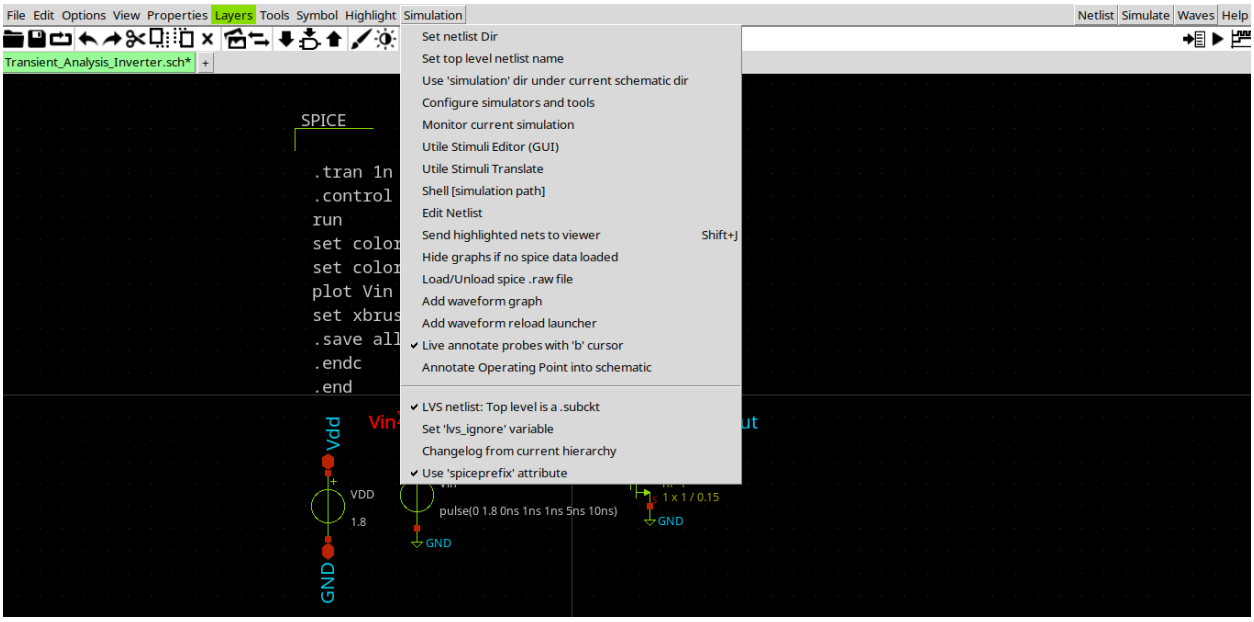
For calculation the schematic and the plot already mentioned earlier. Remove all source to make symbol from schematic. As the symbol will have to be connected to Vdd and GND, those pins are replaced with Vp and Vn accordingly.


Vp
M1
pfet_01v8
nf=1
1 x 25 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 25
M4
nfet_01v8
nf=1
1 x 0.36 / 25
M9
pfet_01v8
nf=1
1 x 0.42 / 25
Vout
M3
nfet_01v8
nf=1
1 x 0.36 / 25
M10
nfet_01v8
nf=1
1 x 25 / 0.15
Vin
M2
pfet_01v8
nf=1
1 x 1 / 0.2
Vn

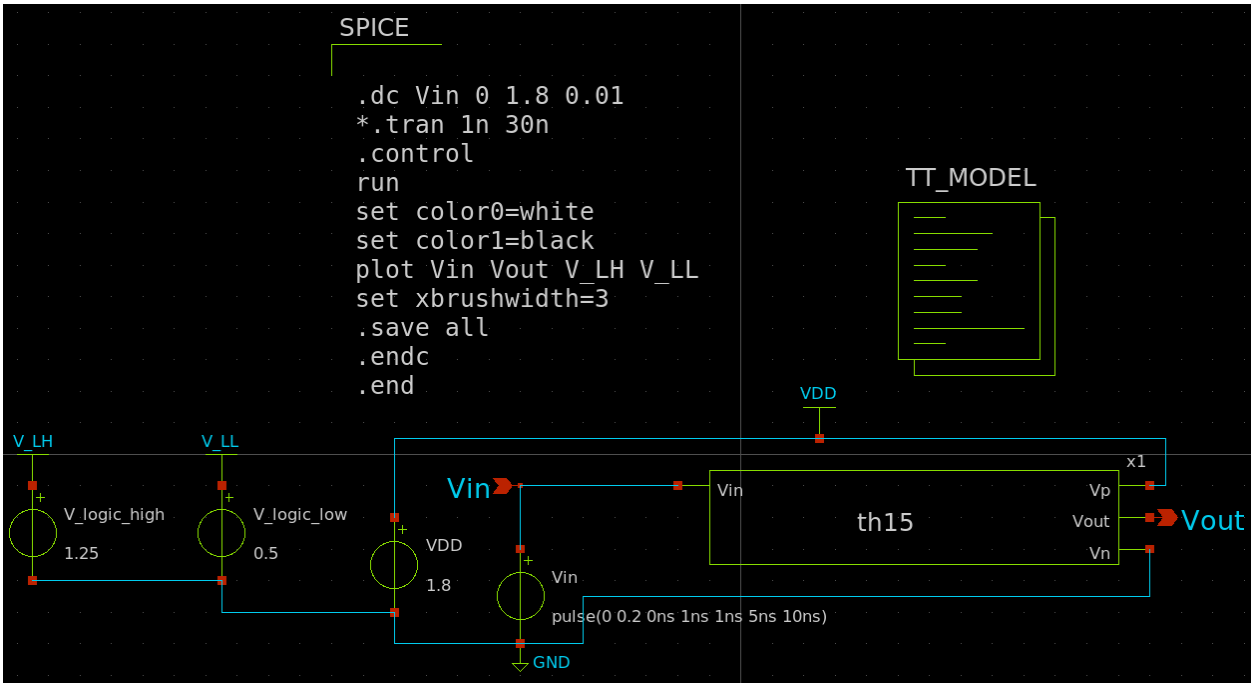

File Edit Options View Properties Layers Tools Symbol Highlight Simulation
Inverter-th15_sym.sch
Inverter-th15_sym.sch
Show symbols Alt+B
Show instance Bounding boxes for subcircuit symbols Alt+B
Show instance Bounding boxes for all symbols Alt+B
Show net names on symbol pins/floaters
Set symbol width
Make symbol from schematic A
Make schematic from symbol Ctrl+L
Make schematic and symbol from selected components Ctrl+Shift+H
Attach net labels to component instance Shift+H
Create symbol pins from selected schematic pins Alt+H
Place symbol pin Alt+P
Print list of highlight nets J
Print list of highlight nets, with buses expanded Alt-Ctrl-J
Create labels from highlight nets Alt-J
Create labels from highlight nets with 'i' prefix Alt-Shift-J
Create pins from highlight nets Ctrl-J
Search all search-paths for schematic associated to symbol
Allow duplicated instance names (refdes)



Magic=>before importing netlist to ngspice check LVS net

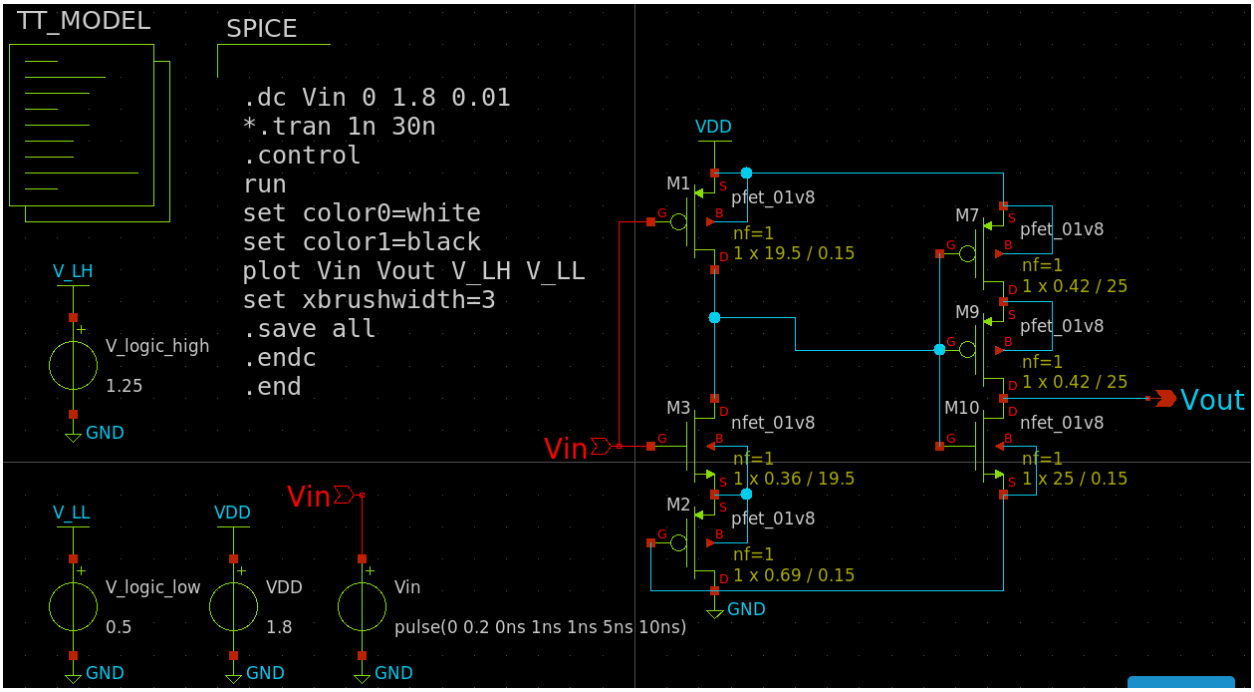


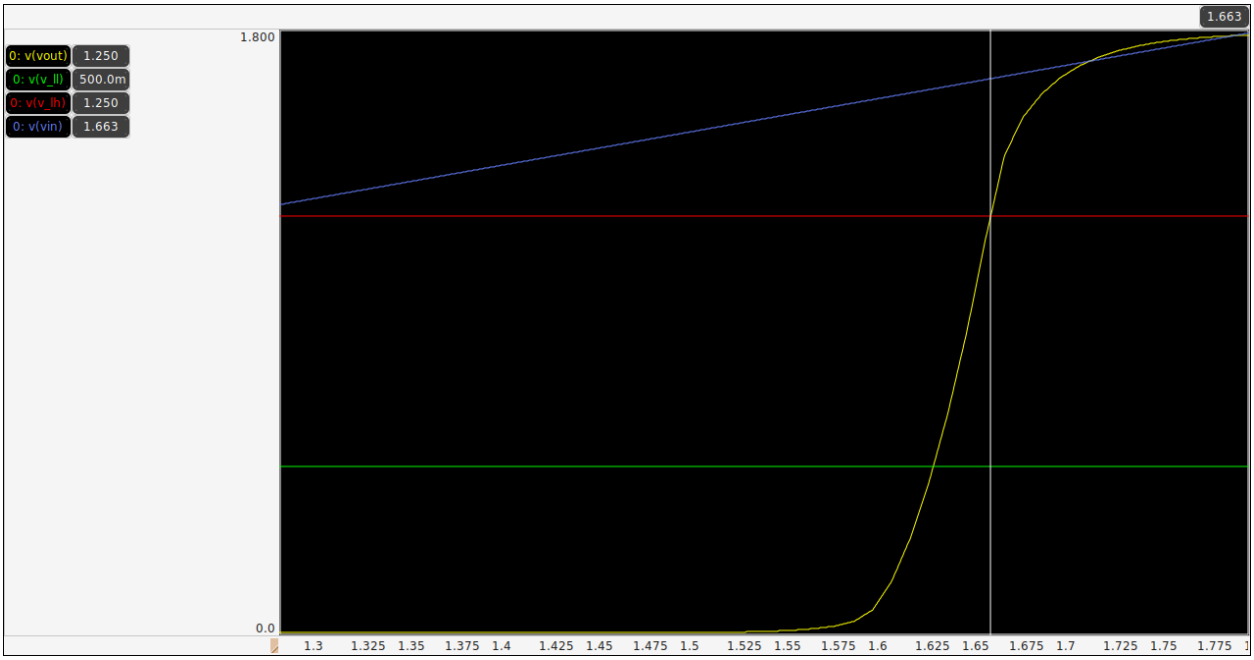
The simplified schematic is as follows:



The plot is similar to the previous figure.

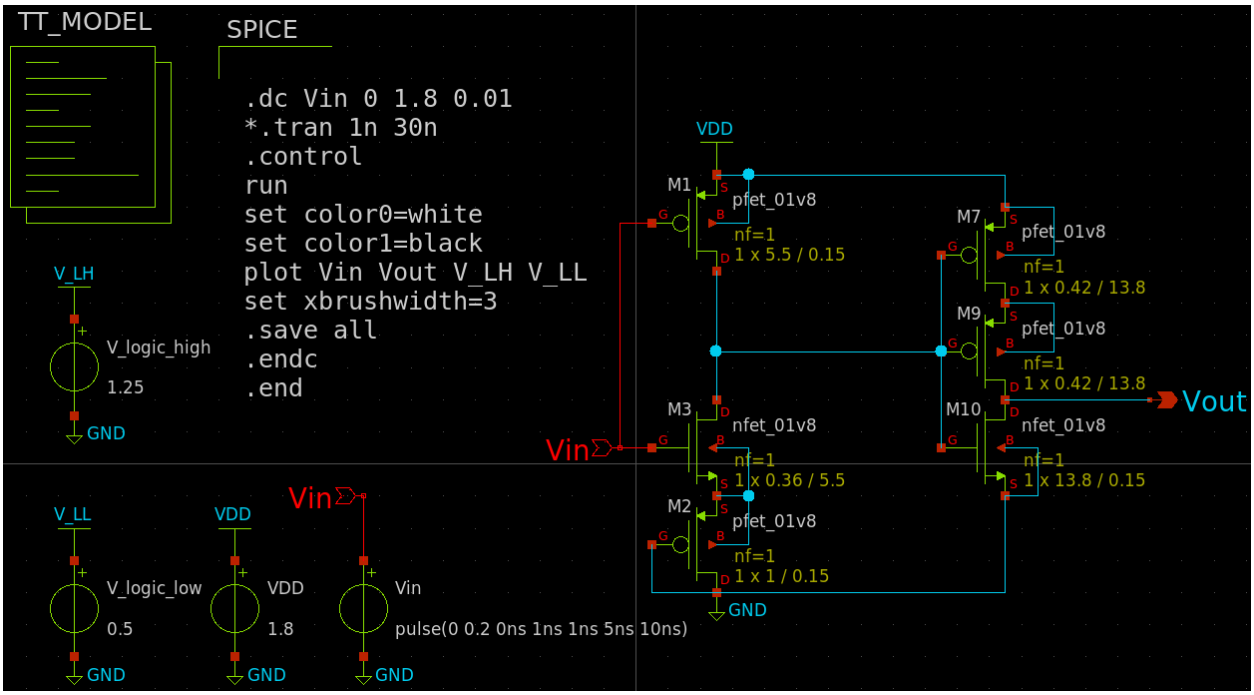
Th. 14: **1.6632**

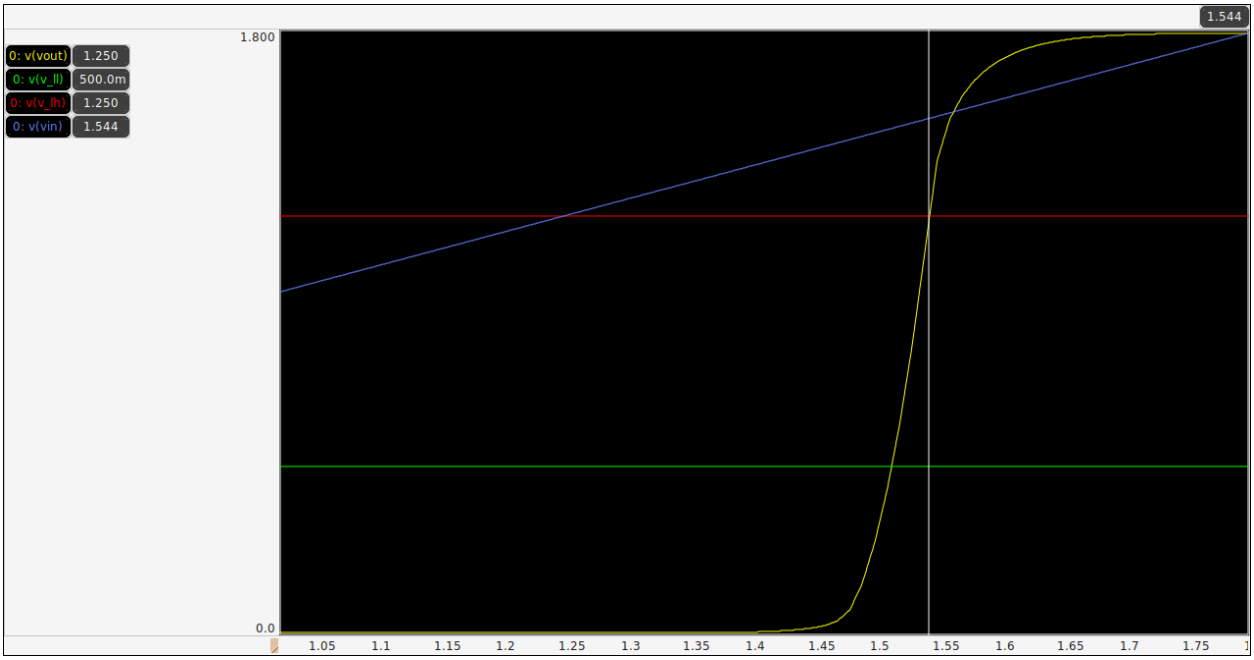




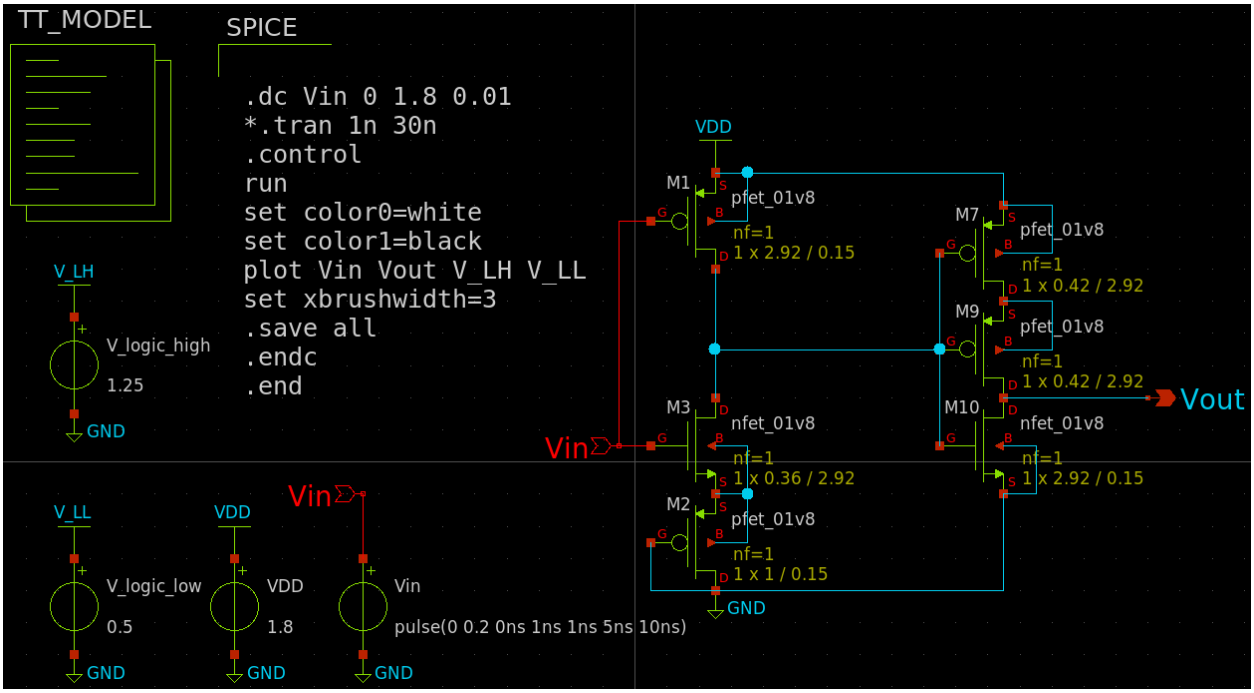
Rest of the figures are similar to the previous figures.

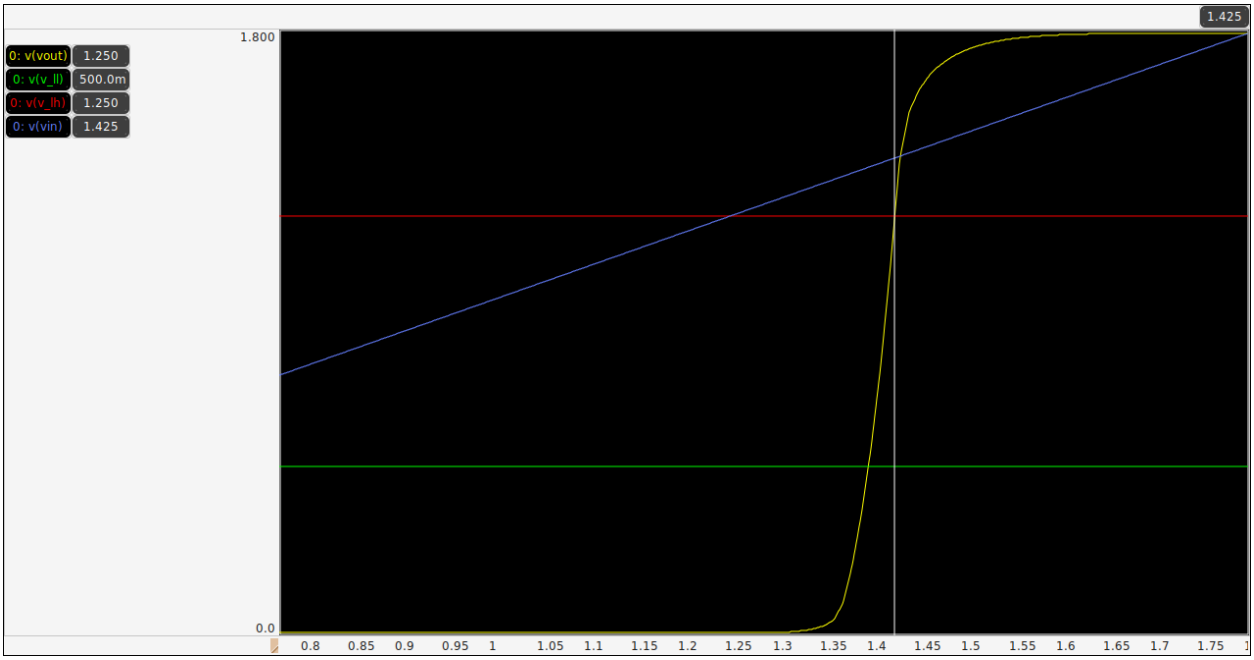
Th. 13: 1.5444:



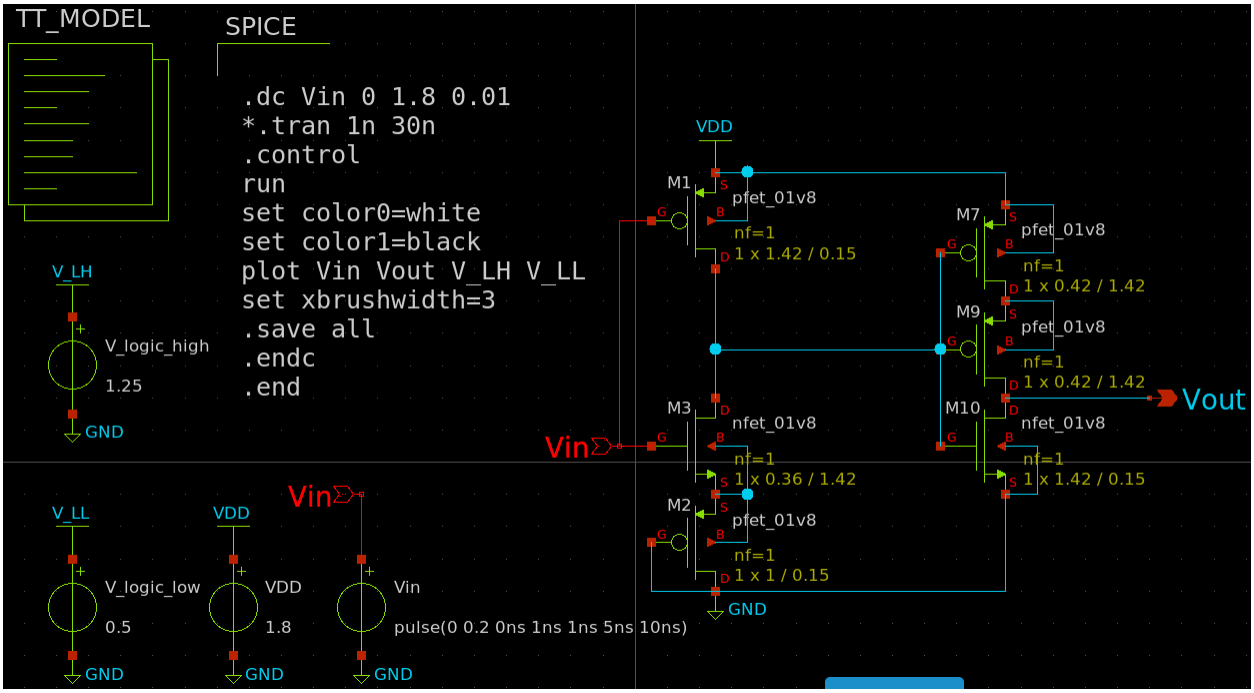

1.544
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 1.544
1.800
0.0
1.05 1.1 1.15 1.2 1.25 1.3 1.35 1.4 1.45 1.5 1.55 1.6 1.65 1.7 1.75

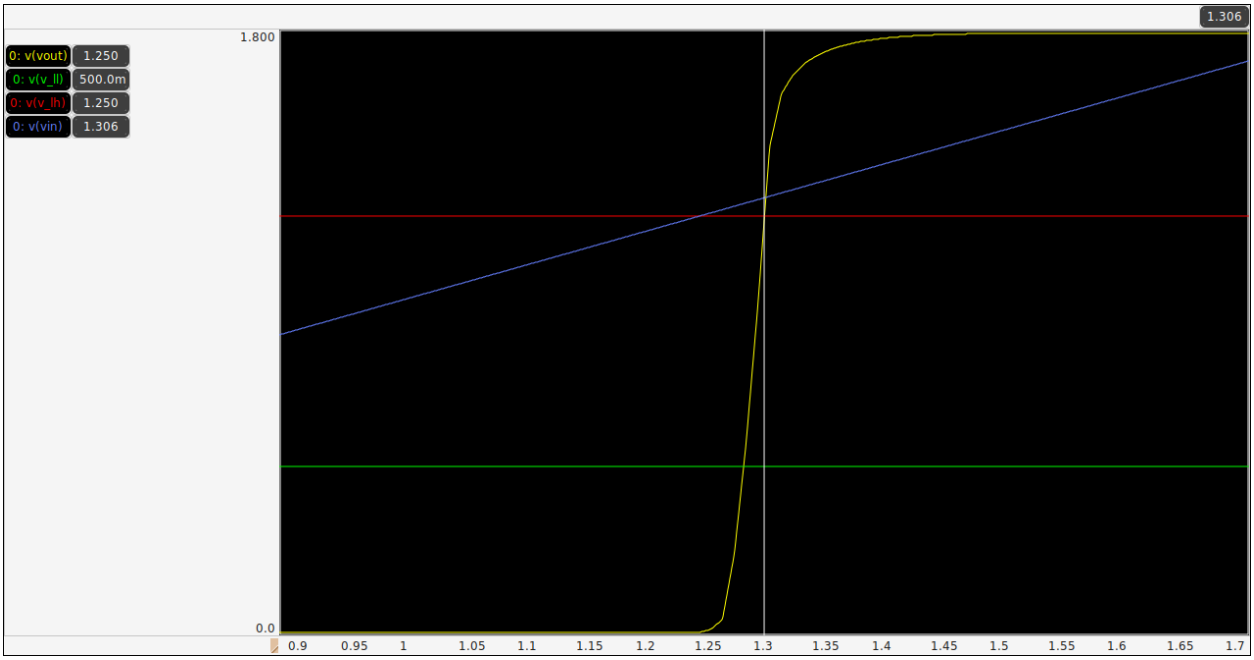
Th. 12: **1.4256**


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
VDD
M1
pfet_01v8
nf=1
1 x 2.92 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 2.92
M9
pfet_01v8
nf=1
1 x 0.42 / 2.92
Vout
M3
nfet_01v8
nf=1
1 x 0.36 / 2.92
M10
nfet_01v8
nf=1
1 x 2.92 / 0.15
M2
pfet_01v8
nf=1
1 x 1 / 0.15
GND

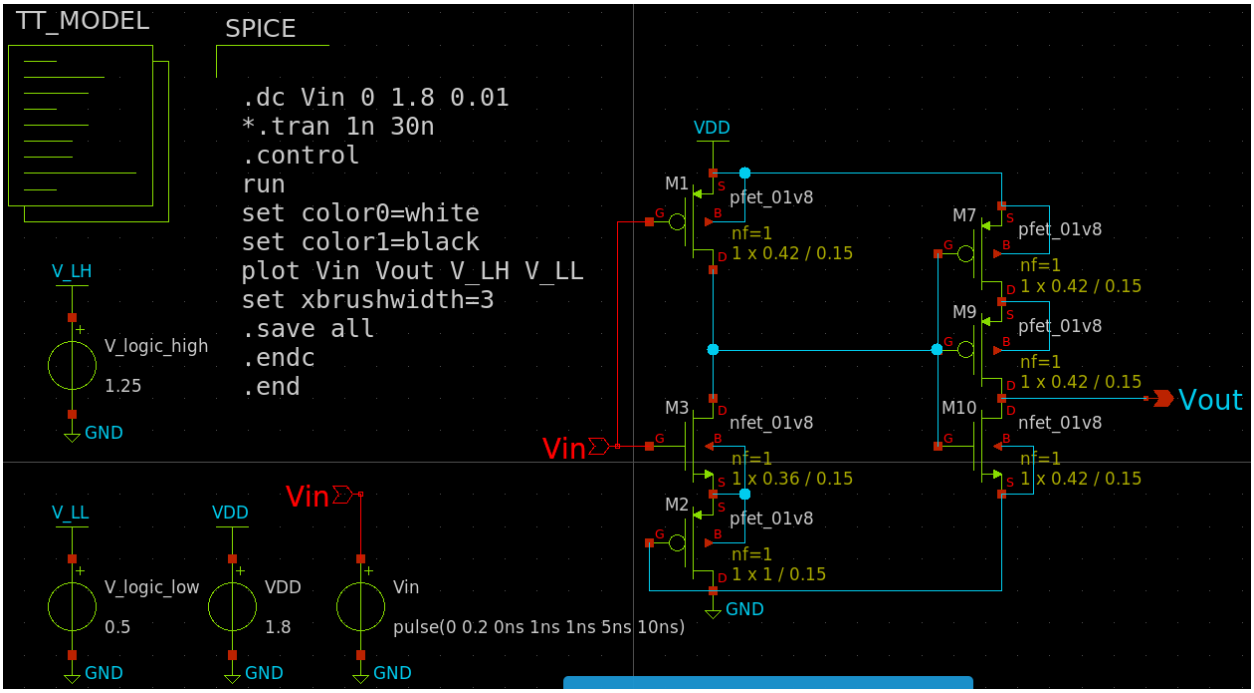

1.425
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 1.425
1.800
0.0
0.8 0.85 0.9 0.95 1 1.05 1.1 1.15 1.2 1.25 1.3 1.35 1.4 1.45 1.5 1.55 1.6 1.65 1.7 1.75

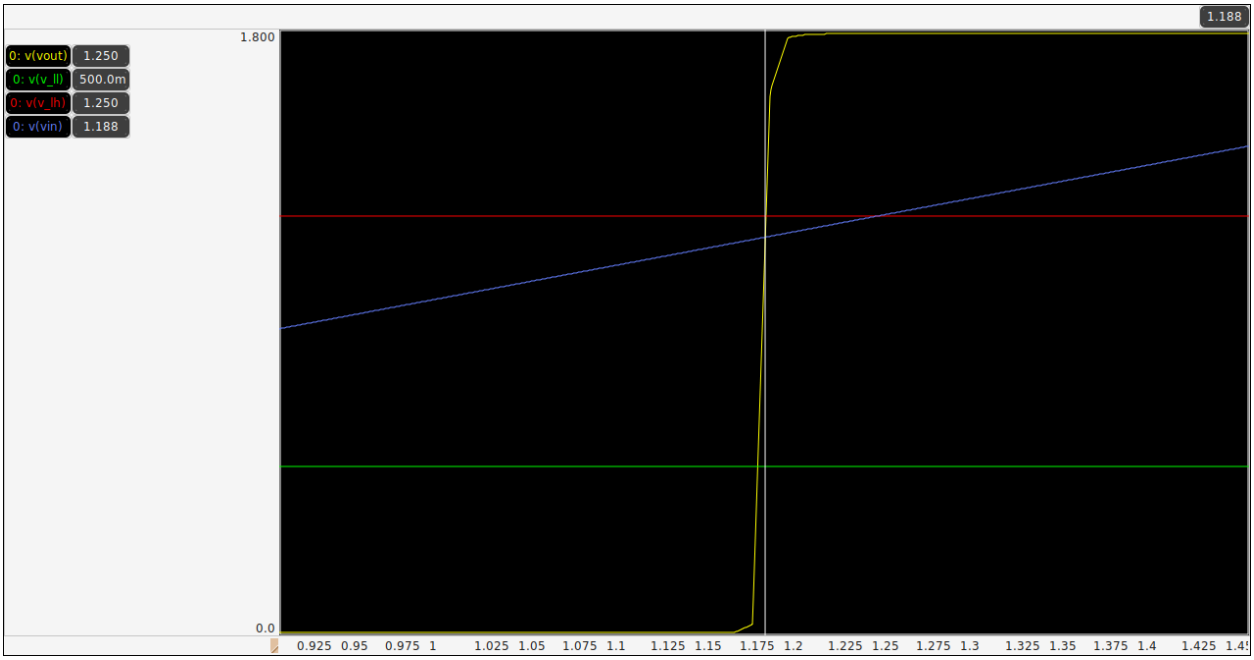
Th. 11: **1.3068**


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
VDD
M1
pfet_01v8
nf=1
1 x 1.42 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 1.42
M9
pfet_01v8
nf=1
1 x 0.42 / 1.42
Vout
M3
nfet_01v8
nf=1
1 x 0.36 / 1.42
M10
nfet_01v8
nf=1
1 x 1.42 / 0.15
M2
pfet_01v8
nf=1
1 x 1 / 0.15
GND

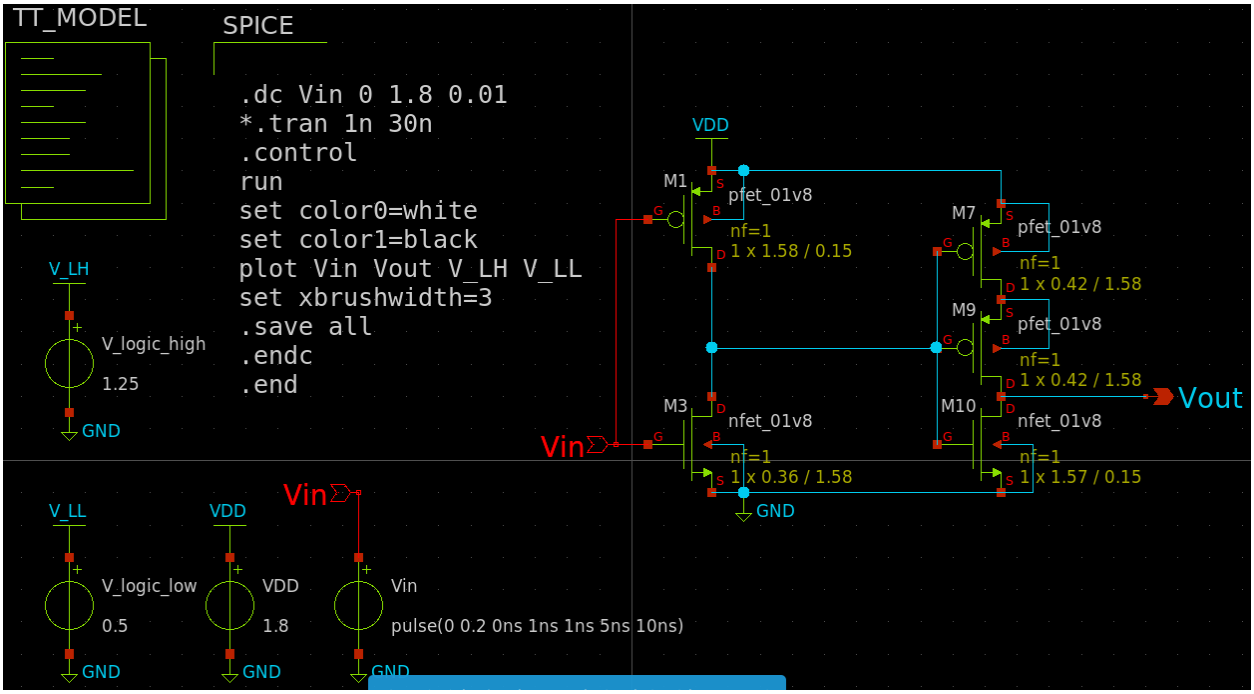

1.306
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 1.306
1.800
0.0
0.9 0.95 1 1.05 1.1 1.15 1.2 1.25 1.3 1.35 1.4 1.45 1.5 1.55 1.6 1.65 1.7

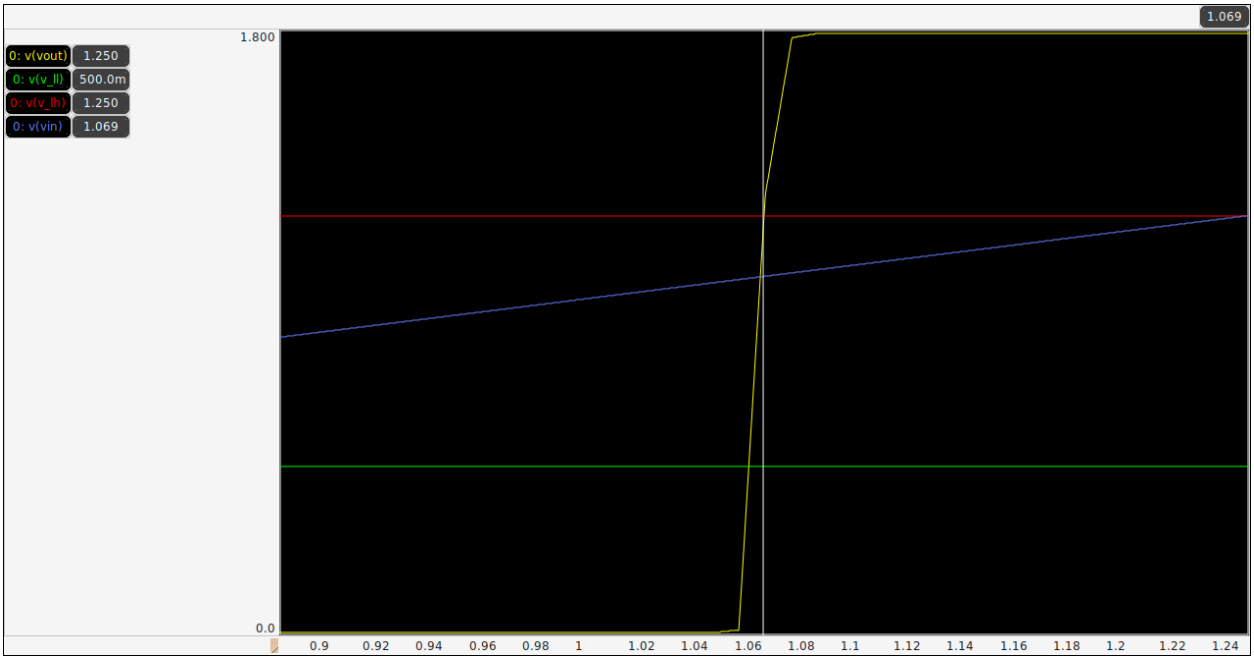
Th. 10: **1.188**


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
VDD
M1
pfet_01v8
nf=1
1 x 0.42 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 0.15
M9
pfet_01v8
nf=1
1 x 0.42 / 0.15
Vout
M3
nfet_01v8
nf=1
1 x 0.36 / 0.15
M10
nfet_01v8
nf=1
1 x 0.42 / 0.15
Vin
M2
pfet_01v8
nf=1
1 x 1 / 0.15
GND

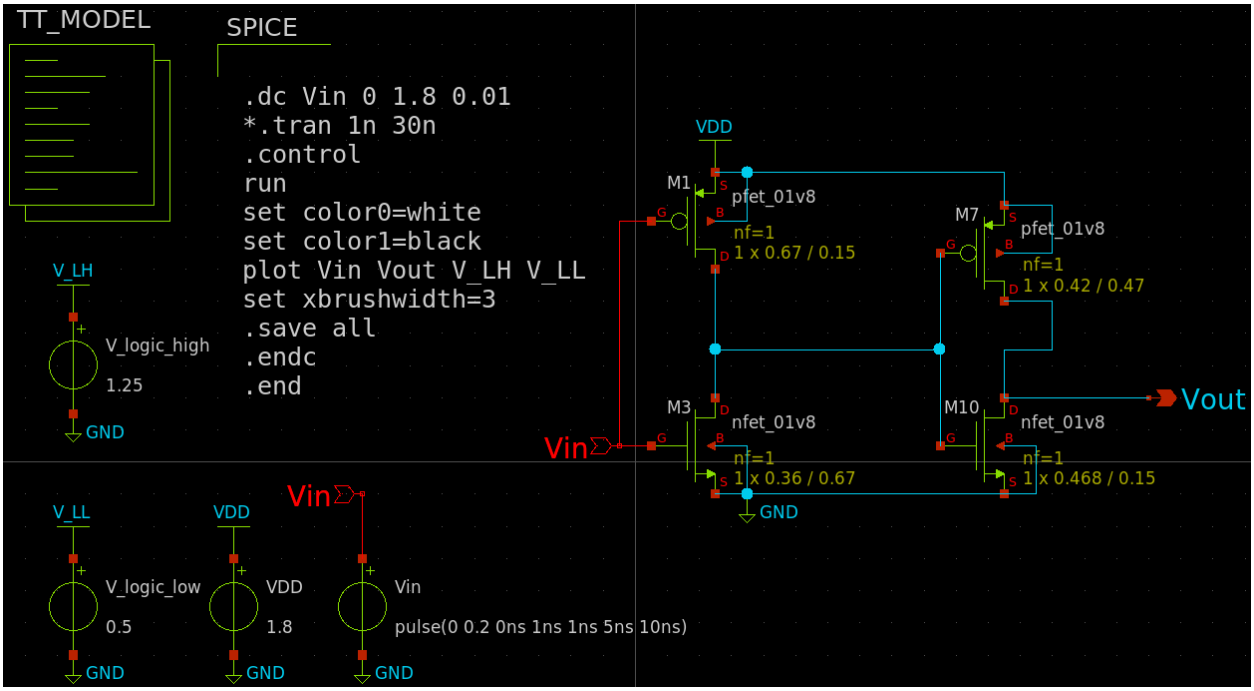

1.188
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 1.188
1.800
0.0
0.925 0.95 0.975 1 1.025 1.05 1.075 1.1 1.125 1.15 1.175 1.2 1.225 1.25 1.275 1.3 1.325 1.35 1.375 1.4 1.425

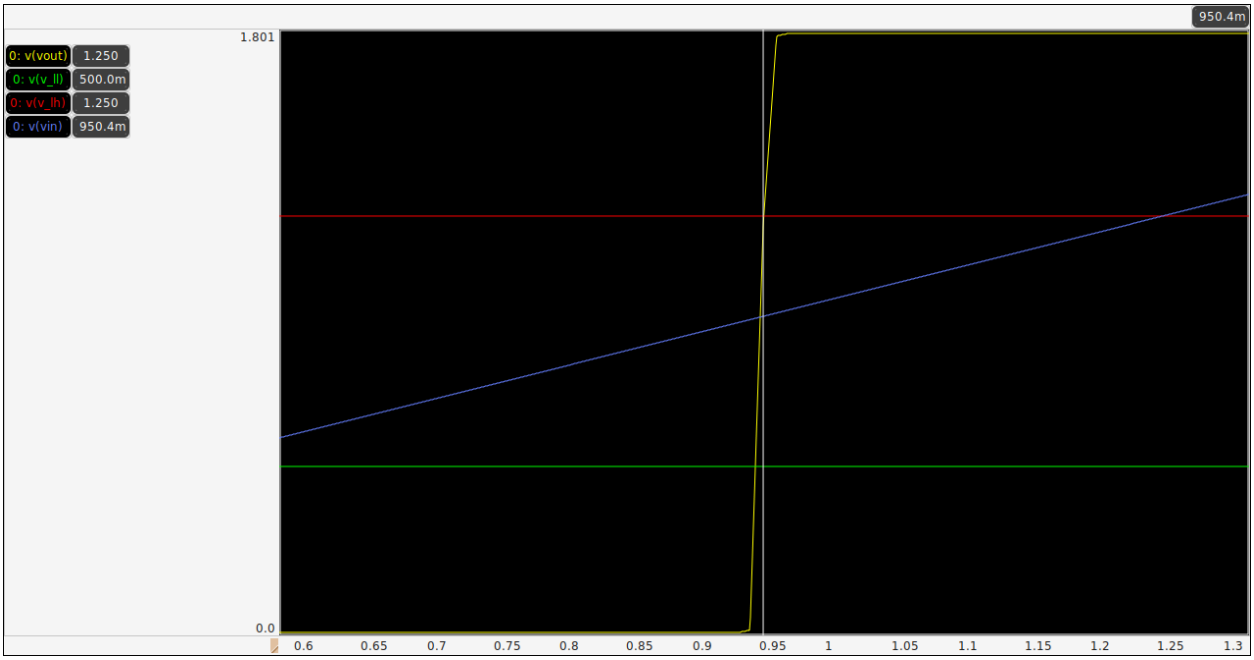
Th. 9: 1.0692


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
VDD
M1
pfet_01v8
nf=1
1 x 1.58 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 1.58
M9
pfet_01v8
nf=1
1 x 0.42 / 1.58
M3
nfet_01v8
nf=1
1 x 0.36 / 1.58
M10
nfet_01v8
nf=1
1 x 1.57 / 0.15
Vout
GND

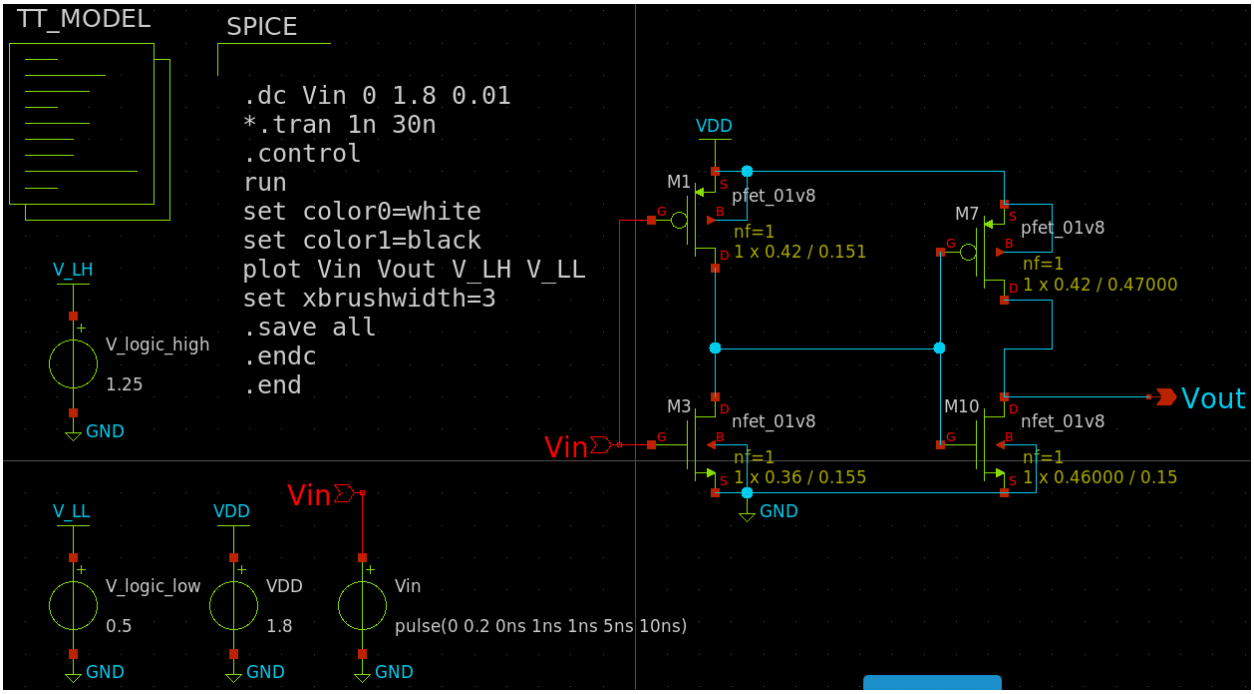

1.069
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 1.069
1.800
0.0
0.9 0.92 0.94 0.96 0.98 1 1.02 1.04 1.06 1.08 1.1 1.12 1.14 1.16 1.18 1.2 1.22 1.24

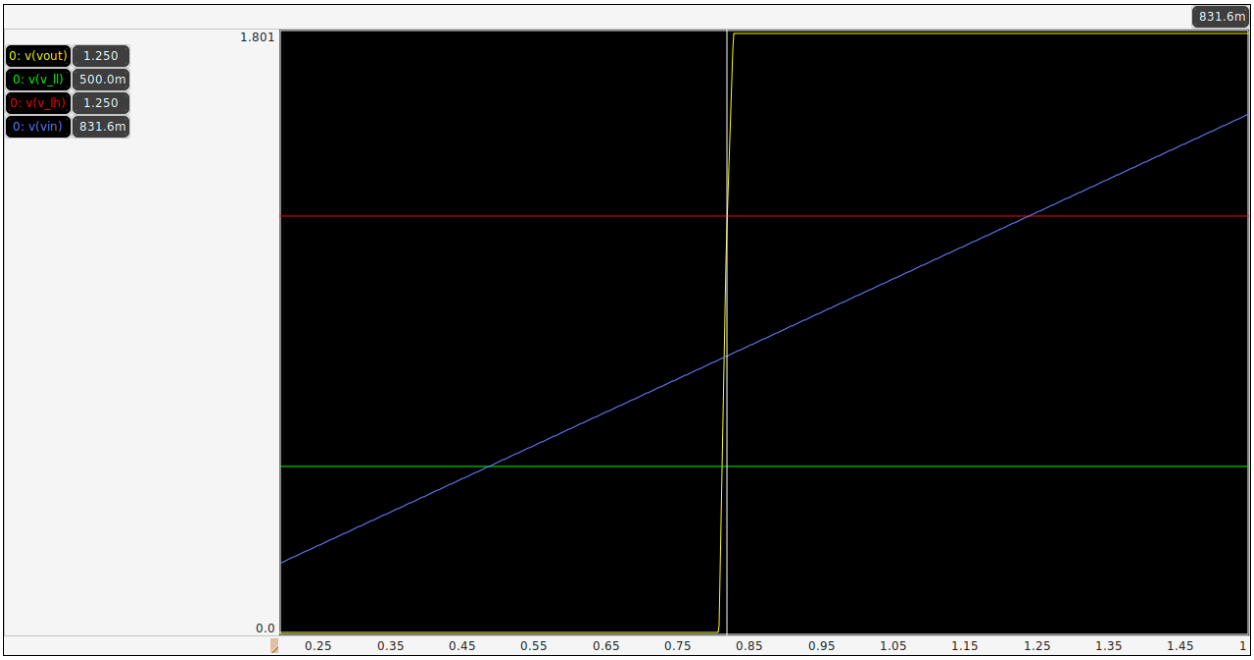
Th. 8: 0.9504


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
VDD
M1
pfet_01v8
nf=1
1 x 0.67 / 0.15
M7
pfet_01v8
nf=1
1 x 0.42 / 0.47
Vout
M3
nfet_01v8
nf=1
1 x 0.36 / 0.67
M10
nfet_01v8
nf=1
1 x 0.468 / 0.15
Vin
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND

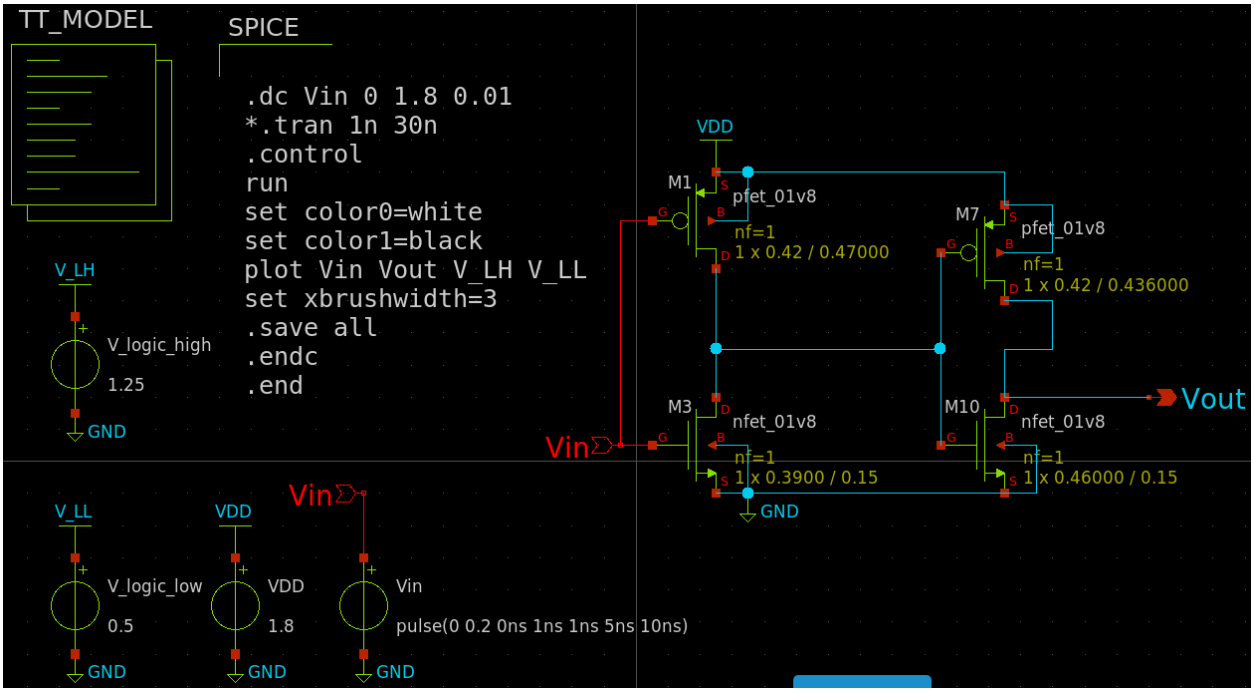

950.4m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 950.4m
1.801
0.0
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
1
1.05
1.1
1.15
1.2
1.25
1.3

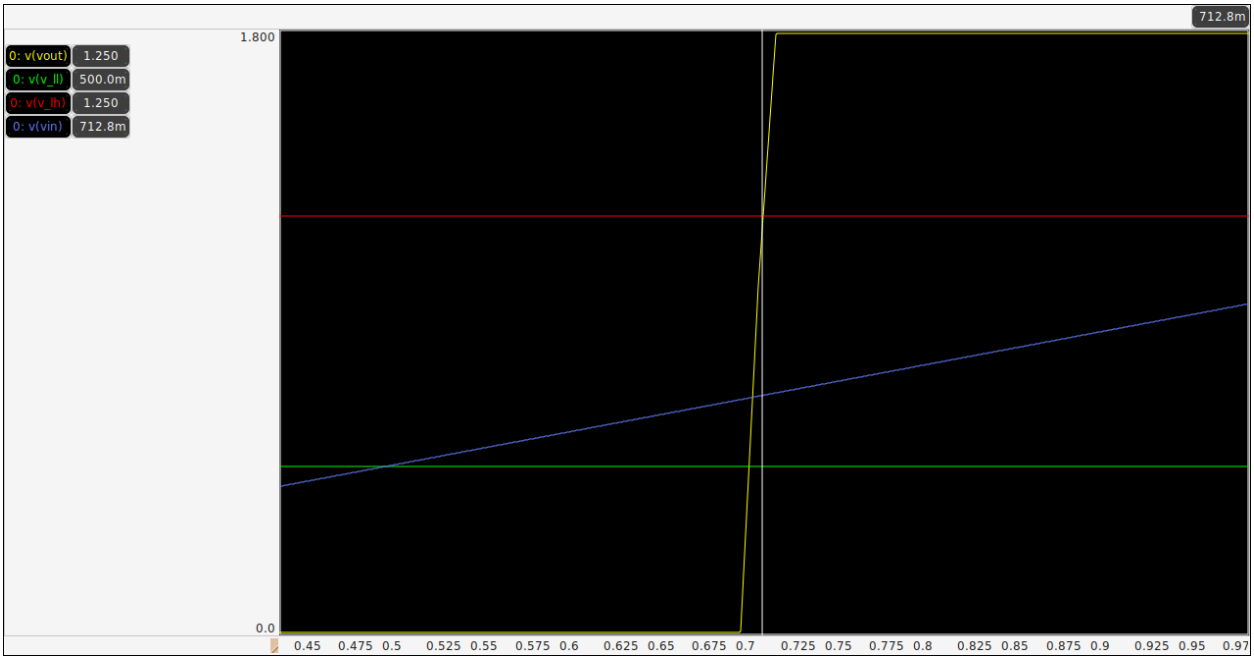
Th. 7: 0.8316


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
VDD
M1
pfet_01v8
nf=1
1 x 0.42 / 0.151
M7
pfet_01v8
nf=1
1 x 0.42 / 0.47000
Vin
M3
nfet_01v8
nf=1
1 x 0.36 / 0.155
M10
nfet_01v8
nf=1
1 x 0.46000 / 0.15
Vout
GND

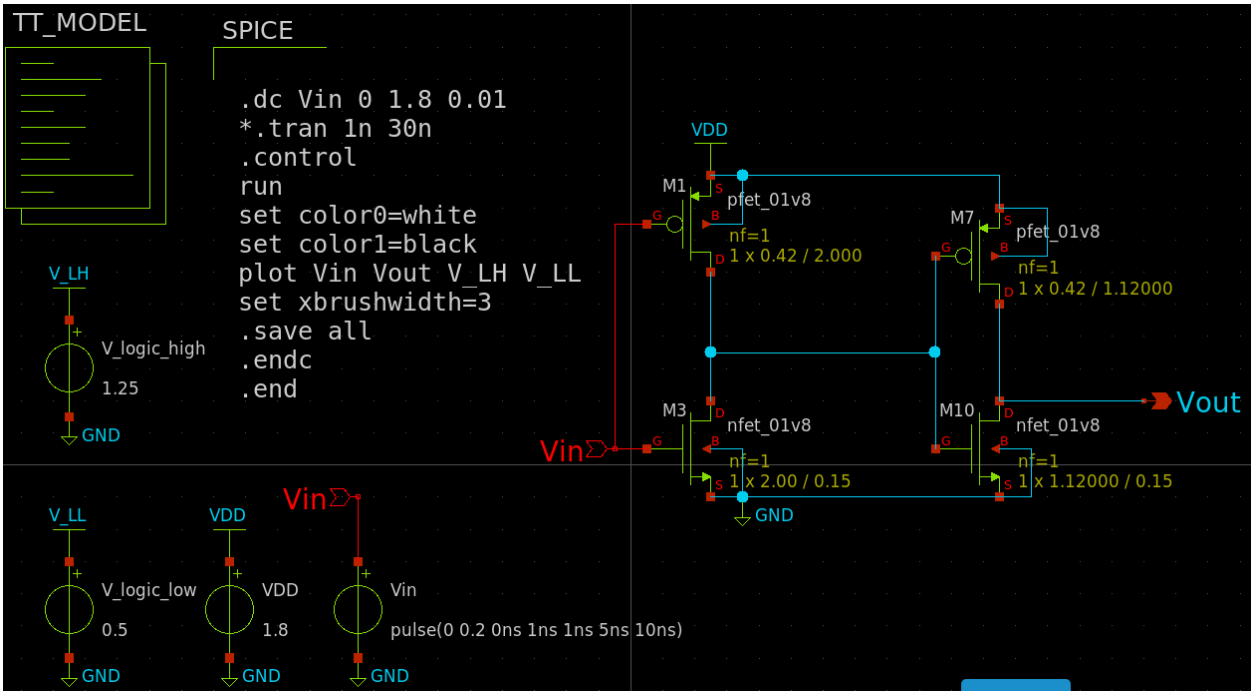

831.6m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 831.6m
1.801
0.0
0.25
0.35
0.45
0.55
0.65
0.75
0.85
0.95
1.05
1.15
1.25
1.35
1.45
1

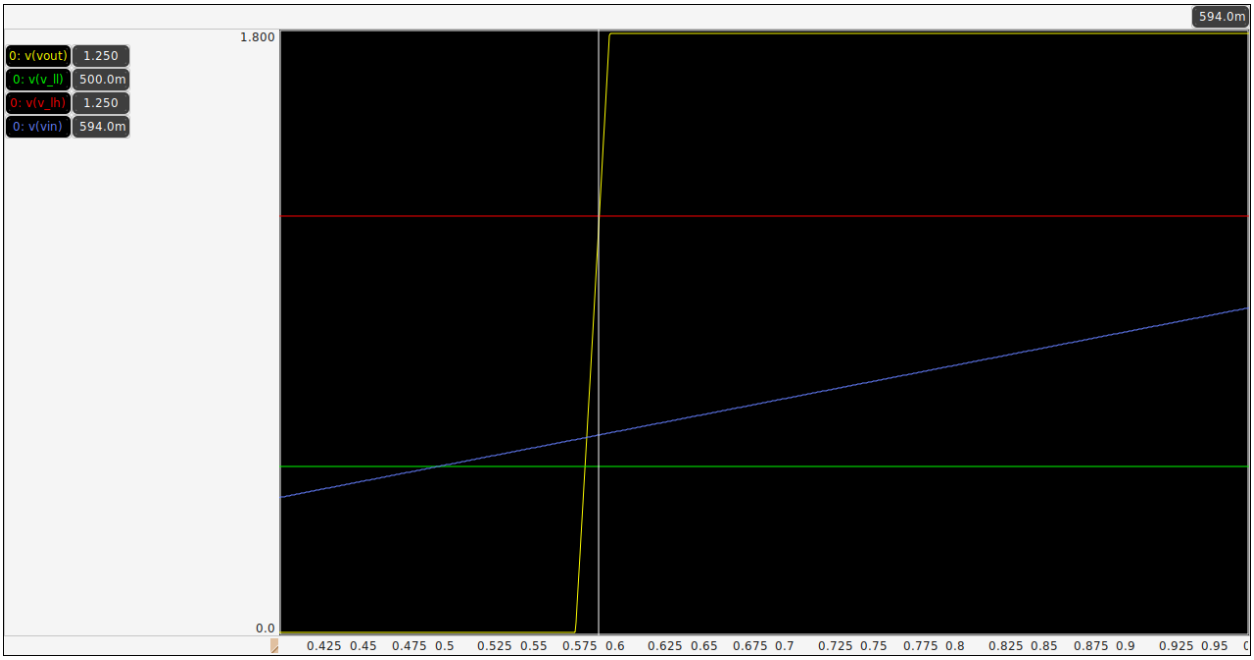
Th. 6: 0.7128


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
VDD
M1
pfet_01v8
nf=1
1 x 0.42 / 0.47000
M7
pfet_01v8
nf=1
1 x 0.42 / 0.436000
Vout
M3
nfet_01v8
nf=1
1 x 0.3900 / 0.15
M10
nfet_01v8
nf=1
1 x 0.46000 / 0.15
Vin
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND

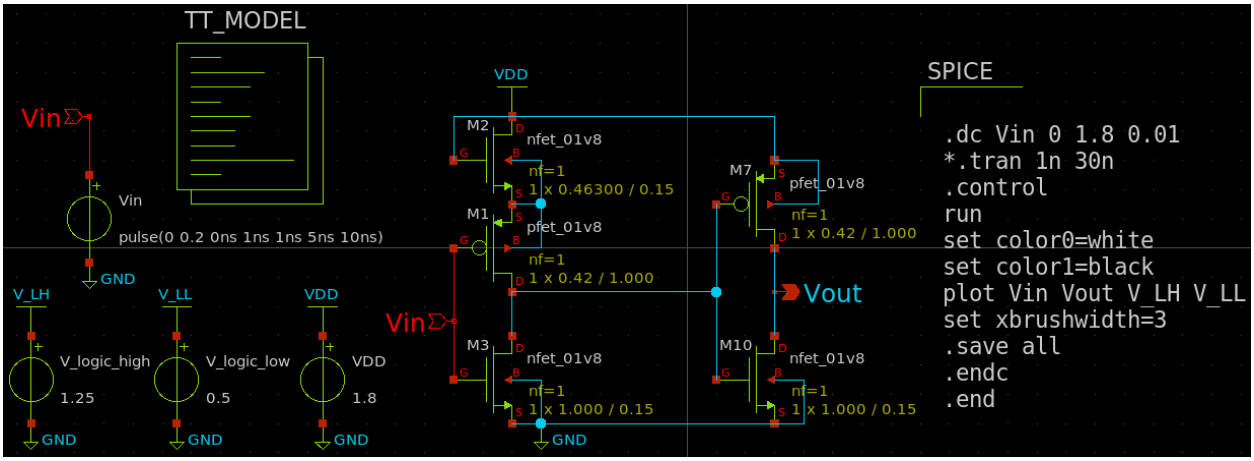

712.8m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 712.8m
1.800
0.0
0.45 0.475 0.5 0.525 0.55 0.575 0.6 0.625 0.65 0.675 0.7 0.725 0.75 0.775 0.8 0.825 0.85 0.875 0.9 0.925 0.95 0.97

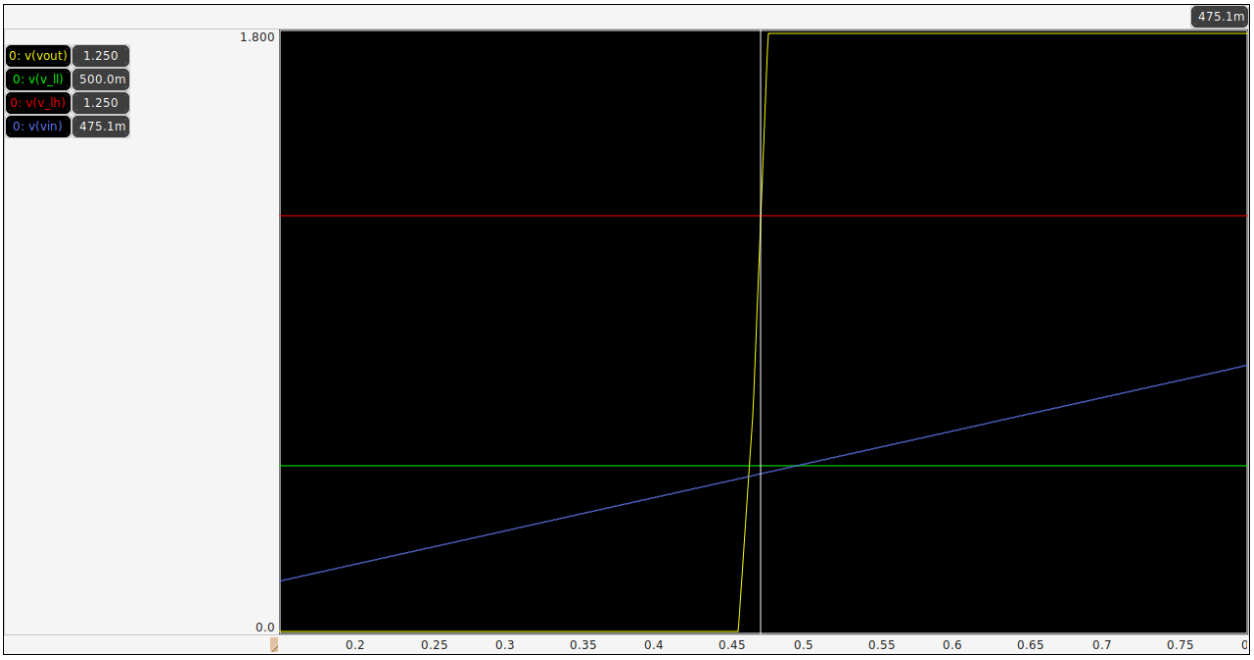
Th. 5: 0.594


TT_MODEL
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end
V_LH
V_logic_high
1.25
GND
VDD
M1
pfet_01v8
nf=1
1 x 0.42 / 2.000
M7
pfet_01v8
nf=1
1 x 0.42 / 1.12000
Vin
M3
nfet_01v8
nf=1
1 x 2.00 / 0.15
M10
nfet_01v8
nf=1
1 x 1.12000 / 0.15
Vout
GND
V_LL
V_logic_low
0.5
GND
VDD
1.8
GND
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND

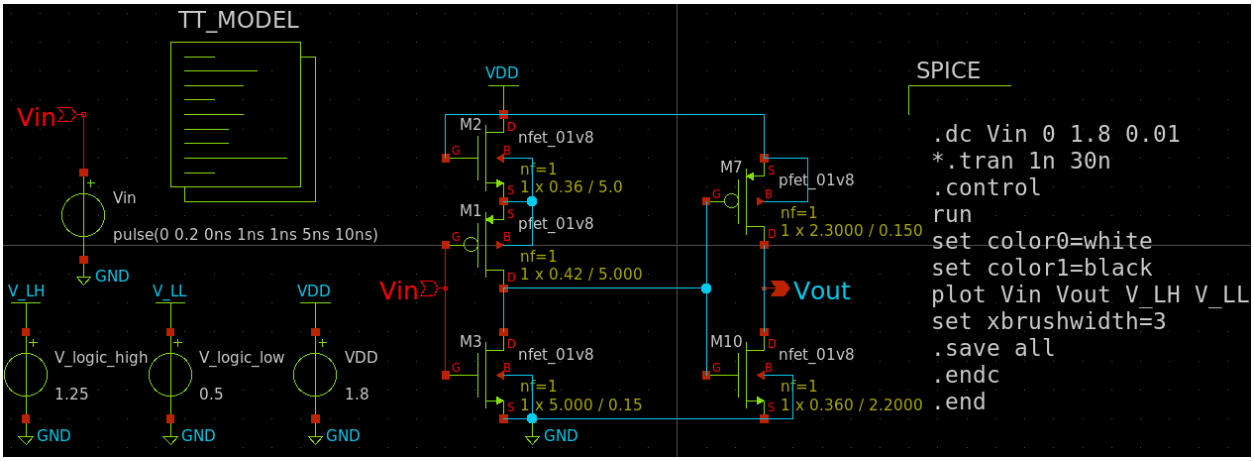

594.0m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 594.0m
1.800
0.0
0.425 0.45 0.475 0.5 0.525 0.55 0.575 0.6 0.625 0.65 0.675 0.7 0.725 0.75 0.775 0.8 0.825 0.85 0.875 0.9 0.925 0.95

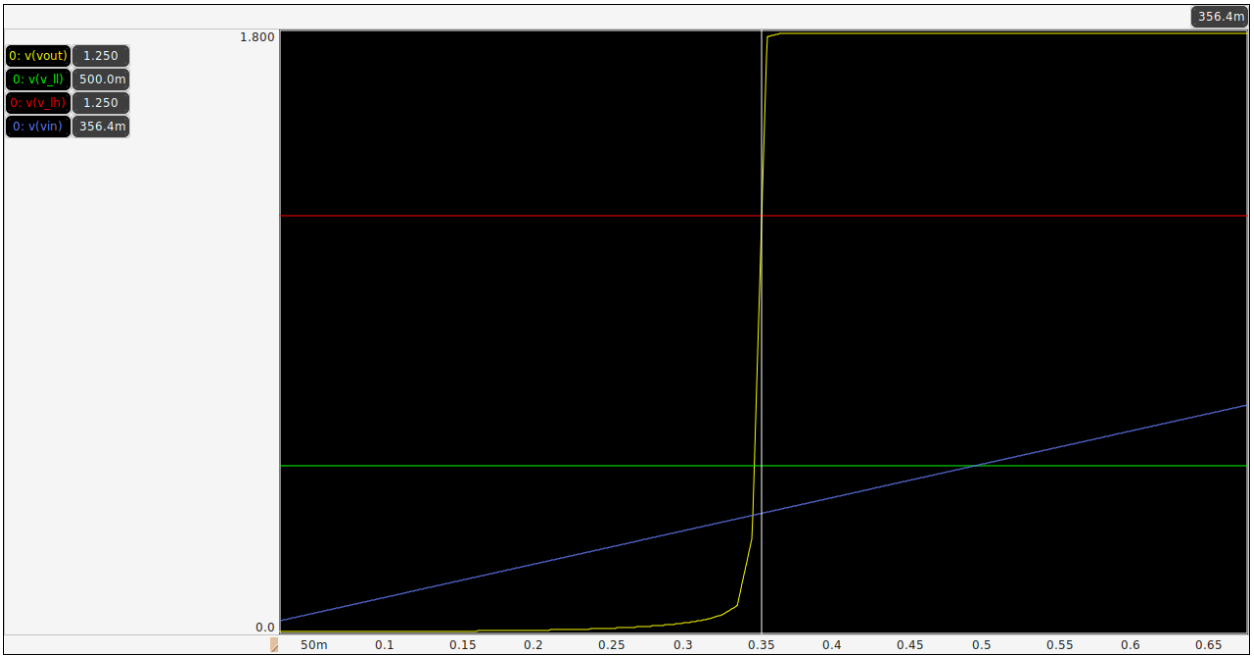
Th. 4: 0.4752


TT_MODEL
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
VDD
M2
nfet_01v8
nf=1
1 x 0.46300 / 0.15
M1
pfet_01v8
nf=1
1 x 0.42 / 1.000
Vin
M3
nfet_01v8
nf=1
1 x 1.000 / 0.15
GND
M7
pfet_01v8
nf=1
1 x 0.42 / 1.000
Vout
M10
nfet_01v8
nf=1
1 x 1.000 / 0.15
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end

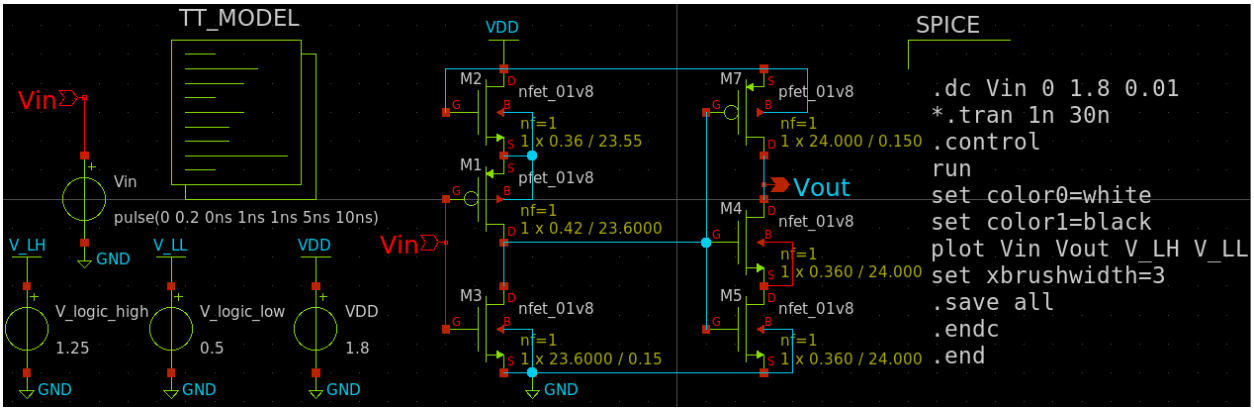

475.1m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 475.1m
1.800
0.0
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75

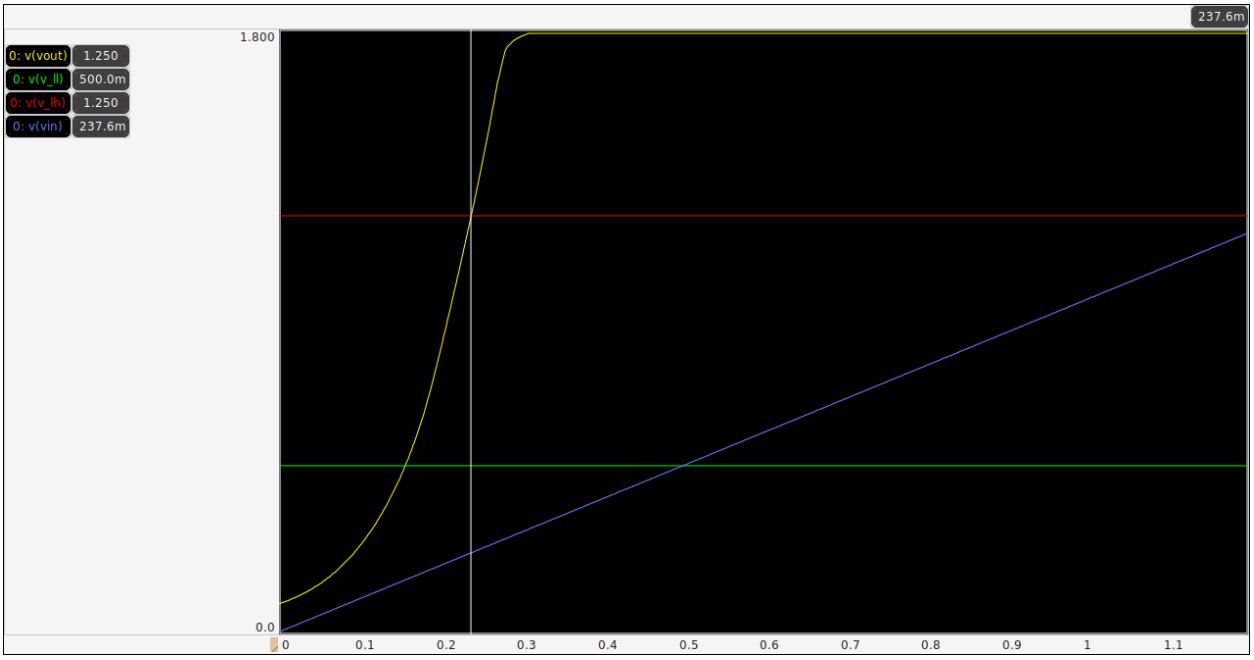
Th. 3: 0.3564


TT_MODEL
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
V_LH
V_LL
VDD
V_logic_high
1.25
V_logic_low
0.5
VDD
1.8
GND
GND
GND
VDD
M2
nfet_01v8
nf=1
1 x 0.36 / 5.0
M1
pfet_01v8
nf=1
1 x 0.42 / 5.000
Vin
M3
nfet_01v8
nf=1
1 x 5.000 / 0.15
GND
M7
pfet_01v8
nf=1
1 x 2.3000 / 0.150
Vout
M10
nfet_01v8
nf=1
1 x 0.360 / 2.2000
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end

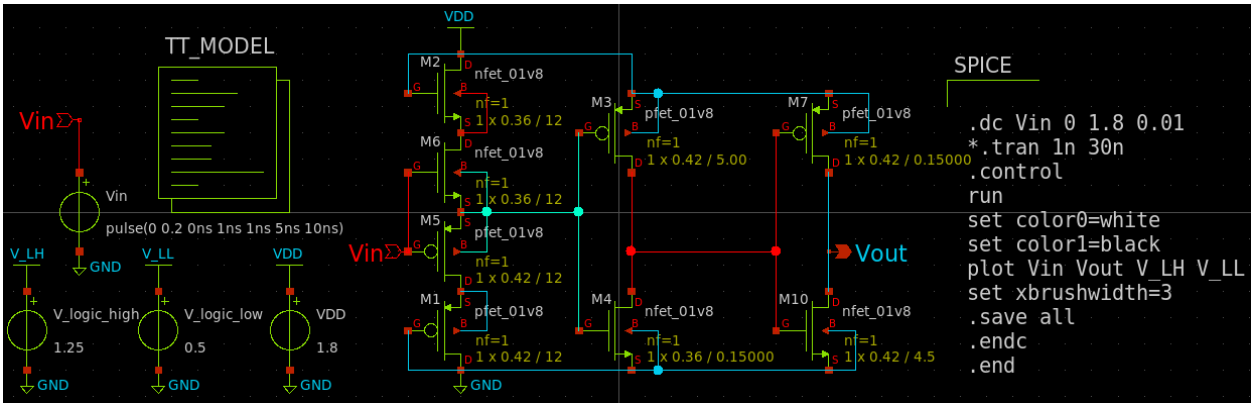

356.4m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 356.4m
1.800
0.0
50m
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.65

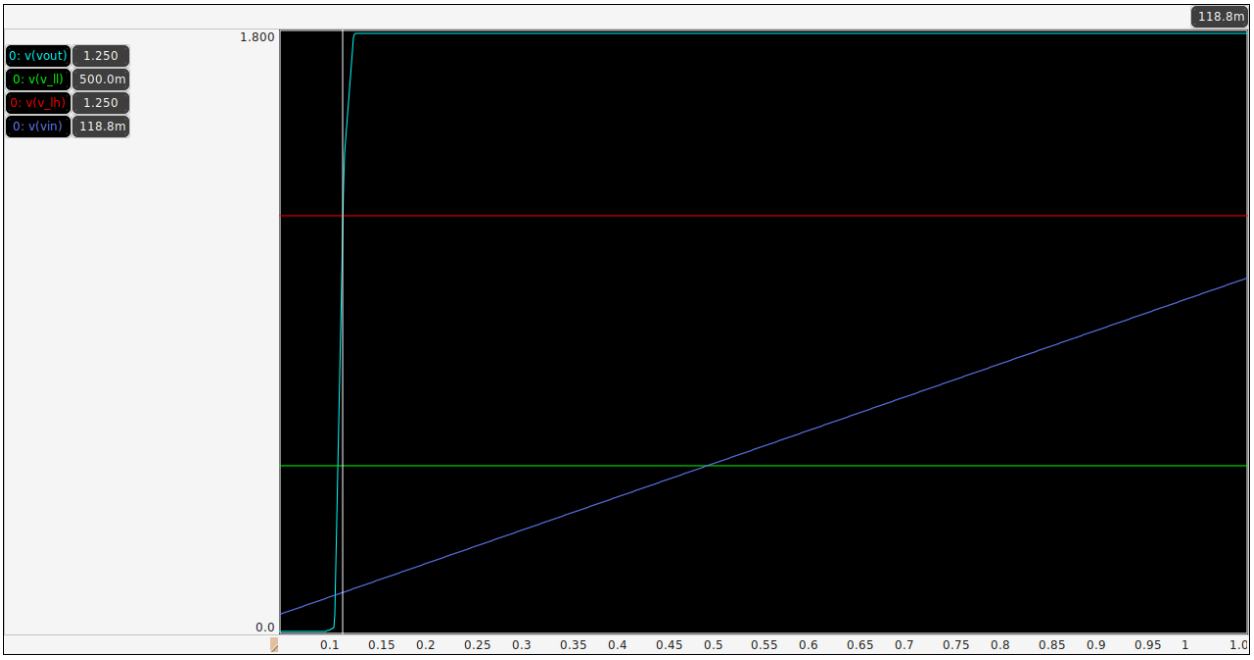
Th. 2: 0.2376


TT_MODEL
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
V_LH
V_logic_high
1.25
GND
V_LL
V_logic_low
0.5
GND
VDD
VDD
1.8
GND
VDD
M2
nfet_01v8
nf=1
1 x 0.36 / 23.55
M1
nfet_01v8
nf=1
1 x 0.42 / 23.6000
Vin
M3
nfet_01v8
nf=1
1 x 23.6000 / 0.15
GND
M7
pfet_01v8
nf=1
1 x 24.000 / 0.150
Vout
M4
nfet_01v8
nf=1
1 x 0.360 / 24.000
M5
nfet_01v8
nf=1
1 x 0.360 / 24.000
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end

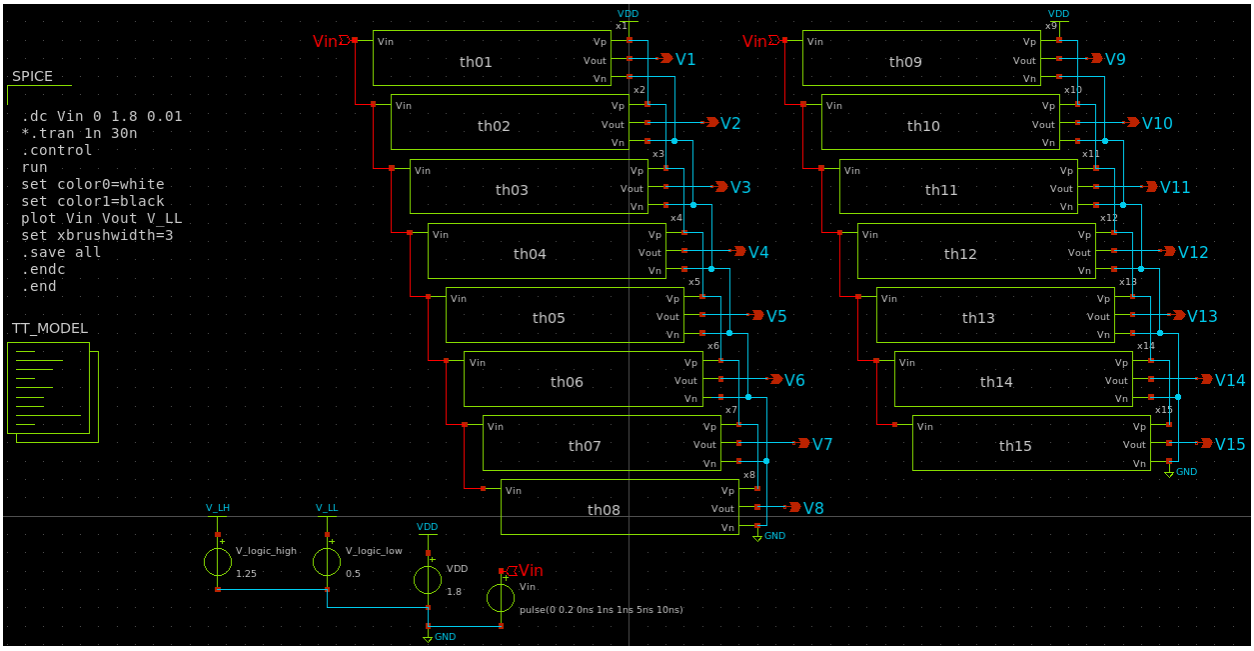

237.6m
0: v(vout) 1.250
0: v(v_ll) 500.0m
0: v(v_lh) 1.250
0: v(vin) 237.6m
1.800
0.0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1

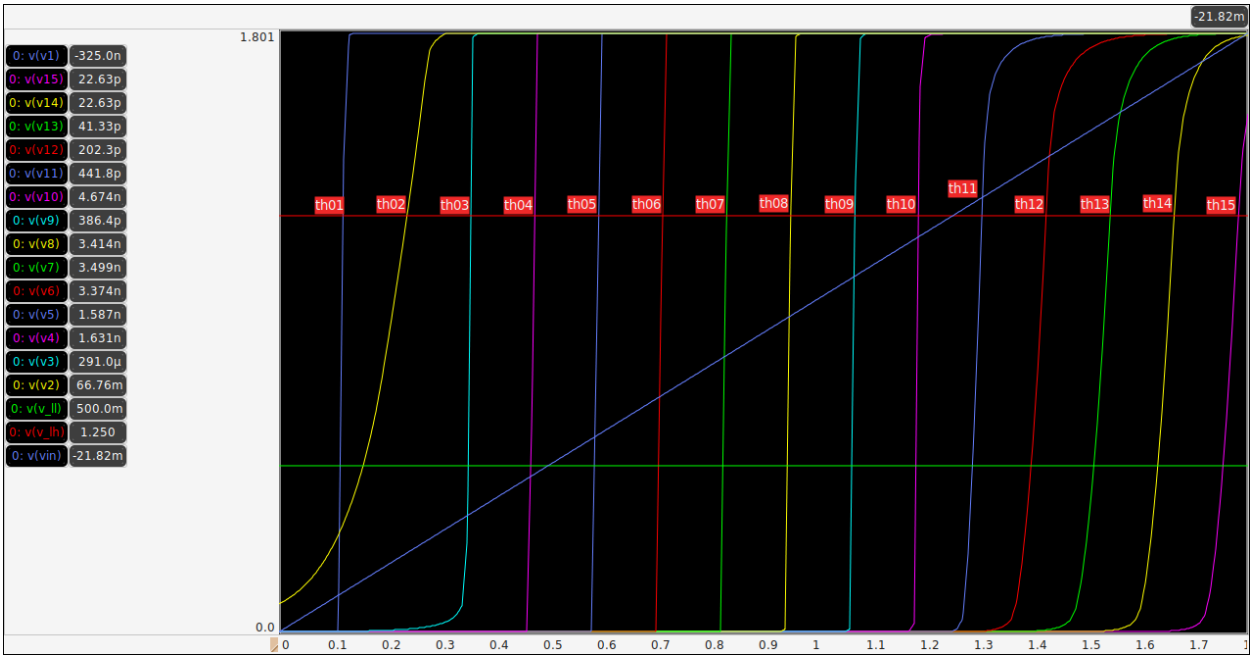
Th. 1: 0.1188


TT_MODEL
Vin
Vin
pulse(0 0.2 0ns 1ns 1ns 5ns 10ns)
GND
V_LH
V_LL
VDD
V_logic_high
1.25
V_logic_low
0.5
VDD
1.8
GND
GND
GND
VDD
M2
nfet_01v8
nf=1
1 x 0.36 / 12
M6
nfet_01v8
nf=1
1 x 0.36 / 12
M5
pfet_01v8
nf=1
1 x 0.42 / 12
M1
pfet_01v8
nf=1
1 x 0.42 / 12
M3
pfet_01v8
nf=1
1 x 0.42 / 5.00
M7
pfet_01v8
nf=1
1 x 0.42 / 0.15000
M4
nfet_01v8
nf=1
1 x 0.36 / 0.15000
M10
nfet_01v8
nf=1
1 x 0.42 / 4.5
Vin
Vout
SPICE
.dc Vin 0 1.8 0.01
*.tran 1n 30n
.control
run
set color0=white
set color1=black
plot Vin Vout V_LH V_LL
set xbrushwidth=3
.save all
.endc
.end



Combined Analog sch.





http://web02.gonzaga.edu/faculty/talarico/vlsi/xschemTut.html

https://ngspice.sourceforge.io/ngspice-control-language-tutorial.html

Alter subckt tutorial—

https://sourceforge.net/p/ngspice/discussion/133842/thread/5ad086c79f

https://sourceforge.net/p/ngspice/discussion/133842/thread/9a75acf2/#bf90/45b3/ea48

Pyspice ngspice interpreter

https://pyspice.fabrice-salvaire.fr/releases/v1.3/examples/ngspice-shared/ngspice-interpreter.html

https://github.com/ashwith/ngspicepy

Read spice raw output data

https://gist.githubusercontent.com/snmishra/27dcc624b639c2626137/raw/742fe0dd59c7b2c41b71a1c8c1c2506d13affc53/rawread.py

ngspice wrapper for python

https://github.com/eps82/lyngspice/wiki

write some verilog code to convert the thermometer code (from the inverter stages) into the binary code

```
module thermometer_to_binary (
    input [14:0] ith,
    output reg [3:0] binary
);


always @(*) begin
    case (ith)
        16'b000000000000000: binary = 4'b0000;    // ~0.0000
        16'b000000000000001: binary = 4'b0001;    // ~0.1188
        16'b000000000000011: binary = 4'b0010;    // ~0.2376
        16'b000000000000111: binary = 4'b0011;    // ~0.3564
        16'b000000000001111: binary = 4'b0100;    // ~0.4752
        16'b000000000011111: binary = 4'b0101;    // ~0.5940
        16'b000000000111111: binary = 4'b0110;    // ~0.7128
        16'b000000001111111: binary = 4'b0111;    // ~0.8316
        16'b000000011111111: binary = 4'b1000;    // ~0.9504
        16'b000000111111111: binary = 4'b1001;    // ~1.0692
        16'b000001111111111: binary = 4'b1010;    // ~1.1880
        16'b000011111111111: binary = 4'b1011;    // ~1.3068
        16'b000111111111111: binary = 4'b1100;    // ~1.4256
        16'b001111111111111: binary = 4'b1101;    // ~1.5444
        16'b011111111111111: binary = 4'b1110;    // ~1.6632
        16'b111111111111111: binary = 4'b1111;    // ~1.7820
        default: binary = 4'bxxxx; // Don't care
    endcase
end
```

endmodule

http://www.asic-world.com/verilog/veritut.html

https://nandland.com/introduction-to-verilog-for-beginners-with-code-examples/

https://www.youtube.com/playlist?list=PLfGJEQLQIDBN0VsXQ68_FEYyqcym8CTDN

https://github.com/Swagatika-Meher/msvsd2bitcomp

ALIGN Tool-

https://www.youtube.com/playlist?list=PLvXKBnlvcSm30Y0zu1765oG_x-ECU8tVG

https://learning.edx.org/course/course-v1:HarveyMuddX+ENGR85A+3T2021/home

https://www.vlsiuniverse.com/digital-thermometer-code-in-verilog-vhdl-flash-adc-binary-encoder/

https://www.classcentral.com/subject/vlsi?free=true

https://www.eng.biu.ac.il/temanad/digital-vlsi-design/

https://www.youtube.com/playlist?list=PLZU5hLL_713x0_AV_rVbay0pWmED7992G

https://youtu.be/BIqLk23hE90?list=PLZU5hLL_713x0_AV_rVbay0pWmED7992G

get familiar with the yosis syntesis tool to convert the verilog code into a CMOS circuit

https://www.mehmetburakaykenar.com/synthesis-n-bit-counter-with-open-source-yosys-synthesizer/294/

https://github.com/spdy1895/RTL_synthesis_using_sky130

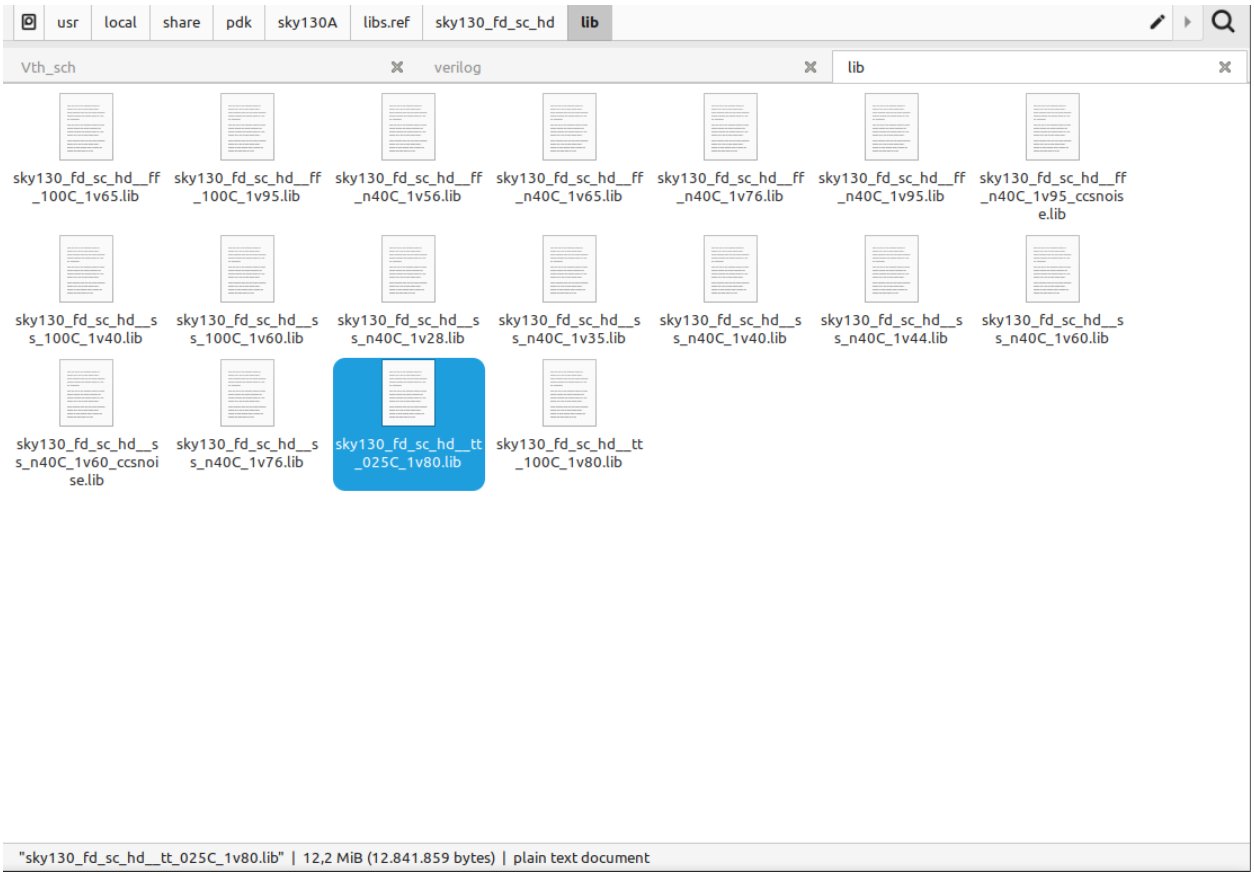
https://github.com/Imellal/RTL-workshop-Sky130-PDK

After install YoSys (see the bash file in the repository), run the following commands—

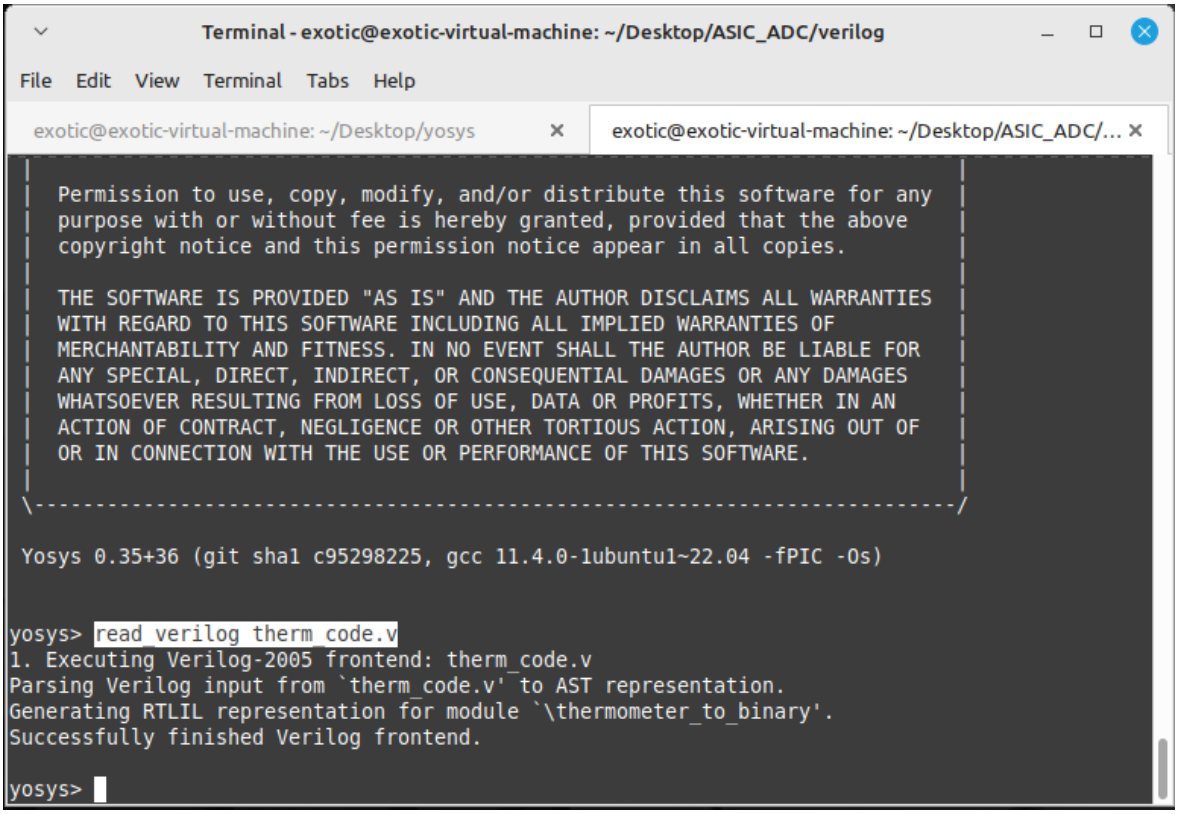
>> yosys // open yosys console in terminal

>> read_liberty -lib /usr/local/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib

// reading the suitable liberty file (see the screenshot below)



>> **read_verilog therm_code.v** // read the verilog file



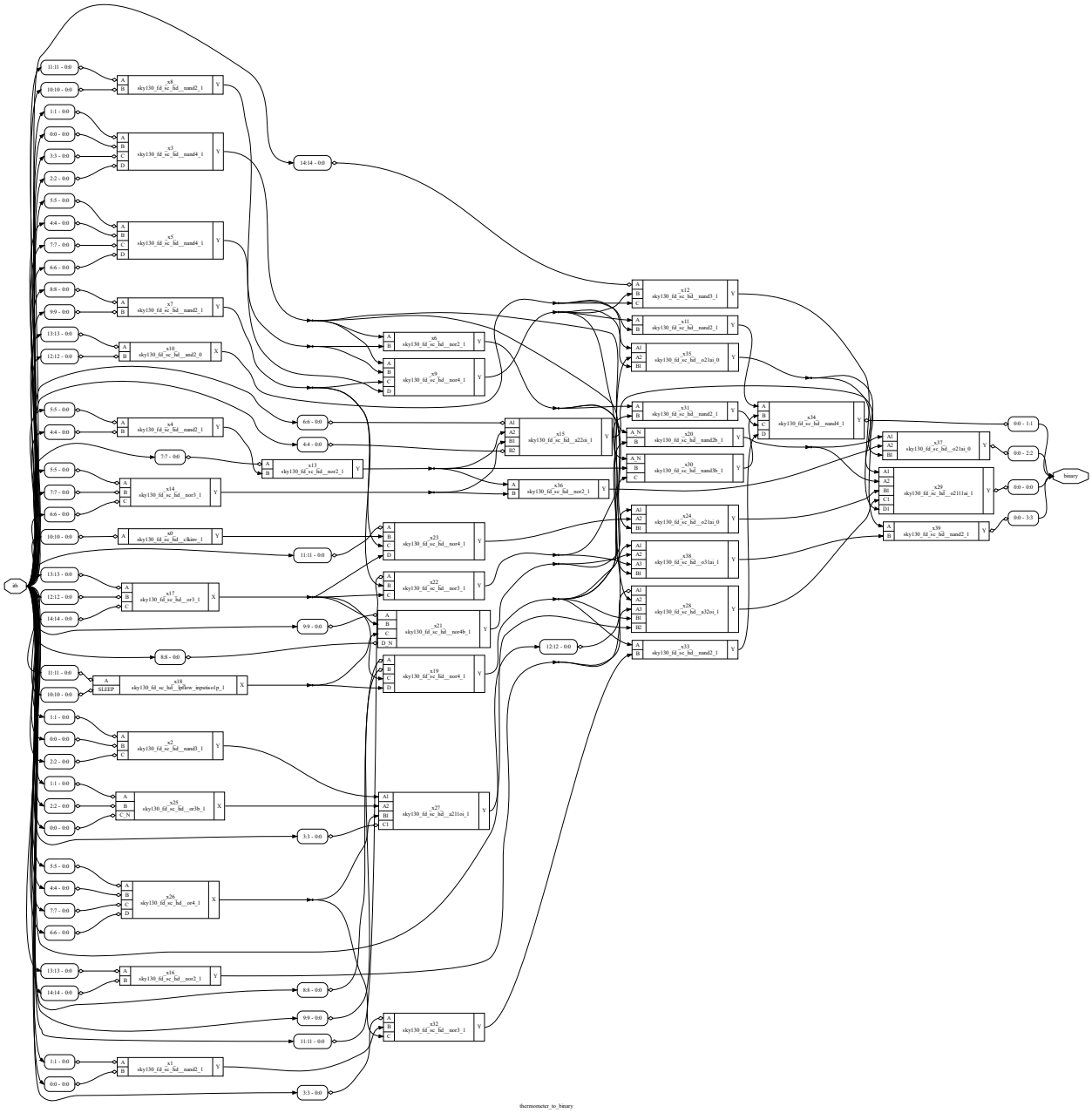
>> **synth -top thermometer_to_binary** // synthesize the module

>> **abc -liberty**
/usr/local/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib

```
>> flatten      // // to invoke flat synthesis after netlist generation
// netlist generation
>> show // vew graphical

>> write_verilog therm.v // write the generated netlist to a new module/verilog file
for verification
Or
>> write_verilog -noattr therm.v // // to write verilog netlist without
attributes(clean)
Optimize:
```
>> **flatten**
>> **opt_clean -purge** // running optimization
```
>> show

```
>> **write_spice therm.spice**
```
>> show -prefix therm -format svg //save diagram in .svg
Or
>> show -prefix therm -format dot //save diagram in .dot
Or
```
>> **show -enum -prefix therm -format dot** //save diagram in .dot with gate numbers



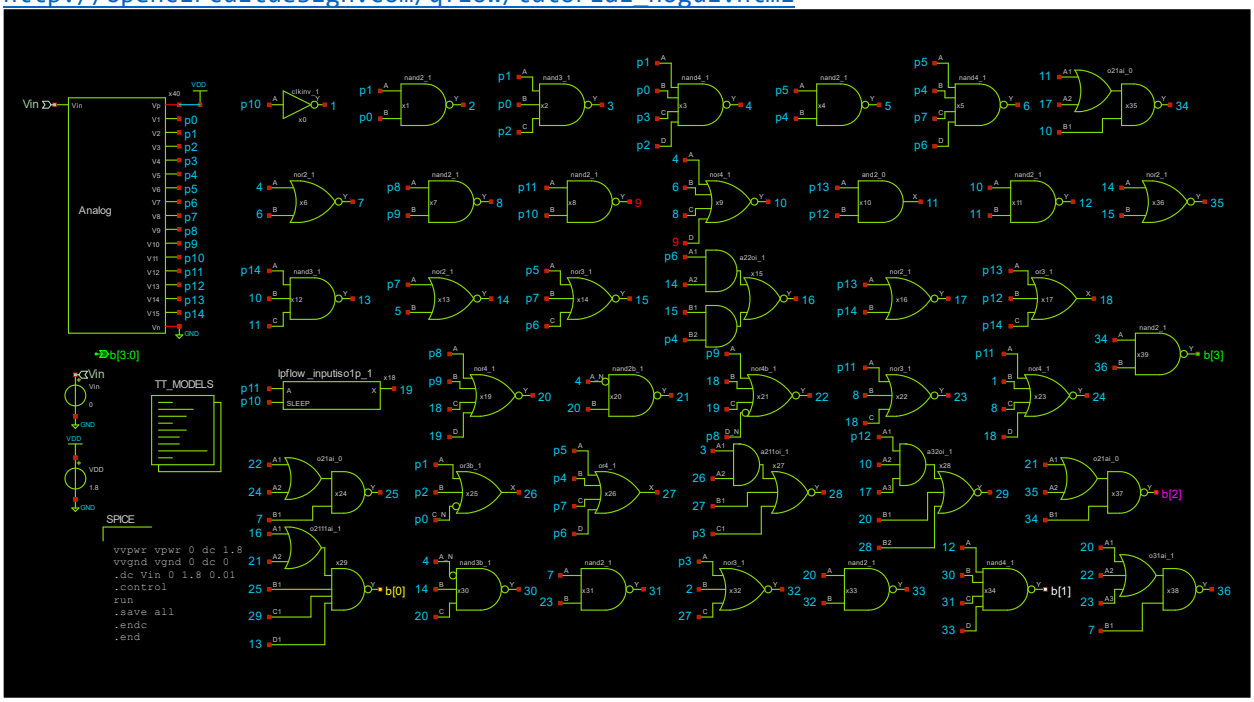
Netlist to schematic conversion:
https://github.com/aidangoettsch/asg

install NetlistViewer:
https://github.com/f18m/netlist-viewer/blob/master/NetlistViewer/build/linux/README.md

doteditor:
https://sourceforge.net/projects/netlistviewer/

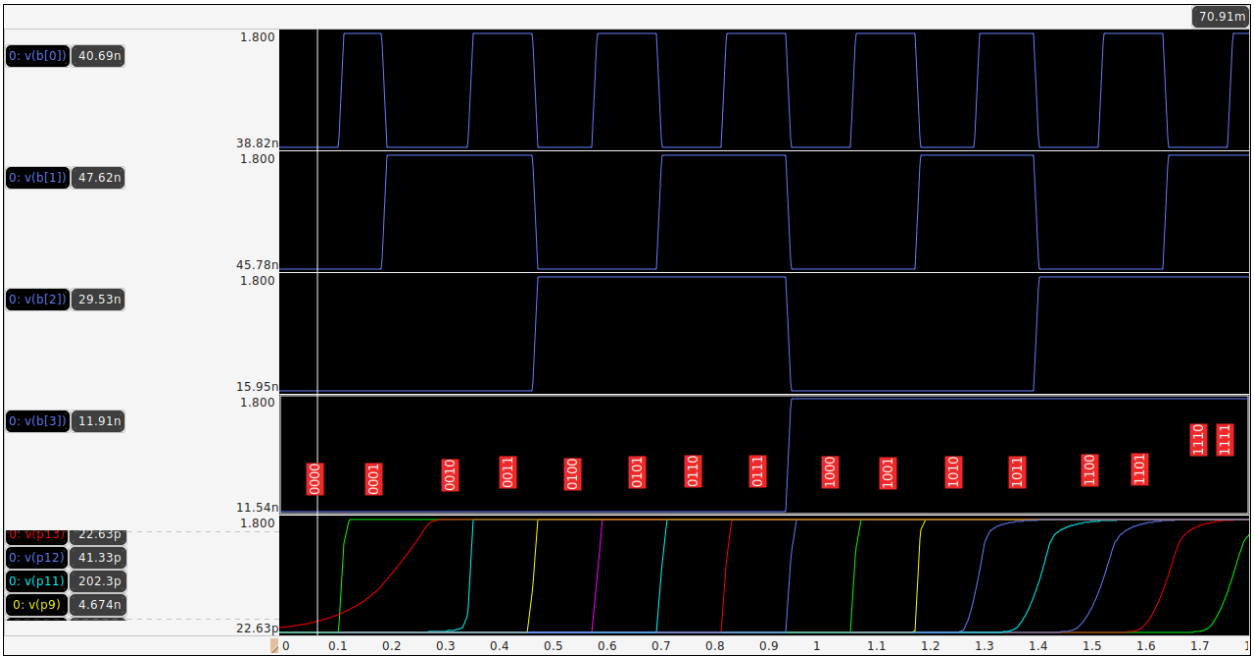
Iverilog with gtkwave:
https://youtu.be/Ryt1ms8Tido

Digital flow with qflow:
http://opencircuitdesign.com/qflow/tutorial_nogui.html



- simulate the complete (ultra small) ADC

Prelayout simulation:



References:

https://github.com/bluecmd/learn-sky130/blob/main/schematic/xschem/getting-started.md

`----------`

Run iverilo/icarus

iverilog file.v

vvp a.out
