OSTBAYERISCHE TECHNISCHE HOCHSCHULE REGENSBURG
ELEKTRO- UND INFORMATIONSTECHNIK

Circuit Integration Internship (PSI)

Experiment No.: **SI3**
Experiment title: **Development of a 5-bit up-counter C.**
Experimental concept: **Schimpfle / F. Aschauer / D. Kohlert**

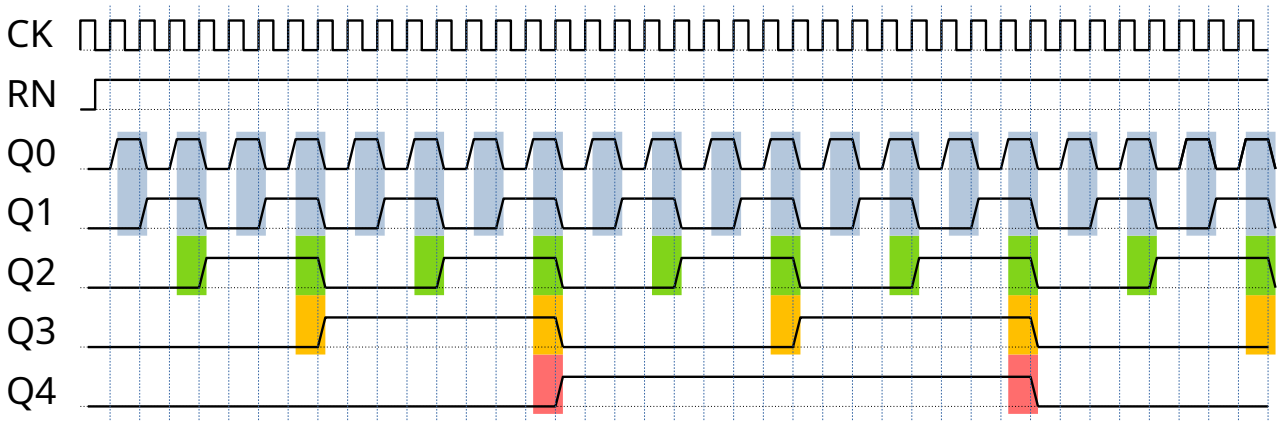
I. Experimental objective

In experiments SI0 to SI3, you will learn how to use a very powerful EDA (Electronic Design Automation) software package used in industry. You will practice using the programs using complete design flows for fully custom and standard cell designs.

II. Brief description of the experiment

III Experimental procedure
III.1 Function of the 5-bit up-counter with T flip-flops

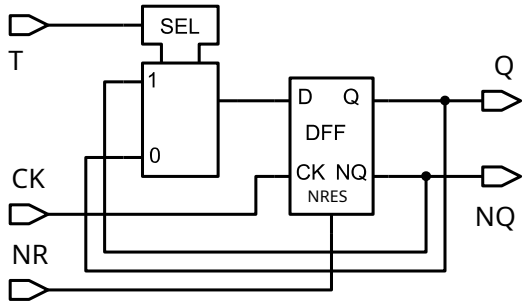
Desired timeline:

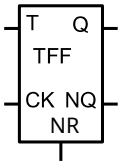


Condition for changing the output value (“Toggle”)

Q0: Every act. Clock edge
Q1: Q0 = 1
Q2: Q0 * Q1 = 1
Q3: Q0 * Q1* Q2 = 1 Q4:
Q0 * Q1* Q2 *Q3 = 1

What's needed is a flip-flop that changes its value when an active control signal is present at the input and when the clock edge is active. It can be constructed from a D flip-flop and a 2:1 multiplexer connected upstream:

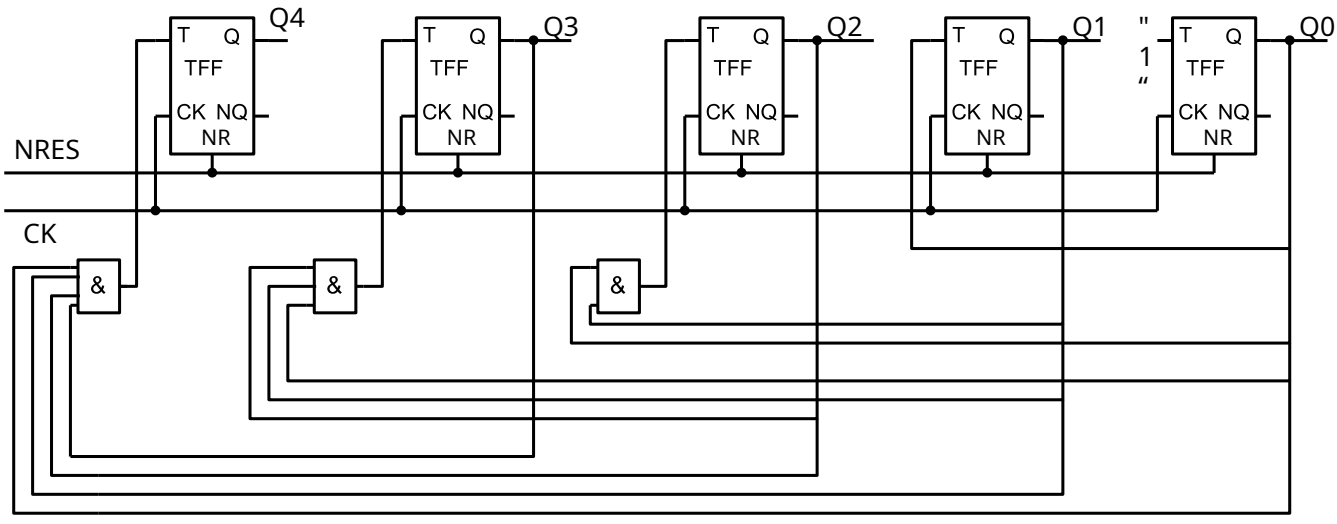




The TFF has a low-active, asynchronous reset input.

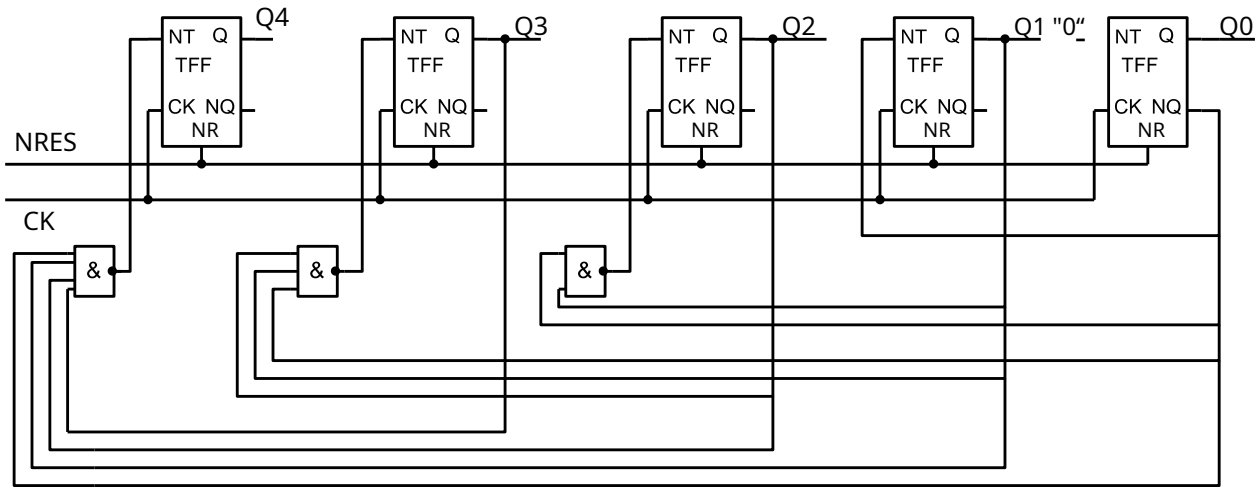
For T=1, the output value changes with the next rising clock edge, as the NQ output of the DFF is adopted. For T = 0, the value at the output remains. The T input is therefore active high, and the corresponding input signals

can therefore be generated with AND gates:



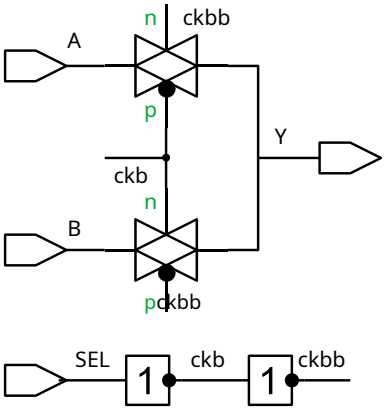
In the lab, there are no AND gates with different numbers available. Using NAND gates is preferable anyway, because AND gates can only be implemented as NAND gates with a downstream inverter.
If TFFs with active-low inputs are used instead of the TFFs with high-active inputs used above, NAND gates can be used instead of the AND gates. A NAND gate with four inputs was already implemented in the practical course, which should provide all the necessary NAND gates. Unneeded inputs are fixed to '1'. While this would be a waste of space on a commercial chip, it is not relevant here.

Implementation of the counter with NAND gates:



Structure of the T flip-flop:

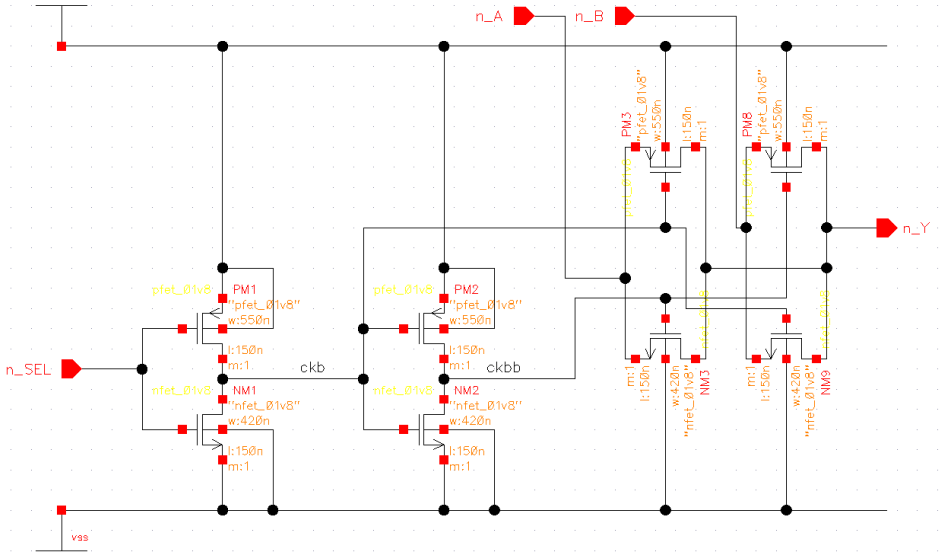
The multiplexer can be constructed from transmission gates



SEL = 1: Y = A

SEL = 0: Y = B

The following figure shows the mux with the two inverters as a transistor circuit:



III.2 T-flip-flop

III.2.1 Structure of the T flip-flop

Preliminary remark:
All provided standard cells can be copied from the "psi" library to your own working library. The various contact cells should also be copied.

The 2:1 multiplexer and the D flip-flop are already specified as schematic and layout (mux2_psi and dff_nr_psi).

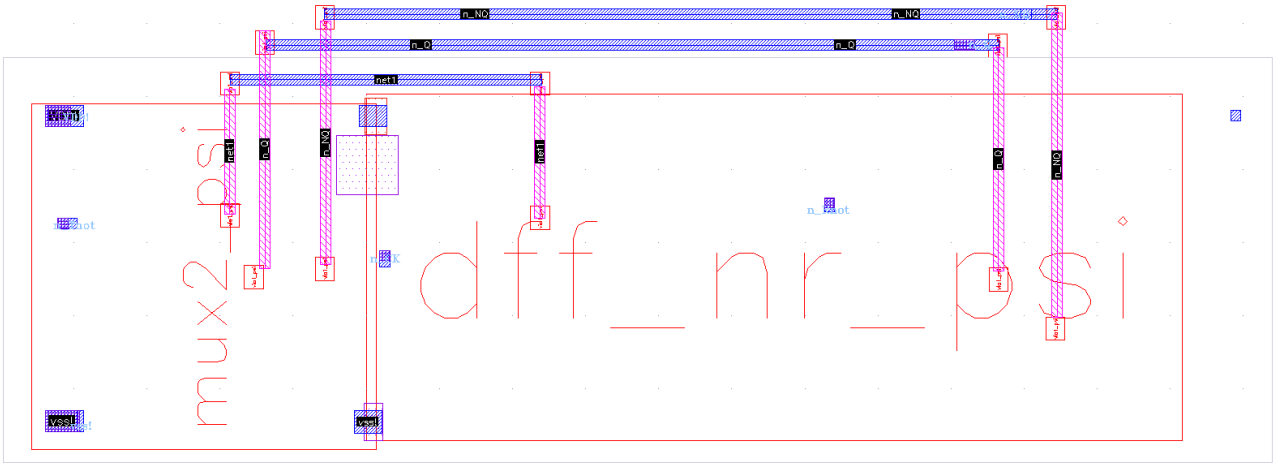
First, build a TFF with a low-active T input from the two cells in the schematic! Equip the circuit with the pins! Symbols for supply voltages do not need to be included here, as they are present as global networks inside the two cells.
Copy the schematic into the log file! Create the symbol!

III.2.2 Functional simulation of the T flip-flop

For simulation, you should create a "testbench", i.e. a circuit that contains the symbol, as well as pins and symbols of the global supply voltages (VDD and vss)
These symbols are located in the "basic" library. Since an error message is generated if unconnected supply voltages are present, both symbols should be connected, for example, with a 1G ohm resistor (res, in the analogLib library).
Consider test signals that can verify the function.
Create a simulation as described in PSI2, IV.2, and verify the function. Copy the timing into the log file!

III.2.3 Layout of the T flip-flop

Create a layout of the circuit!
The wiring of the cells should already be done according to the standard cell methodology, i.e.: A Via1 (contact Met1 - Met2) is placed on the pins in the underlying cells. From this, a vertical M2 path is routed upwards, which leads back to a Via 1. The horizontal connections are then again made in the M1.



The external connections of the overall circuit are placed outside the circuit as M1 squares. These must be moved to the corresponding pins. The pins require a pin designator (M1 pin). Additionally, an M1 patch must be placed on each pin at the highest hierarchy level; this patch should extend beyond the M1 pin area. It has been shown that pins are best placed where the M1 drawing area is located but not the M1 area.

Install all pins as described in PSI2, IV.3!

III.2.4 Check of the T flip-flop (DRC, LVS)

Check the layout with the DRC!
Run a LVS and correct any errors! Document the results!

III.3 Successive construction of the 5-bit counter

III.3.1 Schematic of the overall circuit

First, build the counter circuit in the schematic using the TFFs and the self-made 4-fold NANDs!
Add pins to the circuit! Copy the schematic into the log file! Create the symbol!

III.3.2 Functional simulation of the overall circuit

To simulate the entire circuit, proceed as described under**III.2.2**Consider test signals that can verify the function.
Create a simulation as described in PSI2, IV.2, and verify the function. The simulation can also display signals that are not routed to the outside as pins:

In the Maestro selection window for "Outputs":
Cursor on cell in the schematic (yellow border)
RMB: "Descend Read"
Click cell again
Schematic below appears
If necessary: Click on the cell in this schematic again
RMB: "Descend Read"
Click on signal
Back:
Cursor in the schematic:
RMB / Return

In this way, insert the signal at the D input of the most significant DFF into the simulation!

Determine the signal propagation time from the clock pulse (CK) to this signal (low->high and high->low).
What conclusions can you draw about the maximum clock frequency from this?

III.3.3 Layout of the overall circuit

Create a layout of the circuit!
The wiring of the cells should already be done according to the standard cell methodology.

III.3.4 Check of the entire circuit (DRC, LVS)

Check the layout with the DRC!
Run a LVS and correct any errors! Document the results!

III.3.5 Parasitics Extraction and Post-Simulation

Description Parasitics Extraction . . . . . .

III.3.6 Determination of the maximum possible clock frequency

Determine again the signal propagation time from the clock (CK) to the signal at the D input of the most significant DFF!
What conclusions can be drawn about the maximum clock frequency from this? Compare the result with the previous one.