A sample and hold circuit for pipelined ADC

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Abstract: A high performance sample-and-hold (S/H) circuit used in a pipelined analog-to-digital converter (ADC) is presented in this paper. Fully-differential capacitor flip-around architecture was used in this S/H circuit. A gain-boosted folded cascode operational transconductance amplifier (OTA) with a DC gain of 90 dB and a GBW of 738 MHz was designed. A low supply voltage bootstrapped switch was used to improve the linearity of the S/H circuit. With these techniques, the designed S/H circuit can reach 94 dB SFDR for a 48.9 MHz input frequency with 100 MS/s sampling rate. Measurement results of a 14-bit 100-MS/s pipeline ADC with designed S/H circuit are presented.

Key words: S/H circuit; bootstrapped switch; gain-boosted OTA
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1. Introduction

Wireless communication and wireless data transfer technology has developed rapidly with the advent of the era of the mobile Internet. ADCs are key components in wireless communication systems. With improvements in technology, today's wireless communication systems require high-performance ADCs. Pipeline ADC is probably the optimal choice with the resolution in the range of 12–16 bits, and a sampling rate of 80–250 MS/s[1–4]. As a key part of pipelined ADC, the S/H circuit is widely adopted in high speed pipelined ADC to reduce the aperture error of the signal channel between the MDAC and sub-ADC at the first stage of pipelined ADC[5, 6].

OTA is the core part of the S/H circuit and requires outstanding performance of open loop gain, GBW and slew rate. The on-resistance and nonlinearity of the sampling switch influence the sampling speed and precision of the S/H circuit. In this paper, a differential folded cascode configuration OTA with gain-boost was implemented to attain a high DC gain and large bandwidth, and a low supply voltage bootstrapped switch was used, which could obtain low-on-resistance and considerable linearity by improving the gate voltage.

2. S/H circuit topology

There are two types of structures widely used in S/H circuits: the charge redistribution S/H architecture as shown in Fig. 1(a) and the capacitor flip-around S/H circuit as shown in Fig. 1(b). Fig. 1(c) is the timing diagram, in which ϕ_1 and ϕ_2 are two-phase non-overlapping clocks standing for the sampling phase and holding phase, respectively. The falling edge of ϕ_{1p} is earlier than that of ϕ_1, thus reducing the channel charge injection.

The capacitor flip-around S/H circuit has several advantages against the charge redistribution S/H circuit[7, 8]. First, the former has twice as much feedback factor as the latter, resulting in lower power consumption when the S/H circuit required the same closed-loop bandwidth. Second, the input reference noise power of the former is lower than that of the latter. As a result, the capacitor flip-around S/H circuit is widely used in high speed S/H circuits, which was also adopted in this design.

3. Switches

As the key block of the S/H circuit, sampling switches may impact its precision and linearity. Channel charge injection, finite on-resistance and clock feedthrough are major factors for deteriorating the switch linearity. Clock feedthrough and channel charge injection could be reduced by the bottom-plate sampling technique; while the MOS on-resistance modulation is mainly resulted from the changes in gate-source voltage, it could be reduced by using the bootstrapped switch.

For a short channel device, on-resistance is given by

$$R_{\rm on} = \frac{1 + (V_{\rm D} - V_{\rm s})/E_{\rm c}L}{\mu_{\rm n}C_{\rm ox}W/L(V_{\rm G} - V_{\rm s}/2 - V_{\rm D}/2 - V_{\rm TH})}, \quad (1)$$

in which

$$V_{\rm TH} = V_{\rm THO} + \gamma\left(\sqrt{|2\varphi_{\rm f} + V_{\rm S} - V_{\rm B}|} - \sqrt{|2\varphi_{\rm f}|}\right), \quad (2)$$

where $V_{\rm G}$, $V_{\rm s}$, $V_{\rm D}$ and $V_{\rm B}$ are the voltages on the gate, source, drain and bulk terminals of MOS transistors respectively and $E_{\rm c}$ is electric field intensity. From Eq. (1), MOS on-resistance is mainly influenced by three factors: first, the voltage $V_{\rm G}-V_{\rm s}/2-V_{\rm D}/2-V_{\rm TH}$; second, the drain–source voltage of switch transistors; and third, the change of threshold voltage due to source–bulk voltage[9].

In the designed S/H circuit, the bootstrapped switch was

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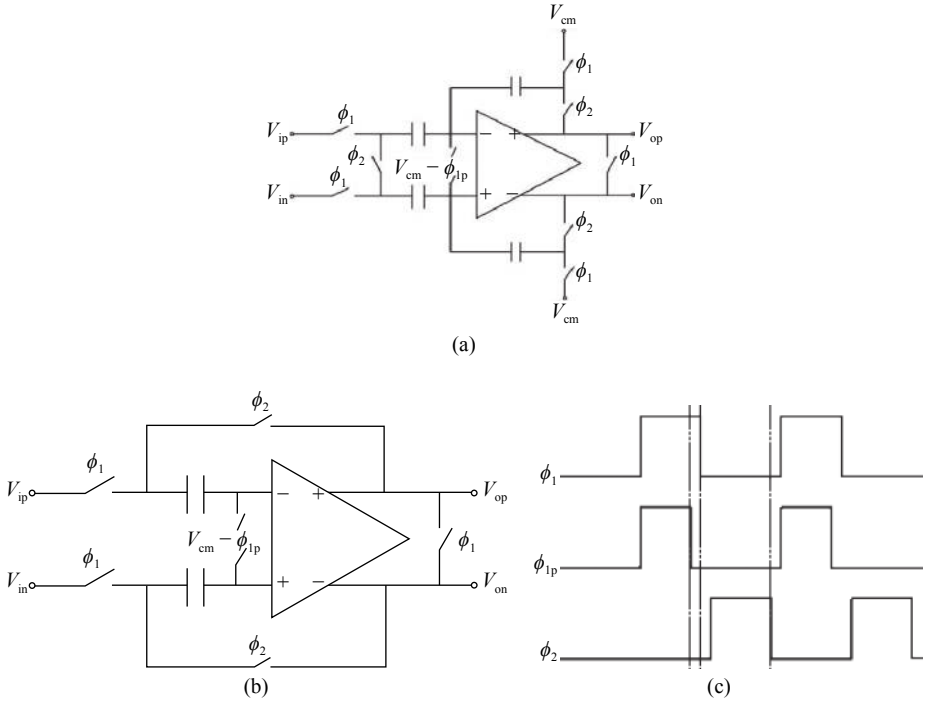

Fig. 1. (a) Charge redistribution S/H circuit. (b) Capacitor flip-around S/H circuit. (c) Timing diagram.

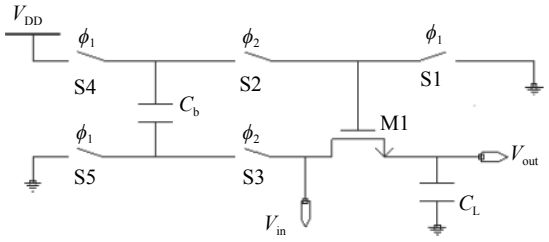

Fig. 2. Bootstrapped switch schematic diagram.

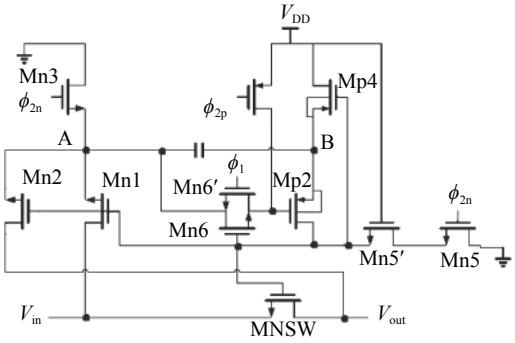

Fig. 3. Bootstrapped switch.

used to connect to the input. Its basic principle is shown in Fig. 2, in which ϕ_1 and ϕ_2 are two-phase non-overlapping clocks. When ϕ_1 is high, S1, S4 and S5 turn on, S2 and S3 turn off, the ground level is added to the gate of the NMOS transistor M1 so that it can be effectively shut off, in the meantime the voltage at both ends of capacitor Cb is charged to V_{DD}. When ϕ_2 is high, S1, S4 and S5 turn off, S2 and S3 turn on, the voltage of capacitor Cb remains V_{DD}, so the voltage of the gate–source of M1 is constant and the conduction resistance of M1 remains the same when V_{in} is changed.

A low supply voltage bootstrapped switch was used as the front-end switch. As shown in Fig. 3, MOS transistors Mn1, Mp2, Mn3, Mp4, and Mn5 correspond to the five ideal switches S1–S5 in Fig. 2 respectively. Additional transistors and modified connectivity shown in Fig. 3 were introduced to extend all switch operations from rail-to-rail while limiting all gate–source voltages to V_{DD}. Gate connections of MP4 and MP2 prevent their overstress as the voltage on node B rises above V_{DD}. Transistor Mn6' triggers Mp2 on at the beginning of Φ_1, while transistor Mn6 keeps it on as the voltage on node A rises to the input voltage. Furthermore, to prevent the gate–drain voltage of Mn5 exceeding V_{DD} during Φ_1 transistor Mn5' is added in this circuit. This bootstrapped switch can operate from rail to rail and all gate–source and gate–drain voltages in this structure are limited to V_{DD}. Thus, harmonic distortion effects are significantly reduced by this switch[10, 11].

4. Operational transconductance amplifier (OTA)

An OTA is the core part of the S/H circuit, which determines the performance of the circuit. According to the requirements of the circuit, there are two most important parameters of OTA: one is the DC gain, while the other is the gain bandwidth (GBW).

The sampling rate of the circuit designed in this paper is 100 MSPS, the time used on the sampling phase is 5 ns, we set 1/2 of the rest time as the slew time, and 1/2 of the rest time as the small signal establishment time.

$$V_{out} = V_{out\text{-}ideal}\,(1 - e^{-\frac{t}{\tau}}), \tag{3}$$

where the V_{out} is the actual voltage, the $V_{out\text{-}ideal}$ is the ideal voltage, and τ is the time constant, assuming that

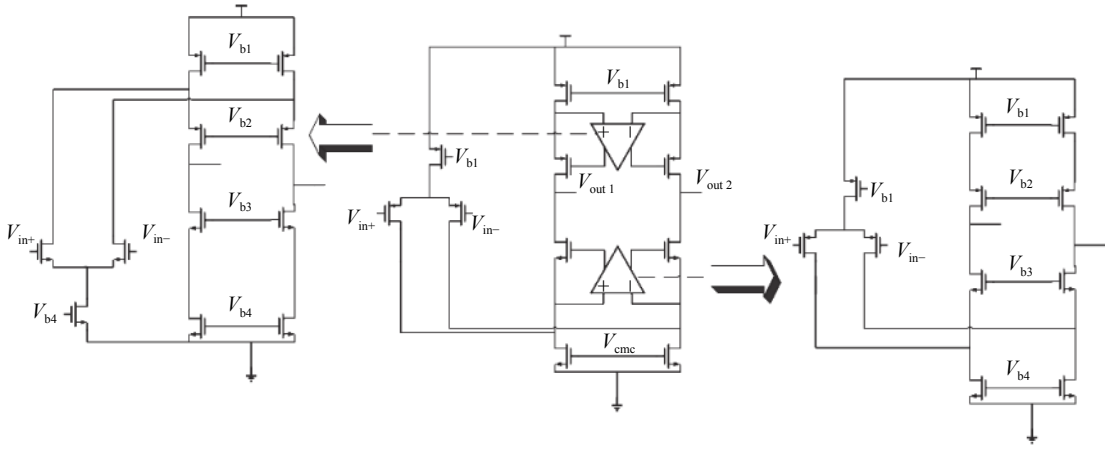

Fig. 4. OTA.

$$V_{\text{out-ideal}}\mathrm{e}^{-\frac{t}{\tau}} < \text{LSB}/2, \tag{4}$$

in which LSB is the least significant bit, thus

$$f_{\text{u}} > \frac{(N+2)\ln 2}{2\pi\beta t}, \tag{5}$$

in the above formula, the operational amplifier GBW is f_{u}, N is the resolution (14 bit), the feedback factor β is 1, t is the small signal establishment time of the OTA (2.5 ns), and calculated from Eq. (5) the GBW of the OTA is 706 MHz.

The input and output voltage of the S/H circuit satisfy the following equation

$$V_{\text{out}} \approx \frac{V_{\text{in}}}{\beta}\left(1-\frac{1}{A\beta}\right), \tag{6}$$

where A is the open loop gain of the OTA, assuming that

$$\frac{1}{A\beta} < \text{LSB}/2, \tag{7}$$

thus

$$\frac{1}{A\beta} < \frac{1}{2^{N+1}}, \tag{8}$$

based on the inequality (8), the open loop gain of the OTA is 90 dB.

It is difficult to combine high DC gain with high GBW in a CMOS OTA. A single-stage OTA is always used in high speed designs; it mainly has a folded cascode structure and telescopic structure. In order to adapt to a variety of common mode signal level and handle single-ended input signals, the OTA needs to have a large range of input voltage, and for high gain, the folded cascode structure with a gain-boosting technique was used in this S/H circuit[12].

The designed OTA schematic is shown in Fig. 4. PMOS transistors were chosen to be input pairs since PMOS transistors have less $1/f$ noise and higher nondominant pole than NMOS transistors. The auxiliary amplifiers also used folded cascode architecture. The gain of OTA can be increased by auxiliary amplifiers, but a zero-pole pair is also introduced. When the GBW of main amplifier ω_{u}, the second pole of the OTA ω_{p}, and the GBW of auxiliary amplifier $\omega_{\text{a-u}}$ meet the following conditions

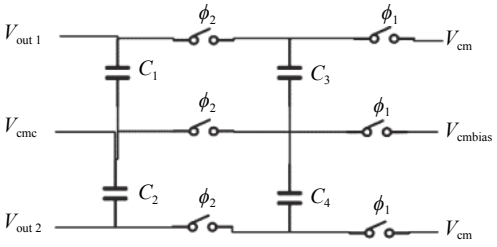

Fig. 5. SC-CMFB.

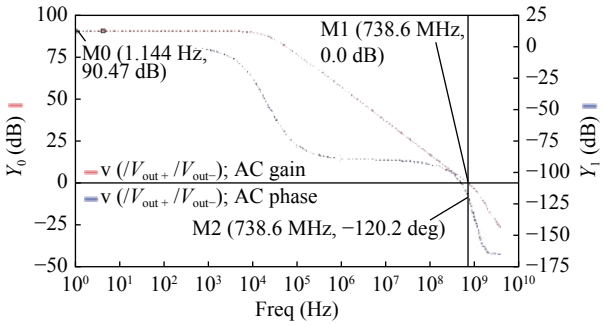

Fig. 6. Simulation of OTA.

$$\omega_{\text{u}}\beta < \omega_{\text{a-u}} < \omega_{\text{p}}, \tag{9}$$

the effect of a zero-pole pair on the settling time can be reduced[13]. A detailed design of this OTA can be found in Refs. [14, 15].

The common-mode feedback circuit is essential for a fully differential OTA. As the switch capacitor common mode feedback (SC-CMFB) has large output swing and no static power consumption, it is widely used in S/H circuits. This design used the SC-CMFB as shown in Fig. 5, ϕ_1 and ϕ_2 are two-phase non-overlapping clocks, V_{cmbias} is bias voltage, and V_{cm} is the ideal output common mode voltage[16].

5. Experimental results

The AC simulation of the designed OTA is shown in Fig. 6, which shows the OTA has 90 dB DC gain, with the GBW of 738 MHz and a phase margin of 60 degrees. Fig. 7

Table 1. The comparison of the performance with other S/H circuits.

Parameter	Ref. [7]	Ref. [8]	Ref. [17]	This work
Technology (μm)	0.18	0.35	0.18	0.18
Sampling rate (MS/s)	50	50	100	100
SFDR (dB)	94.6 @ 5 MHz	67 @ 2.5 MHz	85.4 @ 10 MHz	94 @ 48.9 MHz
Resolution (bit)	14	10	10	14
Power (mW)	15.4	13.6	7.6	28
Supply voltage (V)	3.3	3.3	3.3	1.8

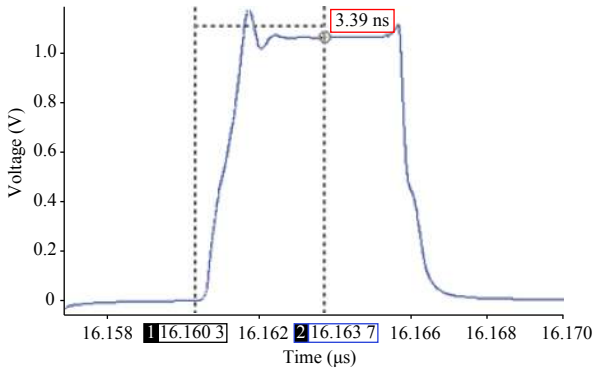

Fig. 7. (Color online) Simulation of one S/H period.

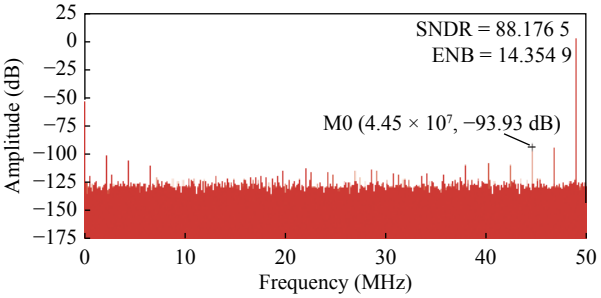

Fig. 8. (Color online) The S/H output spectrum with a 48.9 MHz analog input.

shows the simulation of one S/H period, in which the setting time is 3.39 ns. Fig. 8 shows the FFT results of the S/H circuit at 48.9 MHz input signal frequency with the 100 MHz sampling rate, in which its SFDR is 94 dB and SNDR is 88 dB. The power dissipation of the S/H circuit is 28 mW at a 1.8 V supply voltage.

The designed circuit is compared with that of the published work as shown in Table 1. This work has the best balance of precision and speed while maintaining a competent overall performance.

The die photomicrograph of the S/H circuit using the 0.18 μm CMOS process is shown in Fig. 9. Fig. 10 shows the measurement results of pipelined ADC with the designed S/H circuit at a 100 MHz sampling rate and 29 MHz input signal.

6. Conclusion

This paper describes the design of the S/H circuit used in 14-bit 100 MS/s pipelined ADC. A high performance OTA was realized and a low supply voltage bootstrapped switch was used for good linearity. The simulation results of the S/H

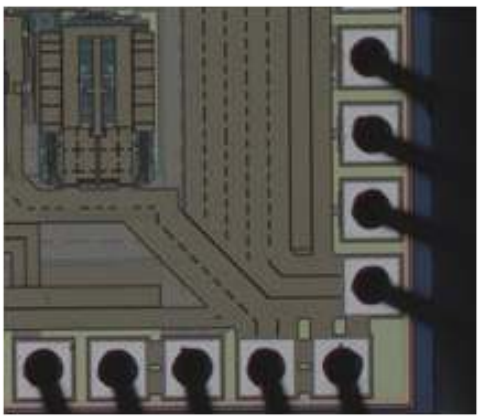

Fig. 9. (Color online) Die photomicrograph.

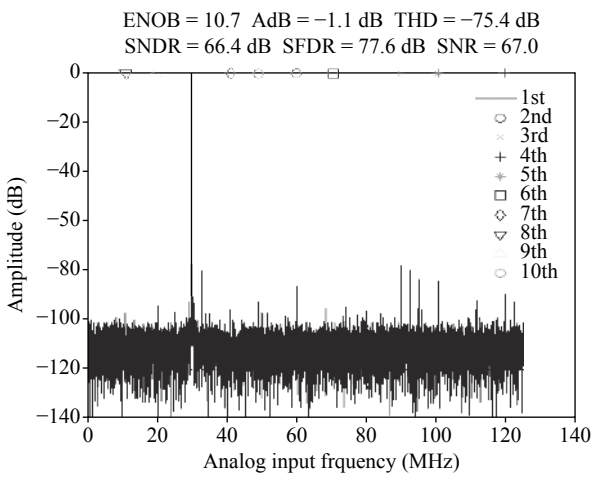

Fig. 10. ADC measurement results.

circuit show that the SNDR is 88 dB and the SFDR is 94 dB at 48.9 MHz input signal frequency with 100 MHz sampling rate. A pipelined ADC with the designed S/H circuit was implemented and measurement results are presented.

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