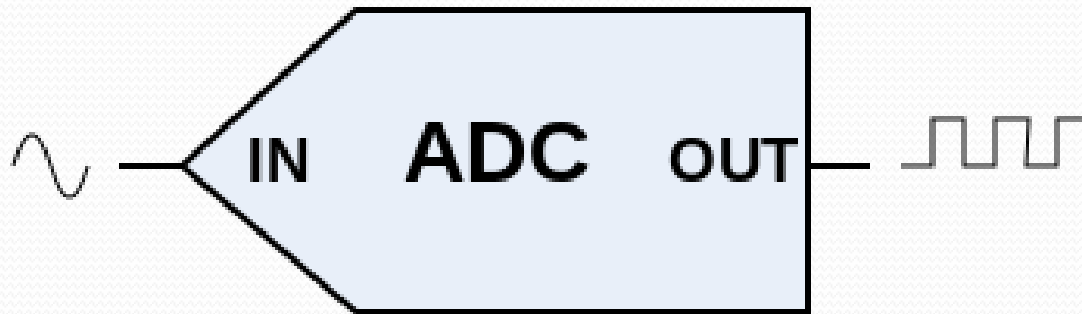


# PIPELINED ADC

# Area of Project :

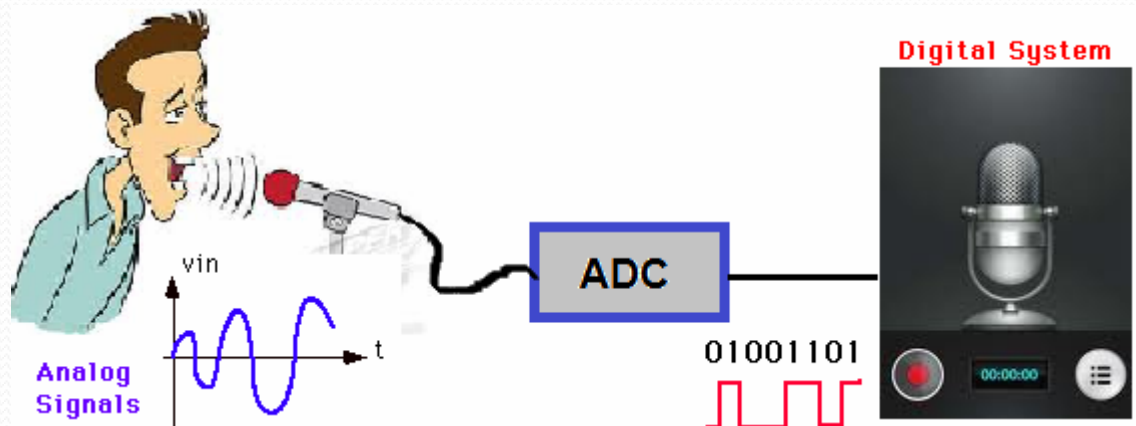
- Project work is in the area of Analog and VLSI Design focussing on data converters.
- Our project deals with ADC.



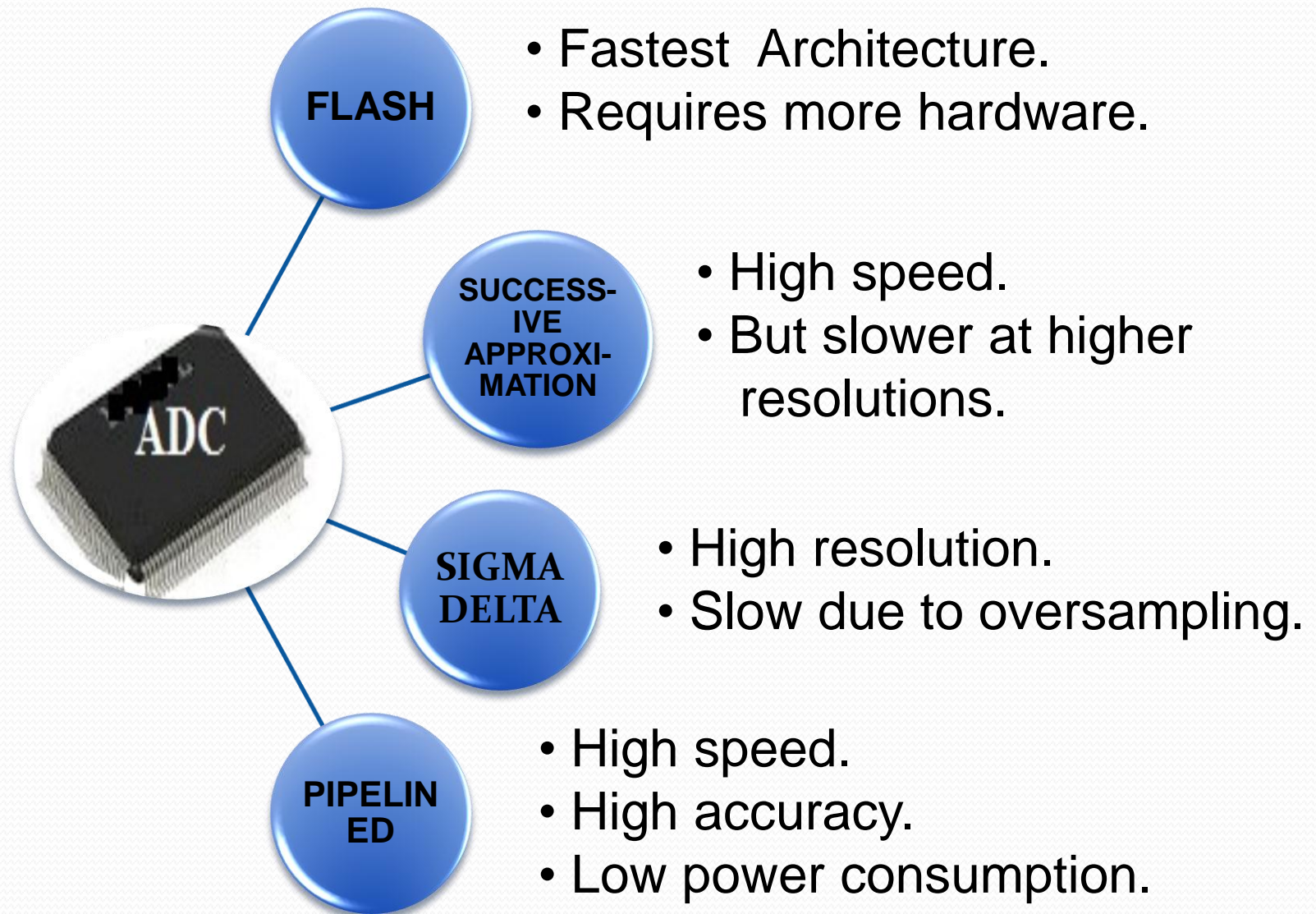
# INTRODUCTION TO ADCs

## ADC???

- Converts analog signals to digital signals.
- Used to establish an interface between analog and digital worlds.



# Types of ADCs :



# Comparison of various ADCs :

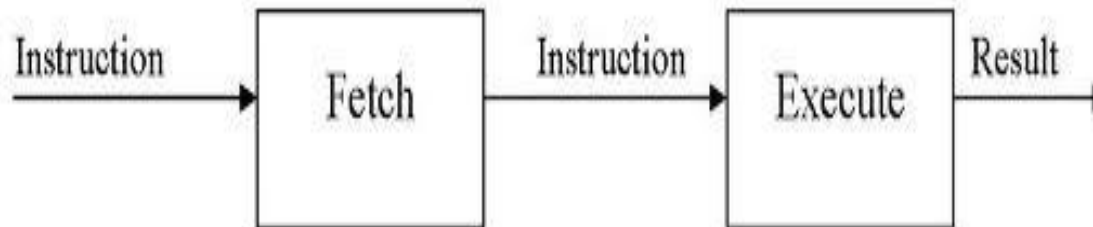
	FLASH ADC	SIGMA DELTA ADC	PIPELINED ADC
Resolution	Low	High	Moderate
Speed	High	Low	High

# Objective of the project :

- This project aims at designing 10-bit Pipelined ADC with high speed (100MHz) and moderate (10 bit) resolution.

# Introduction to pipelined ADC :

- The **Pipelined ADC** uses the concept of pipelining.
- Pipelining is a method of speeding up high volume processes.

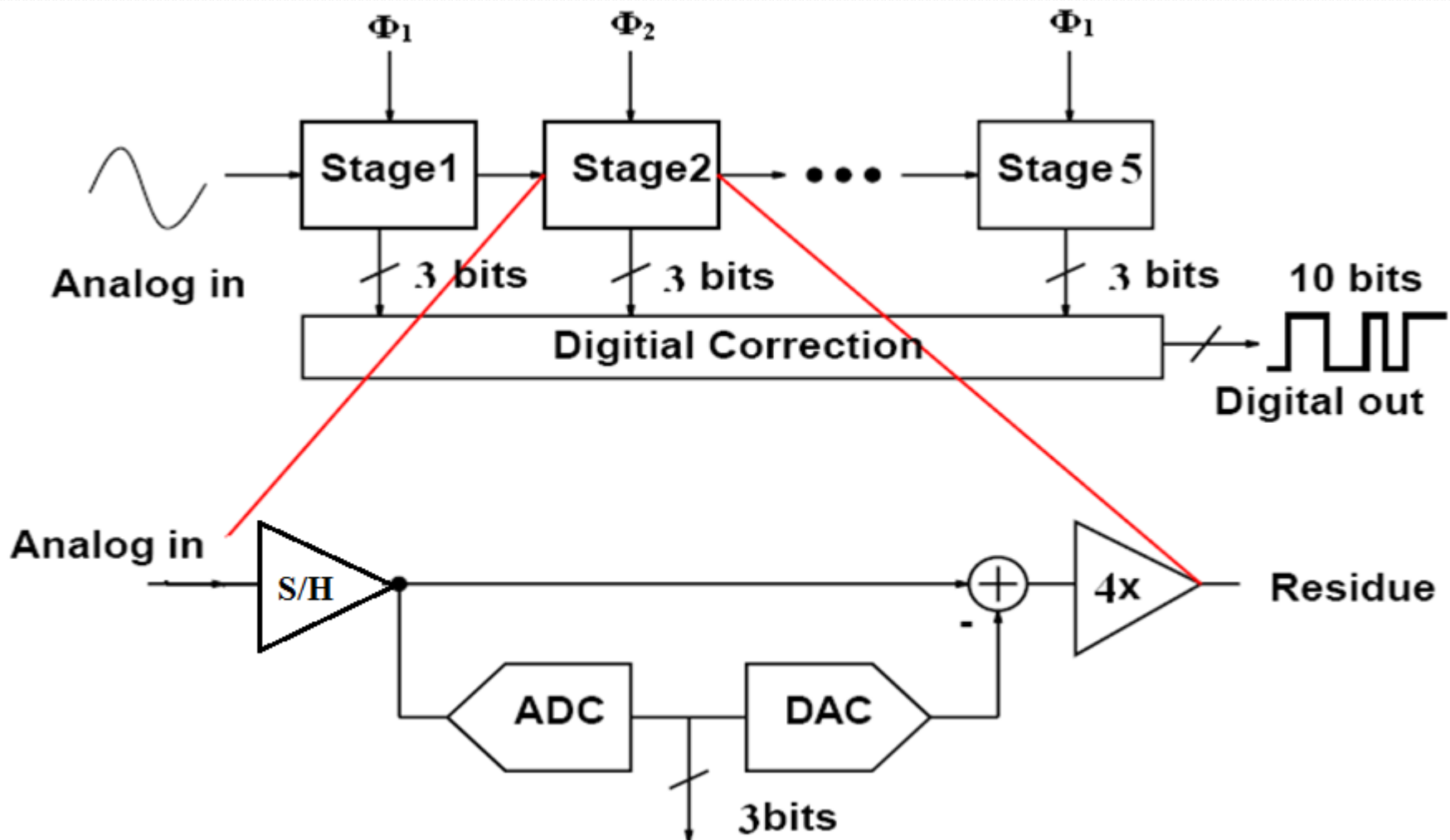


# Specifications :

Stages	5
Resolution	10
No.of bits per stage	3
Sampling Frequency ( $f_s$ )	100 MHz

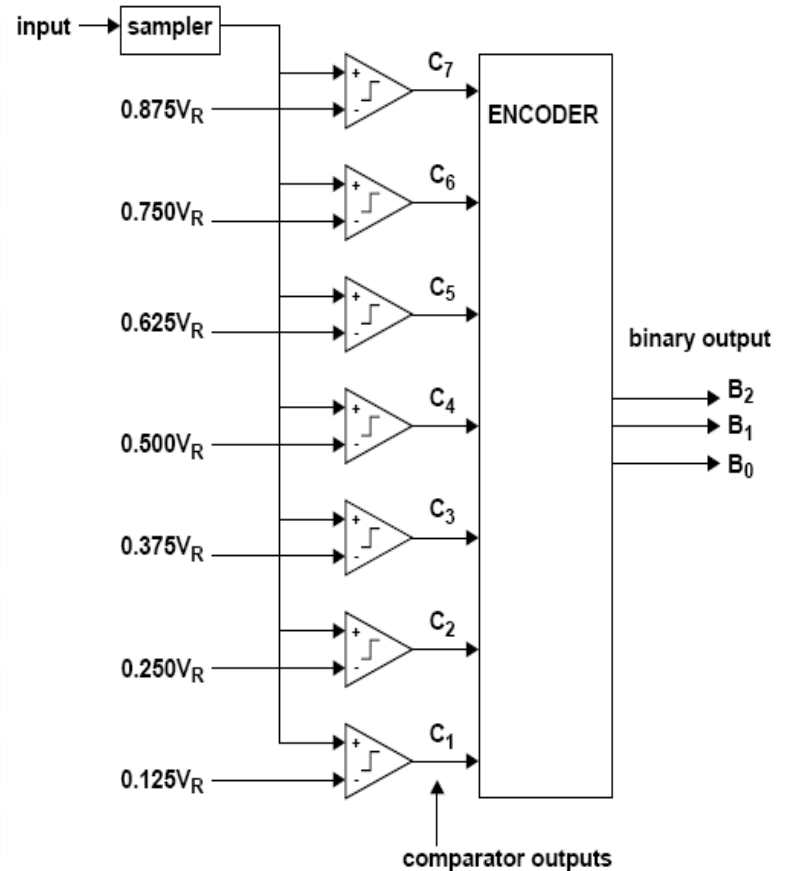


# Block diagram of Pipelined ADC :



# Sub-ADC (Flash) :

- Also known as a fully parallel architecture.
- An n-bit flash ADC consists of an array of  $2^n - 1$  comparators and a set of  $2^n - 1$  reference values.
- The set of  $2^n - 1$  comparator outputs that result is referred to as a thermometer code.
- The encoder converts the thermometer code produced by the comparators to a binary code as shown in the truth table .



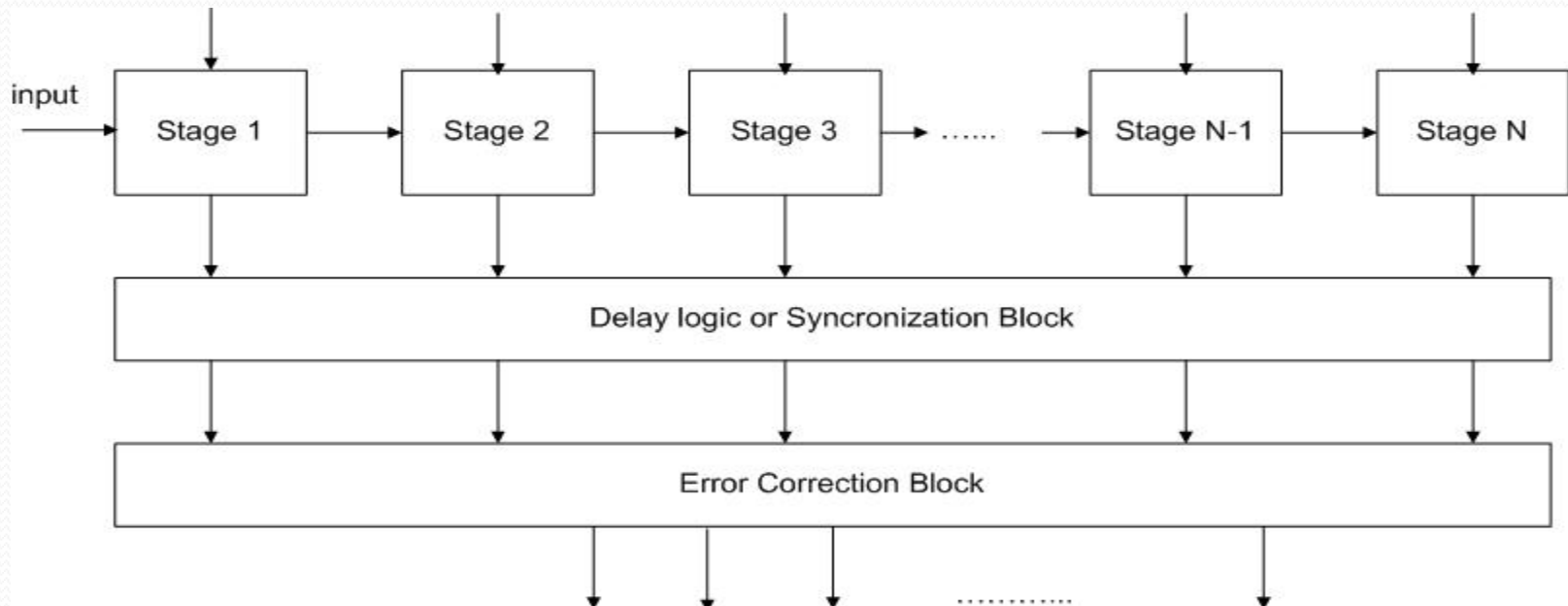
3-BIT FLASH ADC

## Input/Output table of Flash ADC :

[illegible]

# Digital Correction Logic :

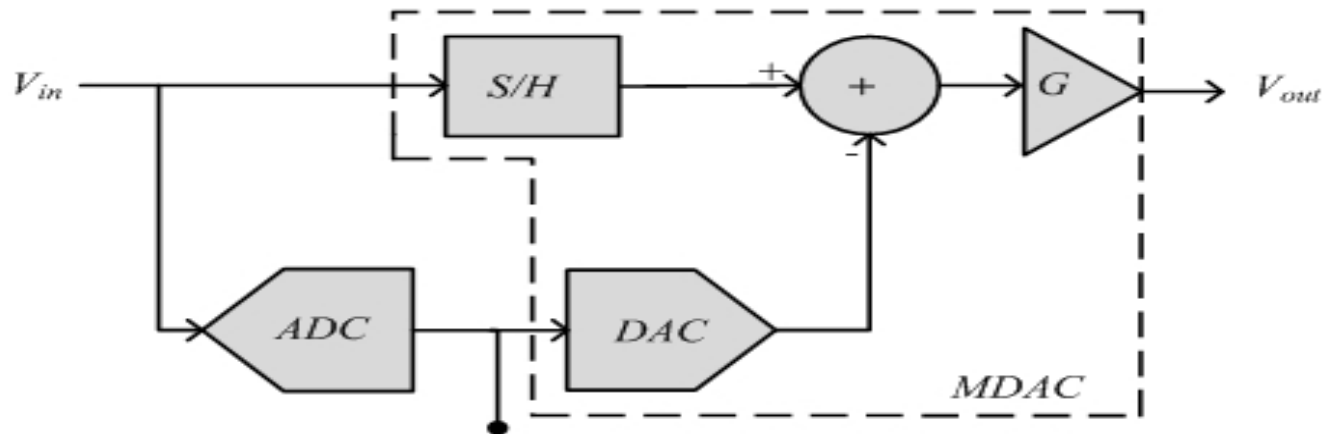
- Consists of shift registers for time alignment.
- It corrects the over ranging problems due to offset and interstage amplifier errors.



# Multiplying DAC :

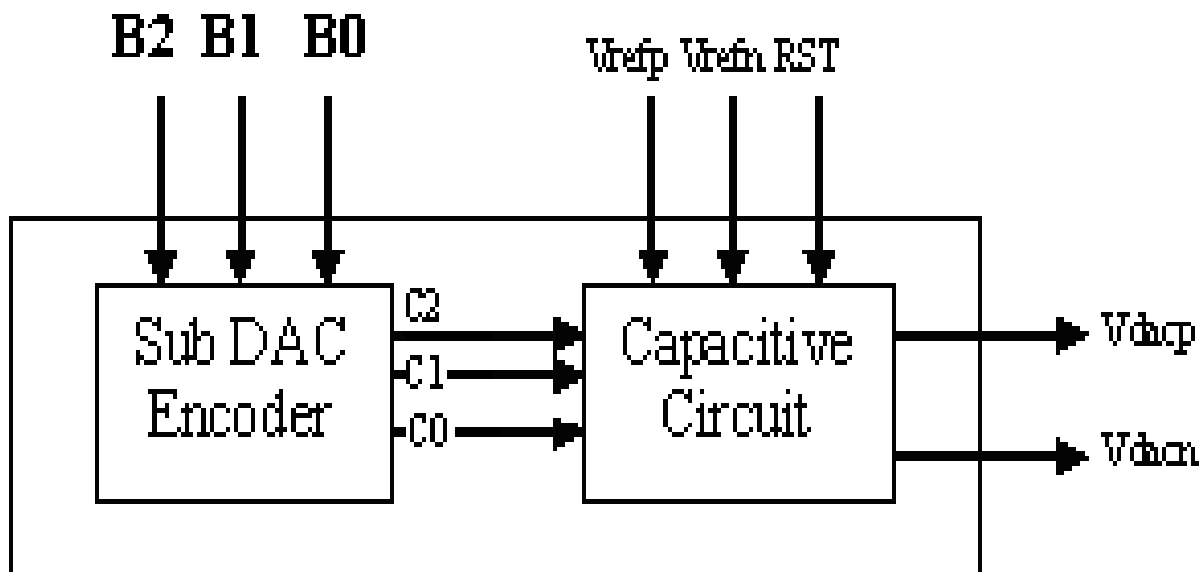
**The function of this circuit is threefold:**

- To sample and hold the input signal.
- To generate a residue that is the difference between the input and sub-DAC output.
- To amplify this residue.



# Sub-DAC :

- Converts the intermediate digital outputs available at every stage into its equivalent analog output.



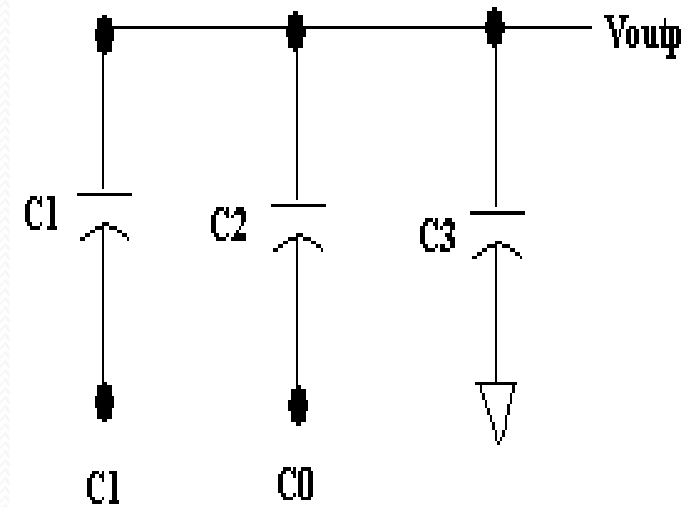
Block Diagram of Sub-DAC

- Inputs for the Sub DAC are the output of Sub ADC (B2, B1, B0), reference voltage ( $V_{\text{ref}}$ ).
- Encoder is used to encode the outputs of the sub-ADC output into the required sequence.

Actual DAC Input B2 B1 B0	Encoded Sequence C2 C1 C0	DAC Output
1 1 0	1 1 1	$V_r$
1 0 1	1 1 0	$2V_r/3$
1 0 0	1 0 1	$V_r/3$
0 1 1	0 0 0	0
0 1 0	0 0 1	$-V_r/3$
0 0 1	0 1 0	$-2V_r/3$
0 0 0	0 1 1	$-V_r$

Input/output Table of Sub-DAC

- To get the required DAC output for the encoded sequence, a capacitive circuit is used.
- It consists of 3 capacitors as shown fig  $C_1$ ,  $C_2$  and  $C_3$  of values  $2C$ ,  $C$  and  $3C$  respectively.
- Two LSB bits  $C_1$  and  $C_0$  are the inputs for the two capacitances and the MSB bit  $C_2$  is used for the sign.





# Example:

- If  $C_1=0$  and  $C_0=0$  then the output is 0, because the capacitors are not charged.
- If  $C_1=0$  and  $C_0=1$  then

$$V_{outp} = \frac{C_2}{C_1 + C_2 + C_3} = \frac{C}{6C} = \frac{1}{6} V_{ref}$$

Similarly,

$$V_{outn} = -\frac{1}{6} V_{ref}$$

It implies

$$V_{out} = V_{outp} - V_{outn} = \frac{1}{3} V_{ref}$$

# Operational Transconductance Amplifier :

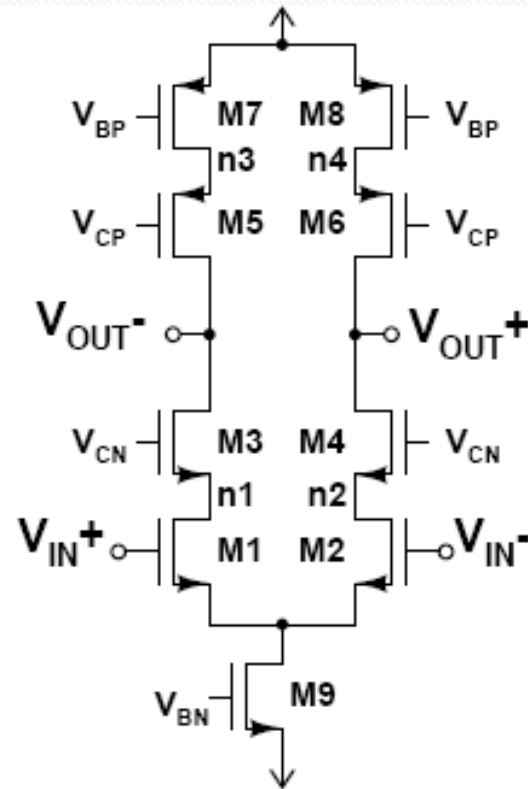
- It is an operational amplifier with high input and output resistance.
- It operates at high frequencies.

## **Types of OTAs :**

- Telescopic OTA
- Folded Cascode OTA
- Gain Boosted OTA

## Telescopic OTA :

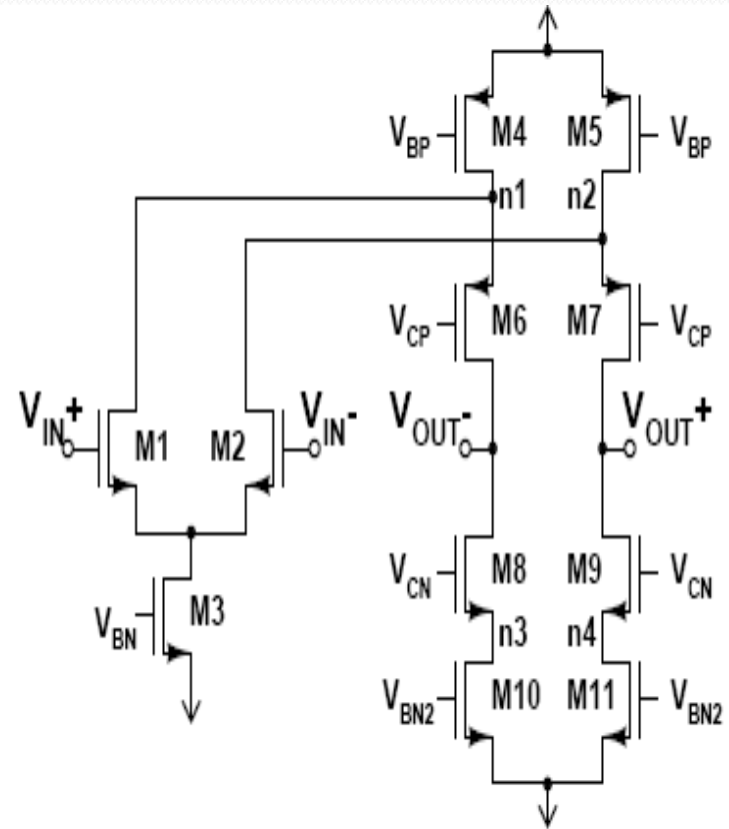
- Fastest possible architecture.
- High voltage gain.
- Large bandwidth.
- Good phase margin.
- Low power consumption.
- Low output swing.



## Telescopic OTA.

# Folded cascode OTA:

- They are of two types namely-
  - Folded cascode top
  - Folded cascode bottom
- Used as auxiliary amplifier.
- Commonly used op-amp architecture .
- Provides a larger output swing.
- Lower voltage gain than that of Telescopic OTA.
- More power dissipation.





High gain



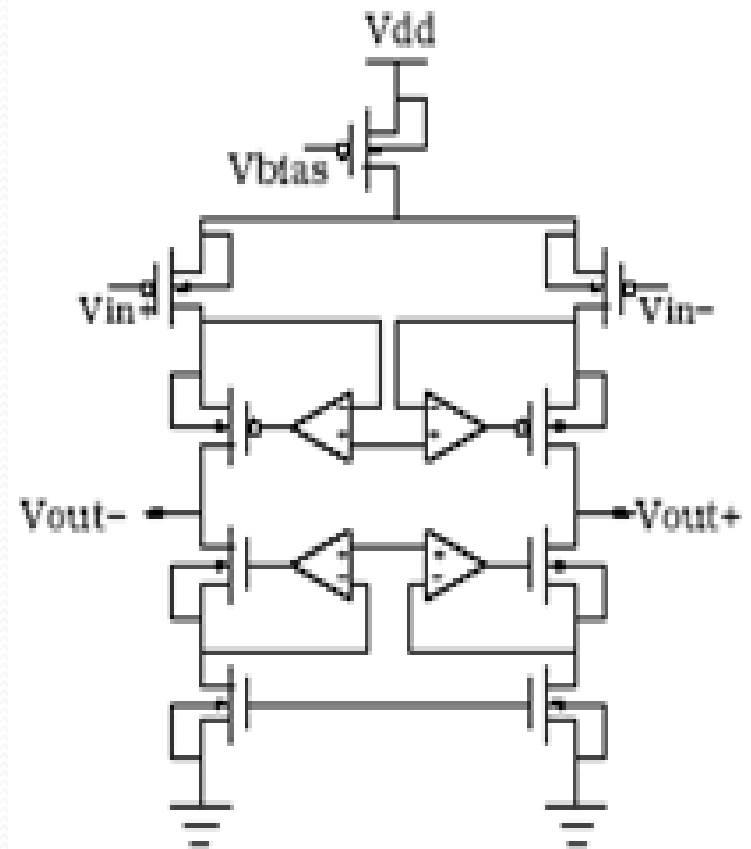
High output swing



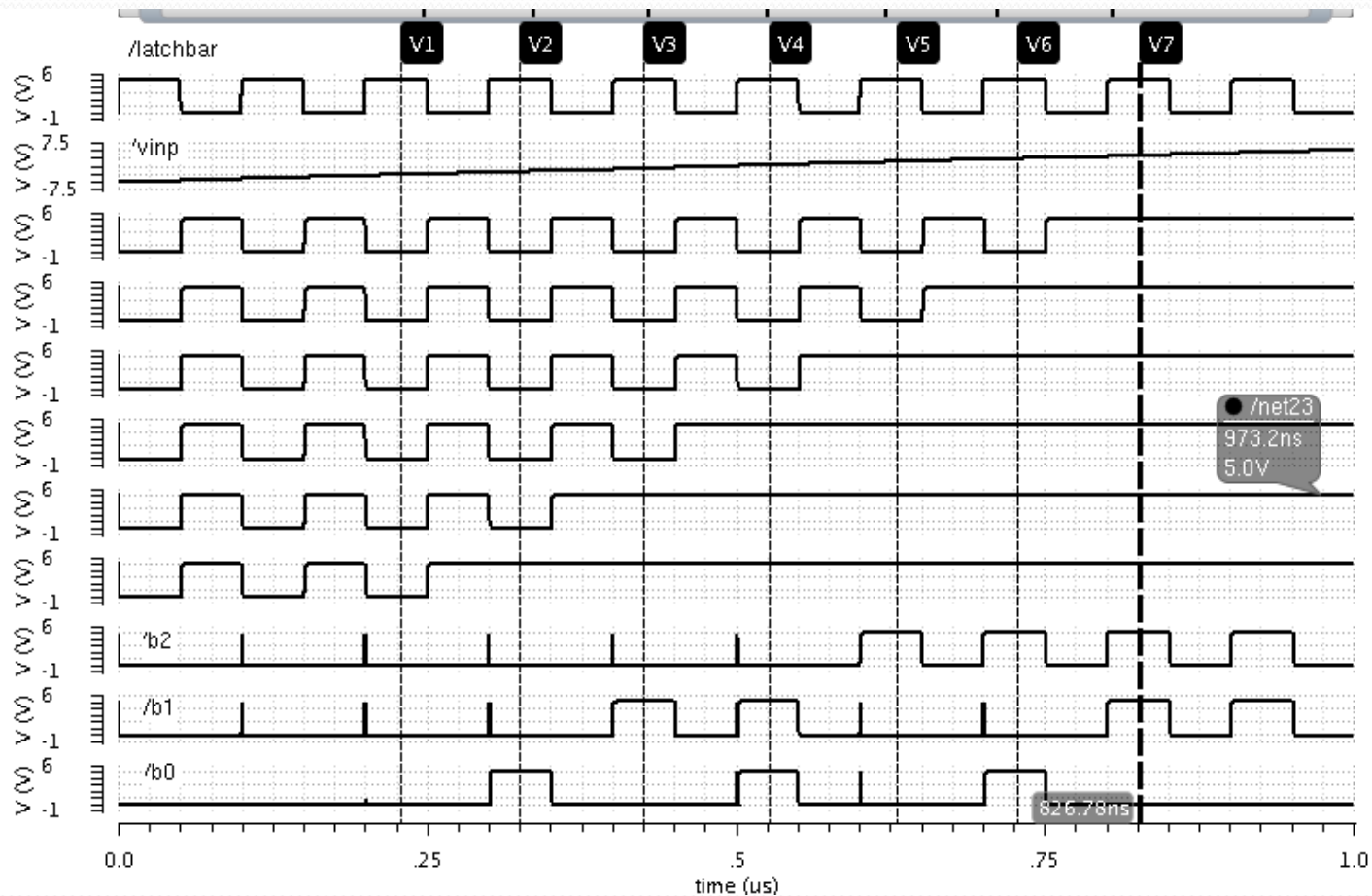
High gain and high output swing

# Gain Boosted Op-amp:

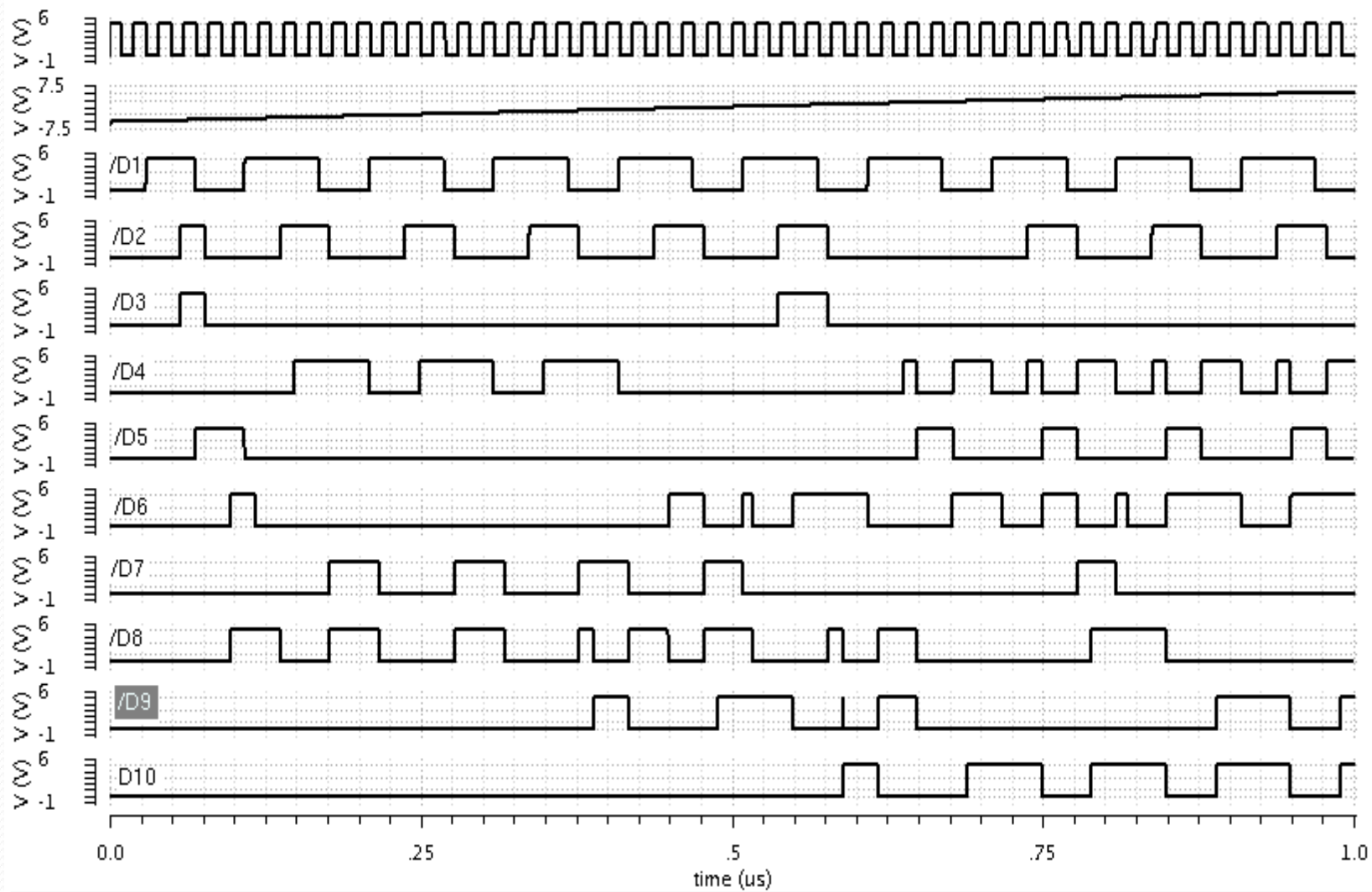
- The two folded cascode auxiliary amplifiers and the telescopic amplifier are integrated together to form the gain boosted OTA.
- The outputs of two folded cascode OTA are connected to the telescopic OTA to provide the bias and the required gain boosting.
- Higher speed operation.
- Higher power efficiency and lower noise factor.



# Simulation Results :



Response of sub-ADC to a ramp input



Digital output of 10-bit pipelined ADC for a ramp input



# Applications:

- The commonly used applications of Pipeline ADCs are high quality video systems, Radio base stations and high performance digital communication system etc.
- Applications of pipelined ADC based on its resolution are:

Resolution	Applications
8	<ul style="list-style-type: none"><li>➤ Lab instrumentation</li><li>➤ Medical Imaging</li><li>➤ Radar</li></ul>
10	<ul style="list-style-type: none"><li>➤ Flat Panel Displays</li><li>➤ CCD imaging</li></ul>
14	<ul style="list-style-type: none"><li>➤ Military</li><li>➤ Aerospace</li></ul>

# References:

1. Thomas Byunghak Cho, Student Member, IEEE, and Paul R. Gray, Fellow, IEEE, "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter", *IEEE J. Solid-State Circuits*, Vol.30, No.3, March 1995.
2. Mark Ferriss, Joshua Kang, "A 10-Bit 100-MHz Pipeline ADC", *University of Michigan*, 598 design project, 2004.
3. Stephen H. Lewis, H.Scott Fetterman, George F. Gross, R. Ramachandran and T. R. Viswanathan, "A 10-b 20-Msample/s Analog-to-Digital Converter", *IEEE J.*
4. Permatasari, Siti Intan, Mervin T. Hutabarat, Adiseno, "Design of 12-Bit, 40 MS/s Pipeline ADC for Application in WiMAX Transceiver," *2011 International Conference on Electrical Engineering and formatics* 17-19 July 2011, Bandung, Indonesia.
5. <http://www.maximintegrated.com/app-notes/index.mvp/id/1023>
6. [http://www.iadc.ca/Pipeline\\_ADC\\_tutorial.htm](http://www.iadc.ca/Pipeline_ADC_tutorial.htm)
7. Digital Gain error correction technique for 8-bit pipelined ADC by Khalid Javeed