

Equivalence Checking Using Cadence Conformal LEC

Formal Hardware Verification

(COEN 7501)

Summer 2010

The Golden and the Revised Designs

```
component EN
  port( A, B : in std_logic; Z : out std_logic);
end component;

signal n248, n249, n250, n251, n252 : std_logic;

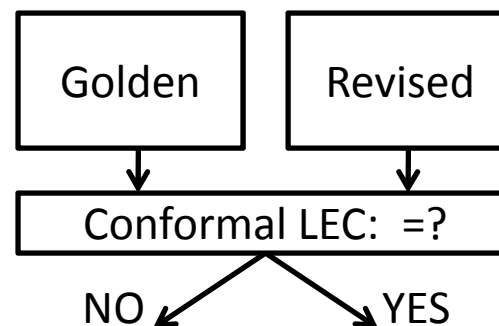
begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U62 : IV port map( A => a(3), Z => n250);
  -- U61 : ANDNA2 port map( A => n249, B => n250, Z => n251);
  -- U61 : NR2 port map( A => n249, B => n250, Z => n251);
  -- U61 : OR2 port map( A => n249, B => n250, Z => n251);
  U61 : E0 port map( A => n249, B => n250, Z => n251);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n249);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n249);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;
```

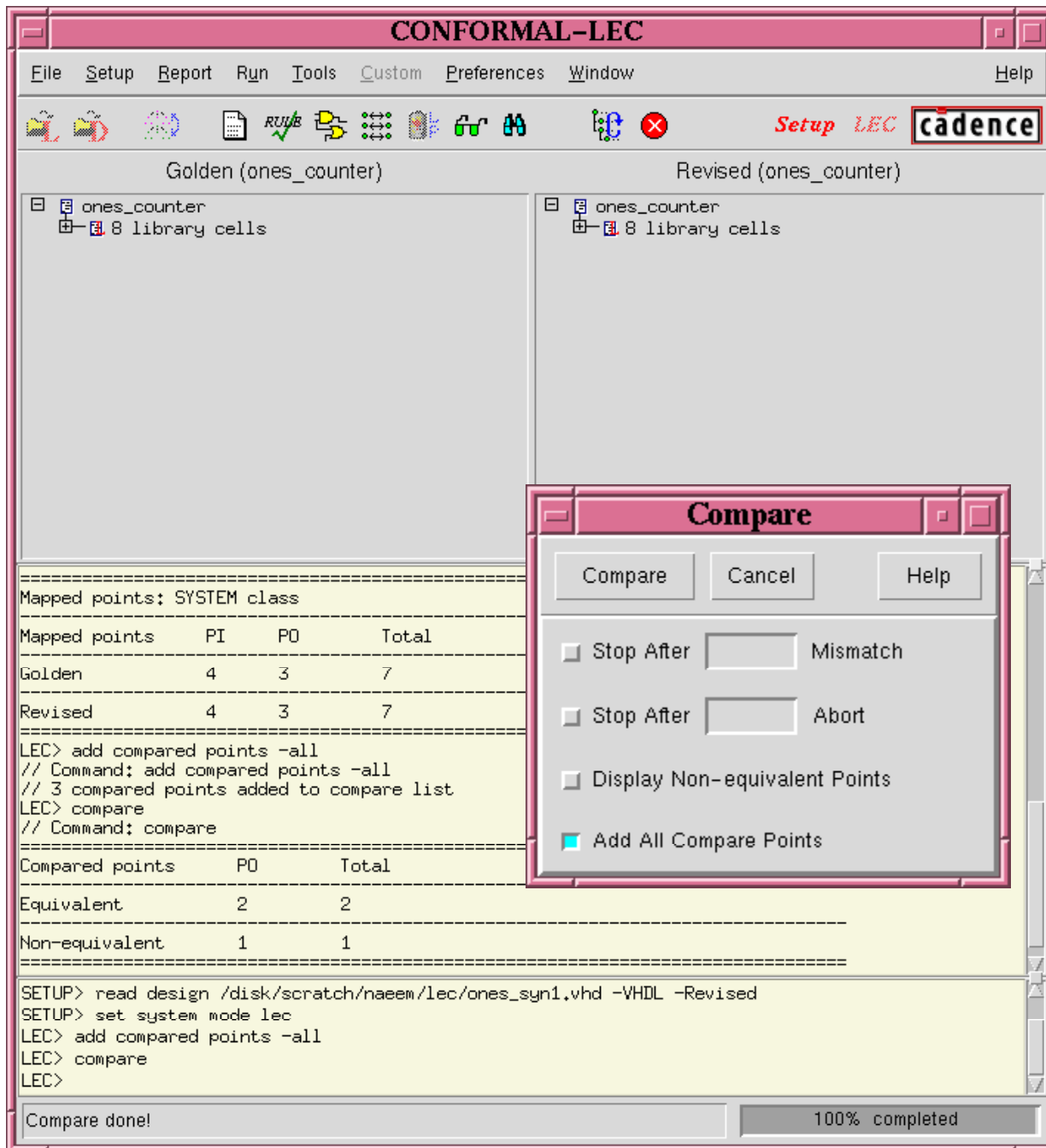
```
signal n248, n249, n250, n251, n252 : std_logic;

begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U61 : NR2 port map( A => n249, B => n250, Z => n251);
  U62 : IV port map( A => a(3), Z => n250);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n249);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n249);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;
```

Revised Design

Golden Design

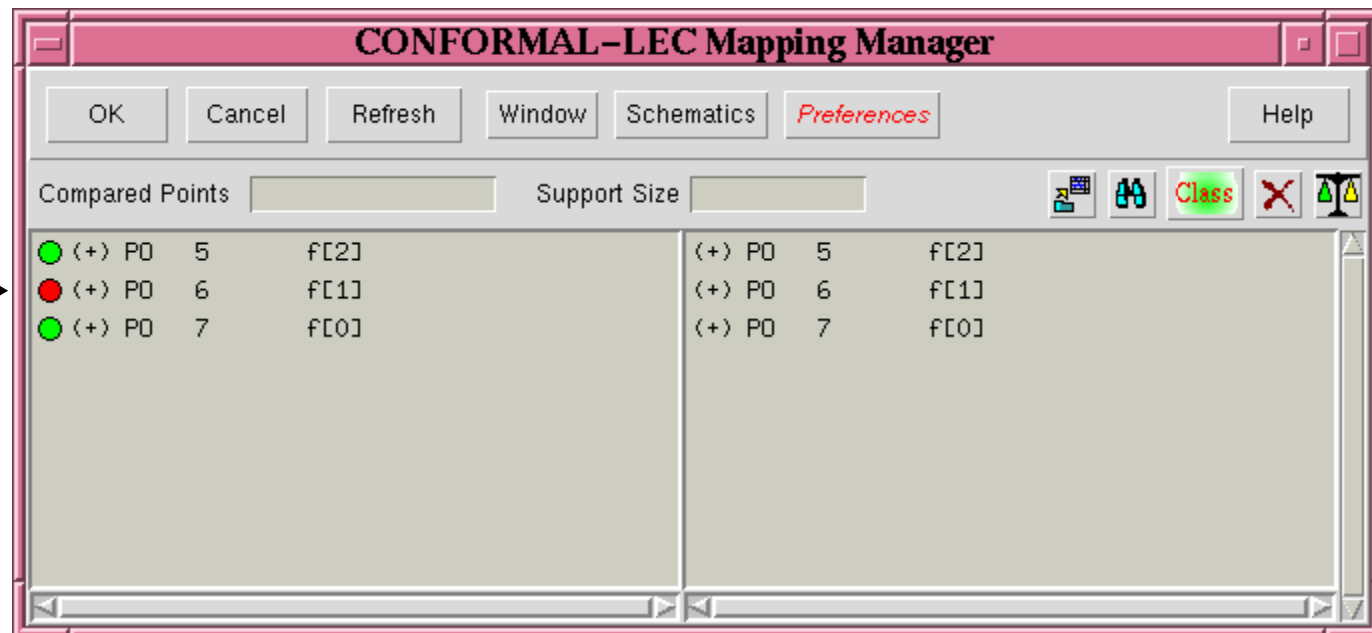




1. In the SETUP mode, Load the Golden and Revised Designs
2. Change System Mode to LEC
3. Add all ports as compare points
4. Compare


Report → Mapped Points

Diagnose →




CONFORMAL-LEC Diagnosis Manager


OK Cancel Refresh Window **Schematics** Preferences Help


Compared Point 

Golden PO 6 f[1] Revised PO 6 f[1]



Diagnosis Point (active) 


Golden (0) PO 6 f[1] Revised (1) PO 6 f[1]

Diagnosis Points (inputs) 


Corresponding Support 

(1)	PI	1	a[3]	(1)	PI	1	a[3]
(0)	PI	2	a[2]	(0)	PI	2	a[2]
(1)	PI	3	a[1]	(1)	PI	3	a[1]
(1)	PI	4	a[0]	(1)	PI	4	a[0]

Non-corresponding Support  

Error Pattern 

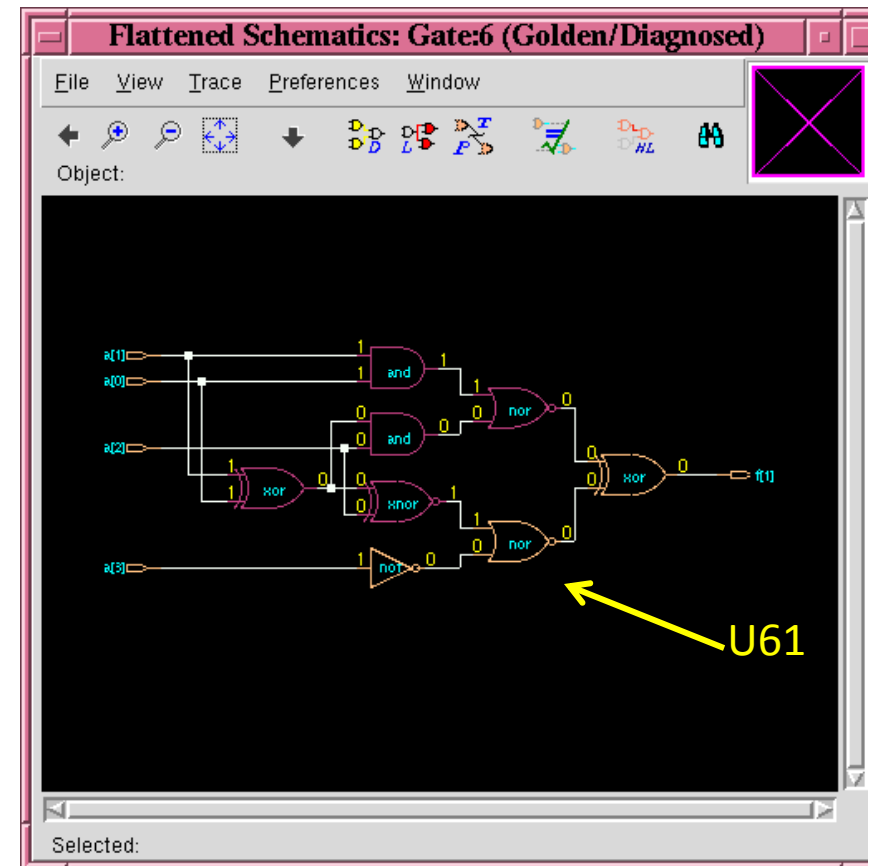
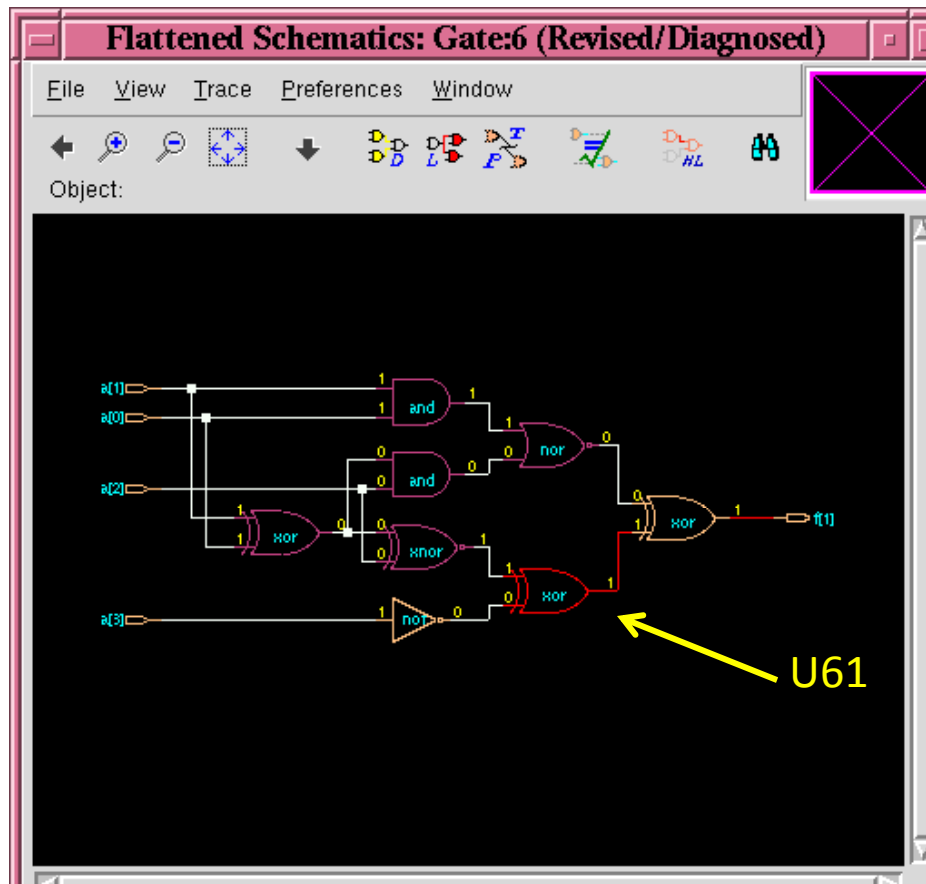
1:	1011
2:	0010
3:	1000
4:	1001
5:	1100
6:	0100
7:	1010
8:	1110
9:	1101
10:	1111
11:	0001

Error Candidate 

(1,00)	XOR	15	U61/U*1
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LEC Diagnosis Manager
Lists the failed compare point

Golden and Revised Schematics



```
48  component IV
49      port( A : in std_logic; Z : out std_logic);
50  end component;
51
52  component A02
53      port( A, B, C, D : in std_logic; Z : out std_logic);
54  end component;
55
56  component EN
57      port( A, B : in std_logic; Z : out std_logic);
58  end component;
59
60  signal n248, n249, n250, n251, n252 : std_logic;
61
62  begin
63
64      U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
65      U60 : EO port map( A => n248, B => n251, Z => f(1));
66      U62 : IV port map( A => a(3), Z => n250);
67  --    U61 : ANDN2 port map( A => n249, B => n250, Z => n251);
68  --    U61 : NR2 port map( A => n249, B => n250, Z => n251);
69  --    U61 : OR2 port map( A => n249, B => n250, Z => n251);
70  → U61 : EO port map( A => n249, B => n250, Z => n251);
71      U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n248);
72      U64 : EO1 port map( A => a(3), B => n249, C => a(3), D => n249, Z => f(0));
73      U65 : EN port map( A => n252, B => a(2), Z => n249);
74      U66 : EO port map( A => a(1), B => a(0), Z => n252);
75
76  end SYN_rtl;
```

Fix the Code and Rerun the Verification