Design Techniques for Ultra-Low-Voltage and Ultra-Low-Power Pipelined ADCs

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Submitted in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy
in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2010

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Abstract

Design Techniques for Ultra-Low-Voltage and Ultra-Low-Power Pipelined ADCs

Junhua Shen

This thesis addresses two important aspects of pipelined analog-to-digital converter (ADC) design. The first one is regarding a pipelined ADC with ultra-low supply voltage. As CMOS technology advances, lower supply voltages are expected in the near future. We explore its design feasibility and implications. The second aspect is related to minimizing the total power consumption of the pipelined ADC. In particular the power associated with the reference voltage buffer is addressed.

A 0.5V 8bit pipelined ADC operating at 10MS/s is proposed. The ADC uses true low-voltage design techniques that do not require any on-chip supply or clock voltage boosting. The switch OFF leakage in the sampling circuit is suppressed using a cascaded sampling technique. A front-end signal-path sample-and-hold amplifier (SHA) is avoided by using a coarse auxiliary sample and hold (S/H) for the sub-ADC and by synchronizing the sub-ADC and signal path sampling circuit. A 0.5V operational transconductance amplifier (OTA) is presented that provides interstage amplification with an 8bit performance for the pipelined ADC operating at 10MS/s. The prototype chip has eight identical stages and stage scaling was not used. It consumes 2.4mW for 10MS/s operation at 0.5V supply voltage.

Measured peak SNDR is 48.1dB and peak SFDR is 57.2dB for a full-scale sinusoidal input. Maximal integral nonlinearity (INL) and differential nonlinearity (DNL) are 1.12LSB/-1.19LSB and 0.55LSB/-0.48LSB, respectively. The prototype achieves a figure-of-merit (FOM) of 1.15pJ/Conv. Step. It was fabricated on a standard 90nm CMOS process and measures 1.2mm×1.2mm.

A low power stage architecture for a 1V 8bit 100MS/s pipelined ADC using current-charge-pump multiplying digital-to-analog conversion (MDAC) circuit is presented. By avoiding the use of OTAs for the interstage amplification and eliminating power hungry buffers for the reference voltages, the proposed current-charge-pump pipelined ADC consumes much less power and thus achieves very high operation efficiency. Two versions of inverter based comparators are employed in the signal and sub-ADC paths. The design involves minimum analog circuitry and is digital dominant. It consumes 1.39mW for 100MS/s operation at 1V supply voltage. Measured peak SNDR and SFDR are 37.1dB and 46.7dB respectively, with a -1dBFS sinusoidal input at Nyquist frequency. Maximum INL and DNL are 2LSB/-2.3LSB and 1LSB/-0.8LSB, respectively. This concept-proving prototype achieves an FOM of 237fJ/Conv. Step while largely alleviating the requirement of reference voltage buffers. The core circuit occupies 0.044mm^2. The design was fabricated on a standard 90nm CMOS process using regular V_T devices.

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Acknowledgments

Throughout my Ph.D. study here at Columbia Integrated Systems Lab, I received numerous help from many people. Without them, I wouldn't be able to finish the dissertation in a timely manner. I hope I could express my gratitude to all of them.

First of all, I am very grateful that I did my Ph.D. under Professor Peter Kinget's guidance. His deep knowledge and insights into circuit design is always a great source for me to learn from. His focus and dedication to the field of integrated circuit is an inspiration to all of his students. He also sets a high standard for us by being hard-working, energetic and highly efficient.

I am also very grateful to Professor Yannis Tsividis, Professor Charles Zukowski, Dr. Kumar Lakshmikumar and Dr. Vincent Leung for serving on my thesis defense committee. Thanks for taking their precious time reviewing my thesis and giving me insightful feedbacks.

I am very thankful to my colleagues at Columbia Integrated Systems Lab (CISL). They are always an essential part of my life here. In my early days and years of Ph.D. study, I got much help from Shouribrata Chatterjee, Frank Zhang, Anuranjan Jha and Babak Soltanian. Learning from the experiences and wisdom of senior students helped me move forward much smoother. For almost my entire stay in the lab, I am grateful that I have the companions of three other fellow Ph.D. students, Ajay Balankutty, Yiping Feng, and Shih-An Yu. I honestly learned as much from them as I did through my own research and study. Whenever

I needed some help or felt like to discuss something, they are always there, willing to share their time and knowledge. Most importantly, it's the time we spend together, inside the lab or outside, that makes my Ph.D. life more dynamic and memorable. My sincere thanks also go to many other colleagues at CISL. In no particular order, they are Kshitij Yadav, Karthik Jayaraman, Baradwaj Vigraham, Jayanth Kuppambatti, Colin Weltin-Wu, Nebojsa Stanic, Na Lei, Bob Schell, Maria Kurchuk, Ari Klein, Christos Vezyrtzis, Kagan Irez, Chen Li, Marco Crepaldi, Jorge Fernandes, Richard Hsieh, Navin Harwalkar, Jonathan Tompson, Robin Stevenson, Ryan Roberts, Mingdong Hu, Frank Fang, etc. I appreciate much all their friendship. I would also like to use this opportunity to thank Dr. Katsu Nakamura for the internship and later a full time position in his group at Analog Devices, and my M. Phil. advisor Dr. Kong-Pang Pun for his encouragement and belief in me. Special thanks to Ajay Balankutty and Colin Weltin-Wu for proofreading my thesis draft.

My Ph.D. study was sponsored by Realtek, Analog Devices, as well as Dept. of Electrical Engineering and Dept. of Physics for teaching and research assistantships. My sincere thanks for their generous financial support for the past four and a half years. Special thanks to Prof. Gustaaf Brooijmans and senior colleague Jaroslav Ban of Physics department. I would also like to thank United Microelectronics (UMC) for chip fabrications.

Lastly, I can't be more grateful to my family members, my sister Xiuhong Shen, my mom Wenjuan Chen and dad Zhiming Shen. Without their support and love, I wouldn't be here pursuing my Ph.D. My girlfriend Qinghui Yu deserves my very special thanks here. Thanks for her love and understanding.

Chapter 1

Introduction

1.1 Overview

Digital CMOS technology has already stepped into the nanometer era and digital signal processors are getting faster and more powerful. As a result, more traditional analog circuit functionalities are being pushed and implemented in the digital domain to take advantage of the process scaling. Nonetheless, the analog-to-digital converter (ADC) can never be replaced by digital circuitry, as it acts as the bridge between digital processing and the analog world [1]. Because of the importance of the ADC, much research has been done in this field in the last few decades and a few of the ADC architectures are widely used for various applications. Each type of ADC has its own pros and cons. They are very briefly reviewed here to provide the context for the pipelined ADC we are focusing on.

Flash ADC

Flash ADC is a fully parallel architecture, and is therefore the fastest ADC. An N-bit flash ADC needs $2^N - 1$ comparators and the same number of reference voltages. The digital outputs from the comparator array are thermometer codes and are further encoded to produce the binary weighted codes. For the flash ADC, the operating frequency is only limited by the speed of a comparator.

The two main drawbacks of the flash ADC are the large hardware requirement and sensitivity to the offset of the comparator. It is suitable for high speed, low resolution applications.

Two Step Flash ADC

Two step flash ADC consists of two stages of flash ADC, namely the first stage coarse ADC and the second stage fine ADC. The coarse ADC produces the most significant bits, and then the residue is applied to the fine ADC to get the least significant bits. This type of ADC takes two clock cycles to do one conversion and is thus considerably slower than the single stage flash ADC. But it substantially saves the hardware requirement.

Subranging ADC

The concept is similar to the two step flash ADC. Subranging ADC breaks the conversion process into multiple steps, thus saves more hardware, but at the cost of longer conversion

time. Each step is responsible for several bits of digital output and sends the residue to the next stage.

Successive Approximation ADC

This kind of ADC is a special type of subranging ADC. It uses a DAC to produce an analog signal to approximate the input signal. By adjusting the DAC until the DAC output matches the input sample, digital code representing the analog input is generated. The successive approximation ADC only consists of one stage and a digital logic circuit that controls the DAC. The accuracy of this ADC can be very high at the cost of long conversion time. In addition, this architecture is also very hardware-efficient.

Dual Slope ADC

A standard dual slope ADC has two parts: an integrator followed by a comparator that produces a pulse with its width proportional to the input signal; a counter that translates the pulse width into digital codes. It is also called an integrating ADC. This type of ADC can achieve very high resolution but is very slow. In the modern days, sigma delta ADCs have virtually replaced integrating ADCs.

Oversampled ADC

Oversampled ADCs started to gain attention a couple of decades ago and have been applied to many fields like audio, digital telephony, etc. The basic concept underlying the oversampled ADC is the use of feedback to track the input signal. Due to the high low-frequency gain from the internal loop filter, the low frequency part of the digital output spectrum virtually replicates that of the input signal, while the quantization noise sees a high pass and is shaped by the noise transfer function. Sigma delta ADC is the main category of oversampled ADCs. They are suitable for very high resolution but relatively low operating speed.

Pipelined ADC

Pipelined ADC has its origin in the subranging ADC, which was first patented in 1959 [2]. It also divides the conversion task into several stages to dramatically save the hardware requirement compared with the flash ADC. But unlike conventional subranging ADC, which takes multiple clock cycles to do one conversion, pipelined ADC has a sample and hold circuit for each stage. The stage track and hold circuit serves as an analog memory cell so that the previous stage can be released to process the next input. In this way, the pipelined ADC works like a shift register and achieves very high throughput rate. The throughput is independent of the number of stages. An interstage amplifier is added to restore the residue from the previous stage back to full scale, thus it alleviates the accuracy requirement of the

succeeding stages. The drawback of the pipelined ADC is its inherent latency, which might cause stability problem in a feedback control system. But for many applications, it is the best choice due to the superior combination of high speed, medium to high resolution and relatively low power consumption. Fig. 1.1 shows the simplified block diagram of the first two stages of the pipelined ADC.

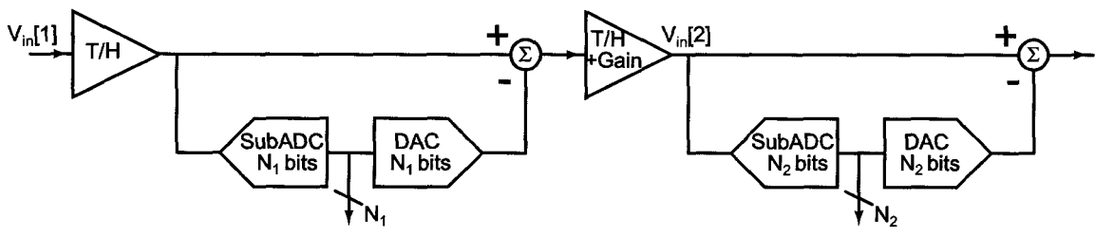
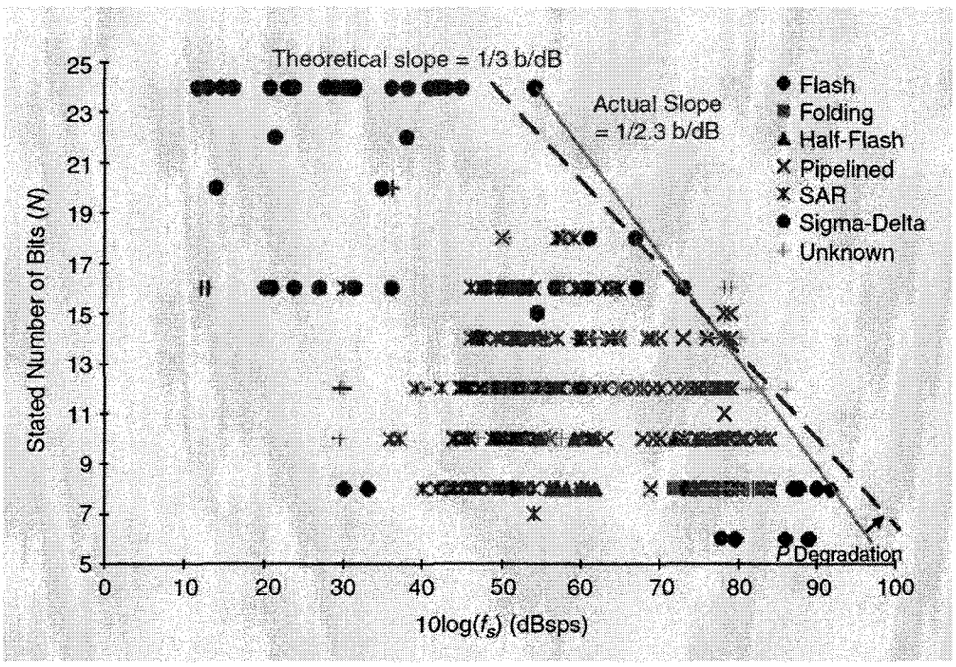


Figure 1.1: Block diagram of the first two stages of a pipelined ADC.

To understand the performance tradeoffs of different types of ADCs, extensive studies on commercially available ADCs have been done and the results are shown in Fig. 1.2 [3]. As we can see, the performance of pipelined ADCs is a compromise between low resolution high speed flash ADCs and high resolution low speed sigma delta or SAR ADCs.

Fig. 1.3 shows the complete diagram of a standard pipelined ADC. There are three inputs to the ADC, namely the analog input signal V_{in}, the reference voltage V_{ref} and the clock CLK_{in}. Any nonideality associated with those inputs will affect the converter's accuracy. The "pipeline" is enabled by the internal sample and hold circuit for each stage. Notice that the clock phases are alternated from stage to stage, therefore each one introduces half a clock cycle latency. The number of bits for each stage is mainly determined by the operating speed and power [4, 5]. Besides a number of pipelined stages, the converter



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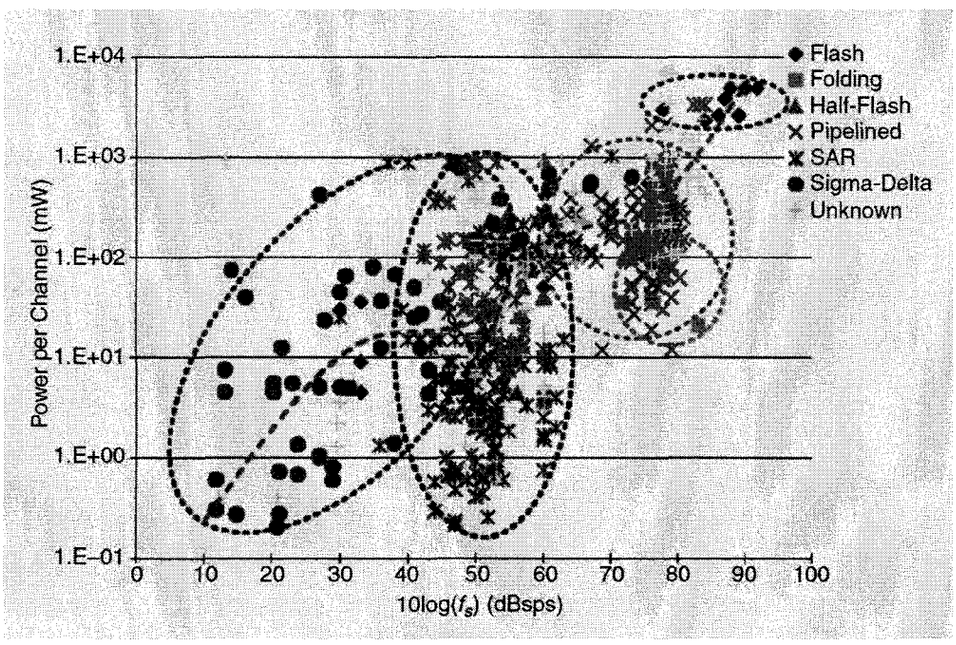


(b)

Figure 1.2: (a) Number of bits versus sampling frequency for different types of ADCs [3]; (b) Power consumption versus sampling frequency for different types of ADCs [3].

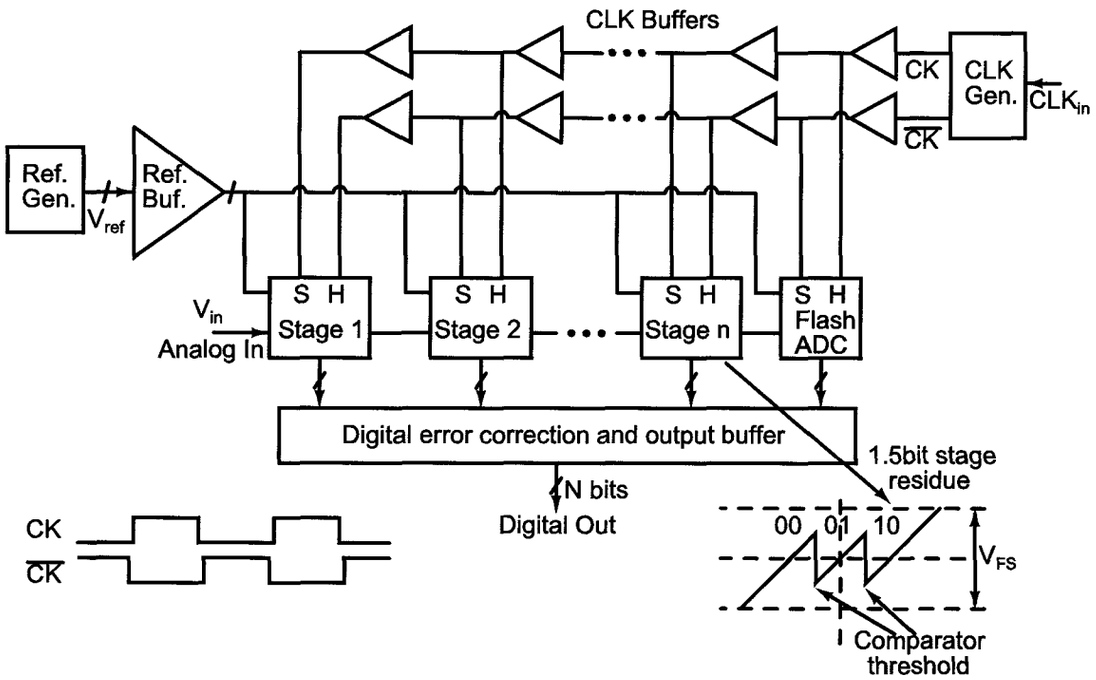


Figure 1.3: Complete diagram of a pipelined ADC.

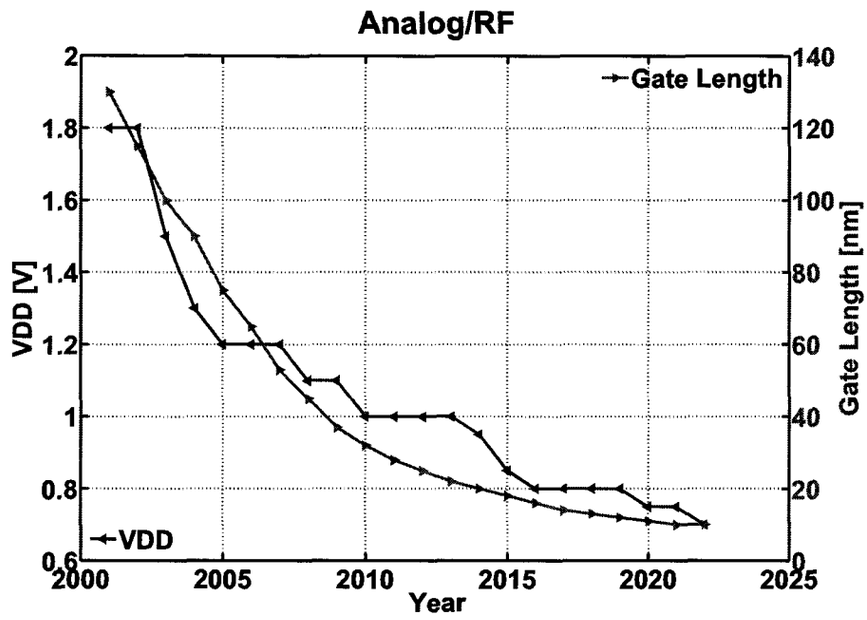
also includes, among others, a non-overlapping clock generator, reference voltage buffer, and sometimes a dedicated front-end track and hold stage (not shown in Fig. 1.3) [6, 7]. A flash type ADC is usually employed for the last pipelined stage, where no residue needs to be generated. The accuracy requirements for the later stages are largely alleviated due to the aggregated gain from the earlier stages. In a typical design, a redundant bit is usually added to each stage to tolerate the threshold offset in the sub-ADC [8]. Accordingly, digital correction logic needs to reconfigure the stages' output bits to the final digital output.

The pipelined ADC architecture is a leading choice where sampling rates from a few MHz to a few hundred MHz are required. Its main applications include communication, video, CCD-based image processing, and data acquisition.

Ultra-low-voltage pipelined ADCs

As CMOS technology advances, which is mainly driven by digital circuits, the supply voltage for digital and analog circuits keeps scaling down. The International Technology Roadmap for Semiconductors (ITRS) reported the trend of supply voltage and technology node in the near future [9], which is shown in Fig. 1.4, 1.5. As projected, the supply voltage for analog and RF transistors is going down to sub-1V in a few years; the supply voltage for digital low power circuit will be down to 0.5V in about 7 years. Serving as an important interfacing circuit between the analog and digital domain, the pipelined ADC needs to keep up with the supply voltage scaling and consistently deliver high performance to meet its applications' requirements.

In the past few years before we published our work [10, 11], a couple of sub-1V pipelined ADC were reported in literature [12,13], both of them operate from a 0.9V supply voltage. While the supply of 0.9V had already started to show the performance implications of the pipelined ADC such as finite OTA gain and sampling switch linearity, more significant supply voltage reduction was desired to further explore the feasibility of high performance ultra-low-voltage pipelined ADCs. On the other hand, the nanometer CMOS technology that demands low supply voltage has its own unique features. We need to take advantage of some new characteristics like reverse short channel effect, and address the issue that comes with it, for instance, high transistor leakage when it is in off-state.



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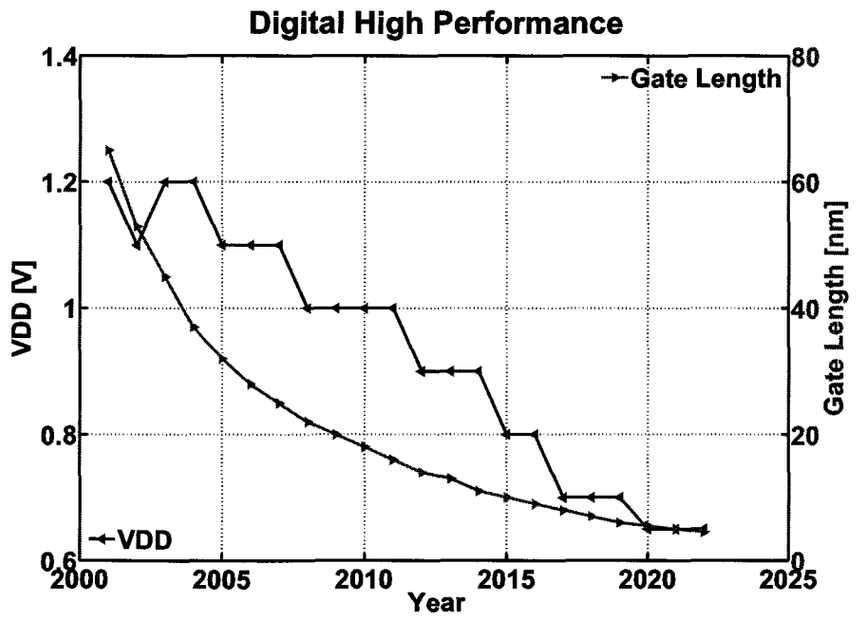
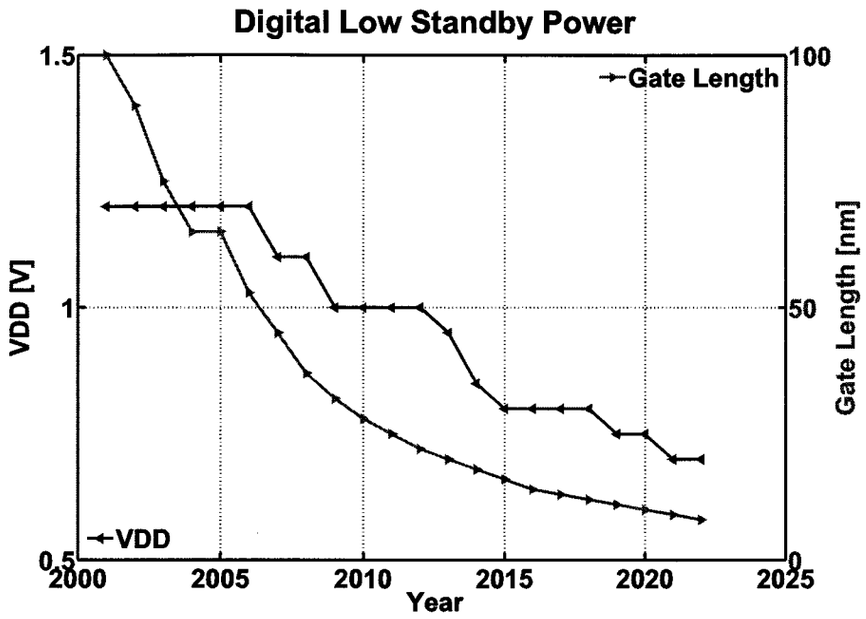


(b)

Figure 1.4: Trend of supply VDD and technology node versus year. (a) Analog and RF; (b) digital high performance.



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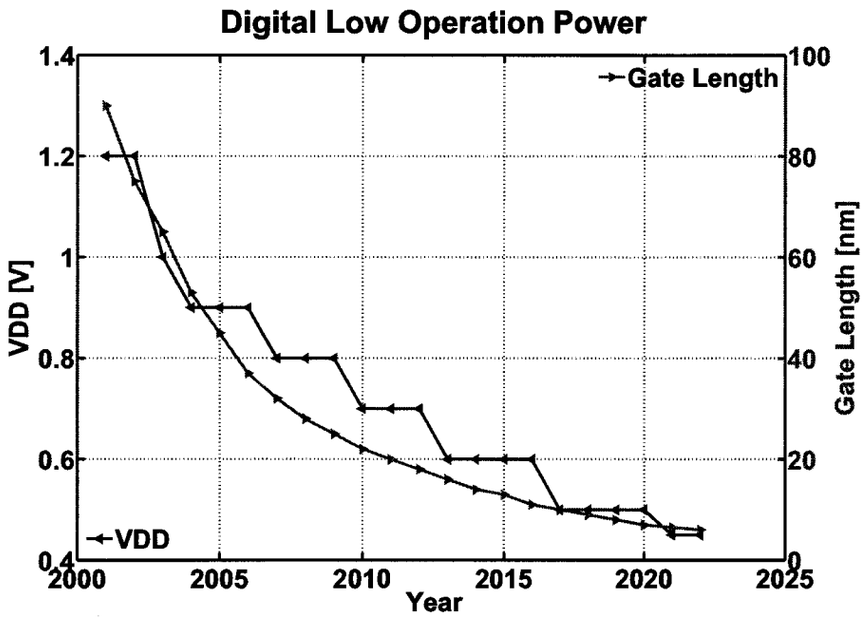


(b)

Figure 1.5: Trend of supply VDD and technology node versus year. (a) digital low standby power; (b) digital low operation power.

Ultra-low-power pipelined ADCs

While ultra-low-voltage pipelined ADCs is a research topic to prepare for the near future, ultra-low-power pipelined ADCs are always of great research interest, especially for battery powered devices. Unlike digital circuits, where power consumption reduces as supply voltage goes down:

$$P_{digital} \propto f_{clk} \times C \times VDD^2 \tag{1.1}$$

Analog circuits' power consumption, taking ADC as an example, goes up as VDD scales down [14]:

$$P_{analog} \propto f_{clk} \times 2^{2B}/VDD \tag{1.2}$$

where B is the resolution of an ADC. To separate the design issues involved with low supply and low power consumption, a regular supply voltage can be used to better focus on the power aspect of the pipelined ADC.

From a general point of view, there are three ways to reduce the power consumption of a pipelined ADC, one is to optimize the design in the circuit level, especially for the main building blocks like OTAs [15–17]; the second way is to innovate in the architectural level, which could potentially increase operating efficiency substantially [18–22]; finally, employing digital calibration to reduce the power. By moving the analog design complex-

ity into the digital domain and taking advantage of the low power consumption of digital circuits in advanced CMOS technology, the total power consumption can be brought down significantly [23–28]. Sometimes, the latter two approaches can be combined to reach a better solution [29–31]. In this thesis, the work on low power pipelined ADC mainly focuses on the architectural innovation, as well as taking advantage of the standard digital calibration.

Implications on pipelined ADC power consumption with lowering supply voltage

Low voltage does not necessarily mean low power. In the case of the pipelined ADC, we have two scenarios when the supply voltage is scaled down. One is that the ADC is noise limited, the other is that the ADC is mismatch limited. The following simplified analyses look at the power change with half the VDD, given the same signal-to-noise (SNR) and sampling frequency f_s.

Noise limited pipelined ADC

In the noise limited scenario which mainly applies to high resolution pipelined ADCs, we can further divide it into the following two cases:

VDD scaling without technology scaling In this case the same CMOS technology is used when VDD is scaled by half, thus the transistor biasing point or g_m/I is kept constant

to maintain the maximum operating speed. Assuming signal swing is proportional to VDD, the sampling capacitor in the pipelined ADC has to be four times larger to achieve the same SNR. This results in four times the biasing current to keep the same GBW and sampling frequency f_s. In conclusion, the power consumption doubles when VDD is half.

VDD scaling with technology scaling As CMOS technology advances, the transistor's peak f_T roughly doubles as channel length goes down by half [32]. This means that we can increase g_m/I by one time (assuming it hasn't reached the maximum yet) while keeping f_T the same as that in the old technology. In this case, the current I only needs to be double to have four times the g_m, thus power consumption will remain the same as VDD scales by half.

Mismatch limited pipelined ADC

The performance of lower resolution pipelined ADCs tends to be mismatch limited. The transistor mismatches in an OTA are not critical because they only cause input referred offset, which can be tolerated in a pipelined ADC. The capacitor matching is critical since it defines the ADC's interstage gain. Here we also divide this category into the following two cases:

VDD scaling without technology scaling If we assume no technology scaling, then the sampling capacitor has to be four times larger to maintain the same signal-to-mismatch

accuracy. This will lead us to four times g_m and I, thus the power consumption is twice as large.

VDD scaling with technology scaling According to the prediction of the ITRS report [32], the matching error of MOM capacitors will go from 0.15% to 0.1% over the following 3-5 years, for a 1pF capacitor. For MIM caps, the matching improves about 40% in the following 5 years. Considering the corresponding VDD for newer technology also scales down modestly, Matching accuracy $A_{cc} = V_{rms}/(3\sigma(V_{os}))$ will roughly stay the same for the same capacitor size, so power consumption will scale proportionally with VDD in this case.

In summary, the FOM versus technology node (thus VDD) roughly stays the same if the pipelined ADC is noise limited and improves if it's mismatch limited. In the case of VDD scaling in the same technology, power always doubles as signal swing is half. Furthermore, unlike the random noise in noise limited pipelined ADC, the error caused by capacitor mismatch only results in fixed interstage gain error and can be compensated using capacitor error-averaging technique [33], digital calibration [23] or trimming.

The power consumption analyses above regarding VDD scaling is highly simplified. In practice there are many other factors that affect the power and technology/VDD relationship. For instance, the digital part in the pipelined ADC can always benefit from VDD scaling; the leakage issue in advanced technology need more power to combat; the ex-

tra power is consumed by biasing circuit; and the available signal range scales faster than VDD.

1.2 Motivations

Ultra-low-voltage pipelined ADC

Digital circuit designers are pushing for lower and lower supply voltages to reduce power consumption. The dynamic digital power consumption is proportional to VDD^2, and the static power consumption due to various leakage mechanisms is often exponentially dependent on VDD. ADCs typically coexist on the digital die, especially in the context of system on a chip (SOC) devices. Sharing the same power supply voltage reduces the power domain complexity.

In some energy scavenging applications like wireless sensor networks, a single solar cell can be used as the power supply when due to space constraints. The supply voltage of a solar cell is around 0.5V.

We also want to explore and push the lower boundary of supply voltage for analog design, to see if it could be fully compatible with the low supply voltage associated with future thin-oxide nano-scale devices and to understand what the performance implications are.

Ultra-low-power pipelined ADC

Power consumption in general has always been an active topic for integrated circuit design. There are two broad aspects to it, one is that high power consumption means less battery life for mobile devices, and the other is that it potentially involves heat dissipation issue.

As the information technology develops, mobile devices like cell phones, and consumer electronics like digital cameras, are reaching more and more people and they are being used much more frequently. Pipelined ADCs are widely used in these devices. By reducing its power consumption, together with other parts of the system, the devices' operating time can be dramatically increased.

The CMOS technology has well entered the nanometer era. While it enables higher integration, more functionalities and cheaper products, it also dramatically increases the power density and thus makes the heat dissipation issue much worse. In applications where numerous channels of pipelined ADCs are used, for example, in a multi-channel readout or detection circuits, the heat dissipation could become a big concern.

1.3 Contributions

Two pipelined ADC chips were designed, fabricated and measured. The first one focuses on ultra-low-voltage power supply for the pipelined ADC, the main contributions are listed below:

- The design feasibility of a 0.5V 8bit 10MS/s pipelined ADC on a 90nm CMOS process is demonstrated, without internal voltage boosting or using special devices.
- A cascaded sampling technique is used to combat switch OFF leakage.
- An auxiliary S/H in the sub-ADC path is introduced to eliminate the front-end S/H.
- A two-stage 0.5V OTA with 50dB DC gain and 32MHz GBW is presented.

The second chip aims at an ultra-low-power pipelined ADC, the main contributions are as follows:

- A 1V 8bit 100MS/s current-charge-pump pipelined ADC in 90nm CMOS process is demonstrated, the FOM of 237fJ/Conv. Step is achieved.
- Current-charge-pump MDAC is introduced, power hungry reference buffers for the ADC are largely eliminated for the proposed stage architecture.
- Two inverter-based comparators are designed for the current-charge-pump pipelined ADC.

1.4 Thesis Organization

The thesis is organized into four chapters. This first chapter provides a brief overview of various types of analog-to-digital converters, which leads to our focus on pipelined ADC

and the background information for the work being presented. It also states the challenges and motivations for our research.

Chapter 2 presents an ultra-low-voltage pipelined ADC in advanced digital CMOS technology. Introduction and brief background of low voltage operation are given at the beginning of the chapter, followed by system level and block level designs of this work, including various proposed design techniques. Theoretical analyses are also given where appropriate. After presenting the measurement results for the prototype, the idea of an improved version of the gate bootstrapped switch for low supply voltage circuit is described.

Chapter 3 addresses the power consumption issue. A current-charge-pump pipelined ADC without a big reference buffer is presented. Similar to chapter 2, introduction and review of other ultra-low-power pipelined ADCs are given before the descriptions of prototype design at system and block levels. After the measurement results, we present several ideas for future improvement, including the schematic of a fully differential version of the proposed circuit and alternatives to a standard MDAC for the pipelined ADC stage to avoid the use of big reference buffers.

Chapter 4 summarizes the results of the two pieces of work and concludes the thesis. Future directions are then discussed for further investigations.

Appendix A presents and analyzes the OTA settling behavior at ultra-low-voltage supply.

Chapter 2

Ultra-Low-Voltage Pipelined ADC

2.1 Introduction

2.1.1 Challenges

The research goal of exploring ultra-low-voltage analog circuit design is motivated by several trends in integrated circuit design and semiconductor technologies, and the applications they enable. System on a chip (SOC) designs have made possible substantial cost and form factor reductions, in part, since they integrate crucial analog interface circuits, such as analog-to-digital converters (ADCs), with digital computing and signal processing circuits on the same die. The interfaces only occupy a small fraction of the chip die and for SOC designs the technology selection and system design choices are mainly driven by digital circuit requirements. In the past decades, design techniques for analog inter-

face circuits, that are fully compatible with scaled standard digital CMOS technologies and do not require special technology options, have been important enablers to continue ever more complex SOC designs (see e.g., [34]). As the feature sizes in modern nanoscale CMOS technologies reduce, the maximum supply voltage also has to be reduced to maintain reliable device operation. The International Technology Roadmap for Semiconductors (ITRS) foresees that the supply voltage for low power digital circuits will scale below 1V for high performance applications and down to 0.5V for low power applications within the next decade or so [35]. Additionally, the most energy efficient operation of digital systems occurs for supply voltages between 0.3 and 0.5V in deeply scaled technologies.

Scavenging energy to operate circuits from the environment is desirable for applications such as wireless sensor nodes or ambient intelligence. For example, if only one solar cell is available due to space constraints, the operational supply voltage is about 0.5V [36, 37].

Pipelined ADCs are a popular choice for analog-to-digital conversion for their attractive features of high operation speed, good resolution, and low power consumption. In this work, an 8bit 10MS/s pipelined ADC is targeted with an aggressive low supply voltage of 0.5V. In prior work, several techniques have been developed to accommodate low voltage analog circuit design such as the use of special low V_T devices [38, 39], on-chip clock and gate voltage boosting [40–43], body driven circuits [44, 45], or switched-opamp [46–48] techniques. Low V_T devices require extra masks during fabrication and thus result in higher cost. On-chip voltage boosting can lead to long-term reliability concerns, especially for nano-scale CMOS devices. Using the body terminal of a MOSFET offers the circuit de-

signer a number of interesting circuit design opportunities, but the body transconductance, g_{mb}, is significantly smaller than the gate transconductance, g_m, which can limit the attainable speed or noise performance. Switched-opamp techniques have been successfully used for very low voltage designs but typically operate at a reduced operation frequency due to the amplifier turn-ON times.

2.1.2 Solutions

The work presented here is using true low voltage design techniques to take full advantage of advanced CMOS technologies without resorting to special devices or on-chip voltage boosting [10]. The switch OFF leakage in the sampling circuit is suppressed using a cascaded sampling technique. A front-end signal-path sample-and-hold amplifier (SHA) is avoided by using a coarse auxiliary S/H for the sub-ADC, and by synchronizing the sub-ADC and pipeline-stage sampling circuit. A 0.5V operational transconductance amplifier is presented that provides interstage amplification with an 8bit performance for the pipelined ADC operating at 10MS/s. The chip was fabricated on a standard 90nm CMOS process and measures 1.2mm$\times$1.2mm. The prototype chip has 8 identical stages and stage scaling was not used. It consumes 2.4mW for 10MS/s operation. Measured peak SNDR is 48.1dB and peak SFDR is 57.2dB for a full-scale sinusoidal input. Maximal INL and DNL are 1.19 and 0.55 LSB respectively.

2.1.3 Chapter Organization

In Section 2.2, the top level design of the pipelined ADC is presented, where system, stage and MDAC design considerations are covered, as well as the introduction of an auxiliary sample and hold for the sub-ADC. Reverse short channel effect (RSCE) can favorably affect the design of the pipelined ADC and is also briefly discussed in this section. Section 2.3 details the block level designs, emphasis are given on the cascaded sampling technique as a solution to address switch-OFF-state leakage and the 0.5V OTA design for the pipelined ADC. Experimental results are presented in Section 2.4. Following that, the design issue regarding the sampling switch at ultra-low supply voltage is investigated in Section 2.5. Finally, the summary of this chapter is given in Section 2.6.

2.2 Ultra-Low-Voltage Pipelined ADC System Design

2.2.1 Top-Level and Stage Design Considerations

In ultra-low-voltage analog design, one intrinsic challenge is the reduced available signal swing. It makes multi-bit stages not desirable due to comparator offset and hysteresis concerns. Multi-bit stages further require a higher open-loop gain-bandwidth (GBW) for the residue amplifiers due to the small feedback factors in the stage. In this design, we use a 1.5bit/stage architecture, which tends to consume less power and retains high throughput. Using digital offset correction, the 1.5bit pipeline stage can tolerate a comparator offset

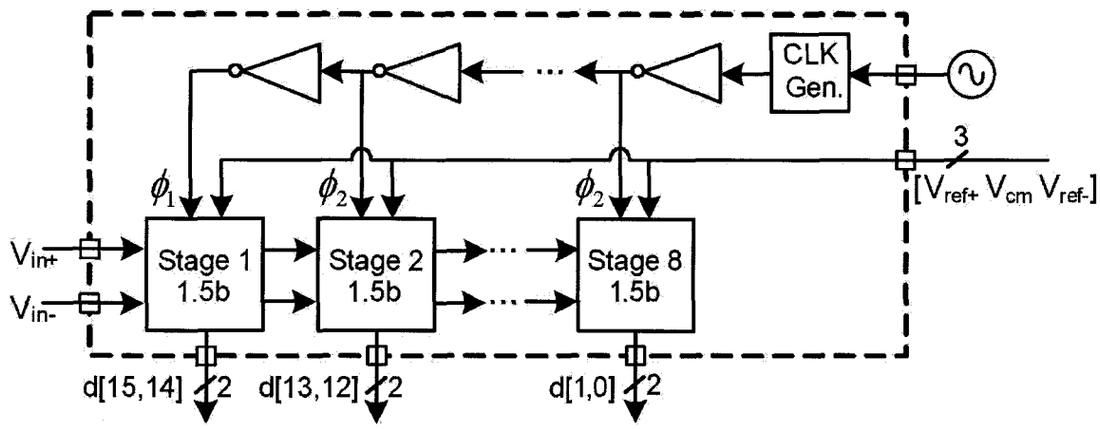


Figure 2.1: Block diagram of the pipeline ADC prototype chip.

magnitude of up to $\frac{1}{2}$LSB of the sub-ADC. Fig. 2.1 shows the block diagram of the converter prototype. To simplify the prototype design, the second through the eighth stage were kept identical to the first stage, which has the most stringent requirements. The performance could be further optimized by applying progressive size and power consumption scaling to the later stages. A front-end SHA of the pipelined ADC is not implemented to save power and reduce noise. This is made possible by the introduction of an auxiliary S/H for the sub-ADC, which will be presented later in this section.

A single-ended diagram of a stage of the pipelined ADC is shown in Fig. 2.2(a) for clarity, but the actual chip implementation is fully differential. It consists of 2 comparators as sub-ADC and an MDAC that performs signal sampling, subtraction and residue amplification. A 400mV peak-to-peak differential full-scale input swing is targeted, taking into account the typical available output swing of a 0.5V OTA. The signal common-mode voltage is set to 250mV and the reference voltages are 250mV$\pm$100mV. For an 8bit accuracy

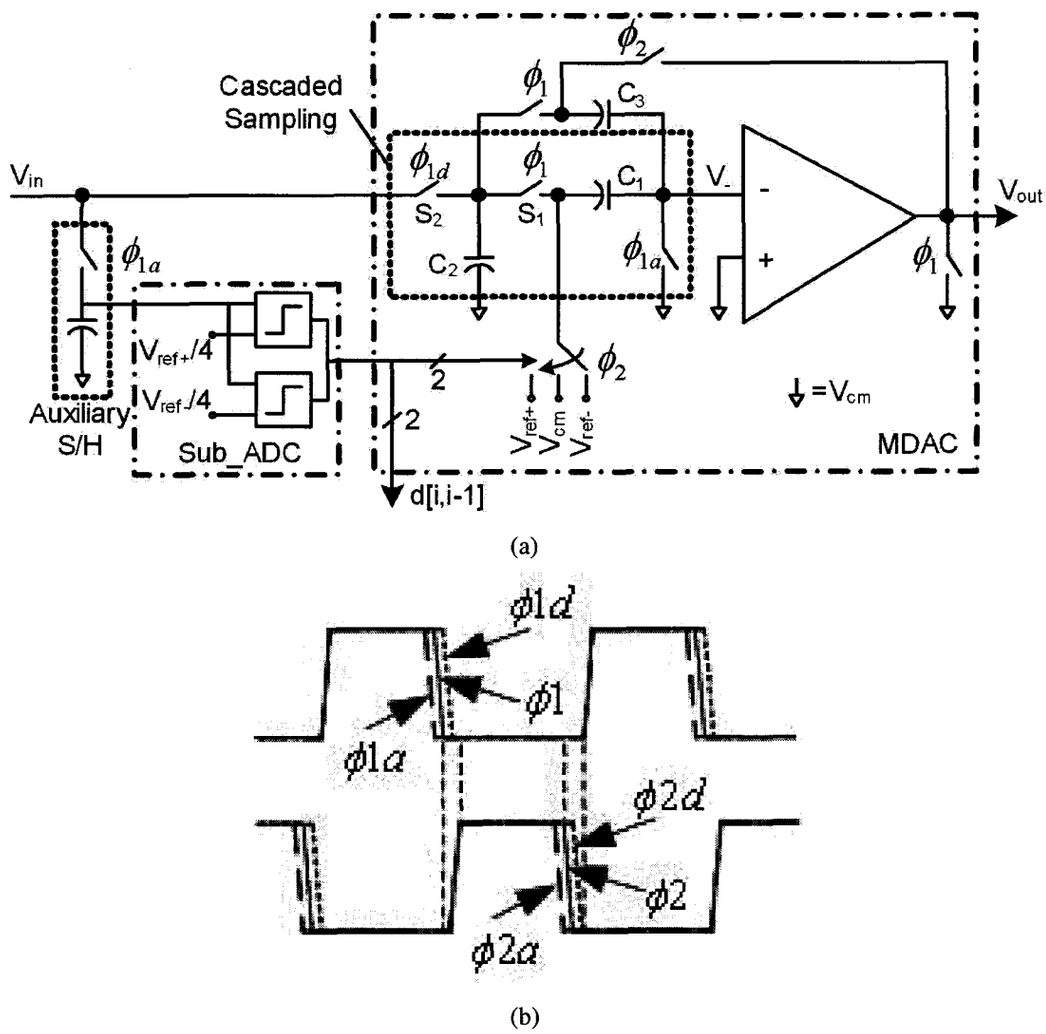


Figure 2.2: (a) Single-ended version of one pipeline stage; (b) non-overlapping clock signals (ϕ_1, ϕ_2) and their advanced (ϕ_{1a}, ϕ_{2a}) and delayed (ϕ_{1d}, ϕ_{2d}) versions used to minimize charge injection, clock feedthrough and to ensure accurate sampling.

level, the LSB of the ADC is still as large as 1.6mV. The choice of the size of the sampling capacitor is driven by the concern of keeping parasitic capacitors sufficiently small. To avoid an extra mask to realize a MIM capacitor, an interdigitated metal-metal capacitor with a unit size of 250fF was custom designed and verified using an electromagnetic simulation. The unit capacitor uses a stack of interdigitated metal combs on Metal1 through Metal6 and occupies $130\mu m^2$. In this design, four unit capacitors in a common-centroid layout for improved matching are used to realize the sampling capacitors C_1 and C_3 (see Fig. 2.2(a)). The RMS value of the thermal noise, $\overline{v^2_{n,RMS}} = kT/C$, for a 1pF sampling capacitor is $64\mu V_{RMS}$ and sufficiently small compared to the LSB value.

The on-chip clock generator generates two non-overlapping clock signals ϕ_1 and ϕ_2 from an external reference. Each clock signal further has an advanced, ϕ_{1a}, and delayed version, ϕ_{1d}, which are used to minimize charge injection, clock feedthrough and ensure accurate sampling as shown in Fig. 2.2(b). At the top level, clock signals are delivered to each stage through a chain of buffers, which are put close to corresponding stages in the layout to sharpen the clock edges. As shown in Fig. 2.1, the stages receive clock signals in reverse order, so that the clock signal edges advance slightly along the pipeline stages. This ensures that a succeeding stage always samples the correct residue signal from preceding stage.

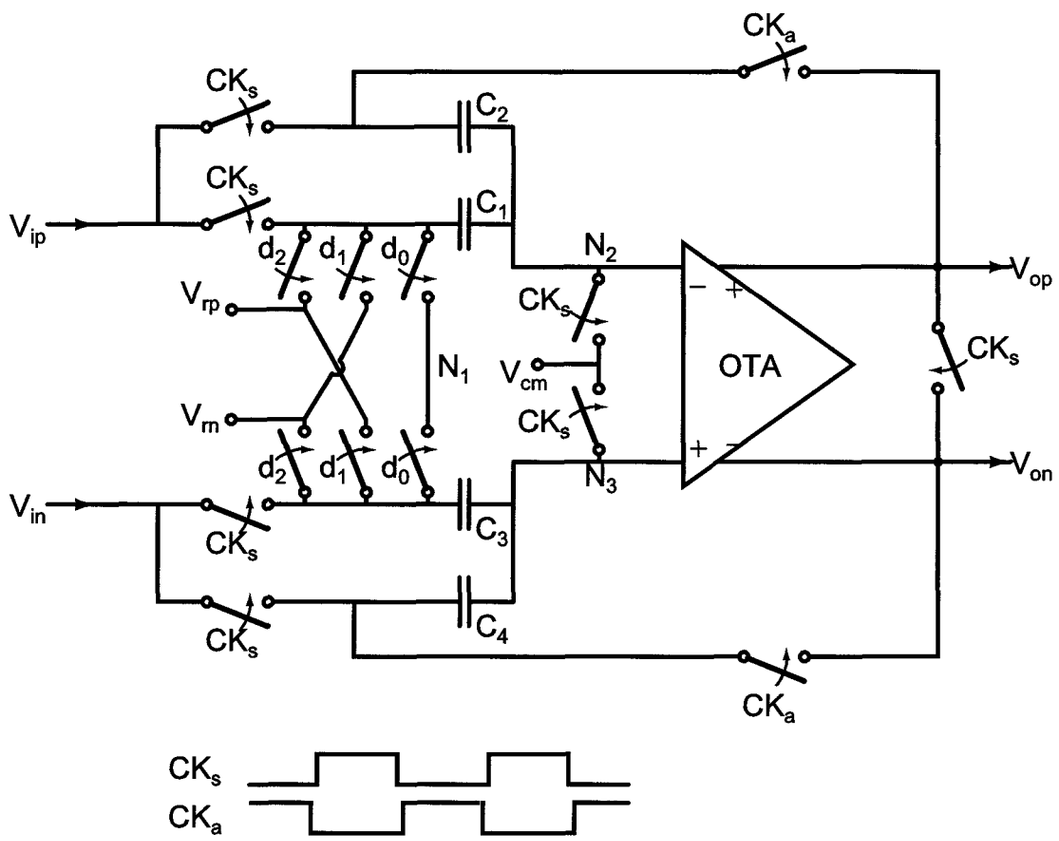


Figure 2.3: A standard fully differential MDAC for a 1.5bit stage, the non-overlapping sampling clock phase CK_s and the amplification phase CK_a are also shown. Switches d_0-d_2 are controlled by the sub-ADC output during CK_a. Center switch d_0 is used to replace the reference voltage V_{cm} for both paths.

2.2.2 MDAC Design Considerations

A standard switched capacitor MDAC is widely used in designing pipelined ADCs [8], and its functionality and performance are well studied. But a few practical design issues might easily be overlooked. Here we will briefly investigate the issues related to input common mode, capacitor matching and noise of the MDAC. Fig. 2.3 shows the standard fully differential MDAC for a 1.5bit stage, center switch d_0 is used to replace the reference voltage V_{cm}. For the following analyses, assuming center switch d_0 is turned on during the CK_a phase.

MDAC Input Common Mode

First we look at the MDAC input common mode issue, to see whether it affects the operation of the circuit. Here we assume all the capacitors in Fig. 2.3 are identical, and the nominal common mode voltage is 0V, for both of the OTA input and output. In the case that there is a common mode voltage shift at the input of the MDAC:

$$V_{ip} = \Delta V_{cmi} + V_i \tag{2.1}$$

$$V_{in} = \Delta V_{cmi} - V_i \tag{2.2}$$

Then, from clock phase CK_s to CK_a, we can apply the charge conservation rule at the input shorted node V_{N_1}, two OTA input virtual ground nodes V_{N_2} and V_{N_3} respectively:

$$(\Delta V_{cmi} + V_i)C + (\Delta V_{cmi} - V_i)C = (V_{N_1} - V_{N_2})C + (V_{N_1} - V_{N_3})C \tag{2.3}$$

$$(-\Delta V_{cmi} - V_i)2C = (V_{N_2} - V_{N_1})C + (V_{N_2} - V_{op})C \tag{2.4}$$

$$(-\Delta V_{cmi} + V_i)2C = (V_{N_3} - V_{N_1})C + (V_{N_3} - V_{on})C \tag{2.5}$$

Assuming the OTA is ideal, $V_{N_2} = V_{N_3}$. From (2.3), we get:

$$\Delta V_{cmi} = V_{N_1} - V_{N_{2,3}} \tag{2.6}$$

From (2.4), (2.5), and $V_{op} + V_{on} = 0$ given OTA output common mode is forced to 0 by its CMFB circuit, we reach the following equation by adding them up:

$$V_{N_1} = 2V_{N_{2,3}} + 2\Delta V_{cmi} \tag{2.7}$$

From (2.6) and (2.7), we arrive at the following equations at the end of the phase CK_a:

$$V_{N_1} = 0 \tag{2.8}$$

$$V_{N_{2,3}} = -\Delta V_{cmi} \tag{2.9}$$

It's evident that even if the MDAC output common mode is not affected by the input common mode, given ideal output common mode rejection, the OTA input common mode will shift the same amount as the MDAC input common mode. Thus we either need to make sure the incoming signal's common mode is well controlled or the OTA is designed to handle large common mode range.

Capacitor Matching

There are in total four capacitors in the 1.5bit fully differential MDAC. Ideally we want all of them to have the same capacitance. Careful layout including common centroid technique can improve the capacitor matching to 0.1% level, but it's much harder trying to match all four of them. Here we'll address the issue whether matching all the capacitors C_1 to C_4 is necessary.

Assuming everything else is ideal, except for the matching of the capacitors, we can again apply the charge conservation rule at nodes V_{N_1}, V_{N_2} and V_{N_3}, respectively. Note that the results from 2.9 might not hold since the capacitors were assumed to be identical in the derivation.

Charge conservation at node V_{N_1}, from the end of the phase CK_s to the end of the phase CK_a:

$$\begin{aligned} C_1V_i - C_3V_i &= (V_{N_1} - V_{N_{2,3}})C_1 + (V_{N_1} - V_{N_{2,3}})C_3 \\ \Rightarrow (C_1 - C_3)V_i &= (C_1 + C_3)(V_{N_1} - V_{N_{2,3}}) \end{aligned} \tag{2.10}$$

Charge conservation at node V_{N_2}:

$$-V_i(C_1 + C_2) = (V_{N_{2,3}} - V_{N_1})C_1 + (V_{N_{2,3}} - V_{op})C_2 \tag{2.11}$$

Charge conservation at node V_{N_3}:

$$V_i(C_3 + C_4) = (V_{N_{2,3}} - V_{N_1})C_3 + (V_{N_{2,3}} - V_{on})C_4 \tag{2.12}$$

Assume OTA output common mode is fixed at 0, we can plug V_{op}=$-V_{on}$=V_o into 2.11 and 2.12. Then there are three variables V_{N_1}, $V_{N_{2,3}}$ and V_o in the three equations above. Solving V_o finally gives:

$$V_o = \frac{1}{2}(\frac{C_3 + C_4}{C_4} + \frac{C_1 + C_2}{C_2})V_i + \frac{1}{2}((\frac{C_3}{C_4} - \frac{C_1}{C_2})\frac{C_1 - C_3}{C_1 + C_3})V_i \tag{2.13}$$

From 2.13, we observe that as long as $C_1 = C_2$ and $C_3 = C_4$, the second term on the right side of the equation will drop out and V_o is exactly equal to $2V_i$, which is the expected output in this case. Note that given $C_1 = C_2$ and $C_3 = C_4$, V_{N_1} and $V_{N_{2,3}}$ are still functions of C_1 and C_3:

$$V_{N_{2,3}} = \frac{C_1 - C_3}{C_1 + C_3}V_i \tag{2.14}$$

$$V_{N_1} = 2\frac{C_1 - C_3}{C_1 + C_3}V_i \tag{2.15}$$

If $C_{1,2}$ is not equal to $C_{3,4}$, the common mode voltage at the OTA virtual ground will be modulated by the input signal. If we further apply a V_{cm} source (which should be 0 here) at node N_1, then 2.10 no longer holds because node N_1 is driven during phase CK_a. In this case derivation shows $V_{N_{2,3}}$ is equal to 0, which means the virtual ground is not modulated by the input signal anymore. In short, for both cases where node N_1 is driven or not, the function of the MDAC does not rely on the matching between $C_{1,2}$ and $C_{3,4}$. But if the node N_1 is floating, the OTA is required to handle a larger input common mode range, depending on how well $C_{1,2}$ and $C_{3,4}$ are matched.

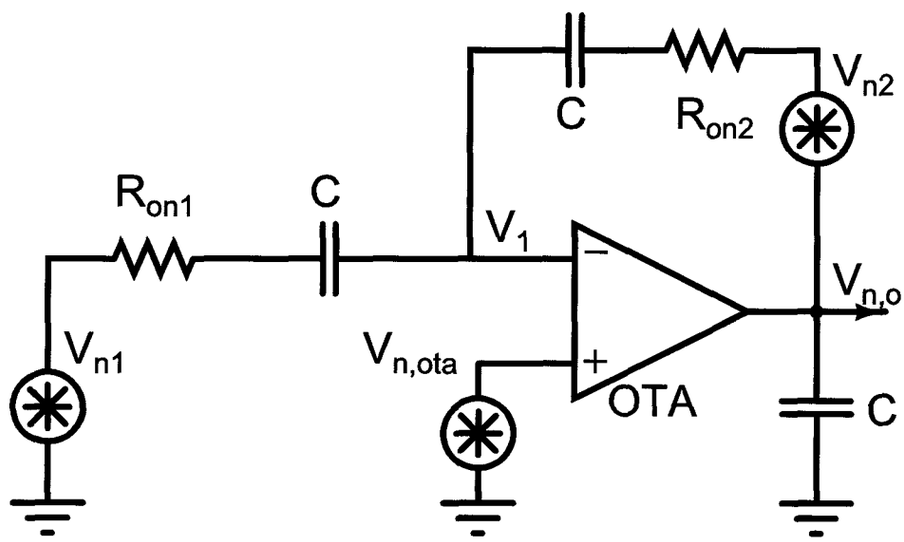


Figure 2.4: Noise sources in a standard MDAC for a 1.5bit stage, during the residue amplification phase.

MDAC Noise

For a typical pipelined ADC, noise is an important design parameter. It often limits the performance especially for a high resolution ADC. Usually we need to make sure that the input referred noise of an ADC is below the quantization noise. For a pipelined ADC, noise is mainly contributed by the MDAC of a pipelined stage, the reference voltage source and the sampling clock jitter. Among them, the noise from the MDAC usually dominates and it receives much attention when designing a pipelined ADC. Due to its discrete nature and involvement of two clock phases, the noise analysis of an MDAC might not appear straightforward. Noise in switched capacitor circuits has been dealt with in various sources [49–52]. In order to better understand how different noise sources in an MDAC play a role, we present a simplified analysis for the MDAC used in a 1.5bit stage. Fig. 2.4 shows the MDAC in the amplification phase. All the switch noises and OTA noise are included. The value of the load capacitor is equal to the unit capacitor in the MDAC, which assumes a stage scaling factor of 2 [5, 15].

During the sampling phase, which is not shown in the schematic, due to aliasing of the sampled noise [53], the total noise power on both capacitors is:

$$V_{n,i,sa}^2 = \frac{kT}{2C} \tag{2.16}$$

It's not a function of switch on resistance, because the power spectral density is proportional to R_{on}, while the bandwidth of the $R_{on} - C$ circuit is inversely proportional to R_{on}. During

this sampling phase, the OTA is being reset and not connected to the sampling network, so the OTA won't contribute any noise. Then we move on to analyze the noise in the amplification phase. As shown in Fig. 2.4, switch on resistance R_{on1} from reference voltage path and R_{on2} from feedback path, as well as OTA contribute to the output noise. Here we can use superposition and calculate each noise source's contribution separately. The output noise can be calculated using the following formula:

$$V_{n,o}^2 = \int_0^{inf} S_{n,i}(\omega)|H(\omega)|^2 \, d\omega \tag{2.17}$$

or it can be simplified if we know the equivalent noise bandwidth of the transfer function $H(\omega)$:

$$V_{n,o}^2 = S_{n,i}(\omega)|H(0)|^2 BW \tag{2.18}$$

In the above formulas, $S_n(\omega)$ is the spectral density of a noise source, $H(0)$ is the noise gain at DC from the noise source to the MDAC output, $H(\omega)$ is the circuit transfer function and BW is the equivalent noise bandwidth from the noise source to the MDAC output. For the simplicity of this analysis, assume a single stage OTA is used and it has an input referred noise spectral density:

$$S_{n,ota}(\omega) = 2 \cdot 2 \cdot 4kT\frac{2}{3}\frac{1}{g_m} \tag{2.19}$$

where the first factor 2 accounts for the two input transistors of the OTA, the second factor 2 roughly accounts for the extra noise from the rest of the OTA, mainly the loading current sources. The spectral density for the two switches are straightforward:

$$S_{n1,2}(\omega) = 4kTR_{on1,2} \tag{2.20}$$

Noise gains at DC for the three noise sources are:

$$H_{n1}(0) = \frac{C}{C} = 1 \tag{2.21}$$

$$H_{n2}(0) = 1 \tag{2.22}$$

$$H_{n,ota}(0) = 1 + \frac{C}{C} = 2 \tag{2.23}$$

It shows that the OTA noise gain is twice as large as those of the R_{on} noise. And in a practical design, switch R_{on} is designed to be 5-10 times smaller than $1/g_m$, so that it doesn't affect the settling during the amplification phase. Thus the OTA noise spectral density in 2.19 dominates over the switch ones in 2.20. It can also be shown that all three noise sources see the same pole to the MDAC output. Based on 2.17, we can see that the OTA noise dominates at the MDAC output during the amplification phase[1]. The GBW of the OTA is $g_m/(C + C//C) = 2g_m/(3C)$ and the feedback factor β of the MDAC is 1/2,

[1]Derivations show that V_{n1} and V_{n2} also see a zero and a non-dominant pole, but their transfer functions are still mainly shaped by the dominant pole, comparable to the transfer function from $V_{n,ota}$ to the output. It would be complex and tedious to derive the exact output noise due to V_{n1} and V_{n2}, using 2.17

thus the effective noise bandwidth that $V_{n,ota}$ sees is [54]:

$$BW = \frac{1}{4}\frac{g_m}{3C} \tag{2.24}$$

After plugging 2.19, 2.23 and 2.24 into 2.18, we get the output noise power due to the dominating OTA noise in the amplification phase:

$$\begin{aligned} V_{n,o}^2 &= 16kT\frac{2}{3}\frac{1}{g_m}\cdot 2^2 \cdot \frac{1}{4}\frac{g_m}{3C} \\ &= \frac{32kT}{9C} \end{aligned} \tag{2.25}$$

Referring the output noise power to the input by dividing the MDAC gain of 2^2, and adding the noise from the sampling phase, we reach the total input referred noise of the MDAC:

$$\begin{aligned} V_{n,i}^2 &= V_{n,i,sa}^2 + V_{n,i,amp}^2 \\ &= \frac{kT}{2C} + \frac{32kT}{9C}/2^2 \\ &= \frac{kT}{2C} + \frac{16}{9}\frac{kT}{2C} \end{aligned} \tag{2.26}$$

The result shows that the noise of the MDAC is not a function of g_m of the OTA. In this particular example with a stage gain of 2, the assumed OTA noise factor and its load, 2.26 shows the noise contributed by the OTA is almost twice as large as the sampling $kT/(2C)$ noise. Note that the calculated output noise power in the amplification phase is assumed

to be sampled by the next stage, so all the noise is aliased to the Nyquist band, similar to the input $kT/(2C)$ noise. Since the sampled noise at the end of the amplification phase is all that counts, it seems that the noise in the sampling phase can be ignored. But note that during the amplification phase, the sampled noise charge from the sampling phase is transferred to the output and has a voltage gain of 2, so it appears in the amplification phase and the voltage gain of 2 from the sampling phase to the amplification phase also explains why the output noise power is divided by 2^2 when referred to the MDAC input.

2.2.3 Auxiliary S/H for Sub-ADC Path

The conventional circuit architecture for the first stage of a pipeline ADC includes a dedicated front-end SHA, as shown in Fig. 2.5(a). This front-end SHA guarantees that the MDAC path and the sub-ADC path operate on the same sample of the input signal. As shown in Fig. 2.5(b), the sub-ADC decides when the MDAC is sampling and the sub-ADC outputs are ready when the MDAC starts amplifying. Additionally, preamplifiers are typically used in the comparators of the sub-ADC to block their kick-back noise [55]. These approaches allow a fast operation of the ADC, but at the cost of a dedicated front-end SHA circuit and comparator preamplifiers.

Design techniques for signal path SHAs at ultra-low voltages have been explored in [56]. In this work, we propose an architectural change to avoid the front-end SHA, as well as the comparator preamplifiers. As shown in Fig. 2.6(a), a simple, coarse, auxiliary S/H is in-

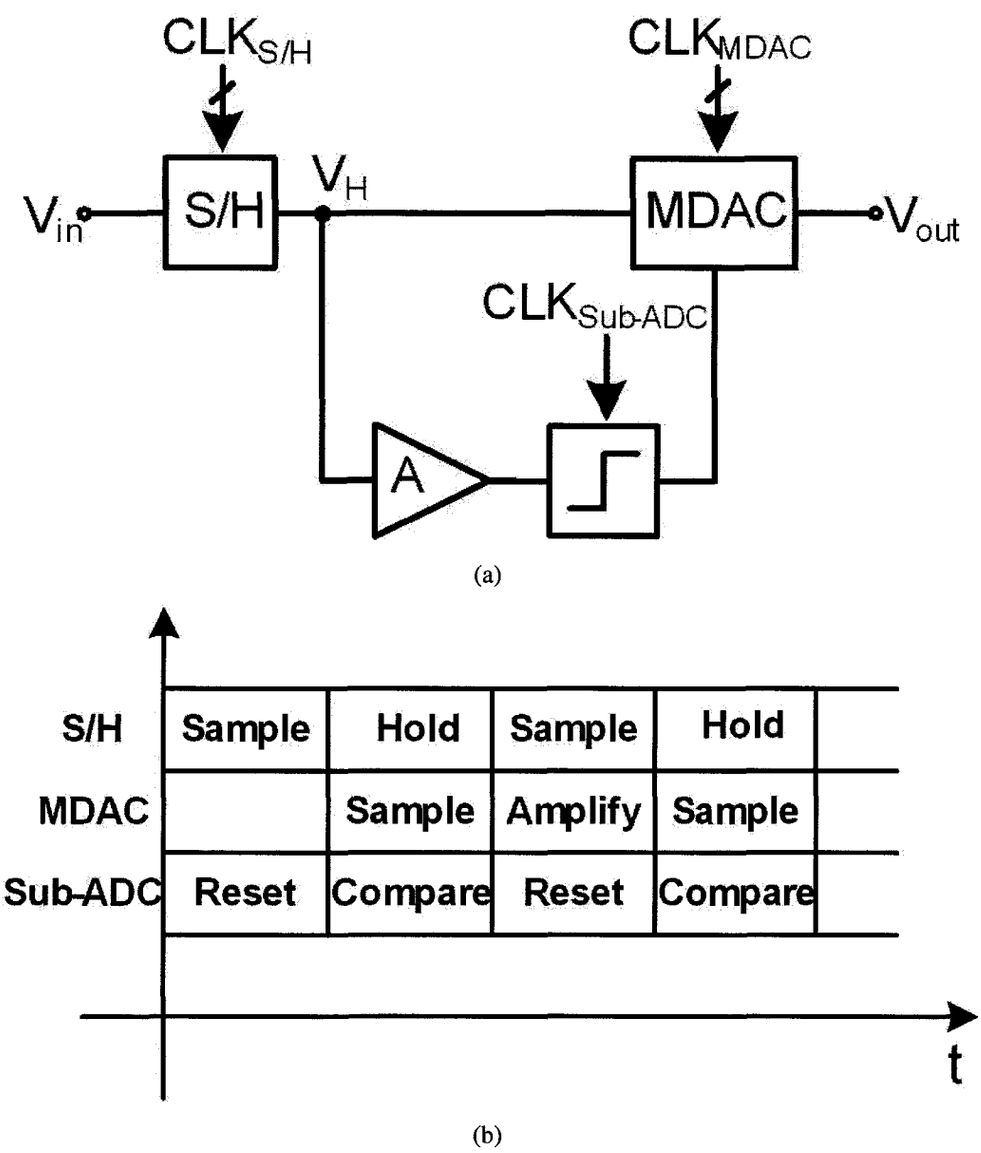
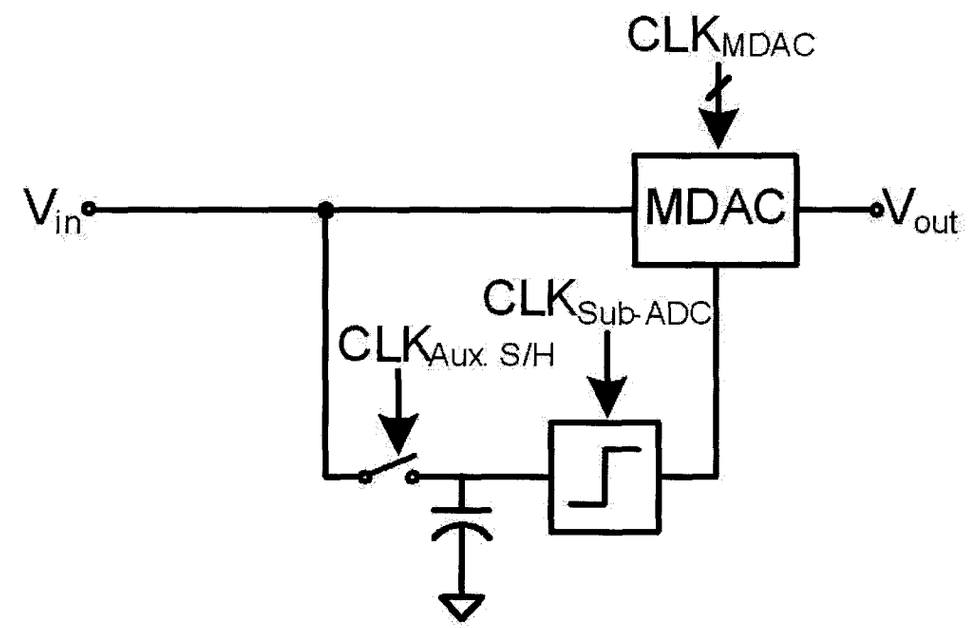
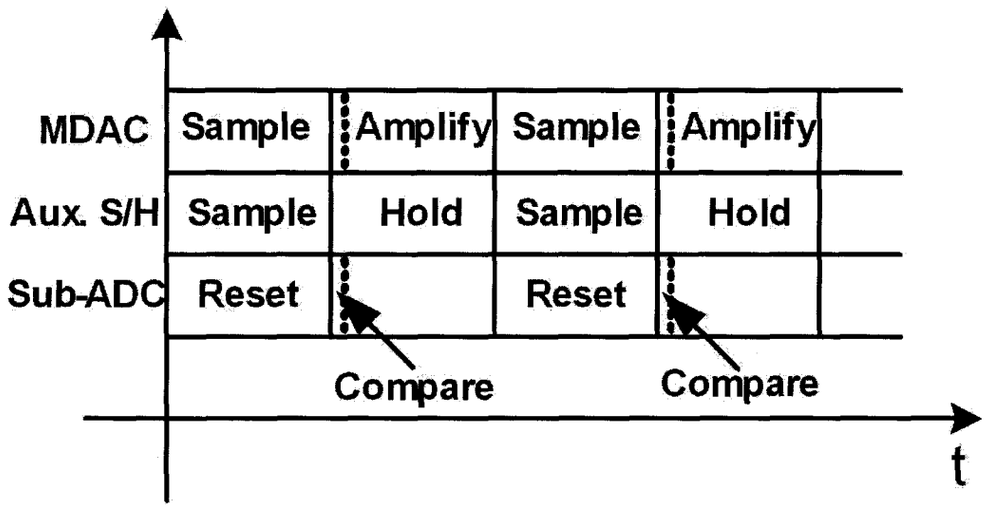


Figure 2.5: (a) Block diagram of the first stage of a conventional pipeline ADC with a dedicated front-end sample and hold (S/H) and preamplifier (A) in the sub-ADC and (b) the associated operation sequence.



(a)



(b)

Figure 2.6: (a) Block diagram of the proposed pipeline stage with auxiliary sample and hold circuit and (b) the associated operation sequence.

serted in the sub-ADC path. This auxiliary S/H samples the input signal during the same sampling phase as the MDAC path. It holds the input signal while the comparators in the sub-ADC make their decision (see Fig. 2.6(b)) at the start of the MDAC's residue amplification phase. The open sampling switch blocks the comparator kickback noise from entering the signal path. In the presented 10MS/s pipelined ADC design, the latched comparators, using the topology presented in [57], reach their decision in less than 2% of the sampling clock period which leaves plenty of time for the MDAC to amplify the residue[2]. This approach is well suited for moderate-speed pipelined ADCs and offers three benefits: the dedicated, high accuracy, front-end SHA, and the associated considerable power consumption and die area, as well as the comparator preamplifiers are eliminated; kickback noise from the comparator is blocked by the switch of the auxiliary S/H; the auxiliary S/H can be significantly less accurate than a front-end SHA, since sampling errors are equivalent to comparator offset and a 1.5 bit/stage pipelined ADC is very robust against such offsets. A mismatch between the time constants of the sampling network in the MDAC path and sub-ADC path translates into an offset in the sub-ADC path [58, 59]. Assuming that the sampling clock skew between these two paths can be neglected, the worst case mismatch error is [58]:

$$V_{error} = A2\pi f_{in}(\tau_{MDAC} - \tau_{sub-ADC}) \tag{2.27}$$

[2]To further improve the design, the non-overlapping time between the sampling and amplifying phase of the MDAC could be used to get the comparator outputs ready earlier.

where A and f_{in} are the full-scale input signal amplitude and maximum signal frequency respectively. τ is defined as the sampling time constant or propagation delay:

$$\tau = \frac{\tan^{-1}(2\pi f_{in} RC)}{2\pi f_{in}} \approx RC \tag{2.28}$$

where RC is the time constant of the sampling network; since the sampling network bandwidth (1/RC) is designed to be much higher than maximum input frequency, f_{in}, the approximation in 2.28 indeed holds. In the presented ADC, the full-scale single-ended signal amplitude, A, is equal to V_{ref}, which is 100mV, and the 1.5 bit sub-ADC can tolerate an offset of $V_{ref}/4$, or 25mV, so that for a maximum signal frequency of 5MHz when sampling at 10MS/s, we obtain the following requirement:

$$\Delta(RC) \approx \Delta\tau < \frac{V_{ref}}{4V_{ref}} \frac{1}{2\pi f_{in}} \approx 8ns \tag{2.29}$$

This derivation assumes there are no other offsets in the sub-ADC path, while in practice, we need to allow for comparator offsets due to device mismatch. If we allocate half of the total tolerable offset to the comparators, the system is able to tolerate a sampling-network time-constant difference between the MDAC and sub-ADC of up to 4ns.

In the presented design, the RC network in the MDAC has a time constant smaller than 4ns to guarantee the dynamic performance in the presence of nonlinear resistance of the switch. It is interesting to note that, theoretically, the auxiliary S/H could be eliminated.

However, it is still used to block the comparator kick-back noise and to allow for larger comparator offsets. The auxiliary S/H is realized with the same sampling switch as the MDAC path but a sampling capacitor of about $\frac{1}{2}$ the size. This sampling capacitor is still large enough so that the clock feed-through from the switch does not affect the sampled voltage significantly.

2.2.4 Reverse Short Channel Effect for Reduced V_T

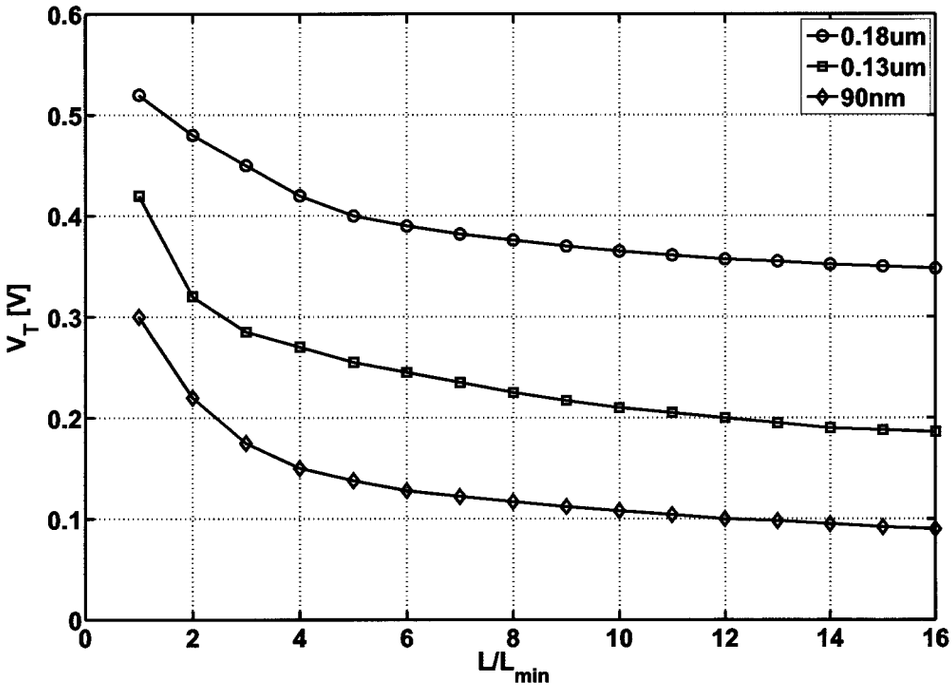


Figure 2.7: Simulation showing the decrease of the threshold voltage, V_T, for increasing device lengths, a.k.a. the Reverse Short Channel Effect (RSCE), for 2μm wide NMOS transistors in different CMOS technologies.

In scaled CMOS technologies (0.18μm and beyond), the reverse short channel effect

(RSCE), i.e., the increase of the transistor threshold voltage,V_T, for decreasing channel length, L, is well known to occur [60,61] and is illustrated in Fig. 2.7. In ultra-low-voltage analog design, we can take advantage of this effect and obtain a lower V_T by choosing a larger L. However, increasing L, increases the transistor's parasitic capacitors, and decreases the its transit frequency f_T. In nano-scale CMOS technologies, the transistor f_Ts are very high and additionally, for analog circuits, the attainable speed performance is typically limited by load or compensation capacitors rather than transistor parasitic capacitors. Moreover, for analog designs, the length is usually chosen as 2 to 5 times the minimum length to improve the output impedance and to reduce 1/f noise, as well as, to improve device matching. A V_T reduction is very welcome for transistors used as active loads or transconductors, since it results in more flexibility in the choice of their bias point even at ultra-low supply voltages. For transistors used as switches, the reduced V_T improves the switch ON conductance for limited gate voltage swings but increases the OFF state leakage. However, the switch OFF leakage is alleviated using cascaded sampling technique as described next.

In the presented prototype in 90nm CMOS, the majority of the transistors are sized 4 times the minimum length or 0.36μm, and have a V_T between 100mV and 200mV across corners in simulation.

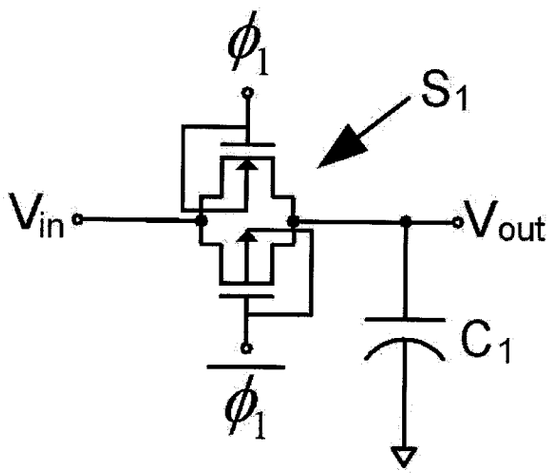
2.3 Circuit Level Design Considerations

2.3.1 Cascaded Sampling Technique and Switches

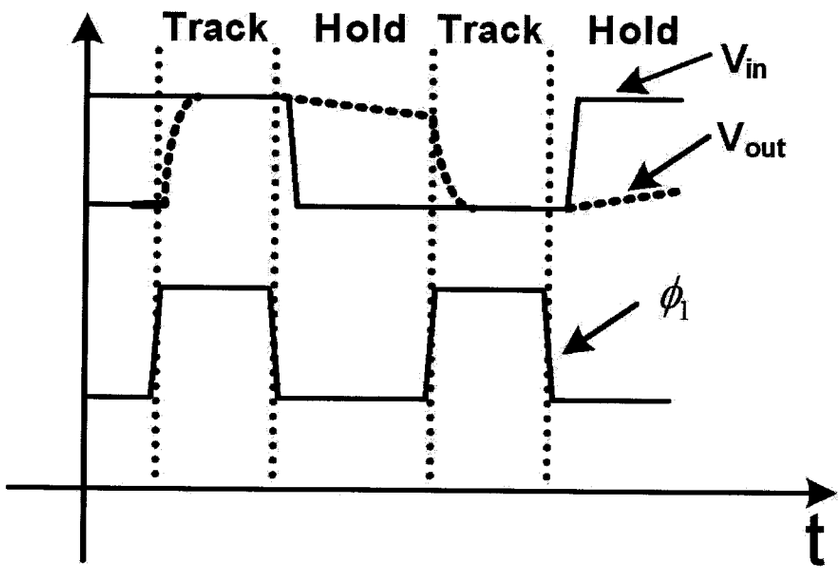
In nano-scale CMOS technologies, sub-threshold MOS channel leakage, MOS gate leakage, and reverse-biased PN junction band-to-band tunneling become more and more significant [62–64]. At an ultra-low supply voltage of 0.5V, MOS gate leakage is substantially reduced since it is exponentially dependent on the gate voltage. The reverse-biased PN junction leakage becomes significant when the reverse biasing voltage exceeds the breakdown voltage, which doesn't occur with a 0.5V supply. The main leakage concern in this design is the sub-threshold leakage of switches in their OFF state, particularly during the non-overlapping time between sampling and holding phases, when a capacitor is not connected to any voltage source. This leakage causes signal dependent distortion in the switched capacitor sample and hold circuits.

To illustrate the effect of this leakage, a basic S/H circuit and the associated waveforms are shown in Fig. 2.8. Due to the sub-threshold switch leakage, the output voltage V_{out} is not held constant when S_1 is OFF. In the worst case, assuming a rail-to-rail input signal at Nyquist frequency, V_{in} changes from VDD to 0 after S_1 turns off; this puts S_1 in weak inversion and saturation. The leakage current $I_{S1,OFF}$ is then given by:

$$I_{S1,OFF} \propto \frac{W}{L} \exp\left(\frac{-V_T}{nkT/q}\right) \tag{2.30}$$

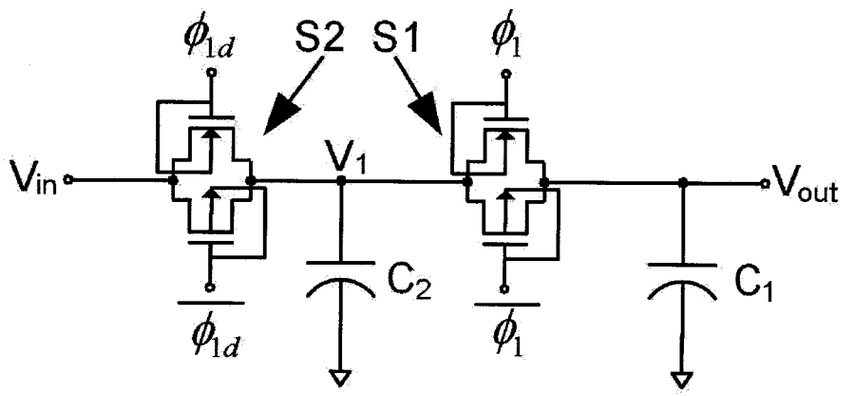


(a)



(b)

Figure 2.8: (a) Standard sample-and-hold circuit (all transistors are sized as 12μm/0.36μm and C_1 is 1pF); and (b) associated node waveforms.



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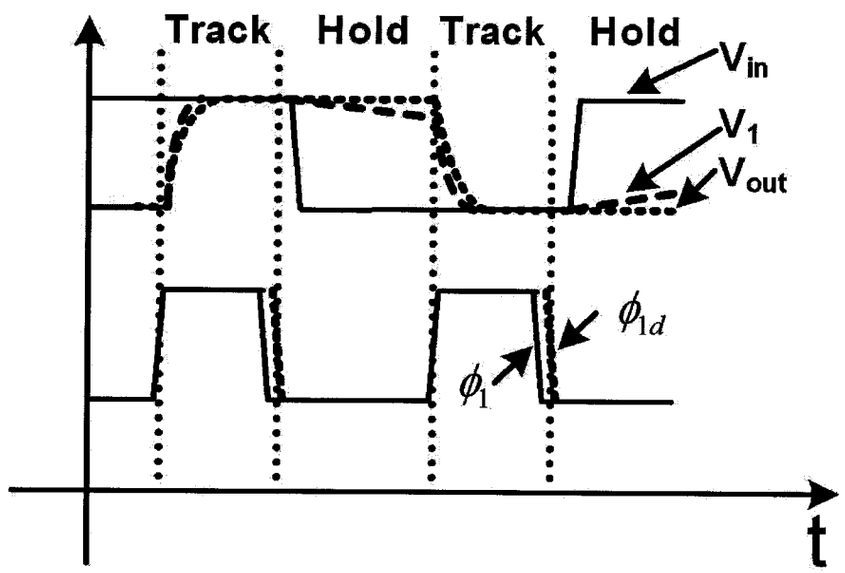

(b)

Figure 2.9: (a) Proposed cascaded sample-and-hold circuit to combat switch OFF leakage (all transistors are sized as 12μm/0.36μm, C_1 is 1pF and C_2 0.25pF) and (b) associated node waveforms.

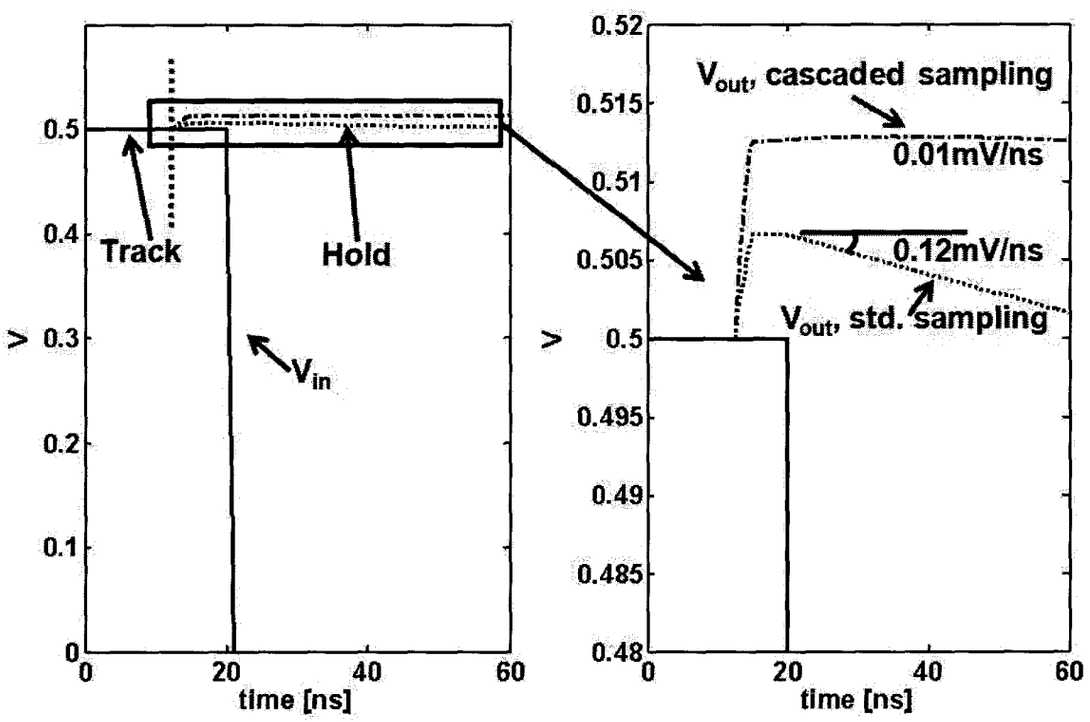

Figure 2.10: Simulation results for the sample-and-hold circuits in Fig. 2.8, 2.9 with rail-to-rail input showing the significant reduction of the effect of leakage during the hold time for the cascaded sample and hold compared to standard sample and hold.

where W/L is the transistor aspect ratio, V_T is the threshold voltage, kT/q is the thermal voltage and n is a technology dependent factor. Similar leakage challenges exist in each stage of the pipelined ADC when the sample and hold switches are OFF. This issue is most severe in the first stage where noise and distortion should be kept well below LSB of the full ADC.

To overcome this problem, a cascaded sampling technique is proposed to alleviate the switch sub-threshold OFF leakage. An extra switch, S_2, and an additional, smaller hold capacitor C_2 are used in front of the main switch S_1 and capacitor C_1, as shown in Fig. 2.9(a). Switch S_1 and S_2 operate during the same clock phase, but S_2 is turned OFF slightly later to ensure that it does not affect the accurate sampling on C_1. An intermediate voltage V_1 is now introduced which is held by the extra capacitor C_2. During the track phase, both switches S_1 and S_2 are ON, and V_{out} and V_1 track V_{in}. In the hold phase, S_1 and S_2 are OFF and enter weak inversion. The difference between V_{out} and V_1 is very small, but slowly grows during the hold phase due to the leakage of S_2 (see Fig. 2.9(b)). S_1 operates in weak inversion but in the linear region with a very small drain-source voltage V_{ds,S_1}; the channel leakage current of S_1 is then:

$$I_{S1} \propto \frac{W}{L}\exp(\frac{-V_T}{nkT/q})[1-\exp(\frac{-V_{ds,S_1}}{kT/q})] \approx 0 \tag{2.31}$$

Since V_{ds,S_1} remains very small, the OFF current in S_1 is very small and V_{out} is kept close to constant during the hold phase. The simulation results in Fig. 2.10 show that the slope

of the output voltage for the cascaded sample and hold is about one tenth of the slope for the conventional one. In the worst case leakage scenario, when the transistors are in the fast-fast process corner and operate at a temperature of 85°C, the proposed sampling circuit still has a 4-fold reduction in leakage. In digital circuit, stacking of two OFF devices [65] are sometimes employed to reduce static channel leakage current. In our proposed cascaded sampling technique, an extra capacitor is introduced to make sure the main switch remains in linear region when it is in OFF state, thus reducing channel leakage current more effectively.

Since there are two switches in series in the proposed scheme, the switch size needs to be increased. The extra sampling capacitor C_2 can be kept much smaller than sampling capacitor C_1 to limit the area overhead and settling time impact. C_2 was set to $\frac{1}{4}C_1$ or 250fF in this design. The leakage caused by the path connecting to V_{DAC} during the non-overlap period does not introduce distortion since the reference voltages are constant.

Switch nonidealities result in important error contributions including settling errors, charge injection errors and clock feedthrough errors. The fully differential circuit topology largely eliminates the latter two, but the voltage-dependent gate capacitance causes slightly different errors in the two differential paths. A switch design using a CMOS transmission gate with $\frac{1}{2}$ sized dummy switches was adopted to largely suppress clock feedthrough and charge injection. To reduce the switch threshold voltage and improve settling during the ON state, the switch-transistor gate and body terminals are shorted and connected to the

clock signal [56]. With a supply of only 0.5V, latch-up due to the forward biased body junction is not a concern [66].

2.3.2 0.5V OTA Design

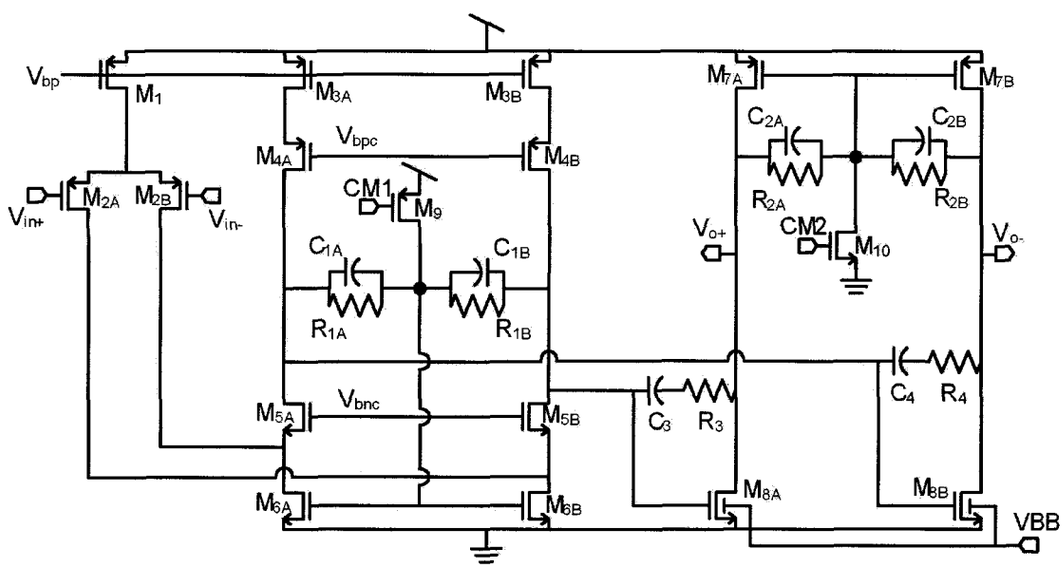

Figure 2.11: Schematic of the 0.5V operational transconductance amplifier. Device sizes shown in Table 2.1, The bodies of all transistors are shorted to their source terminals, except for the bodies of M_{8A} and M_{8B}.

The residue amplifier is the most important active block in a pipelined ADC design. To achieve 8bit resolution, the OTA DC gain in the first pipeline stage should exceed 50dB. Assuming a feedback factor of 1/3, which takes into account the input parasitic capacitance of the OTA, the GBW should be at least 18MHz to achieve a settling accuracy better than 0.4% for a 10MHz sampling frequency.

A two-stage OTA with Miller compensation has been designed, as shown in Fig. 2.11.

Table 2.1: Device sizes for the 0.5V OTA

Transistors	W(μm)	L(μm)	Transistors	W(μm)	L(μm)
M_1	150	0.36	M_{6A}, M_{6B}	18	0.36
M_{2A}, M_{2B}	360	0.18	M_{7A}, M_{7B}	56	0.18
M_{3A}, M_{3B}	12	0.36	M_{8A}, M_{8B}	50	0.18
M_{4A}, M_{4B}	12	0.36	M_9	0.4	4
M_{5A}, M_{5B}	8	0.36	M_{10}	1.2	1
Resistors and Capacitors					
R_{1A}, R_{1B}	500kΩ		C_{1A}, C_{1B}	0.2pF	
R_{2A}, R_{2B}	30kΩ		C_{2A}, C_{2B}	0.2pF	
R_3, R_4	0.8kΩ		C_3, C_4	1.8pF	

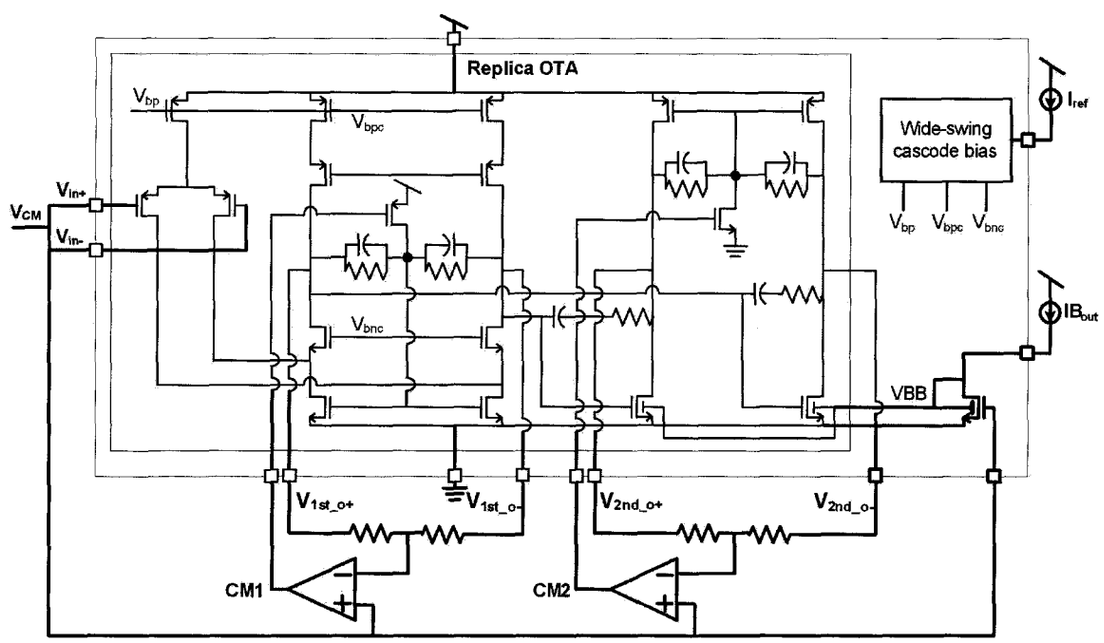

Figure 2.12: Biasing loops using an on-chip replica OTA to generate the bias voltages CM1, CM2 and VBB for the OTA in Fig. 2.11.

The first stage (M_1-M_6) uses a folded cascode topology to achieve higher gain, and a common-source, second stage (M_7-M_8) is adopted to further increase the gain and to maximize the available output swing. The input and output common-mode voltages are set to 250mV. The sizes of the devices in the OTA are summarized in Table 2.1. As mentioned earlier, the transistors are sized with larger than minimum length to improve their output impedance and reduce their V_T. The input differential pair transistors M_{2A}/M_{2B} have a length of only 2 times L_{min} to reduce their parasitic gate-source capacitance which affects the feedback factor; they are biased in weak inversion to maximize their (g_m/I) and reduce their V_{GS} to leave sufficient headroom for the tail current source M_1.

The OTA has a minimum single-ended output swing of 200mV_{p-p}. The second stage has a gain larger than 20dB (in simulation across corners) which results in a 20mV_{p-p} single-ended signal swing at the output of the first stage. In order to stack four transistors (M_3-M_6) in the cascode stage, their overdrive voltage, ($V_{GS} - V_T$), was designed to be around 100mV, resulting in a $V_{DS,sat}$ of about 80mV. For a 0.5V supply and a 20mV_{p-p} single-ended signal swing, each transistor in the stack can be allocated a nominal V_{DS} of 120mV, which guarantees operation in the saturation region.

Two local common-mode feedback loops have been adopted so that the output common mode of each stage is set to 250mV. A single common-mode feedback loop for the full OTA is not suitable, since the output common-mode voltage of the first stage would change too much due to process, voltage and temperature (PVT) variations and affect the operation of the cascode transistors M_3-M_6. Local common-mode feedback further offers

easier control of the loop dynamics and stability. In each stage, common-mode sensing resistors (R_{1A} & R_{1B}, R_{2A} & R_{2B}) feed back the common-mode signals to the gates of the active loads. Shunt capacitors (C_{1A} & C_{1B}, C_{2A} & C_{2B}) improve the high-frequency common-mode feedback and maintain the common-mode gain well below 0dB at higher frequencies. M_9 and M_{10} push a small DC current through the resistors to generate a voltage drop that determines the DC output common-mode voltages. The appropriate bias voltages for nodes CM1 and CM2 to set the level shift currents and maintain the common-mode voltages at 250mV across PVT variations, are generated on-chip using servo loops across a replica OTA as shown in Fig. 2.12. For testing flexibility the servo loop error amplifiers were implemented on the PCB test board. The V_{GS} of the output transistors M_{8A}/M_{8B} is kept at 250mV by the common-mode biasing and, due to PVT variations, the current in the output stage is not well controlled. An on-chip bias circuit, also shown in Fig. 2.12, adjusts the body voltage of the output transistors to control their DC bias current. The bias voltages V_{bp}, V_{bpc} and V_{bnc} are generated on-chip using standard wide-swing cascode biasing circuits. Each of these bias circuits is implemented once on the prototype chip and is shared by all stages; they have been laid out next to the first stage in the pipeline since its requirements are most stringent.

The measured performance of the replica OTA on our prototype chip was a DC gain of 50dB and a GBW of 32MHz for a differential load of 3pF. Each OTA draws 530μA under nominal conditions.

2.3.3 Comparator

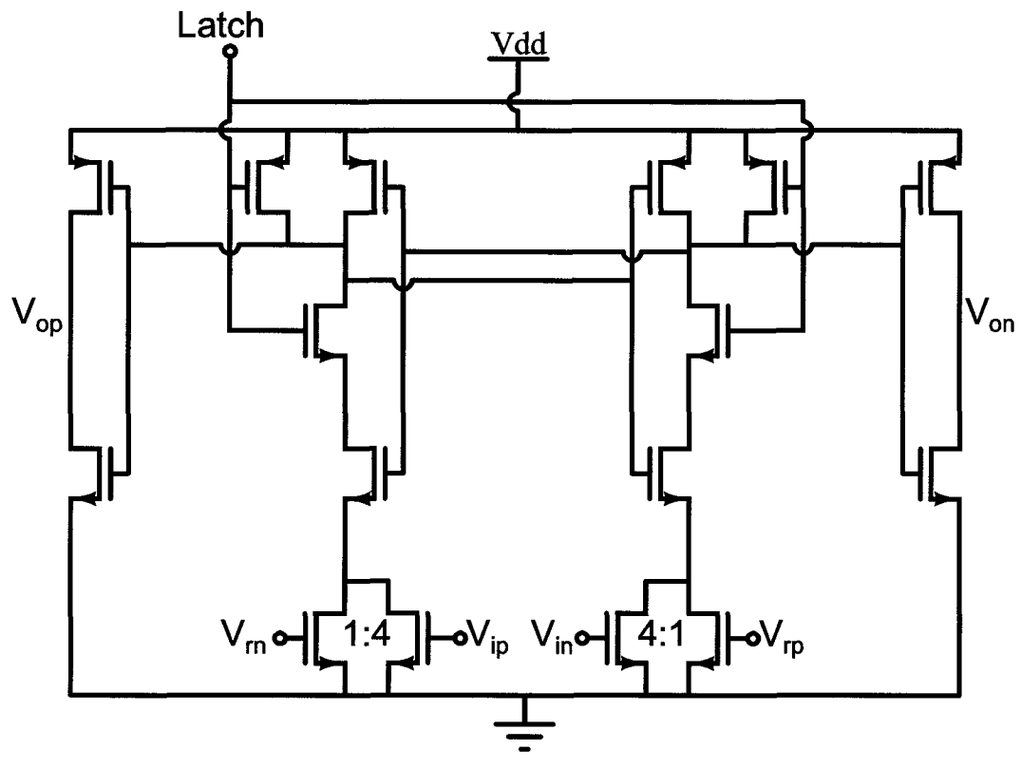

Figure 2.13: A standard dynamic latch based fully differential difference comparator.

Comparator used in the stage sub-ADCs is shown in Fig. 2.13. A preamplifier is avoided as described in section B. Besides, at 0.5V, simple differential pair preamplifier with diode connected transistor load hardly has any gain. Kick-back noise of the comparator is largely isolated from residue output of previous stage by auxiliary SHA circuit.

Input transistors are sized four times the transistors connected to reference voltages. Thus differential input is essentially comparing to one quarter of V_{ref} difference [57]. These

four transistors have larger W and L to improve their matching [67]. The comparator consumes 65μW at 5MHz sinusoidal input.

2.3.4 Non-Overlapping Clock Generator

Two non-overlapping clock signals at 10MHz are required to operate the pipelined ADC. Each clock signal has two additional variations to minimize charge injection, clock feedthrough and ensure accurate sampling. Fig. 2.14 shows the clock generator and waveform. The inverter chain with feedback generates non-overlapped clock signal. Clock falling edge delay is mainly achieved by inserting NMOS M_1-M_4.

2.4 Measurement Results

The die photo and layout of the chip prototype is shown in Fig. 2.15. It was fabricated on a 90nm CMOS process using regular V_T devices. The chip size is 1.2mm$\times$1.2mm and active area is 0.95mm$\times$0.9mm. The chip is covered by metal 9 fill structures; the main chip sections are shown on the layout: eight identical pipeline stages, the clock generator and buffer, and the OTA replica biasing.

The dies were packaged in a 64-pin QFP package and mounted on a circuit board which included the external voltage reference generators and the error amplifiers for the biasing loops. A Tektronix AWG2021 arbitrary waveform generator provided the differential input signals, and an Agilent 33220A generated the input clock; an Agilent 1692AD logic ana-

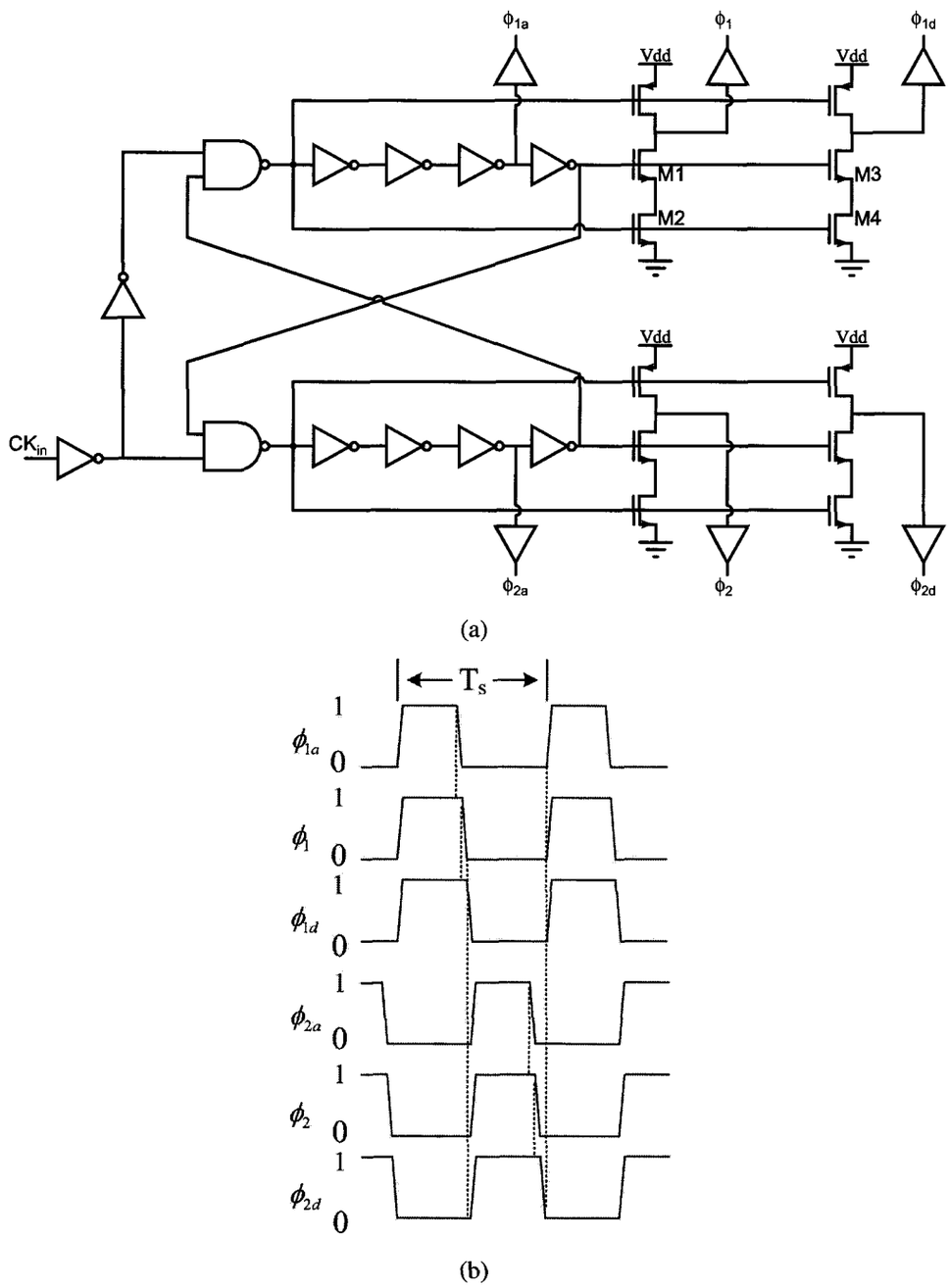

Figure 2.14: (a) Non-overlapping clock generator, the advanced and delayed clock phases are achieved by inserting NMOS M_1-M_4; (b) Two clock phases with advanced and delayed versions from the clock generator.

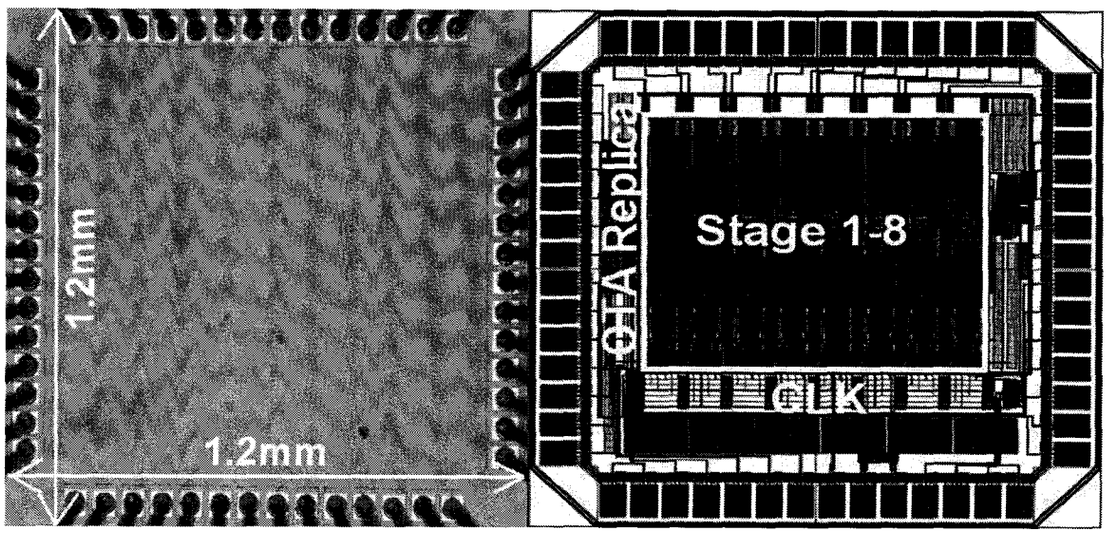

Figure 2.15: Die photo (left) and layout plot (right).

lyzer collected the uncorrected bits from all the stages. The digital offset correction was performed off-line.

Fig. 2.16 shows the digital output spectrum for a full-scale, 109kHz input signal while operating from a 0.5V supply and sampling at 10MS/s. The third order harmonic is -57dB below the signal. This distortion is probably due to the finite gain of the OTA in the residue amplifier or possibly due to capacitor mismatch. The signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) for full-scale input signals with frequencies ranging from 101kHz to 4.9MHz is shown in Fig. 2.17; the dynamic performance of the converter is quite flat with about a 4dB drop in the SNDR at the Nyquist frequency. This illustrates the effectiveness of the adopted pipeline stage topology using an additional coarse sub-ADC S/H while eliminating the front-end SHA.

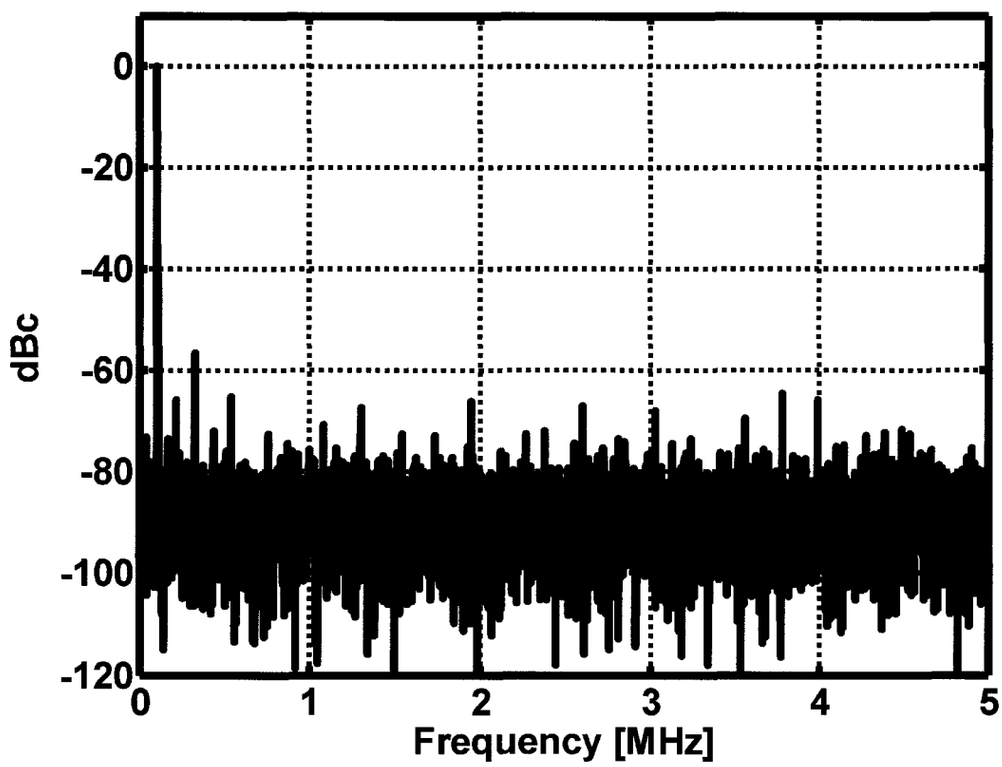

Figure 2.16: Measured output spectrum at 10MS/s with a full-scale 109kHz sinewave input using a 16384-point FFT.

The ADC's SNR, SNDR, and SFDR are very consistent for sampling frequencies ranging from 100kHz to 10MHz, as shown in Fig. 2.18. This demonstrates that the switch leakage of the cascaded sampling circuit is not significant even at 100ksps. The ADC is also characterized with varying input signal amplitudes from -45dBFS to 0dBFS, Fig. 2.19 shows the corresponding SNR, SNDR, and SFDR. The static performance of the ADC was determined by taking 2048 samples at 10MS/s of a full-scale ramp input signal and is shown in Fig. 2.20; the maximum |DNL |and |INL |is 0.55 and 1.19 LSB respectively.

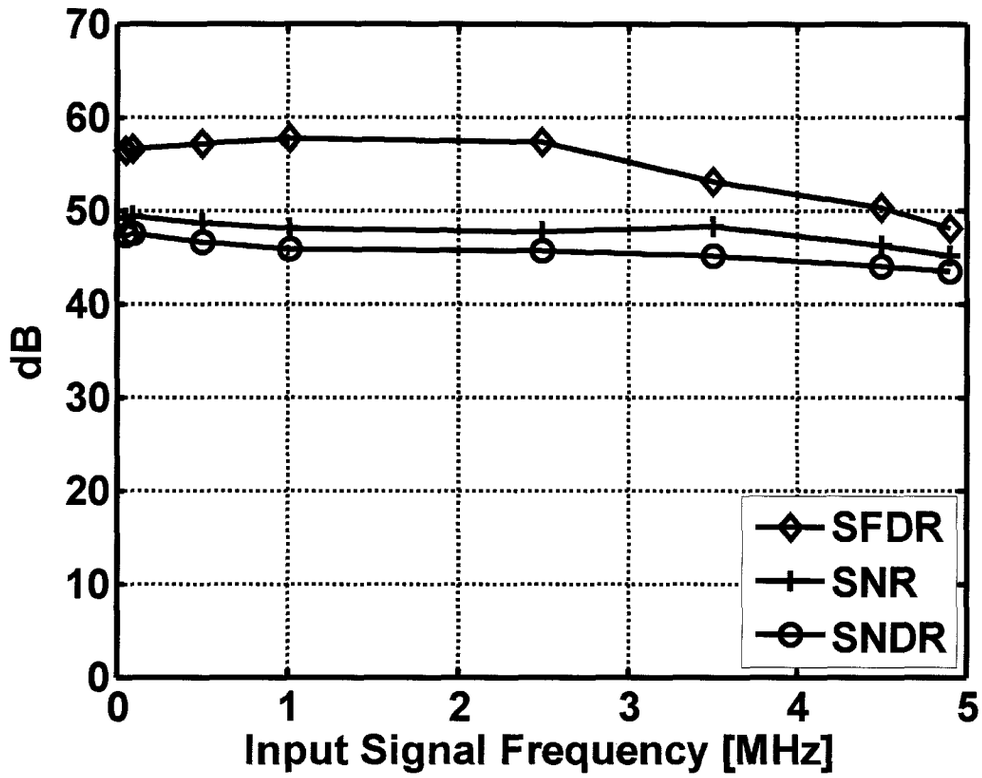

Figure 2.17: Measured SNDR, SNR, SFDR at 10MS/s for a full-scale input sinewave with frequencies varying from 101kHz to 4.9MHz.

Table 2.2 summarizes the measured results including the performance for ±10% supply voltage variations; the performance is consistent from 0.45V to 0.55V, with less than 1.9dB difference. The chip was further tested at 80°C and a degradation of less than 3dB in the SNDR degradation was observed for 0.5V and 10MS/s operation. The pipelined ADC nominally consumes 2.4mW from a 0.5V supply. Ten chip samples were tested and the variation in their SNDR performance was within a ±0.75dB range.

A comparison of the sub-1V ADCs with different architectures is shown in Table 2.3.

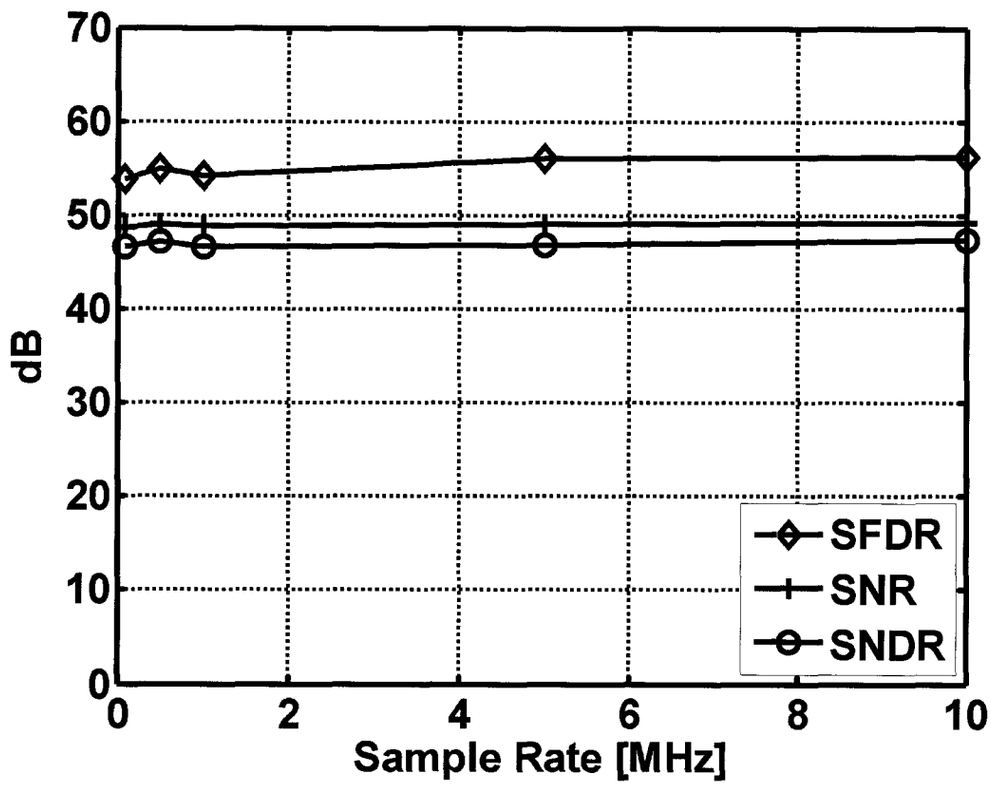

Figure 2.18: Measured SNDR, SNR, and SFDR for a full-scale input sinewave at 49kHz with sampling frequencies varying from 100kHz to 10MHz.

Fig. 2.21 illustrates the FOM versus the supply voltage of the ADC. The ADC presented in this work operates at the highest sampling speed for the lowest supply voltage. Its FOM is 1.15pJ/Conv., which is among the best in ADCs below 0.7V. If we further assume that stage scaling is used and the second and third stage are scaled by half compared to the previous stage, the FOM can be improved to 0.5pJ/Conv. Step or less.

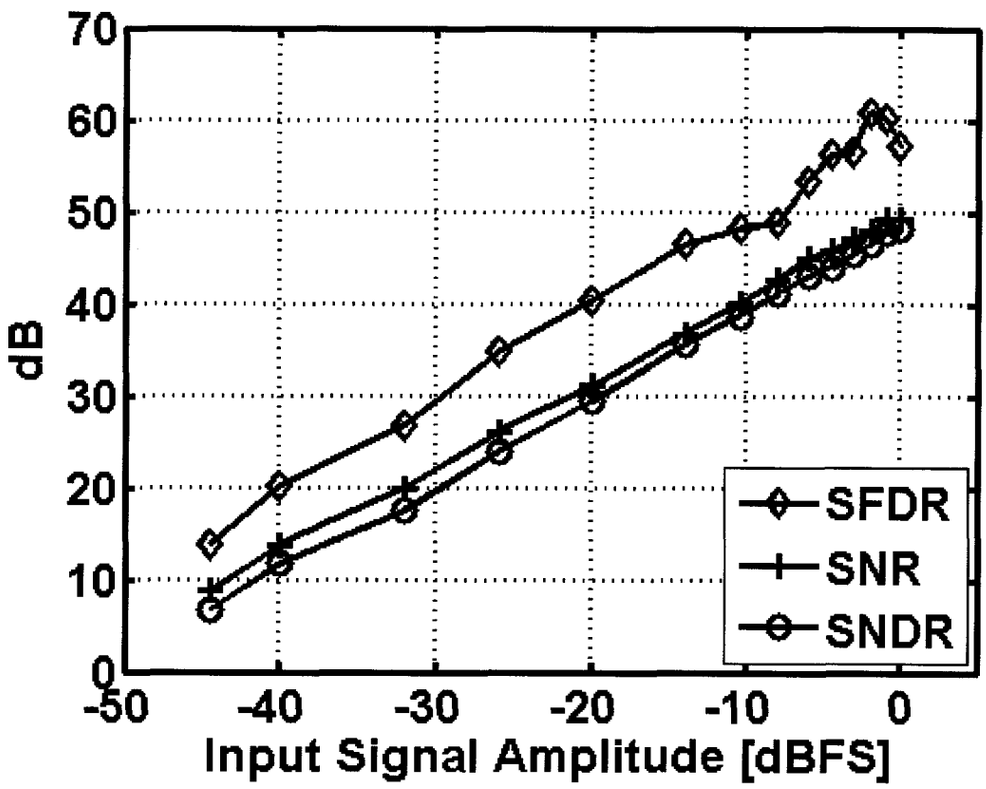

Figure 2.19: Measured SNDR, SNR, and SFDR at 10MS/s with a 109kHz sinewave input of varying amplitude from -45dBFS to 0dBFS.

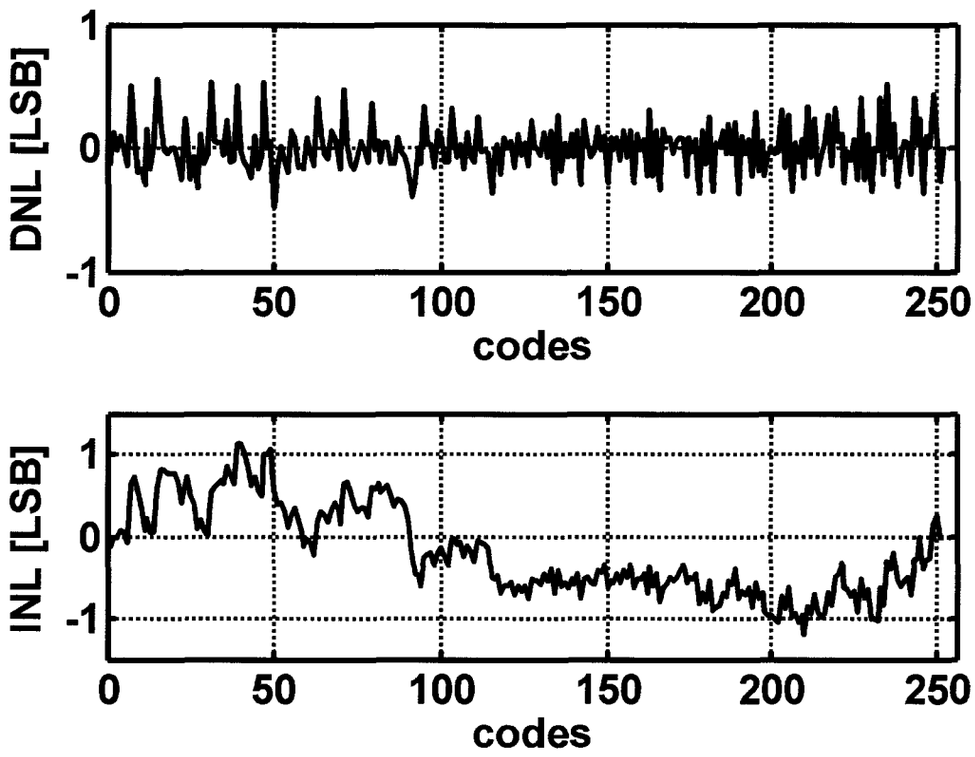

Figure 2.20: Measured DNL and INL.

Table 2.2: ADC performance summary from 0.45V−0.55V @ 25°C

Resolution	8			bits
Sample Rate	10			MS/s
Input Signal Range	0.4			$V_{pp,diff}$
VDD	0.45	0.5	0.55	V
SNDR[a]	46.8	48.1	47.2	dB
SNR[a]	48.4	49.3	48.9	dB
SFDR[a]	55.1	57.2	56.5	dB
DNL	-0.54/0.65	-0.48/0.55	-0.59/0.85	LSB
INL	-1.6/0.89	-1.19/1.12	-1.8/1.1	LSB
Power	2.3	2.4	2.6	mW
Die Size	1.2×1.2			mm^2
Technology	90nm CMOS with regular V_T devices			

[a]Measured with a 109kHz, full scale, sinusoidal input signal.

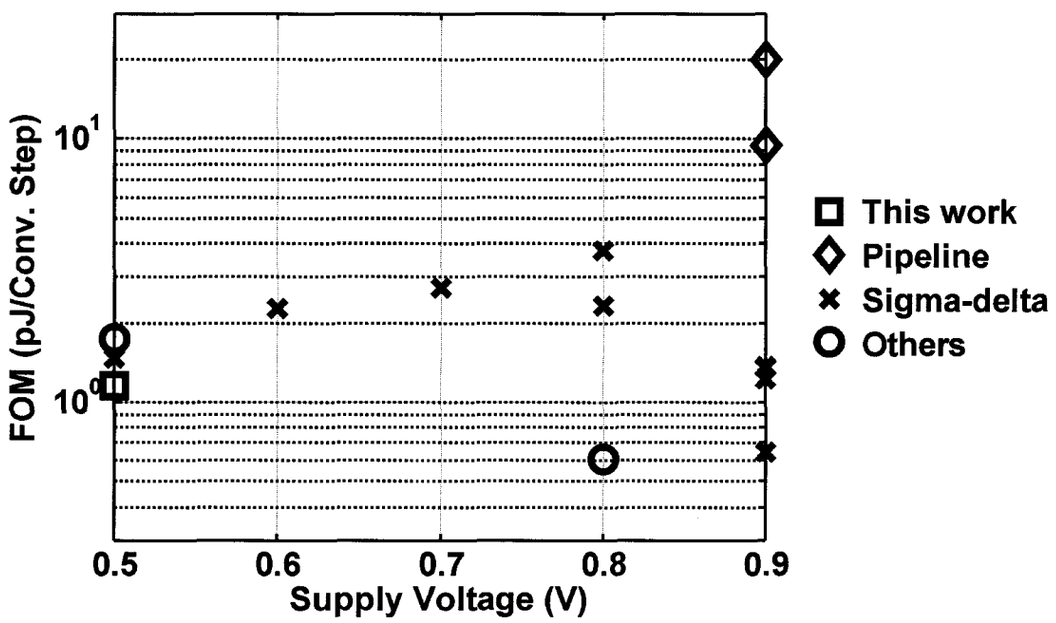

Figure 2.21: Sub-1V ADC Performance Comparison; SNDR and signal bandwidth are shown next to reference number.

Table 2.3: Sub-1V ADC Performance Comparison

Author&Year	VDD(V)	BW(kHz)	Type	SNDR(dB)	Power(mW)	Fs(MS/s)	Area(mm^2)	Tech.(μm)	FOM[a]
Goes 06 [68]	0.9	10	SDM	80.1	0.2	5	0.06	0.18	1.22
Kim 06 [69]	0.9	24	SDM	89	1.5	6.144	1.44	0.13	1.35
Kim 06 [70]	0.9	8	SDM	70	0.026	1.024	0.4	0.25	0.65
Ueno 04 [71]	0.9	1920	SDM	50.9	1.5	61.44	0.12	0.13	1.36
Peluso 98 [72]	0.9	16	SDM	62	0.04	1.538	0.85	0.5	1.22
Li 05 [12]	0.9	2500	Pipeline	50	12	5	1.4	0.18	9.43
Chang 05 [13]	0.9	500	Pipeline	55	9	1	1.44	0.18	20
Reverend 03 [73]	0.8	10	SDM	64	0.06	1.28	0.23	0.35	2.33
Chang 02 [74]	0.8	30	SDM	60.6	2.5	5	2.11	0.25	45.5
Sauerbrey 01 [75]	0.8	16	SDM	66.1	0.2	1.536	0.17	0.18	3.76
Lin 02 [76]	0.8	1100	Flash	33	0.48	22	0.3	0.13	0.61
Sauerbrey 02 [47]	0.7	8	SDM	67	0.08	1.024	0.082	0.18	2.73
Ahn 05 [77]	0.6	24	SDM	81	1	3.072	2.9	0.35	2.27
Pun 06 [78]	0.5	25	SDM	74	0.3	3.2	0.6	0.18	1.47
Sauerbrey 03 [79]	0.5	2.05	SAR	43.3	0.85	0.0041	0.11	0.18	1.74
This Work	0.5	5000	Pipeline	48.1	2.4	10	0.85	0.09	1.15

[a]

$$\text{FOM} = \frac{\text{Power}}{2^{(\text{SNDR}-1.76)/6.02} * 2 * \text{Bandwidth}} 10^{12}[\text{pJ/Conv. Step}]$$

2.5 Idea for Future Improvement

2.5.1 Switch Gate-Bootstrapping

One potential challenge for high performance ADCs at ultra-low supply voltage would be the design of a sampling switch. As VDD scales down for nano-meter CMOS technologies, threshold voltage V_T doesn't scale much, mainly due to the concern of standby current leakage in digital circuit. A transmission gate is often used as a sampling switch to accommodate for rail-to-rail input signal. But in the case where $V_{TN} + V_{TP} > VDD$, the switch will not be conductive when the input signal is in the middle range. Besides, the transistor conductance is a function of the input voltage, as shown in the equation:

$$G_{DS} = \beta(VDD - V_{IN} - V_T) \tag{2.32}$$

for an NMOS in linear region and strong inversion. To overcome these limitations and improve the linearity of the sampling circuit, gate bootstrapped circuit are often used for critical sampling switches [5–7, 80–83]. The main advantage of the gate bootstrapped switch is that its gate voltage tracks the input voltage, thus the conductance is:

$$\begin{aligned} G_{DS} &= \beta(VDD + V_{IN} - V_{IN} - V_T) \\ &= \beta(VDD - V_T) \end{aligned} \tag{2.33}$$

Fig 2.22 illustrated the relationship of the transconductance versus input voltage for both transmission gate and bootstrapped gate switches.

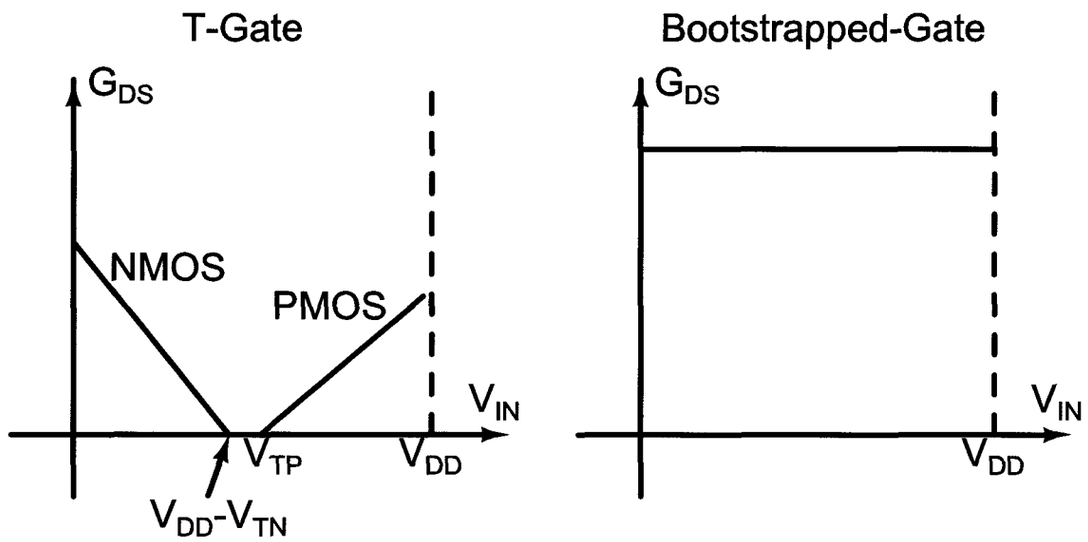

Figure 2.22: Transconductance versus input voltage for both transmission gate and bootstrapped gate switches.

A standard implementation of the gate bootstrapped switching circuit is shown in Fig 2.23 [81]. The input signal is applied at the source S of M_{11}. In steady stage, when $\overline{\phi}$ is high, the switch M_{11} is off and there is a voltage drop VDD over C_3; when ϕ is high, the switch M_8 is on and thus M_9 is also turned on. Consequently, the lower plate of C_3 sees the input voltage and the voltage at the top plate becomes VDD+Vin, because both M_3 and M_{12} are off in this phase. Thus the V_{GS} of M_{11} is equal to VDD. The main drawback of this circuit is that it requires two extra capacitors C_1 and C_2 to generate the boosted gate voltage for M_3. The transistor M_3 is controlled in such a way that it is turned off when M_{11} is conducting and on when M_{11} is off. It needs a boosted gate voltage because the drain and source

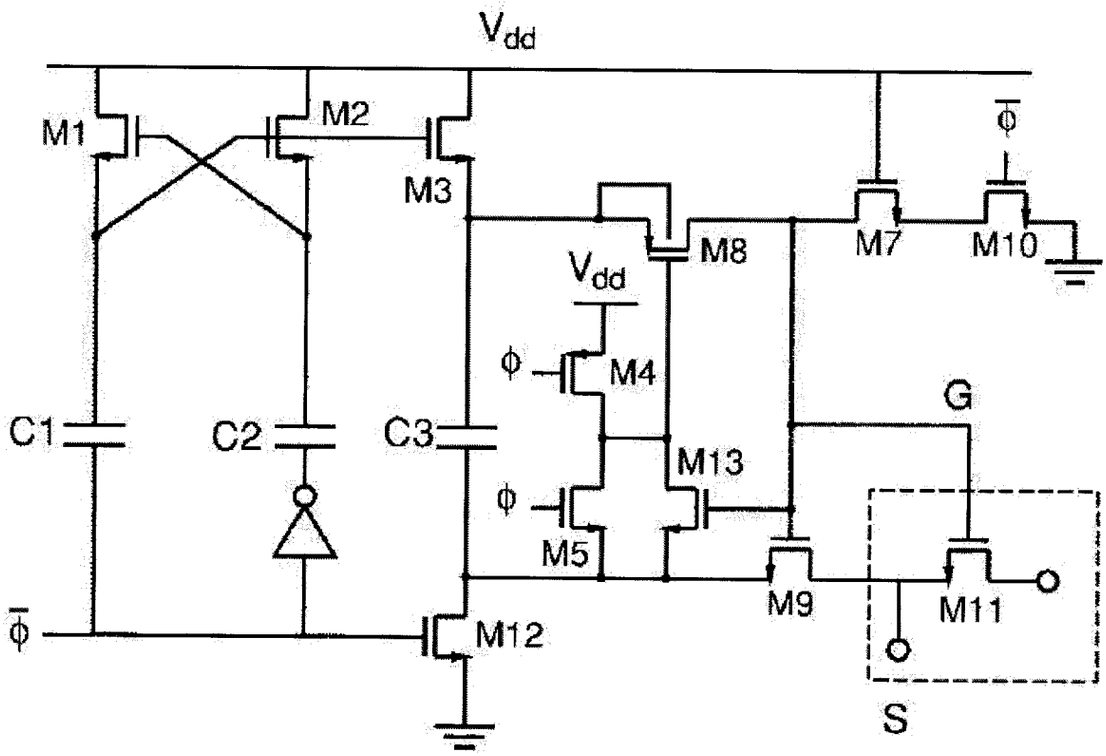

Figure 2.23: A standard implementation of the gate bootstrapped switching circuit [81].

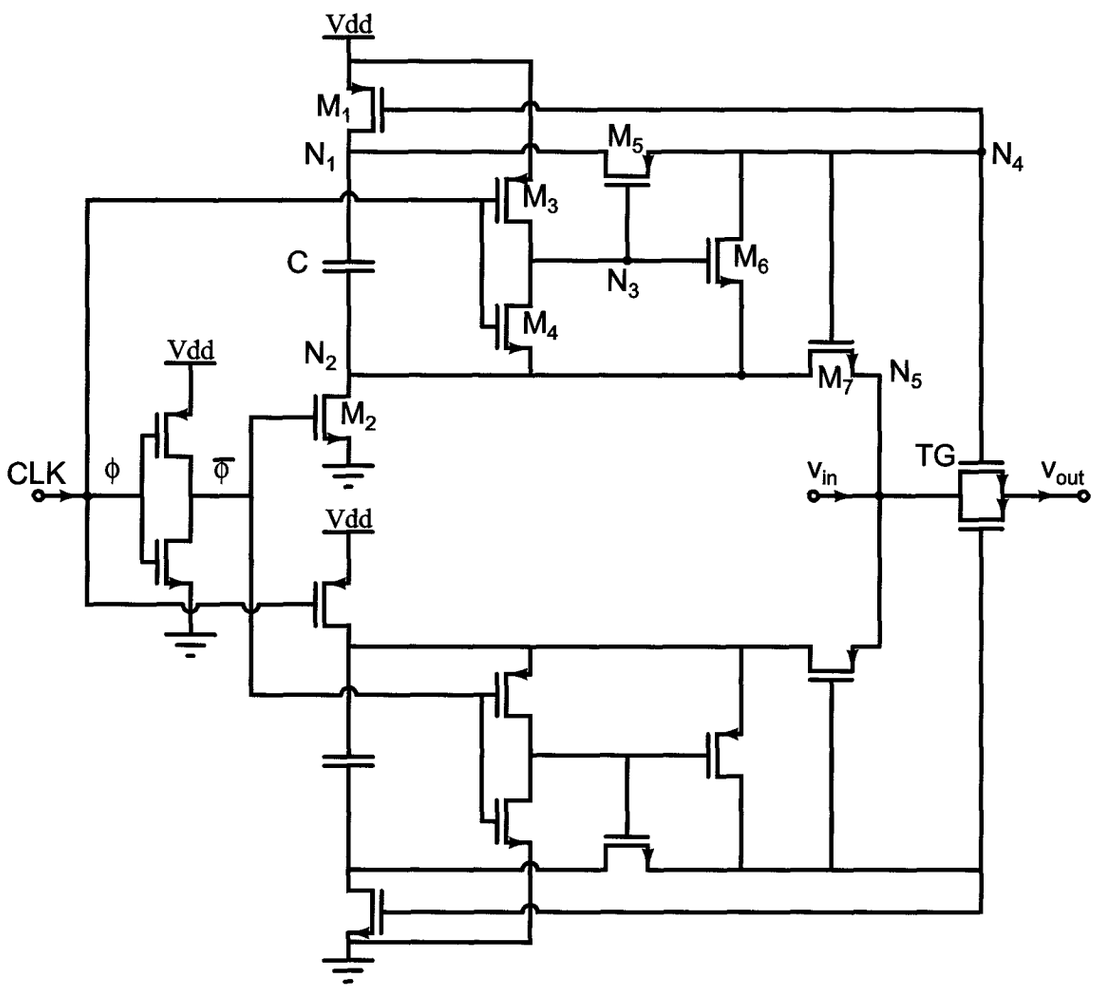

Figure 2.24: A modified version of the gate bootstrapped circuit, where two extra capacitors in [81] are avoided.

ϕ	ϕ̄	N_1	N_2	N_3	N_4	N_5
0	1	vdd	gnd	vdd	gnd	vin
1	0	vdd+vin	vin	vin	vdd+vin	vin

Figure 2.25: The operating sequence of the circuit in Fig. 2.24.

Table 2.4: SFDRs of two gate-bootstrapped sampling switches and a transmission gate sampling switch

Sampling transistor size	T-gate	Bootstrap [81]	Bootstrap modified
20μm/80nm	31dB	103dB	100dB
20μm/320nm	56dB	102dB	103dB

of M_3 is always equal to VDD or VDD+Vin. If we could replace the N-type M_3 with a PMOS transistor, its gate control voltage should be GND to turn it on and VDD+Vin to turn it off. Thus the gate voltage of the sampling switch M_{11} can be used for this purpose. Fig 2.24 shows the modified version of the bootstrapped switch circuit, a transmission gate is employed here to further reduce the input voltage dependency of the transconductance and achieve higher linearity[3]. Its operation principle is similar to the previous one and is briefly summarized in Fig 2.25. Note that for both of these two bootstrapped circuit, the voltage drop over any two terminals of a transistor is within VDD, given its source body are shorted for a triple well process.

Sampling switches at the input stage are critical to the overall performance of an ADC, they mainly cause signal distortion due to their input signal dependent transconductance and finite on resistance. In Table 2.4 we compare the spurious free dynamic range (SFDR) performance of the three sampling switches we discussed. The supply voltage is set to 0.5V. For all these three cases, the same transmission gate, with or without gate bootstrapping, is used as the sampling switch. The PMOS and NMOS in the T-gate are sized the same.

The simulation results show that both bootstrapped circuits achieve much better linear-

[3]A conceptually similar circuit was presented in [84]

ity than the T-gate alone sampling switch. When minimum gate length is used, the T-gate shows even worse SFDR due to larger transistor threshold voltage, while bootstrapped circuits are insensitive to the transistor gate length.

2.6 Summary

In this chapter, a 0.5V 8bit 10MS/s pipelined ADC using a 90nm standard CMOS technology has been presented. A cascaded sampling technique was introduced to combat the switch OFF leakage. The separate front-end SHA in conventional topologies has been eliminated by adding an auxiliary S/H circuit for the sub-ADC path to the pipeline stage topology and by synchronizing the sampling of the pipeline residue amplifier and sub-ADC. A 0.5V two-stage OTA with replica biasing and output current control has been designed. The design issues involving the system and the MDAC have also been investigated. Throughout the design, the V_T reduction thanks to the RSCE has been used to optimize the device sizing and operation and to enable high performance analog/mixed signal design for ultra-low supply voltages. The presented prototype has 8 identical stages and achieves a conversion efficiency of 1.15pJ/Conv. Step. If the stages of the pipelined ADC are progressively scaled, the efficiency of this pipelined ADC can be further improved to below 0.5pJ/Conv. Step. This prototype demonstrates that true low voltage pipelined ADCs operating from 0.5V are feasible in nano-scale CMOS technologies without resorting to special devices or voltage boosting techniques.

Furthermore, the sampling switch for an ADC, specifically the gate-bootstrapped switch circuit is investigated. This issue would be critical if a high resolution, high speed ADC is to be designed. Lastly, the settling of an OTA is also analyzed to see its implications at ultra-low-voltage operation.

Chapter 3

Current-Charge-Pump Ultra-Low-Power Pipelined ADC

3.1 Introduction

3.1.1 Challenges

With the development of wireless communication systems and the prevalence of portable wireless terminals, high energy efficient transceivers are becoming highly desirable for longer wireless terminal operating time. Pipelined ADCs are widely used in high speed communication systems for their high-speed and medium-resolution capability. In most literatures on pipelined ADCs, the switched-capacitor MDAC is used as the main building block for a pipelined stage [8]. It performs the digital to analog conversion, subtraction

and amplification all in one circuit block. High gain and high unity gain bandwidth OTAs are required in the MDACs to achieve accurate interstage gain in a feedback configuration [85]. The accurate gain comes at the cost of high power consumption. To alleviate this problem, several techniques have been introduced so far. Among them, digital calibration techniques move part of the analog design complexity to the digital domain, which ease analog design and reduces power consumption [24, 86, 87]. Correlated level shifting technique [22] significantly reduces the OTA gain requirement to make the analog design simpler. Recently, comparator based pipelined ADC [18, 19, 88, 89] was implemented to eliminate the power hungry OTA, thus substantially reducing the power consumption. The same goal is achieved by using dynamic residue amplifier [30], boosted charge transfer stage [29] and capacitive charge-pump [31]. While all these techniques reduce power consumption and improve on the operation efficiency of the pipelined ADC, the reference buffers for the MDAC, which are power hungry to generate low output impedance reference voltages to drive sampling capacitors, are still consuming a significant portion of the power budget [90–92]. Fig. 3.1 illustrates the rough power breakdown of a pipelined ADC [91, 93, 94].

3.1.2 Solutions

To address the issue of power hungry reference buffers, this work proposes a pipelined ADC stage architecture using current charge-pumps and comparators. By avoiding the use

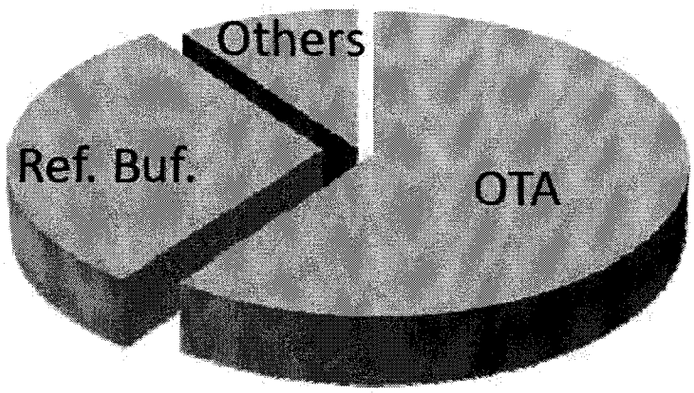

Figure 3.1: Power breakdown of a typical pipelined ADC, reference buffer consumes a significant portion of the total power.

of OTA for the interstage amplification and eliminating big buffers for the reference voltages, the proposed current-charge-pump pipelined ADC consumes much less power and thus achieves very high operation efficiency. Two versions of inverter based comparators are employed in the signal path and sub-ADC path. The design involves minimum analog circuitry and is highly digitized. It consumes 1.39mW for 100MS/s operation at 1V supply voltage. Measured peak SNDR and SFDR are 37.1dB and 46.7dB respectively, with a -1dBFS sinusoidal input at Nyquist frequency. Maximum DNL and INL are 1LSB/-0.8LSB and 2LSB/-2.3LSB, respectively. This concept-proving prototype achieves an FOM of 237fJ/Conv. Step while largely alleviating the requirement of reference voltage buffers. The core circuit occupies 0.044mm^2. The design was fabricated on a standard 90nm digital CMOS process.

3.1.3 Chapter Organization

The chapter is organized as follows, Section 3.2 and 3.3 review ultra-low-power pipelined ADC architectures and reference buffer designs, respectively. The system and block level designs are then presented in Section 3.4 and 3.5, where the current-charge-pump technique is introduced and building block designs are described. Following the prototype measurement results in Section 3.7, ideas for future improvement are presented in Section 3.8, including a fully differential version of the proposed charge-pump circuit and alternative MDACs for the pipelined ADC stage. Finally the chapter is briefly summarized in Section 3.9.

3.2 Review of Ultra-Low-Power Pipelined ADC Architectures

It has been one of the trends to replace the power hungry OTA in a traditional pipelined ADC stage with other power efficient circuitries. In this section, a brief review is given for the four representative OTA-less pipelined ADCs that were developed in the past few years.

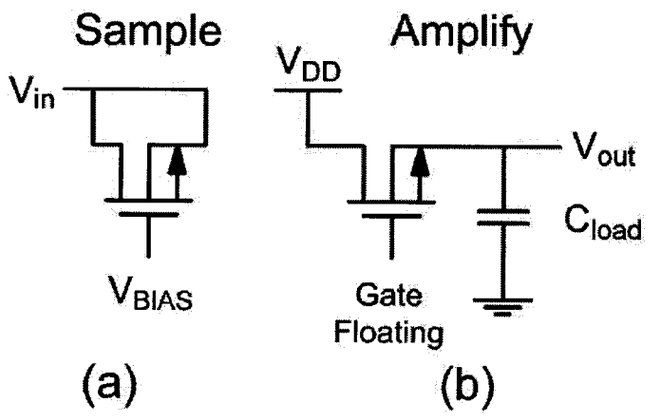

Figure 3.2: Basic operation of the dynamic source follower amplifier [30].

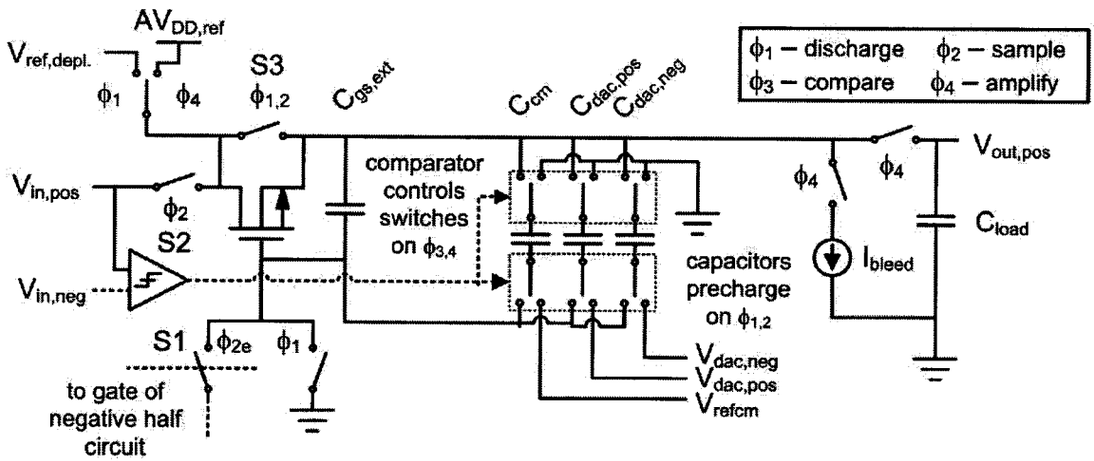

Figure 3.3: Half circuit pseudo differential stage implementation [30].

Pipelined ADC using dynamic source follower residue amplification [30]

This architecture is based on the dynamic source follower. Compared to the traditional OTA-based MDAC circuit, this design charges the load capacitor dynamically and thus saves considerable power. Fig. 3.2 shows the basic operation of the adopted dynamic source follower amplifier. During the sampling phase, the MOS transistor is biased in depletion region; during the amplifying phase, the transistor acts as a source follower and the output capacitor is being charged until V_{gs} approaches V_t. The charge redistribution from the uniquely configured sampling phase to the amplifying phase, together with the voltage dependent transistor parasitic capacitors, provides passive voltage gain. One of the drawbacks is that the gain achieved in this approach is not accurate, since it relies on the ratio of nonlinear transistor parasitic capacitors. Thus gain calibration is required to restore the performance. For the similar reason, the accuracy of the sampled signal is limited to around 8bit level under 1.2V supply. The half circuit pseudo differential stage implementation is shown in Fig. 3.3, where it shows how the reference voltages are precharged in the sampling phase and applied in the amplifying phase. A small I_{bleed} is introduced to avoid slow settling when the MOS transistor enters subthreshold region.

Pipelined ADC using comparator-based switched-capacitor circuits [18]

The main difference between the comparator based switched capacitor (CBSC) pipelined ADC and the traditional OTA based one is the way to take advantage of the virtual ground

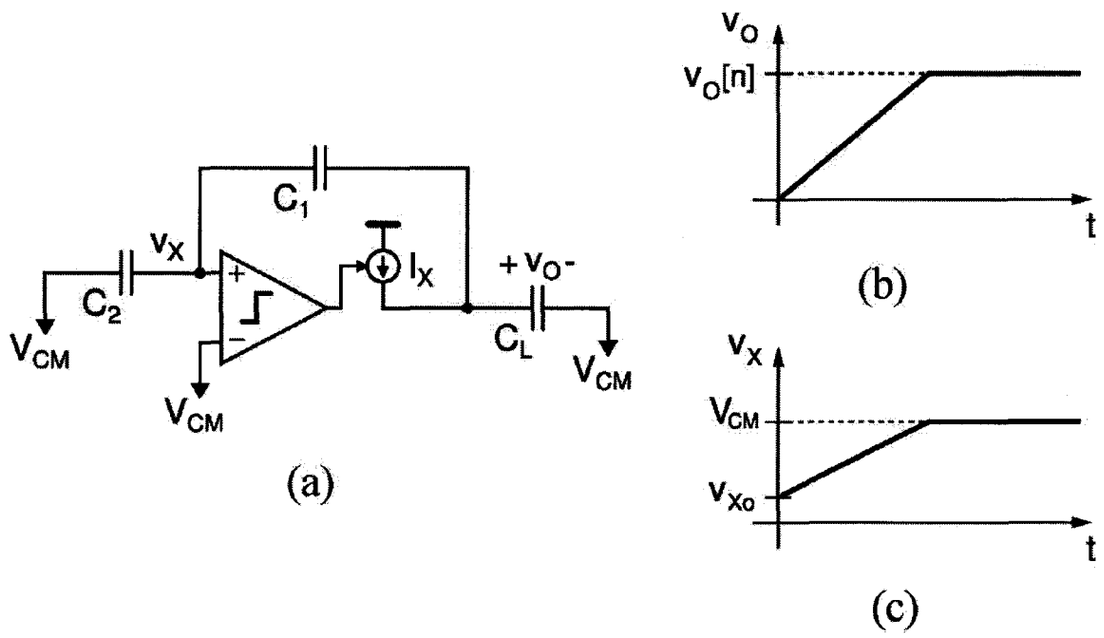

Figure 3.4: Comparator based switched capacitor circuit, a comparator and a current source is adopted to replace the OTA in a traditional implementation. Output voltage is obtained when the comparator virtual ground is detected and the comparator output toggles [18].

to realize a precision gain. The traditional OTA based switched capacitor circuit forces the input of the OTA to virtual ground in a feedback configuration, which requires a high gain and high GBW OTA. The CBSC circuit replaces the OTA with a comparator and a current source, which is shown in Fig. 3.4. Now, instead of forcing V_x to virtual ground, the comparator monitors the voltage V_x while the current source I_x is on, and turns off I_x when V_x crosses the virtual ground, when the output voltage V_o is finalized and held on C_L. Note that in this scheme, it operates as a class-B circuit where all the current from the current source goes to the load capacitors. Assuming the comparator has no delay, if we apply charge conservation rule at node V_x, we will get the exact same V_o as the OTA

based switched capacitor circuit. The CBSC technique can be applied to all the circuits that switched-capacitor loads are driven. One of the main downsides is that the finite delay of the comparator will cause output voltage overshoot, which requires a fine current source to correct the error.

In short, the CBSC based pipelined ADC reduces the design complexity and increases the power efficiency by replacing the OTA with a comparator and a current source.

Charge-domain pipeline ADC using bucket-brigade circuitry [29]

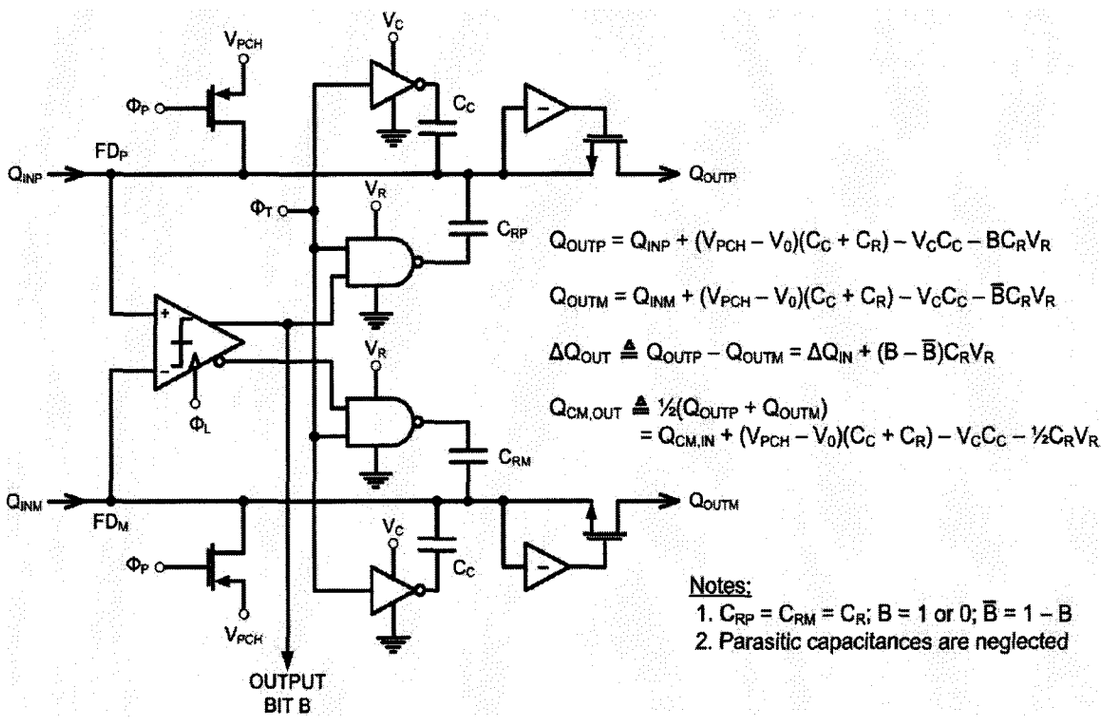

Figure 3.5: 1 bit charge domain pipelined ADC stage [29].

This pipelined ADC uses charge domain signal processing. The stage architecture of

the ADC is shown in Fig. 3.5. The advantage of this design is that charges are being reused efficiently, as charge packet drawn from the supply is passed from one stage to the next. Stage transfer function for differential charge is similar to the voltage transfer function of the traditional MDAC-based stage, but there is no charge gain. To achieve interstage voltage gain so that the offset requirement for the sub-ADC and the accuracy requirement for the later stages are relaxed, the capacitors of the following stage are scaled proportionally. To maintain the CM voltage for each stage, the CM charge needs to be reduced from stage to stage, which is controlled by a feedback loop in this design. The high performance of the pipelined ADC is also aided by the power-up calibration to adjust for various circuit parameters.

Pipelined ADC using capacitive charge-pumps [31]

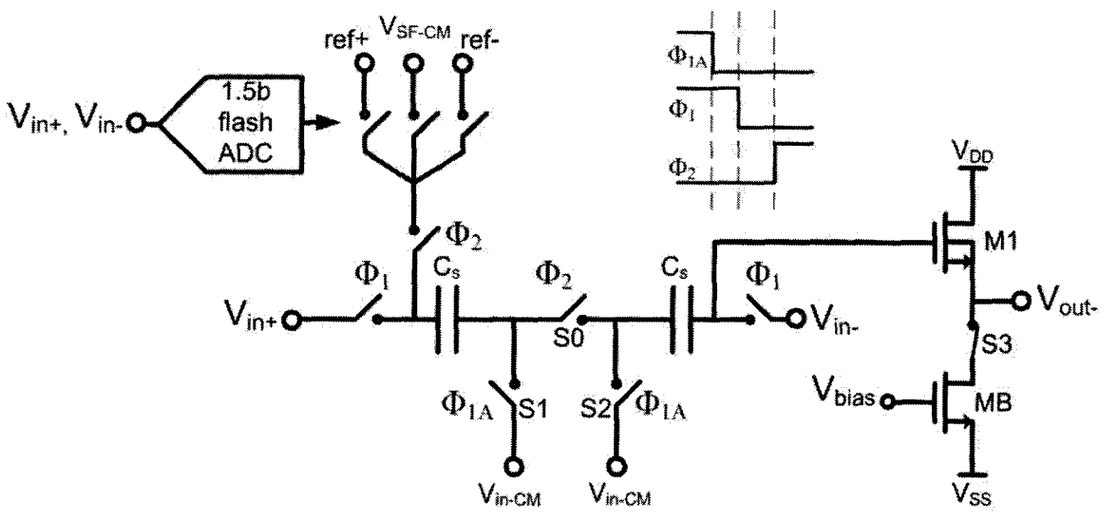

Figure 3.6: Capacitive charge-pump based pipelined ADC stage [31].

This architecture realizes the stage gain using capacitive charge-pumps, by sampling the input to two identical capacitors and then stacking them on each other, a gain of 2 is achieved. Fig. 3.6 shows the stage implementation with clock phases. Compared with the traditional OTA based approach, this approach breaks the trade off of gain and bandwidth requirements by using a separate wide-band source follower to drive the next stage. Significant power saving is thus achieved for this architecture. Another advantage of this approach is that the noise contribution from the source follower is attenuated by the preceding passive gain stage, again due to the decoupling of the circuit requirements of gain and bandwidth. The drawback of the circuit is that its gain is sensitive to the parasitic capacitors and the source follower linearity. The source follower limits the available stage output signal range too. Interstage gain calibration is also needed to compensate for the passive gain errors.

All of the above OTA-less pipelined ADCs presented new circuit techniques to avoid the use of power hungry signal-path OTAs, but they didn't address the power consumption associated with the reference voltage buffers.

3.3 Reference Buffer Design Review and Its Challenges

Before we move on to introduce our work that tackles the power consumption issue of both signal path OTAs and reference voltage buffers, we take a close look at the reference buffer designs for the pipelined ADC and their design challenges. This review on reference

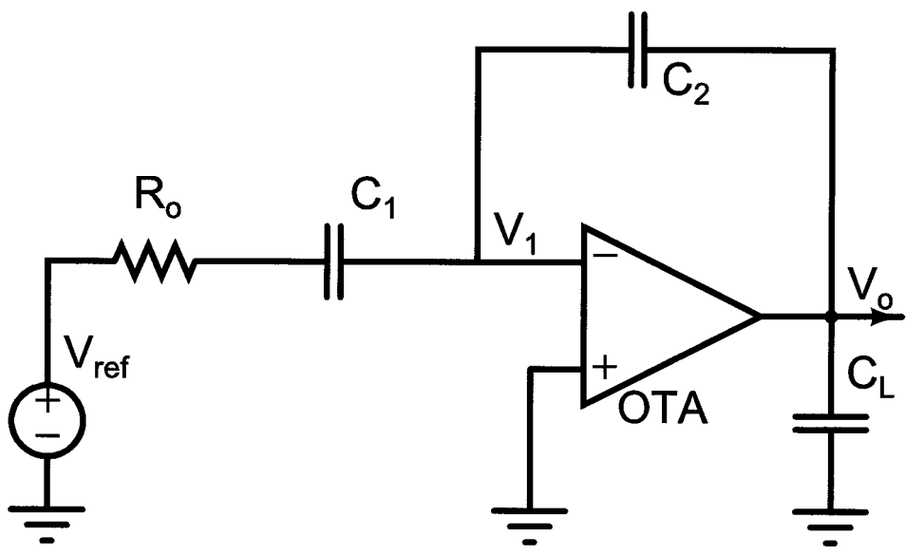

Figure 3.7: A standard MDAC in the amplifying phase, with the reference voltage connected to the sampling capacitor.

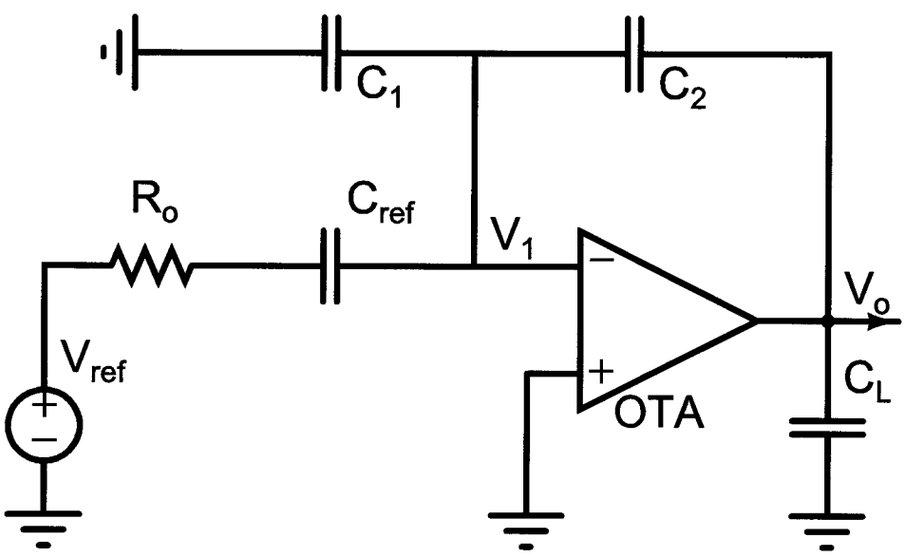

Figure 3.8: An MDAC with a dedicated reference capacitor C_{ref}, during the amplifying phase.

buffers is intended to provide part of the research background as they are not extensively discussed in literatures.

Reference voltage is one of the three inputs to a typical ADC, along with the signal input and the clock input. Similar to the input signal, the accuracy of the reference voltage directly affects the ADC resolution, as the input signal is referenced to the reference voltage. Fig. 3.7 shows a standard MDAC when it is in the amplifying phase. Based on the sub-ADC's decision, one of the reference voltages is selected and applied to the sampling capacitor C_1. As shown in the schematic, an ideal voltage source and a finite output resistance is used to model the reference voltage source. In order for the MDAC to settle to a desired accuracy level within half a clock period, the R_o of the reference voltage source need to be small enough. For example, at 10 bit resolution and 10MS/s, $7R_oC_1$ should be much smaller than 50ns, allowing time for the finite bandwidth OTA to settle. One alternative to this implementation is shown in Fig. 3.8, where a dedicated reference capacitor is introduced [95]. The difference is that, for the standard implementation in Fig. 3.7, sampling capacitor C_1 has different initial voltage when V_{ref} is applied due to the changing nature of the input signal in the sampling phase. But for the one in Fig. 3.8, the dedicated C_{ref} can be reset during the sampling phase, thus the initial voltage is always 0 when V_{ref} is applied. In that case, a weak reference buffer with a large R_o would only cause a fixed reference voltage settling error which can often be tolerated. The caveat in the description above is that it assumes the OTA is operating in small signal region and V_1 is always close to virtual ground during the entire amplifying phase. In a real scenario, V_1 will experience

large excursion when the sampling capacitor C_1 is switched to a fixed reference voltage at the beginning of the amplifying phase, and the OTA will go through nonlinear slewing before it settles linearly.

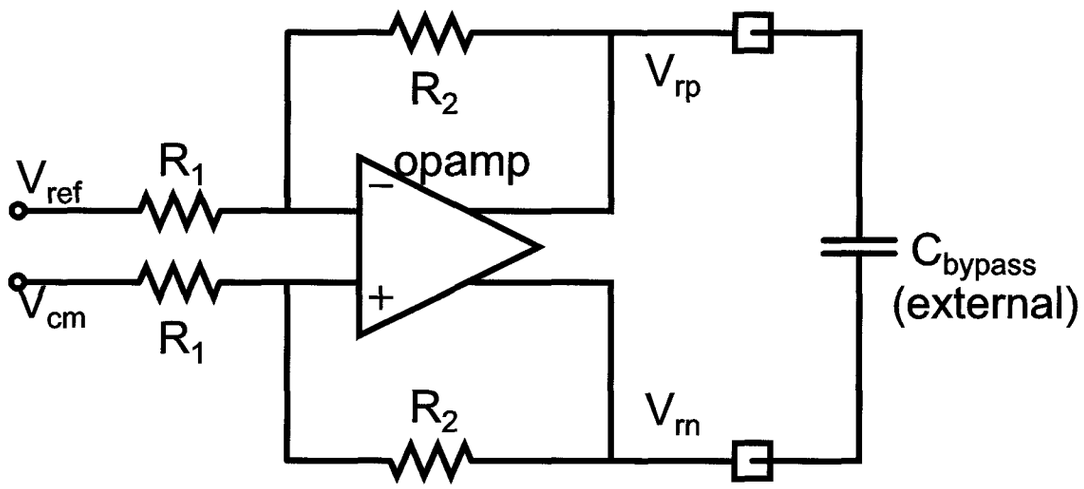

Figure 3.9: A fully differential opamp with resistive feedback to generate the positive and negative reference voltage.

There are in general two options to generate an accurate reference voltage that has sufficient drivability to drive the sampling capacitor in a pipelined ADC. One is to have a weak reference buffer but with a very big bypassing capacitor, which is often off chip. The other is to design a strong reference buffer that is capable of handling a specified dynamic capacitive load [95, 96]. In the case that a big bypassing capacitor is available, a relatively weak buffer can be conceptually implemented in several ways. Fig. 3.9 shows a fully differential opamp with resistive feedback to generate the positive and negative reference voltage [42, 97]. Here the opamp needs to be able to drive the resistive load and we need to watch out the extra pole at the opamp virtual ground nodes. Fig. 3.10

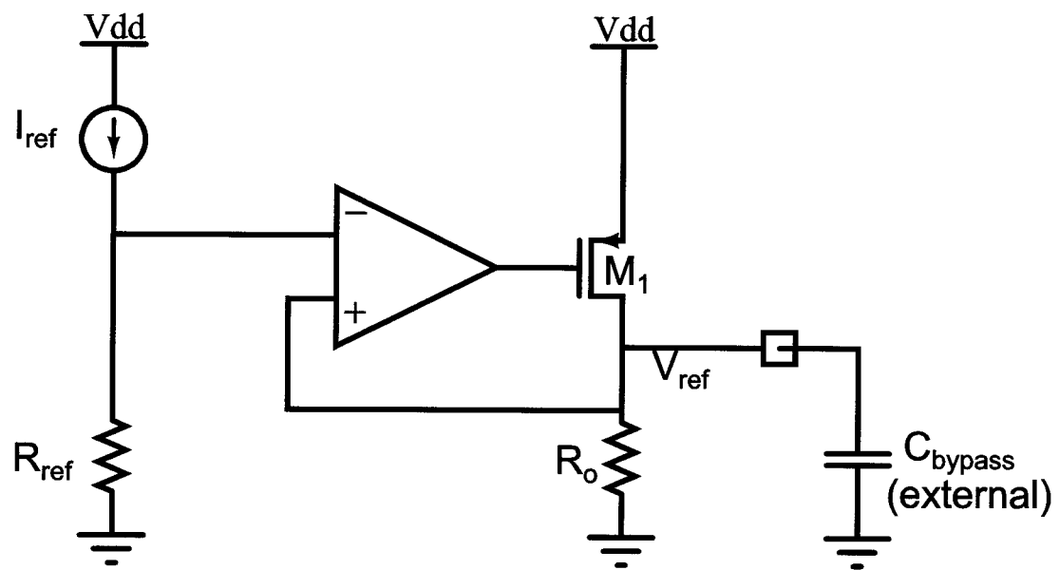

Figure 3.10: A reference buffer with the same form of a standard low dropout linear regulator.

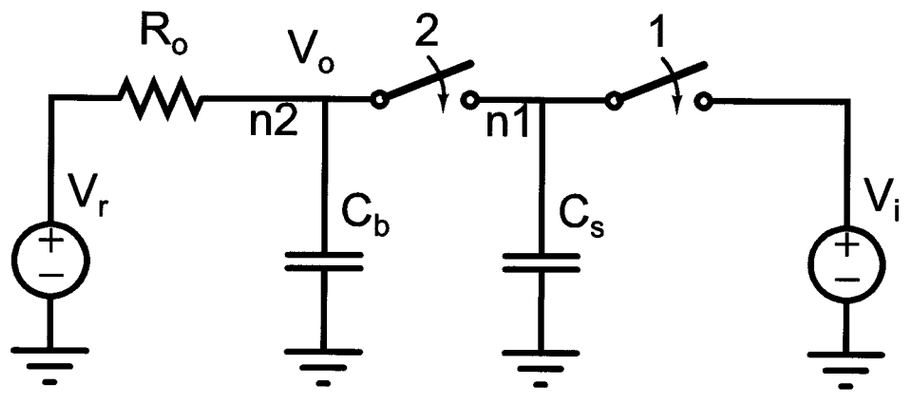

Figure 3.11: Model for the reference buffer driving the sampling capacitor in the MDAC, the buffer has a finite R_o and a bypass capacitor C_b is added. Phase 1 is the sampling phase and phase 2 is the amplifying phase.

shows another implementation of a possibly weak reference buffer [98]. It is similar to a low dropout linear regulator, the only difference is that it does not need to drive the entire circuit as the power supply does. A common source output stage is used to allow for closer to V_{DD} reference voltage V_r but it has limited slew rate given a quiescent current level, and the PSRR is also worse than a source follower output stage. Intuitively, it seems that as long as we have a big reservoir capacitor stabilizing the reference output of a weak buffer, the capacitive load from the MDAC can always take charges from the reservoir while the voltage on the reservoir capacitor is set by the weak buffer. But this is not the real case, Fig. 3.11 illustrates the scenario, where C_b is the bypass capacitor and C_s is the sampling capacitor in an MDAC. If V_i is a fixed DC voltage, then during phase 1, it will take away charges from or provide charges to the sampling capacitor C_s, depending on whether V_i is smaller or larger than V_r. Let's assume V_i is smaller than V_r and R_o is big for a weak buffer, even though the big reservoir capacitor C_b can provide charge that C_s lost during the sampling phase, C_b will eventually be drained without enough fresh charge from the reference buffer. So as long as there is a net charge change on C_s, ultimately the charge has to be compensated by the infinite charge reservoir–the reference buffer. If we treat the switch-C_s-switch circuit as an equivalent resistor R_{eq}, which is equal to T/C_s, then we can get the average voltage at node n2. The sampled reference voltage we are concerned about is at node n1 at the end of phase 2, or the amplifying phase in the MDAC. To calculate its value, we have the following three equations in the charge domain,

Total charge on C_b and C_s at the end of phase 2, time $(n-1)T$:

$$Q_1 = (C_b + C_s)V_o(n-1) \tag{3.1}$$

Total charge on C_b and C_s at the end of phase 1, time $(n-1/2)T$:

$$Q_2 = C_s V_i(n-1/2) + C_b V_o(n-1/2) \tag{3.2}$$

Total charge on C_b and C_s at the end of phase 2, time nT:

$$Q_3 = (C_b + C_s)V_o(n) \tag{3.3}$$

Here we assume the switches are ideal, therefore at phase 2, the voltage on the sampling capacitor C_s is equal to V_o. Since there is a reference voltage source connected to C_b, we cannot apply the charge conservation rule directly. Instead, we need to factor in the extra charges from $(n-1)T$ to nT,

Extra charges from $(n-1)T$ to $(n-1/2)T$,

For C_s, V_i takes charge away during this half period:

$$\Delta Q_{Cs1} = (V_i(n-1/2) - V_o(n-1))C_s \tag{3.4}$$

For C_b, reference buffer charges onto it:

$$\begin{aligned}\Delta Q_{Cb1} &= \int_0^{T/2} I_{R_o}\, dt \\ &= \int_0^{T/2} (V_r - V_o(n-1))e^{-t/\tau_1}\, dt \\ &= C_b(V_r - V_o(n-1))(1 - e^{-T/(2R_oC_b)}) \end{aligned} \tag{3.5}$$

Extra charges from $(n - 1/2)T$ to nT,

For C_b and C_s, reference buffer charges onto both of them:

$$\begin{aligned}\Delta Q_{Cbs2} &= \int_0^{T/2} I_{R_o}\, dt \\ &= \int_0^{T/2} (V_r - V_{ini})e^{-t/\tau_2}\, dt \\ &= (C_b + C_s)(V_r - V_{ini})(1 - e^{-T/(2R_o(C_b+C_s))}) \end{aligned} \tag{3.6}$$

where V_{ini} is the initial voltage at the beginning of phase 2, time $(n-1/2)T$, from (3.1), (3.4) and (3.5), we get:

$$\begin{aligned}V_{ini} &= \frac{(C_s + C_b)V_o(n-1) + \Delta Q_{Cs1} + \Delta Q_{Cb1}}{C_s + C_b} \\ &= \frac{C_sV_i(n - 1/2) + C_bV_r + C_be^{-T/(2R_oC_b)}(V_o(n-1) - V_r)}{C_s + C_b} \end{aligned} \tag{3.7}$$

since the total charges on C_b and C_s at the end of phase 2 and time nT is equal to the total charges on C_b and C_s at the end of phase 2 and time $(n-1)T$, plus all the extra charges

from sources V_i and V_r over that period, then from (3.1), (3.3)– (3.6), we arrive at:

$$\begin{aligned}(C_b + C_s)V_o(n) &= (C_b + C_s)V_o(n-1) + \Delta Q_{Cs1} + \Delta Q_{Cb1} + \Delta Q_{Cbs2} \\ &= (C_b + C_s)V_o(n-1) + (V_i(n-1/2) - V_o(n-1))C_s \\ &\quad + C_b(V_r - V_o(n-1))(1 - e^{-T/(2R_oC_b)}) \\ &\quad + (C_b + C_s)(V_r - V_{ini})(1 - e^{-T/(2R_o(C_b+C_s))}) \end{aligned} \tag{3.8}$$

after plugging in (3.7) and rearranging:

$$\begin{aligned}&(C_b + C_s)V_o(n) - C_bk_1k_2V_o(n-1) \\ &= C_sk_2V_i(n-1/2) + (C_b + C_s - C_sk_2 - C_bk_1k_2)V_r \end{aligned} \tag{3.9}$$

where

$$k_1 = e^{-T/(2R_oC_b)} \tag{3.10}$$

$$k_2 = e^{-T/(2R_o(C_b+C_s))} \tag{3.11}$$

To arrive at the V_o here, we could also use superposition where V_i and V_r are applied separately. From (3.9) we can perform Z-transform:

$$V_o(z) = \frac{C_sk_2V_i(z)z^{-1/2} + (C_b + C_s - C_sk_2 - C_bk_1k_2)V_r(z)}{(C_b + C_s) - C_bk_1k_2z^{-1}} \tag{3.12}$$

where V_r is a DC. When V_i is also a DC, in steady state, V_o is a scaled constant voltage. Its value at the end of phase 2 is given by:

$$V_o = \frac{C_s k_2 V_i + (C_b + C_s - C_s k_2 - C_b k_1 k_2) V_r}{(C_b + C_s) - C_b k_1 k_2} \tag{3.13}$$

(3.13) tells that, once all the values of passive components R and C are given and the sampling frequency is fixed, V_o at the end of phase 2 is also a known DC value. But in a real scenario where C_s of the MDAC samples the changing input signal V_i, V_o is a scaled version of V_i centering on a DC value (3.12). This would effectively cause pipelined ADC interstage gain error. Even worse, the gain error is also a function of the input signal frequency, as reflected in (3.12). Intuitively, from V_i to V_o, there is a low pass filter formed by the equivalent resistor of switched C_s and C_b. Even though we can afford a big off-chip bypass capacitor C_b, at low input frequency, the output voltage V_o won't be stabilized. In some wideband communication systems where low frequency band is not used to avoid DC offset and $1/f$ noise, the option of weak reference buffer with big bypass capacitor may be adopted; In systems where the ADC is only operating for a short period of time periodically, the voltage on the big bypass capacitor might never drop below $V_r - 1/2V_{LSB}$, then the weak buffer is also an option provided it can replenish the bypass capacitor when the ADC is not operating.

A big bypass capacitor can often be used to stabilize the reference voltage, rather than allowing for a weak buffer. In this way, the bypass capacitor provides fast dynamic current

when the sampling capacitor from the MDAC is connected to the reference buffer, thus avoiding sudden voltage change at the reference output. It also makes the reference line more immune to noise coupling from substrate and power supply lines. We need to be aware that proper damping techniques should be adopted to avoid ringing on the reference line, especially when the bypass capacitor is offchip and a high Q bonding wire is present. Furthermore, we should be aware that some type of reference buffers are not designed for big capacitive load, which might cause stability problem.

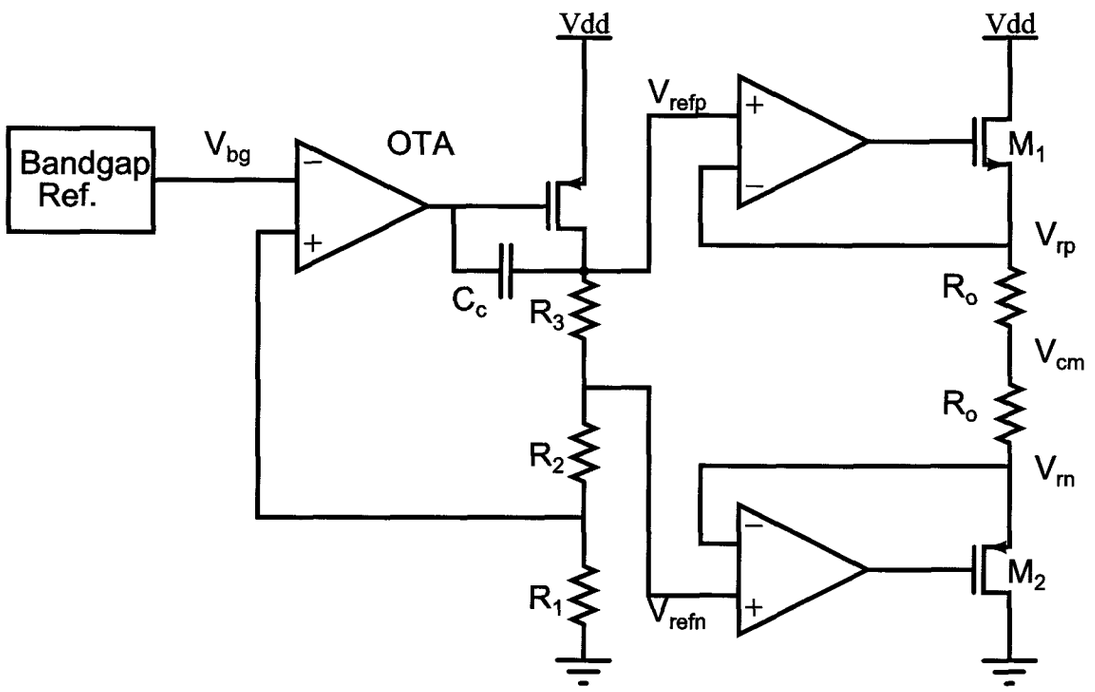

Figure 3.12: A reference buffer with source follower output stage.

The second option in generating a stable reference voltage is to design a strong reference buffer. In cases where a big bypassing capacitor is also a choice, this second option basically trades power with area. There are many different ways of implementing

a strong reference buffer [93, 94, 99–105] including the reference buffers mentioned before [42, 97, 98], as long as more current is pumped into the circuit. In general, in order to improve the power efficiency, a source follower output stage is preferred over a common source output stage. Fig. 3.12 shows a common implementation where a source follower stage is used. Here the bandgap generates the reference voltage and then the desired reference voltages V_{refp} and V_{refn} are produced through a slow unity gain follower with resistive divider at the output stage. The buffer stage is also configured as a unity gain follower, but it is faster and the output stage is a much stronger source follower. The output stage is shared for positive and negative reference drivers for higher power efficiency. Typically the positive reference voltage is the highest voltage potential in the signal range and the negative one is the lowest. So when the sampling capacitor is connected to V_{rp}, its value will drop momentarily. This lowers the output impedance of transistor M_1 which leads to a fast recovery. From another perspective, the slew rate of the output stage is not limited. To understand intuitively how the two interconnected reference drivers for V_{rp} and V_{rn} work, we could also think of one of them as a regulated load for the other one. Another popular implementation of the strong reference buffer is shown in Fig. 3.13, where the generation and the driving stage of the differential reference voltages are realized in one opamp circuit. Here the output common mode is set in a feedback loop to make sure the two reference voltages are centered around the middle of the power supply. Again source follower stages are used to provide high driving capability. For the two reference buffers described above, an improved design would be to use an open loop source follower stage as

the driver while only a replica driver stage is in the feedback loop [100,101,104]. Fig. 3.14 illustrates this approach. By isolating the driver stage from the feedback loop, it prevents the signal dependent current from the MDAC from injecting into the loop, which would otherwise cause slow settling [104]. For all the reference buffers with source follower output stage, one drawback is that it presents wideband noise which would be folded back to signal band once they are sampled onto the sampling capacitor. A low pass filtering capacitor should be added at the output to limit the noise bandwidth as long as stability is not affected. Otherwise the wide band noise would become a concern when designing a high resolution ADC.

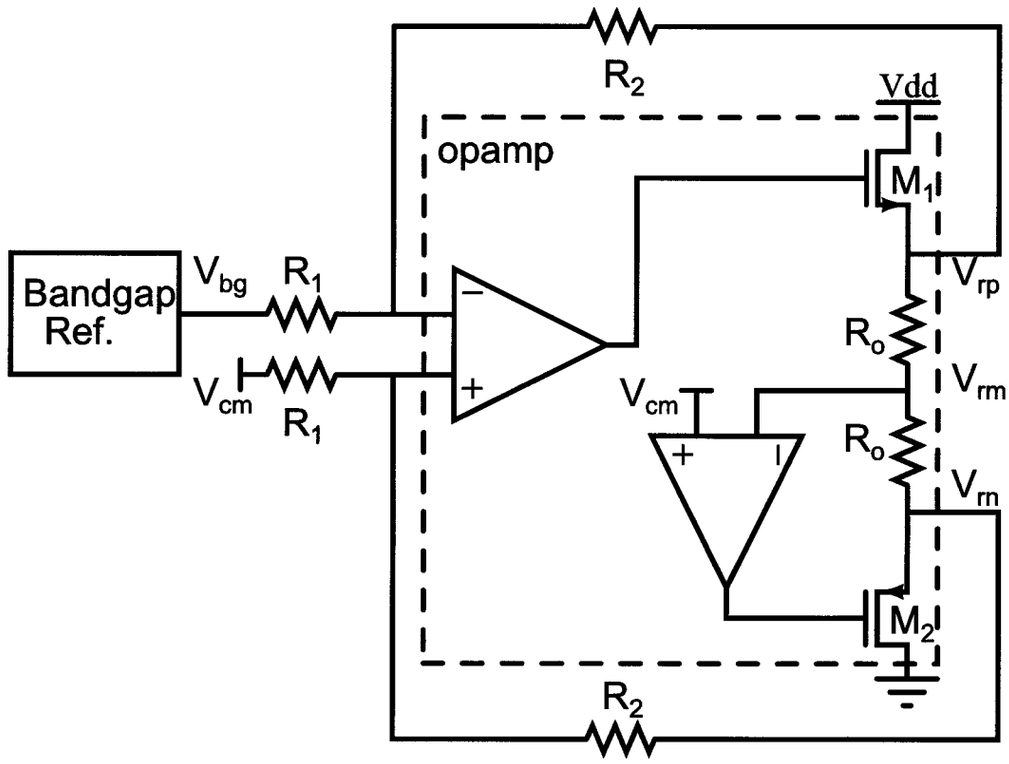

Figure 3.13: A reference buffer using resistive feedback and source follower output stage.

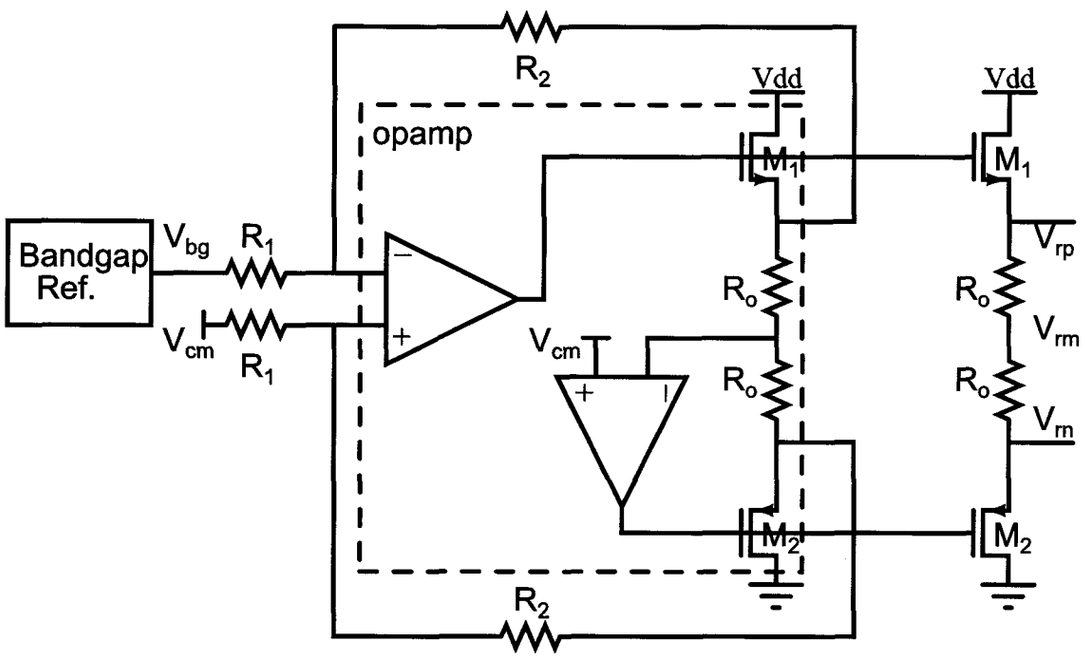

Figure 3.14: A reference buffer with open loop source follower driving stage.

As we mentioned earlier, the reference buffer consumes a significant portion of the pipelined ADC power consumption. To illustrate this, we consider a typical switched capacitor MDAC in a 1.5bit pipeline stage (refer to Fig: 2.3) and the reference buffer shown in Fig: 3.9. The power consumption of the residue OTA is mainly determined by its load capacitance and the open loop gain requirement, assuming noise is dominated by the sampling kT/C noise. The power consumption of the reference buffer is mainly a function of its load capacitance, the open loop gain requirement is relaxed as it only introduces fixed reference voltage error. Therefore, smaller transistor channel length is allowed and g_m/I can be increased without sacrificing operation speed. As an example, we assume the load capacitor of the residue OTA is 1.5 times that of the reference buffer, which implies the

capacitor in the succeeding stage is scaled by half, and g_m/I of the reference buffer is assumed to be 2 times that of the residue OTA, we can see that the power consumption of the reference buffer will be roughly 1/3 that of the residue OTA.

3.4 Current-Charge-Pump Pipelined ADC System Design

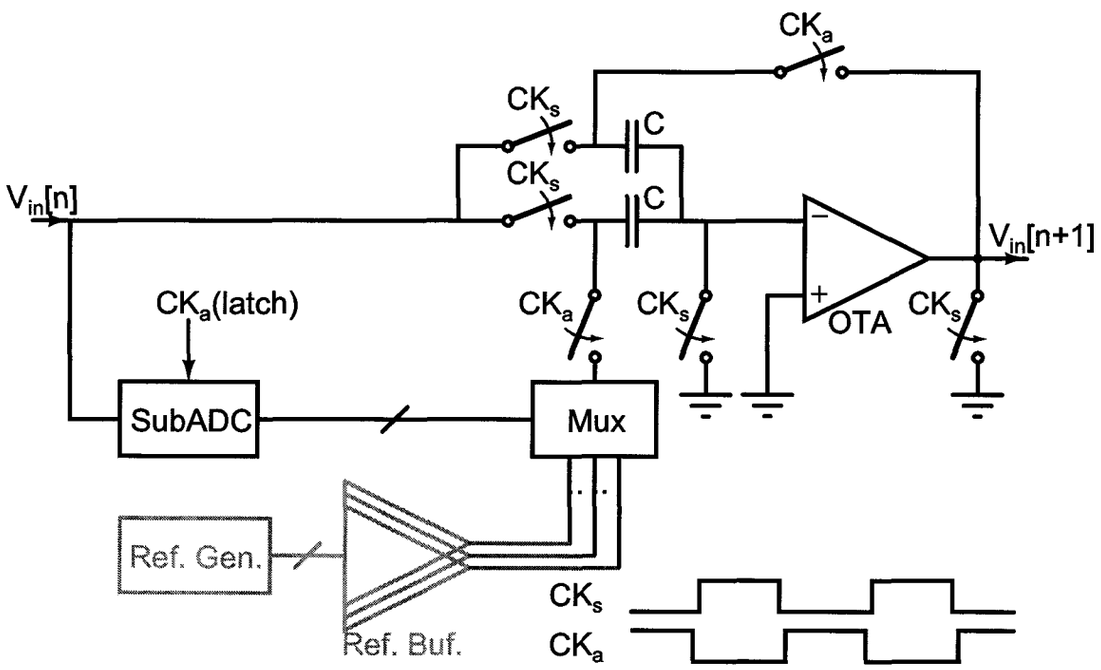

Figure 3.15: Standard stage implementation of a pipelined ADC. High performance OTA and reference buffer are used to achieve high accuracy, but at the cost of high power consumption.

To achieve ultra-low power consumption of a pipelined ADC, we need to look at its most power hungry building blocks. Fig. 3.15 shows the standard stage implementation of a pipelined ADC. The OTA for residue amplification and OTA based reference buffer

consume most of the power, since both need to drive the sampling capacitor to a required accuracy level. The linear settling of a class A OTA is not efficient in terms of delivering the current to the load capacitor [106, 107], the majority of the current circles through the OTA itself while charging or discharging the load capacitor. Furthermore, in the standard implementation of a pipelined ADC, the OTA is idle during the sampling phase, which results in wasted static power.

If we further examine the standard stage implementation from a higher level of abstraction, we see that it essentially performs two functions, producing stage output bits and amplifying residue signal to pass to the next stage. To produce the digital output, a flash sub-ADC that comprises dynamic comparators is usually used. This part mainly consumes small dynamic power and the power consumption is largely determined by speed and offset requirement. For the residue amplification, it realizes the following function in the case of a 1.5 bit/stage implementation:

$$V_o = 2V_{in} - V_{DAC} \tag{3.14}$$

where V_{DAC} is a reference voltage determined by the sub-ADC digital output. The accurate gain of 2 is achieved by capacitor matching and a high gain, high gain-bandwidth OTA in the feedback configuration. A reference buffer is employed to charge or discharge the sampling capacitor to a desired voltage during stage amplifying phase.

In order to avoid using the power hungry building blocks while realizing the stage trans-

fer function in equation (3.14), a current-charge-pump circuit is proposed and described in the following sub-section.

3.4.1 Current-Charge-Pump Residue Amplification

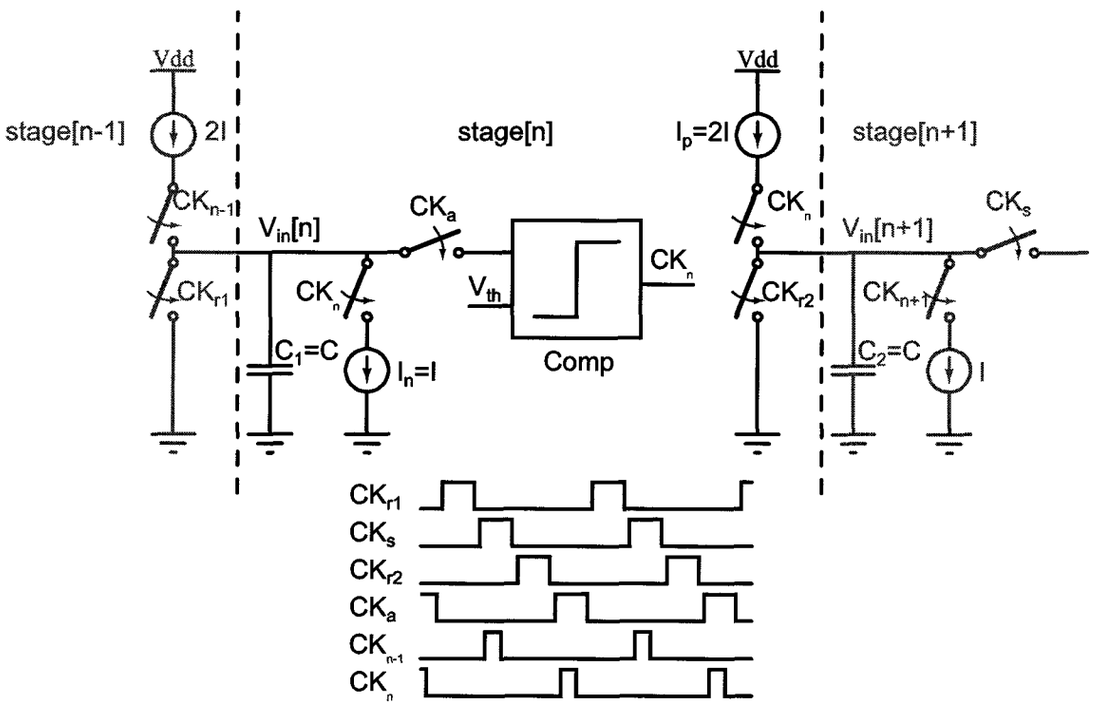

Figure 3.16: Proposed current-charge-pump residue amplifying circuit for a pipelined ADC stage.

Fig. 3.16 shows the current-charge-pump residue amplifying circuit for a pipelined ADC stage, where a 1.5bit stage is assumed for an interstage gain of 2. The circuit is comprised of current-charge-pumps and a comparator. To achieve the gain of 2, the charging current source I_p is twice as large as the discharging current source I_n, while both capacitors C_1 and C_2 are identical. The comparator output controls the switches of both

current sources I_n and I_p to turn on and off at the same time. When the current source is on, voltage change over the capacitor that is being charged or discharged is given by:

$$\Delta V = \frac{I}{C}\Delta t \tag{3.15}$$

Since the charging rate of the current charge-pump I_p-C_2 is twice of the discharging rate of I_n-C_1, a gain of 2 is achieved by synchronizing both current charge-pumps.

To understand better how the circuit works, we can look at the sequential operation at each clock phases. At phase CK_{r1}, capacitor C_1 is being reset; At phase CK_s when CK_{n-1} is high, the capacitor C_1 is being charged to a certain input voltage $V_{in}[n]$ for stage[n]; At phase CK_{r2}, the capacitor C_2 is being reset and stage[n] input voltage on C_1 is being held; When CK_a becomes high, input of stage[n] is connected to the input of the comparator, and the comparator output CK_n becomes high. Then I_p and I_n start charging C_2 and discharging C_1 respectively. Once the voltage on C_1 crosses the comparator threshold voltage V_{th}, the comparator output CK_n toggles and both current sources are turned off. Now the voltage on C_2 is held at:

$$\begin{aligned} V_{in}[n+1] &= 2\frac{I}{C}\Delta t \\ &= 2(V_{in}[n] - V_{th}) \end{aligned} \tag{3.16}$$

Thus it amplifies the input voltage by a factor of 2. If we further set V_{th} to $V_{DAC}/2$, namely

applying the reference voltage at the input of the comparator, the circuit in Fig. 3.16 realizes the function of residue amplification as described in equation (3.14).

The proposed circuit performs the multiply-by-2 operation using current charge-pumps and a comparator, thus reduces design complexity originally involved in the signal-path OTA, and there is no stability issue involved in this open loop architecture. The current sources operate in principle as class B circuit, where there is no static biasing current and all the current is delivered to the load capacitor. More importantly, now the reference voltage is applied to the comparator input instead of driving one of the input sampling capacitors shown in Fig. 3.15. Effectively, the big reference buffer in Fig. 3.15 which drives the sampling capacitor can be removed. Only a small reference buffer that can drive the input parasitic capacitor of the comparator is required. The proposed design thus achieves significant power saving over the conventional residue amplification circuit.

To design a pipelined ADC based on the current-charge-pump circuit, some potential design issues that come with this architecture need to be addressed. First, the gain accuracy is a concern. Since the design is an open loop circuit, the interstage gain relies entirely on the matching of the current sources and the capacitors. The static gain error can be calibrated out using standard bootstrapping gain calibration technique [23, 108]. The nonlinearity of the current source is kept at minimum for the targeted 8bit resolution by using cascoded current sources and avoiding pushing the transistors into linear region. To achieve higher resolution, current compensation technique can be employed by sensing the output voltage of the current source and controlling the body or a fraction of the gate of the current

source transistor[1]. Secondly, the comparator has a finite delay. When the input of the comparator crosses its threshold voltage while discharging, the comparator output CK_n will not toggle immediately, thus causing output voltage overshoot. This can be referred back as input signal offset as long as the overshoot is constant. The overshoot voltage is a function of I, C and comparator delay time t_d. It is a constant value to the first order because the sampling capacitor value is fixed, the current is linear for the target performance, and the comparator delay is constant as it sees the same slope of its input signal. Simulation results of different corners show the gain linearity at around 55dB.

Other than the nonidealities from the current source and comparator, the switches contribute charge injection and also present some nonlinear parasitic capacitor. To minimize the undesired effects, small transmission gates are employed and dummies are used where appropriate.

3.4.2 Current-Charge-Pump Pipelined ADC Stage

A simplified pipelined ADC stage employing current-charge-pump MDAC is illustrated in Fig. 3.17. To prove the concept of the current-charge-pump pipelined ADC, a single-ended version with 1.5bit/stage is implemented in this prototype. A separate scaled current-charge-pump is used for the sub-ADC path to protect $V_{in}[n]$ from any kickback noise from the sub-ADC. The sub-ADC is latched during the clock phase CK_{r2}, so that V_r is ready for the amplifying phase CK_a. To avoid the transient of turning on and off a current source,

[1]The current compensation technique is not implemented in this prototype

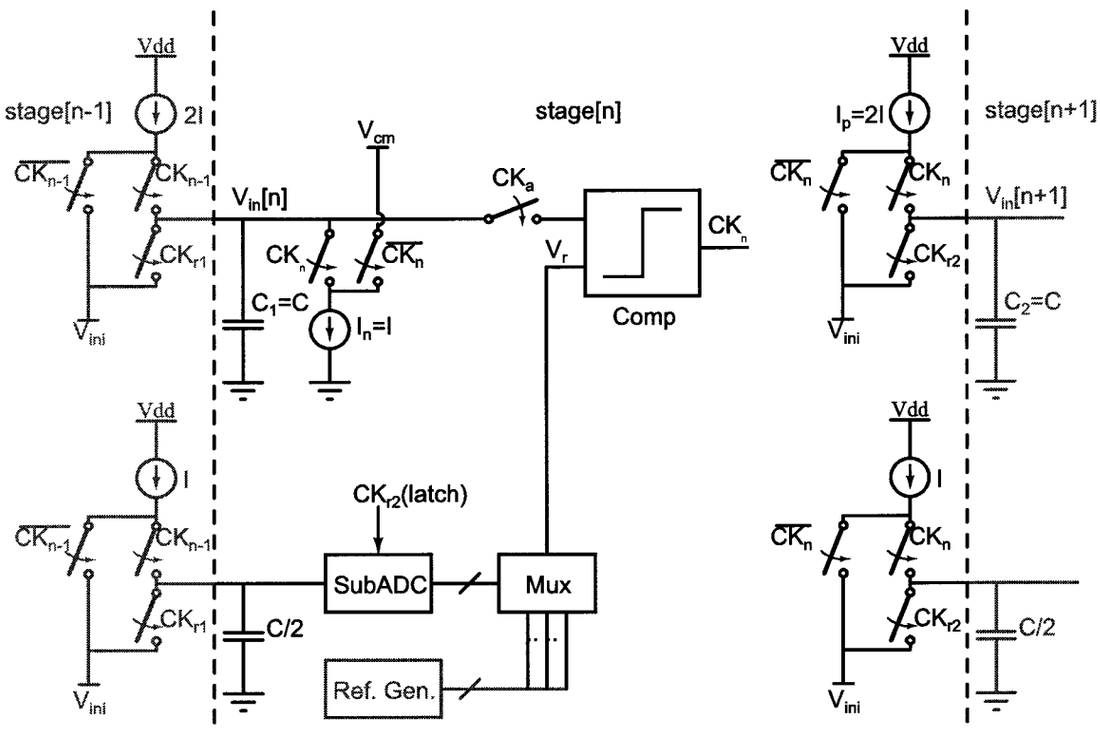

Figure 3.17: Simplified diagram of the proposed pipelined ADC stage.

the current source is switched away to another path when it is not charging or discharging a sampling capacitor, which comes at a cost of static biasing current consumption. Notice that I_n is switched out to V_{cm} while I_p is switched to V_{ini}. V_{cm} is chosen to be $V_{DD}/2$ here, but other values are also fine and it only needs to provide current I to accommodate the current source I_n. V_{ini} has two purposes here, one is to sink current 2I from current source I_p, the other is to reset the sampling capacitor to an initial start voltage V_{ini}. To understand its operation, the 1.5bit stage's input-output transfer curve is shown in Fig. 3.18. The signal range for this ADC is set to 350mV-750mV. For each section of the transfer curve, $V_{in}[n+1]$ is a linear function of its input $V_{in}[n]$. After rearranging, their relationship can

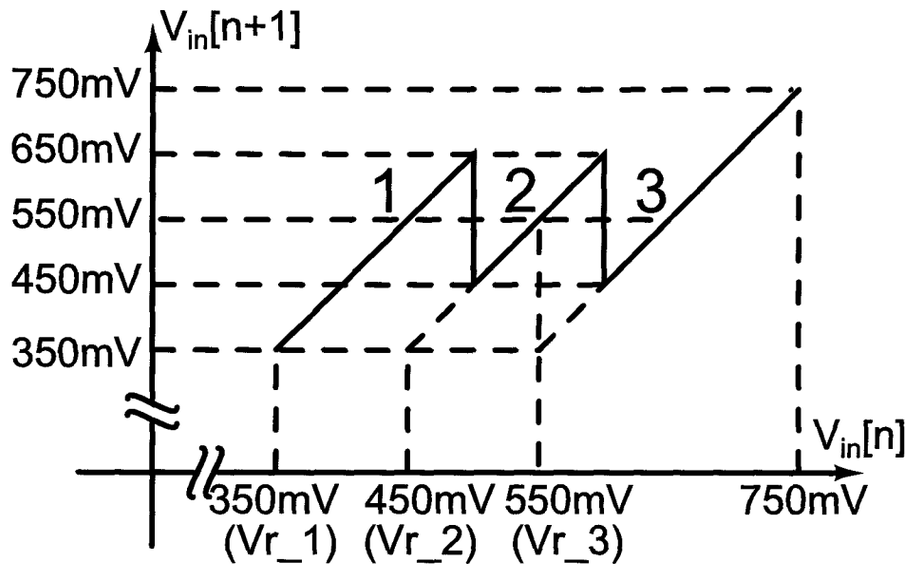

Figure 3.18: Input-output transfer curve for an 1.5bit stage, reference voltage for each section 1, 2, 3 is 350mV, 450mV and 550mV respectively.

be expressed in the following three equations:

$$V_{in}[n+1] = 2(V_{in}[n] - 350m) + 350m \quad \text{For } V_{in}[n] \text{ in section 1} \tag{3.17}$$

$$V_{in}[n+1] = 2(V_{in}[n] - 450m) + 350m \quad \text{For } V_{in}[n] \text{ in section 2} \tag{3.18}$$

$$V_{in}[n+1] = 2(V_{in}[n] - 550m) + 350m \quad \text{For } V_{in}[n] \text{ in section 3} \tag{3.19}$$

Thus the start voltage V_{ini} is set to 350mV and reference voltages for three sections are set to 350mV, 450mV and 550mV respectively, as indicated in Fig. 3.18. In practice, V_{ini} is set a little bit lower to accommodate for the overshoot due to finite comparator delay. Reasonable voltage deviation from nominal V_{ini} can be tolerated, as it is referred back as input offset. On the other hand, the initial voltage on the capacitor C_1 before the reset phase

CK_{r1} is $V_r - V_{ov}$, where V_{ov} is the input side overshoot voltage due to finite comparator delay during the amplifying phase CK_a. Since V_r can be any of the three reference voltages, an appropriate voltage buffer might be needed for V_{ini} to make sure the reset voltage on C_1 is consistent for all three scenarios. Alternatively, to save power, a weaker buffer can be used in combination with settling error compensation given that the error only depends on the known initial value on C_1. For the ease of implementation and testability, we used external voltage source for V_{ini} in this work.

The size of the sampling capacitor C_1 is set to 100fF to meet the kT/C noise requirement, it is also big enough that the parasitic capacitor will not noticeably affect the performance. Once the capacitance is known, the current of the charge-pump is determined by the operating speed of the ADC and the signal range. For this design, I_n is equal to $15\mu A$ and I_p is set to $30\mu A$.

3.4.3 Architecture of the Current-Charge-Pump Pipelined ADC

The high level architecture of the proposed current-charge-pump ADC is similar to the conventional one. Fig. 3.19 shows the standard block diagram of a traditional pipelined ADC, where two clock phases, sampling and amplifying, are required for the operation. The clocks run from the last stage to the first to ensure proper input sampling for each stage. As a result, extra delay elements might be needed to align the stage output bits correctly. Fig. 3.20 shows the architecture of the current-charge-pump pipelined ADC. A

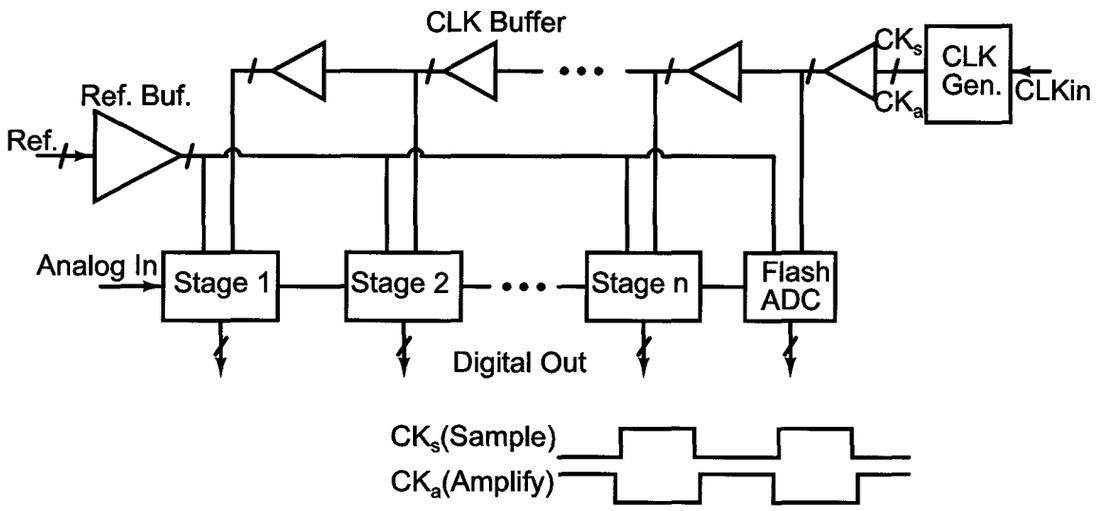

Figure 3.19: Simplified architecture of a conventional pipelined ADC, including two clock phases.

reset phase is needed before the sampling phase, as explained earlier. Since the sampling and amplifying phases alternate for odd-numbered and even-numbered stages, four clock phases are required as shown in the figure, where the duty cycle of the reset phases can be made smaller to optimize operating speed. To generate the four clocks, a divide-by-2 circuit is employed in the clock generator. The global clocks can be distributed to each stage with equal delay since the sampling instant for each stage is defined by comparator output CK_n as illustrated in Fig. 3.17. The large reference voltage buffer for stage sampling capacitors in the conventional pipelined ADC is removed. Instead, only a small buffer is needed to drive the parasitic input capacitors of the signal-path comparators. Note that regular switch capacitor sampling circuit is used at the input of the first stage.

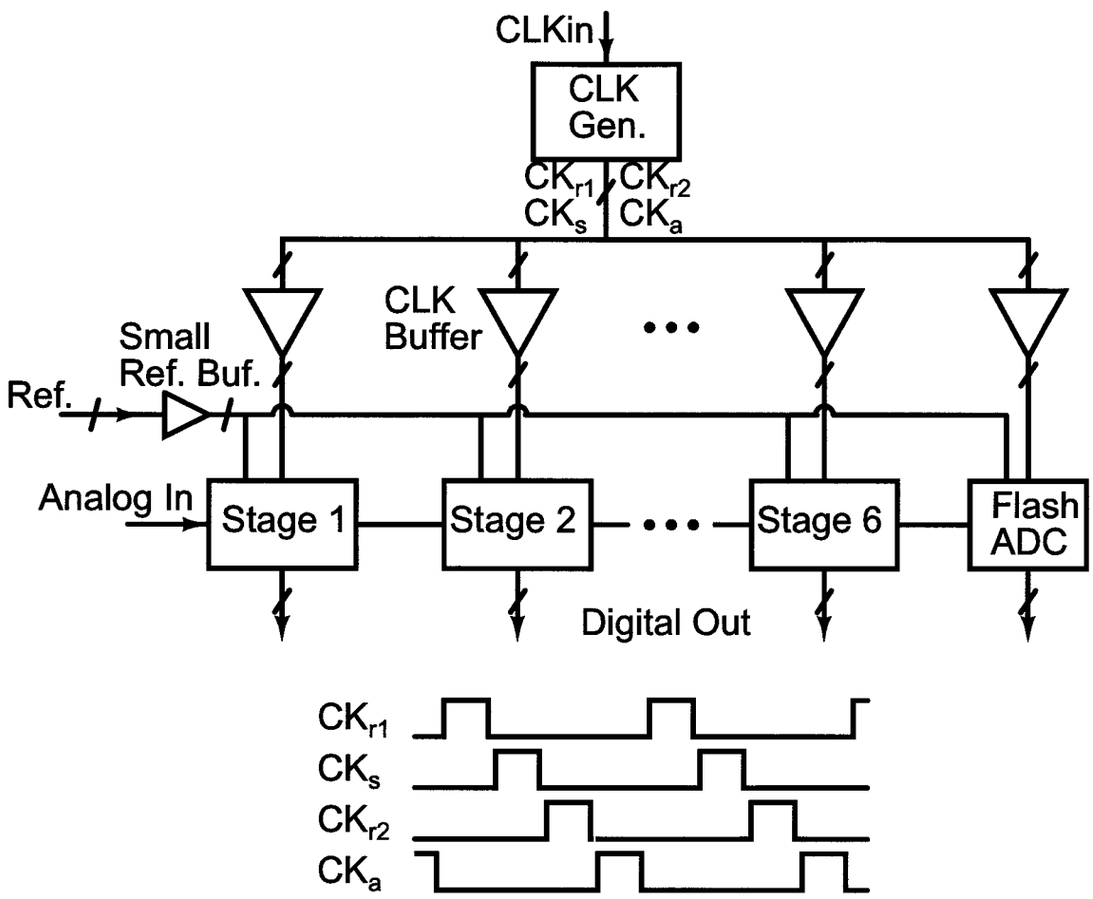

Figure 3.20: Simplified architecture of the current-charge-pump pipelined ADC, including four clock phases.

3.5 Circuit Level Design Considerations

As the OTA based residue amplification and big reference buffer are avoided in this approach, the comparators in the signal path and sub-ADC path become the dominant power consuming building blocks. To minimize the power consumption, inverter based comparators are designed for both paths. They mainly consume dynamic power and are compatible with digital circuit, which scales easily as technology advances. The comparator for signal

path is essentially a zero crossing detector while the sub-ADC comparator is a dynamic latch which is triggered by a clock signal.

3.5.1 Signal-Path Comparator with Signal-Independent Delay

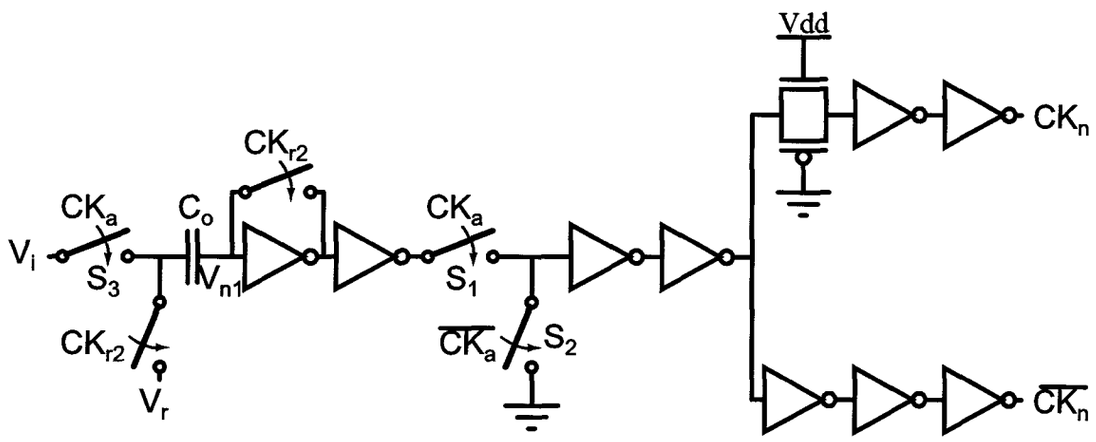

Figure 3.21: Inverter based signal-path comparator with differential output, offset of the first stage is calibrated during the clock phase CK_{r2}.

Fig. 3.21 shows the schematic of the signal-path comparator. Transmission gates are used for the switches to minimize charge injection. An always-on transmission gate is also used to balance the delay of the two output paths, which generate differential control pulses for charge-pump switches. Reasonable input referred offset of the signal-path comparator can be tolerated in the 1.5bit/stage implementation, but the inverter's threshold deviation due to process variation could well exceed the maximum tolerable $V_{ref}/4$. Since the comparator offset is dominated by the first stage, standard offset cancellation technique for the first inverter is used as shown in Fig. 3.21, where the offset of the first inverter is sampled

onto C_o during the clock phase CK_{r2} and subtracted when the input V_i is applied during the clock phase CK_a. By employing the offset cancellation technique, the threshold of this inverter based comparator is defined at the clock phase CK_{r2}, when the reference voltage V_r from the multiplexer output (see Fig. 3.17) is applied.

The comparator is only operating during the amplifying phase CK_a, when switch S_1 is ON and S_2 is OFF. When CK_a is 0, S_2 is ON and the comparator output is reset. After offset calibration at phase CK_{r2}, V_{n1} is the threshold voltage V_{th1} of the first inverter. At phase CK_a, switch S_3 is ON and V_{n1} jumps up by $V_i - V_r$, which is a positive value as V_i is always larger than its reference voltage (see Fig. 3.18). Then V_{n1} begins dropping at a rate of I_n/C since the comparator output CK_n is high. Once V_{n1} crosses V_{th1}, assuming the input referred offset from the later inverter stages is negligible, the comparator output toggles after a finite delay, when the amplified residue is passed to the next stage. To the first order, the comparator delay is independent of V_i and V_r, because it always sees the same ramp signal V_{n1} crossing the same comparator threshold voltage. Practically, when V_i is very close to the comparator threshold voltage, the initial voltage at the first inverter output is also near the triggering point of the later inverter stages. Thus the initial output transient of the first inverter stage will modulate the slope at the triggering point of the later stages and affect comparator delay time. Simulation results show that, when the input voltage V_i is 10mV above the comparator threshold voltage, the comparator delay decreases by 1.2ps compared to the delay with a larger V_i, which translates to less than 0.2mV error at the designed charge-pump charging rate. As the initial V_i gets even closer to the comparator

threshold voltage, the comparator delay starts to decrease faster. In this design, the input signal between 350mV to roughly 355mV will cause larger than 1LSB distortion as the reference voltage for this section is 350mV (refer to Fig. 3.18).

As mentioned in section 3.4.2, the equivalent offset of the signal-path comparator due to its finite delay is accommodated by lowering the start voltage V_{ini} of the following stage. Simulation results show that the equivalent offset deviation due to process variation is small enough to be tolerated by the redundancy of the stage. Six inverters are cascaded in the CK_n path to generate a sharp control pulse. The last few inverter stages are a little bigger to drive the load switches, while the first few inverters are small to minimize the static current consumption during CK_{r2}.

In this proposed implementation of the signal-path comparator, an offset calibration capacitor is used and it samples the reference voltage, the resulting kT/C noise needs to be lower than V_{LSB} of the ADC. Since the initial voltage on the offset calibration capacitor C_o is input signal independent, a relatively weak reference buffer only results in a fixed settling error. C_o is set to 20fF in this design.

3.5.2 Sub-ADC Path Comparator with Offset Calibration

Another inverter based comparator is proposed for the sub-ADC path, as shown in Fig. 3.22. A gated dynamic latch is inserted after the first inverter. Compared with the standard differential input pair based dynamic comparator [109], the proposed comparator detaches the

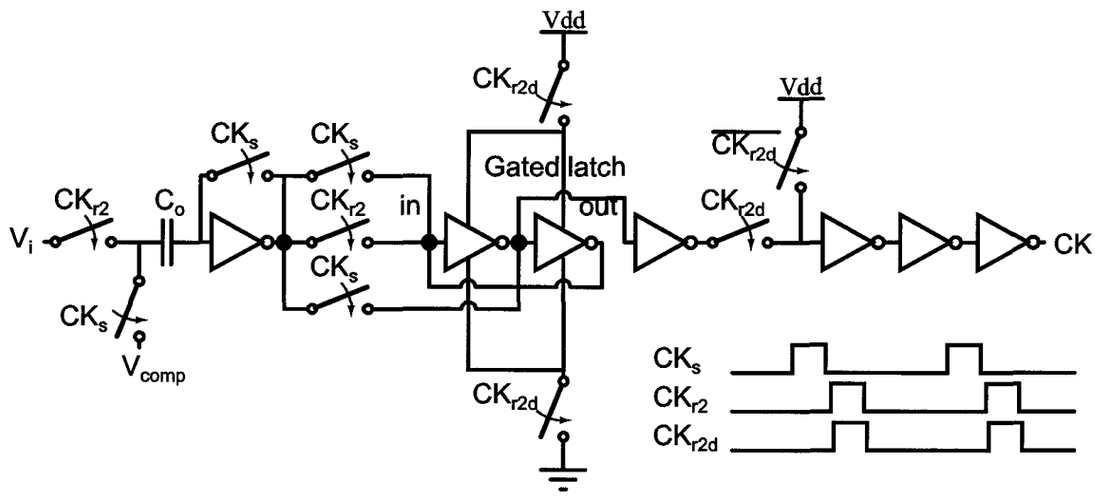

Figure 3.22: Inverter based sub-ADC path comparator, dynamic latch is gated at the clock phase CK_{r2dd} to ensure proper latching.

dynamic latch from being the dominant offset contributing source. Thus, by doing offset calibration for the first inverter gain stage, the comparator can be designed much smaller in area while achieving a low input referred offset. As a result, more offset from the signal path can be tolerated.

During the clock phase CK_s, the offset of first inverter stage is sampled onto C_o, when comparator reference voltage V_{comp} is also sampled. At the same time, the initial input and output of the latch are set to the threshold voltage of the first inverter. When the clock phase CK_{r2} goes high, input V_i is applied to C_o and output of the first inverter is connected to the input of the latch. After the latch input settles for a short time, CK_{r2d}, a delayed version of CK_{r2}, becomes high and the latch starts regenerating to produce a digital output bit.

3.5.3 Four-Phase Non-Overlapping Clock Generator

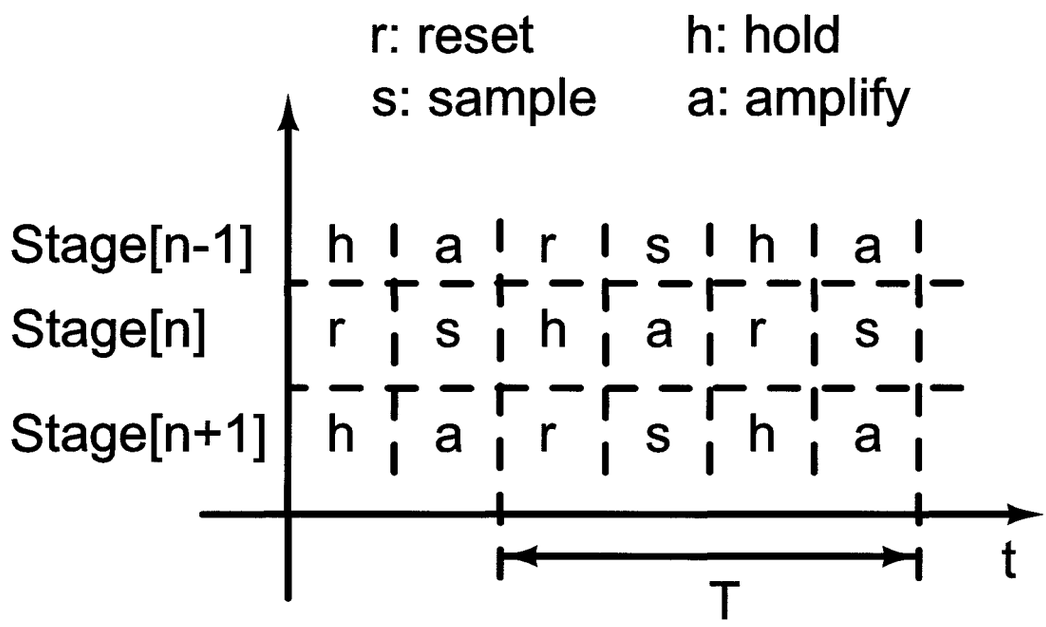

Figure 3.23: Operation sequences for stages in the current-charge-pump pipelined ADC.

For the proposed current-charge-pump pipelined ADC, four non-overlapping clock phases are required. The operation sequences for odd and even numbered stages are illustrated in Fig. 3.23. Fig. 3.24 shows the clock phase generator based on a frequency divide-by-2 circuit. A D flip-flop in negative feedback configuration is used to generate the four 50% duty-cycled clock phases at nodes N_1-N_4, each spaced 90° apart. Logic gates are employed to produce the 25% duty-cycled clock phases. A 50% duty-cycled clock $CK_{s,1st}$ is also generated for the sampling in the first stage, where reset phase is not required as the sampling capacitor is driven by the circuit preceding the pipelined ADC. The finite delays in the two latches and the extra buffers inserted make sure there are about 3% non-

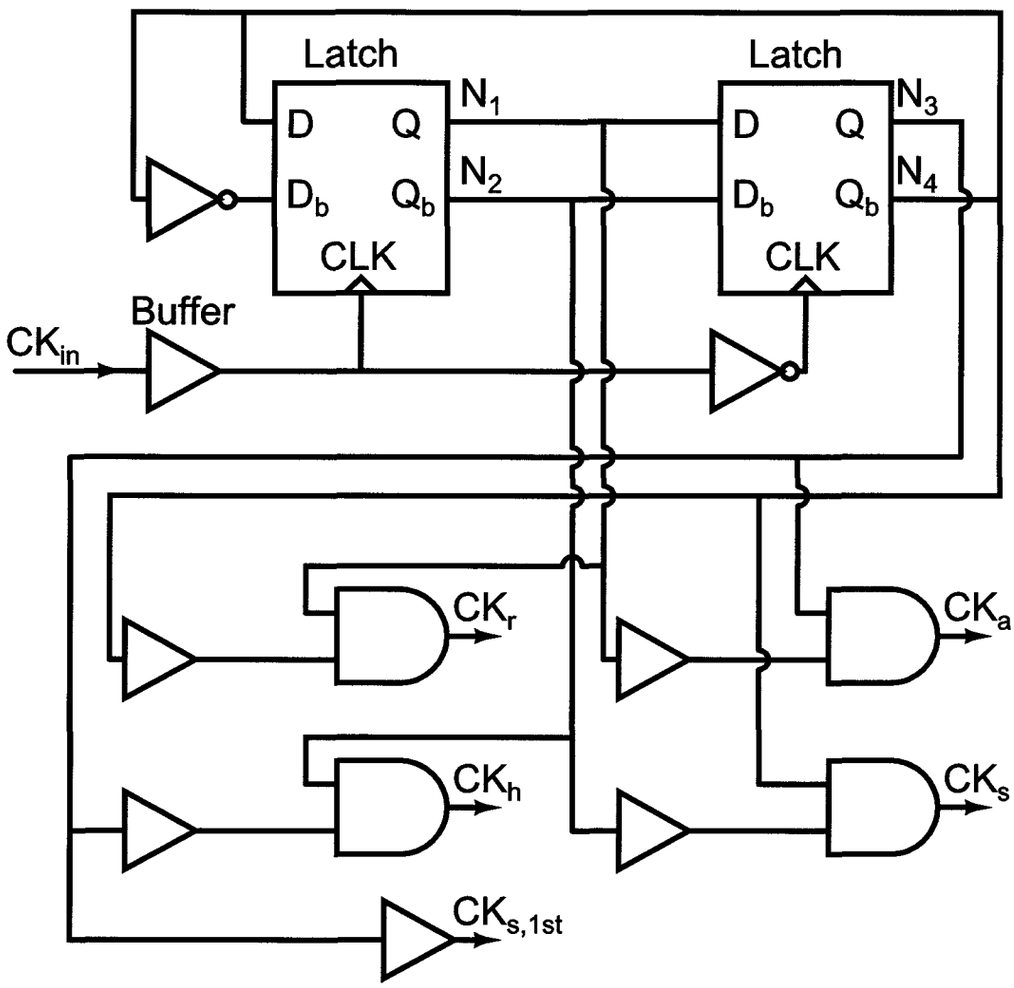

Figure 3.24: Generation of four non-overlapping clock phases from a frequency divide-by-2 circuit.

overlapping times between adjacent clock phases. Corner simulations with 200MHz input sinewave show the nominal non-overlapping time is 280ps (1V, TT, 27°), and it varies from 220ps (1.05V, FF, 0°) to 420ps (0.95V, SS, 85°). Further Monte-Carlo simulations show that transistor mismatches introduce less than 10% non-overlapping time variation.

3.6 Noise and Nonlinearity of Current-Charge-Pump MDAC

3.6.1 Noise of Current-Charge-Pump MDAC

The current-charge-pump pipelined ADC operates in four clock phases for each conversion period. Noise from the sub-ADC can be tolerated as a standard redundancy bit is built in for the 1.5bit stage. The MDAC noise, on the other hand, affects the accuracy of the pipelined ADC directly. Here we analyze the noise performance of the current-charge-pump MDAC. In order to derive the total input referred noise of the MDAC, noise associated with each one of the four clock phases needs to be considered.

During the reset phase CK_{r1} (refer to Fig. 3.17), the noise on the sampling capacitor C_1 is:

$$V_{n,r1}^2 = \frac{kT}{C_1} \tag{3.20}$$

During the following sampling phase CK_s, when C_1 is charged by the PMOS current source, the noise accumulated on C_1 is a random walk resulting from the channel noise of the PMOS current source [18, 110]:

$$V_{n,s}^2 = \frac{2kTg_{m,cpp}}{C_1^2} t_s \tag{3.21}$$

where the PMOS current-charge-pump noise current power spectral density (PSD) is as-

sumed to be $4kTg_{m,cpp}$, t_s is the charging or integration time. So far the total noise power on C_1 from the reset and sampling phases is:

$$V^2_{n,r1s} = \frac{kT}{C_1} + \frac{2kTg_{m,cpp}}{C_1^2}t_s \tag{3.22}$$

During the hold phase CK_{r2}, which is also the reset phase for the preceding and succeeding stages, the noise on the sampling capacitor C_1 remains. At the same phase, sampling noise develops on the offset calibration capacitor C_o of the signal-path comparator (refer to Fig. 3.21), as the input-output shorted inverter provides a low impedance path for reference voltage sampling:

$$V^2_{n,r2} = \frac{kT}{C_o} \tag{3.23}$$

At the start of the amplifying phase CK_a, the voltage on sampling capacitor C_1 is applied to the signal-path comparator and offset calibration capacitor C_o begins to act as an AC coupling capacitor. Therefore the uncorrelated noise previously stored on C_1 and C_o add up in power:

$$V^2_{n,r1sr2} = \frac{kT}{C_1} + \frac{2kTg_{m,cpp}}{C_1^2}t_s + \frac{kT}{C_o} \tag{3.24}$$

Finally, during the amplifying phase, NMOS current source discharges C_1 and signal-path comparator is turned on. The noise contributed by the NMOS current source is a random

walk, similar to the one from PMOS current source. The noise from the nonlinear comparator is non-stationary. Here the comparator functions as a threshold-detecting circuit, thus only the noise accumulated till the comparator triggers is of concern. Furthermore, the comparator noise is dominated by the first stage inverter, where it has reasonably large gain. From another perspective, the first stage noise dominates because the signal slope at the comparator input is the smallest while the slope at the output of the first stage is much higher, which makes the later comparator stages relatively insensitive to noise. The total noise contribution from the amplifying phase is thus:

$$V_{n,a}^2 = \frac{2kTg_{m,cpn}}{C_1^2}t_a + \frac{2kTg_{n,inv}}{C_{L,inv}^2}t_a \tag{3.25}$$

where $4kTg_{m,cpn}$ is the NMOS current-charge-pump noise current PSD, t_a is the discharging time, $g_{n,inv}$ is the equivalent noise transconductance of the first inverter stage during the time t_a, and $C_{L,inv}$ is the load capacitor of the first inverter. Low frequency flicker noise is not considered here. From (3.24) and (3.25), we arrive at the total noise of the MDAC circuit:

$$V_{n,mdac}^2 = \frac{kT}{C_1} + \frac{2kT(g_{m,cpp}t_s + g_{m,cpn}t_a)}{C_1^2} + \frac{kT}{C_o} + \frac{2kTg_{n,inv}t_a}{C_{L,inv}^2} \tag{3.26}$$

The total noise of the pipelined ADC is dominated by its first stage, as each stage has a power gain of 4 in this design. Note that the first stage of this pipelined ADC is slightly

different from the one analyzed here. Standard switch capacitor sampling circuit is used to acquire the input signal for the first stage, while the later stages use current-charge-pump circuit to sample residue signal. Nonetheless, the derivation of the MDAC noise in the first stage is very similar and not repeated here.

3.6.2 Nonlinearity of Current-Charge-Pump MDAC

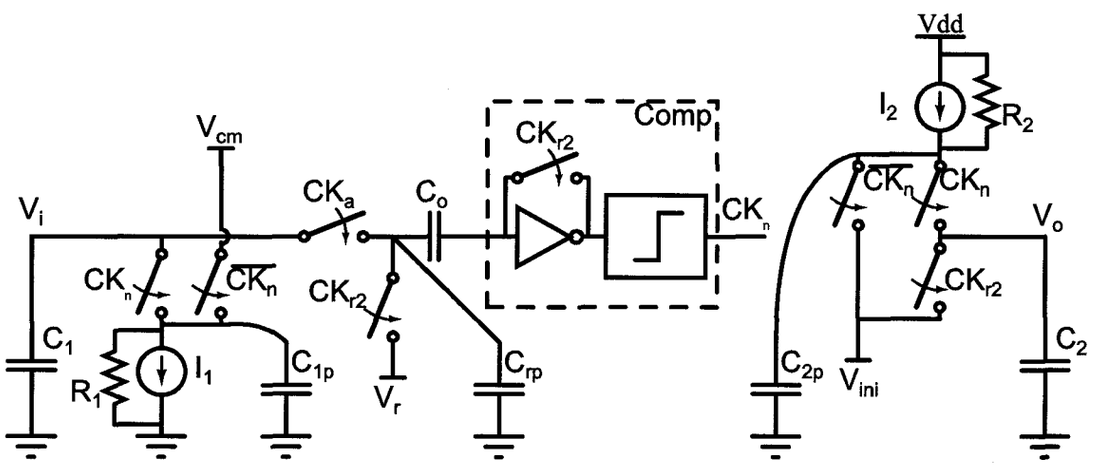

Figure 3.25: Current-charge-pump multply-by-2 circuit, only phases CK_{r2} and CK_a are shown for circuit distortion analysis. C_{1p}, C_{rp}, C_{2p} are parasitic capacitors.

The residue signal sampling for each stage of the current-charge-pump pipelined ADC relies on the matchings of current sources and capacitors, where fixed matching errors result in interstage gain deviations and the nonlinear errors lead to signal distortion. The nonlinearity of the proposed MDAC mainly comes from the current-charge-pump circuit. Fig. 3.25 shows the multiply-by-2 circuit with parasitic capacitors and current sources with finite output impedance. In the analysis here, comparator finite delay is not considered as

it only causes a constant output voltage shift, which can be absorbed into the output initial voltage V_{ini}. Ideally, the output voltage of the circuit at the end of the amplifying phase is:

$$V_o = \frac{I_2}{C_2}\frac{C_1}{I_1}(V_i - V_r) + V_{ini} \tag{3.27}$$

Due to charge sharing from the parasitic capacitors at the beginning of the amplifying phase:

$$V'_i = \frac{C_1 V_i + C_{1p} V_{cm} + C_{rp} V_r}{C_1} \tag{3.28}$$

$$V'_{o,ini} = \frac{C_2 V_{ini} + C_{2p} V_{ini}}{C_2} = V_{ini} \tag{3.29}$$

where $V_{o,ini}$ is the start voltage at the output. The average currents over the discharging/charging time from the two current sources are:

$$I_i = I_1 + \frac{V'_i - V_r}{2R_1} \tag{3.30}$$

$$I_o = I_2 + \frac{V'_o - V_{ini}}{2R_2} \tag{3.31}$$

Now we also consider all the parasitic capacitors, the sampled voltage at the end of the amplifying phase determined by:

$$V'_o = \frac{I_o}{C_2 + C_{2p}}\frac{C_1 + C_{1p} + C_{rp}}{I_i}(V'_i - V_r) + V_{ini} \tag{3.32}$$

To get the final analytical expression for the output voltage V'_o, we need to plug 3.28, 3.30 and 3.31 into 3.32. It turned out that the expression for V'_o is complex and can hardly be simplified to give meaningful insights. Nonetheless, from 3.30, 3.31 and 3.32, we can tell that the signal dependent current sources will cause signal dependent interstage gain distortion. As the sampling of the first stage is a standard switch capacitor circuit, which doesn't suffer from the distortion described here, thus the gain distortion from the current-charge-pump circuit need to be below 2LSB for this 8bit pipelined ADC. We mentioned in Section 3.4.1 that the simulated gain linearity is 55dB, which is better than the required accuracy for the design.

Due to its open-loop nature and thus the sensitivity to nonlinear current sources, parasitic capacitors, and wiring capacitors from the layout, the proposed current-charge-pump circuit is only suitable for medium resolution ADCs. Section 3.8.2 proposes some alternative circuits that could potentially achieve better accuracy.

3.7 Measurement Results

The prototype current-charge-pump pipelined ADC was fabricated on a 90nm digital CMOS process. Fig. 3.26 shows the die photogragh and the main sections of the prototype. The active area of the chip is $0.044mm^2$. 48-pin QFN is used to package the chip. To characterize the design, on-board regulators are employed for the ADC reference voltages. An Agilent 33250A is used to generate the input signal and an HP 8648B to generate the exter-

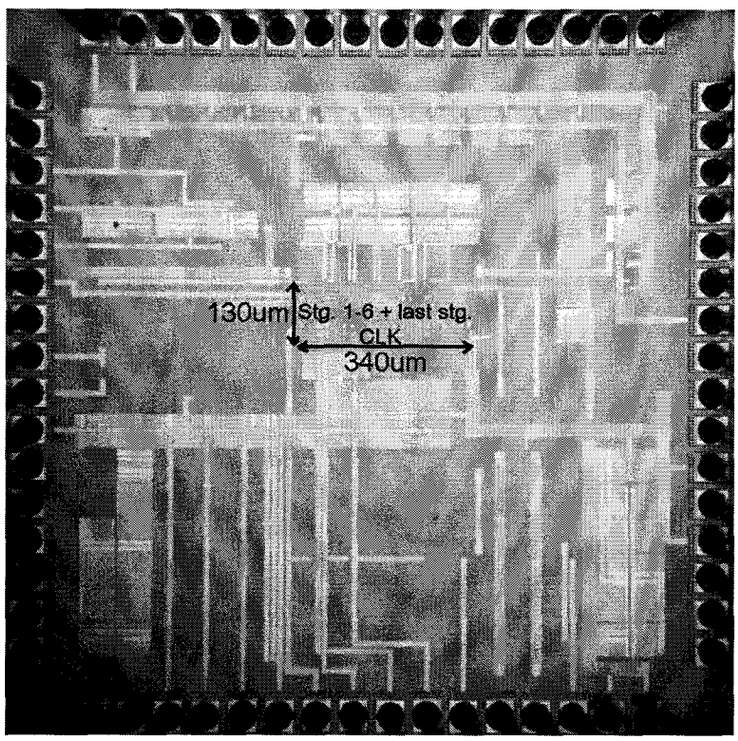

Figure 3.26: Die photo.

nal 200MHz reference clock signal. The raw digital output bits are collected by an Agilent 1692AD logic analyzer. Static interstage gain errors for the first three stages are calibrated offline after optimal radix search.

The chip operates from a 1V supply and the sampling frequency is 100MHz. Fig. 3.27 shows the FFT spectrum with a -1dBFS 49MHz input signal. The SFDR, SNDR and SNR are 46.7dB, 37.1dB and 37.7dB respectively, where SNDR is mainly limited by the noise. Experimental results show that the SNR is strongly correlated with the supply voltage of the digital output buffer. The single-ended design suffers from noise coupling from digital circuits and other common mode noise. The SFDR, SNDR and SNR for -1dBFS input

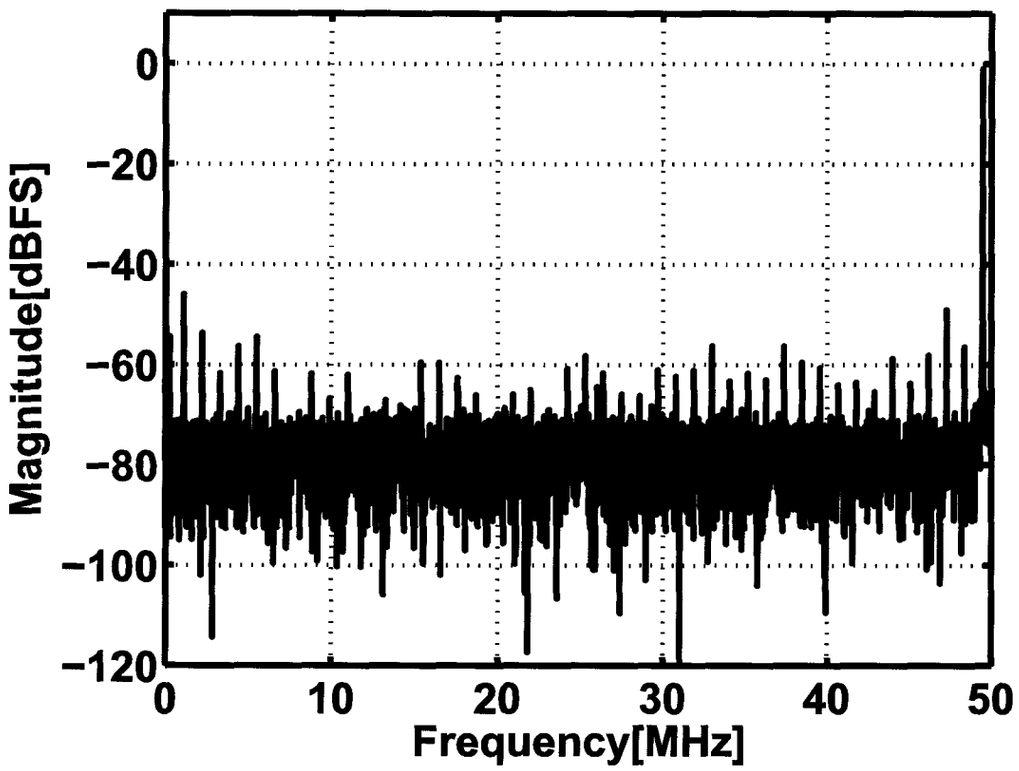

Figure 3.27: Measured output spectrum at 100MS/s with a -1dBFS input sinewave near Nyquist.

signals with frequencies from 101kHz to 49MHz are shown in Fig. 3.29. Fig. 3.28 shows the measured dynamic performance when input signal is swept from -37dBFS to 0dBFS. Dynamic performance with different sampling frequency is also shown in Fig. 3.30. The static performance for the ADC is characterized by applying a ramp input and sampling 64k data points. Fig. 3.31 shows the DNL and INL performance[2]. The maximum DNL and INL is 1LSB/-0.8LSB and 2LSB/-2.3LSB respectively.

The power consumption of the chip is 1.39mW (excluding output buffer). Simulated

[2]The number of output code levels is slightly less than 256 due to interstage gain deviation

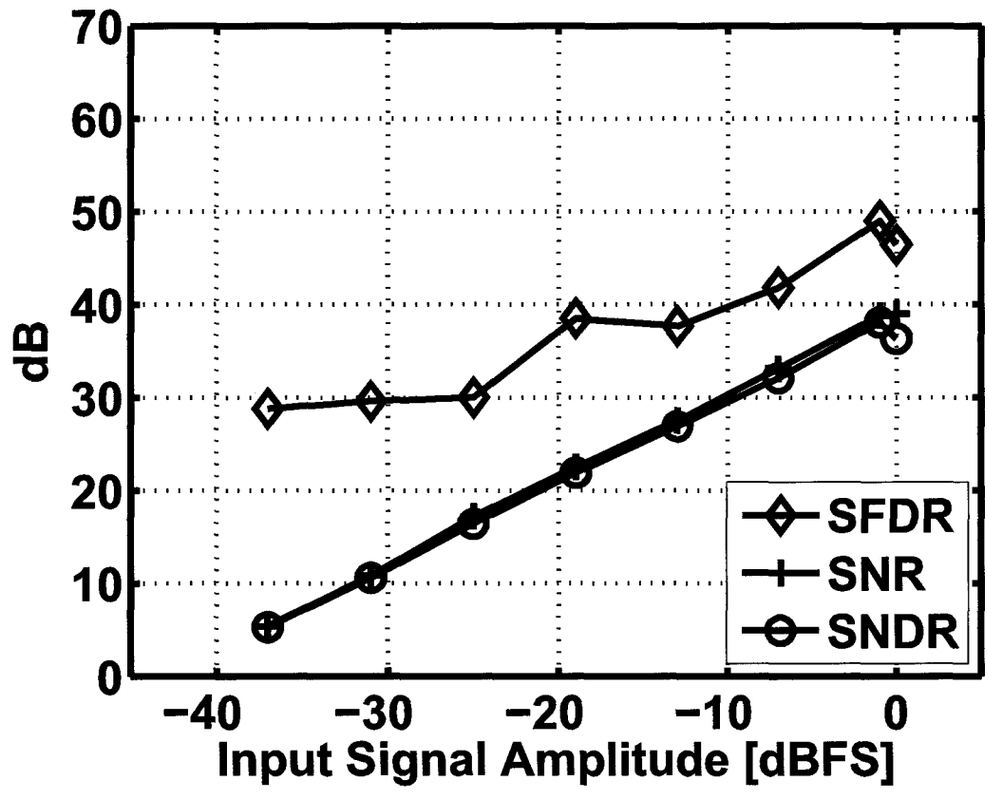

Figure 3.28: Measured SNDR, SNR, and SFDR at 100MS/s for a Nyquist input with amplitudes varying from -37dBFS to 0dBFS.

power breakdown shows that 45% of the power consumption is from the comparator offset calibration inverters.

The measured results including the performance for ±5% supply voltage variations are summarized in Table 3.1. The performance is consistent for ±5% VDD variation, with less than 1dB difference. The current-charge-pump pipelined ADC achieves an FOM of 237fJ/Conv. Step, which is the best among the 8bit ADCs shown in Table 3.2. Table 3.3

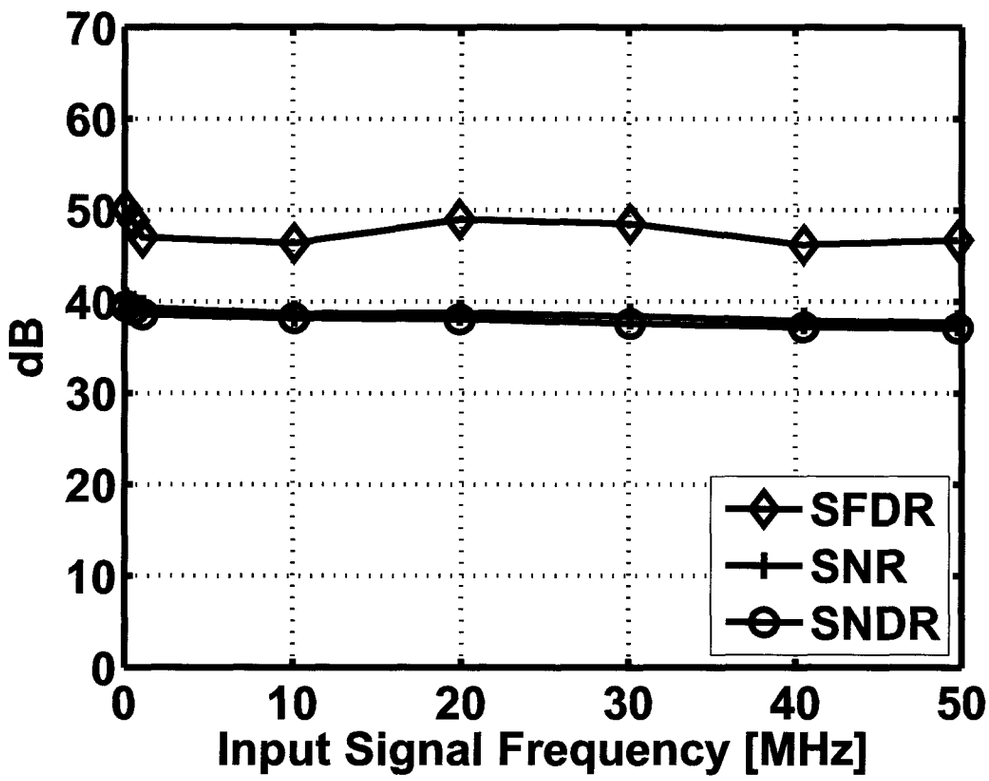

Figure 3.29: Measured SNDR, SNR, and SFDR at 100MS/s for a -1dBFS input sinewave with frequencies varying from 101kHz to 49MHz.

lists the recently published OTA-less pipelined ADCs. The FOM of this work is also among the best and the reference buffer requirement is largely relaxed (section 3.5.1).

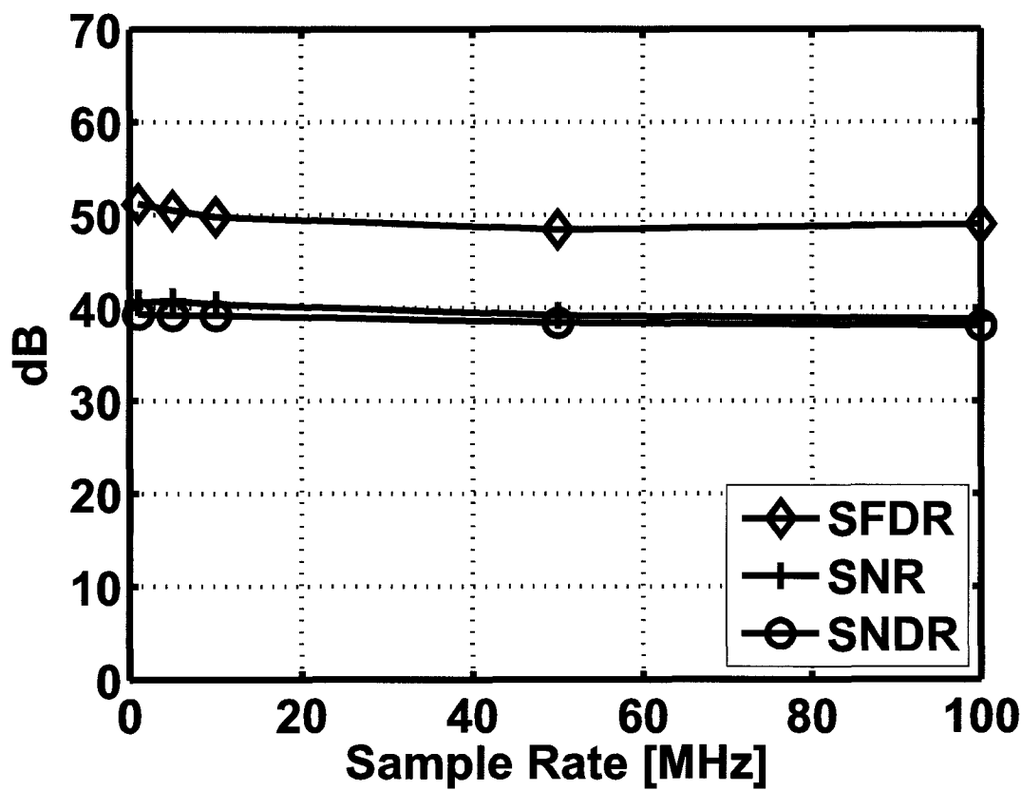

Figure 3.30: Measured SNDR, SNR, and SFDR for a -1dBFS input sinewave at 49kHz with sampling frequencies varying from 1MHz to 100MHz.

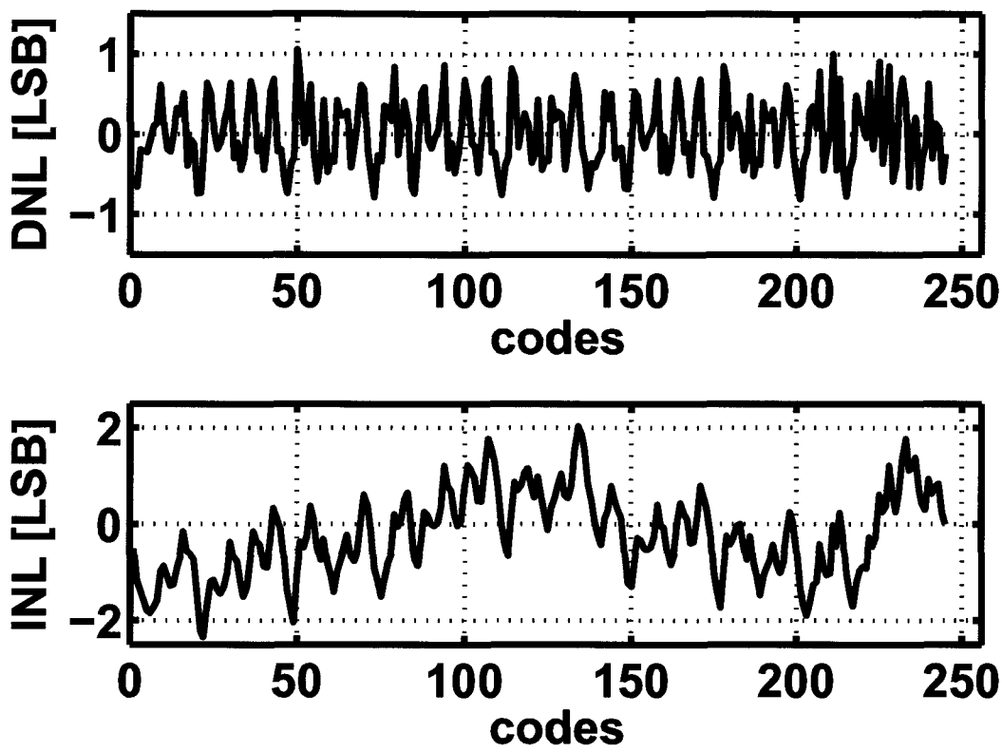

Figure 3.31: Measured DNL and INL.

Table 3.1: ADC performance summary from 0.95V–1.05V @ 25°C

Sampling rate [MS/s]	100		
Resolution [Bit]	8		
Input signal range [V_{pp}]	0.4		
Active area [mm^2]	0.044		
Technology	90nm standard digital CMOS		
Supply voltage [V]	0.95	1	1.05
SNR[a] [dB]	37	37.7	38.6
SNDR[a] [dB]	36.3	37.1	37.6
SFDR[a] [dB]	46.2	46.7	48.3
DNL [LSB]	1.2/-0.8	1/-0.8	1/-0.7
INL [LSB]	2.6/-2.1	2/-2.3	2.1/-1.8
Power dissipation [mW]	1.15	1.39	1.59

[a]Measured with a -1dBFS input signal at Nyquist

Table 3.2: 8bit ADC performance comparison

Author&Year	VDD(V)	V_{inp-p}	Type	SNDR(dB)	Power(mW)	Fs(MS/s)	Area(mm^2)	Tech.(μm)	FOM[a]
Taft 04 [111]	1.8	1.6	Folding	45.5	1270	1600	3.6	0.18	5.2
Mulder 04 [112]	2.5/1.2		Subranging	47.5	21	125	0.09	0.13	0.86
Limotyrakis 04 [113]	1.8	1.6	Interleave	45.4	71	150	1.8	0.18	3.1
Geelen 04 [114]	3.3/1.8	2	Folding	46.9	200	600	0.2	0.35/0.18	2.8
Kim 05 [115]	1.8	1	Pipeline	48	30	200	0.15	0.18	0.73
Brooks 07 [19]	1.8	1	Pipeline	40.3	8.5	200	0.05	0.18	0.51
Shimizu 08 [116]	2.5/1.2	1.4	Subranging	45	34	300	0.29	0.09	0.78
Wang 04 [117]	1.8		Folding	38	207	600	0.5	0.18	5.3
Wu 06 [118]	1	1	Pipeline	37	30	100	2.04	0.18	5.2
Shen 07 [10]	0.5	0.4	Pipeline	48.1	2.4	10	0.86	0.09	1.15
Tu 08 [119]	1.2	0.8	Interleave	44.2	30	800	0.12	0.065	0.28
This Work	1	0.4	Pipeline	37.1	1.39	100	0.04	0.09	0.237

[a]

$$\text{FOM} = \frac{\text{Power}}{2^{(\text{SNDR}-1.76)/6.02} * 2 * \text{Bandwidth}} 10^{12}[\text{pJ/Conv. Step}]$$

Table 3.3: OTA-less Pipelined ADC performance comparison

Author&Year	VDD(V)	V_{inp-p}	Type	SNDR(dB)	Power(mW)	Fs(MS/s)	Area(mm^2)	Tech.(μm)	FOM[a]
Fiorenza 06 [18]	1.8	1	Pipeline	52	2.5	7.9	1.2	0.18	0.8
Brooks 07 [19]	1.8	1	Pipeline	40.3	8.5	200	0.05	0.18	0.51
Anthony 08 [29]	1.8		Pipeline	65.9	140	250	2.57	0.18	0.28
Shin 08 [89]	1.2	1	Pipeline	54.3	5.51	26	0.56	0.065	0.5
Hu 09 [30]	1.2		Pipeline	47.7	1.44	50	0.123	0.09	0.145
Brooks 09 [88]	1.2	2	Pipeline	62	4.5	50	0.3	0.09	0.088
Ahmed 09 [31]	1.8	1	Pipeline	56	9.9	50	1.4	0.18	0.384
This Work	1	0.4	Pipeline	37.1	1.39	100	0.04	0.09	0.237

[a]

$$\text{FOM} = \frac{\text{Power}}{2^{(\text{SNDR}-1.76)/6.02} * 2 * \text{Bandwidth}} 10^{12}[\text{pJ/Conv. Step}]$$

3.8 Ideas for Future Improvement

3.8.1 Fully Differential Design

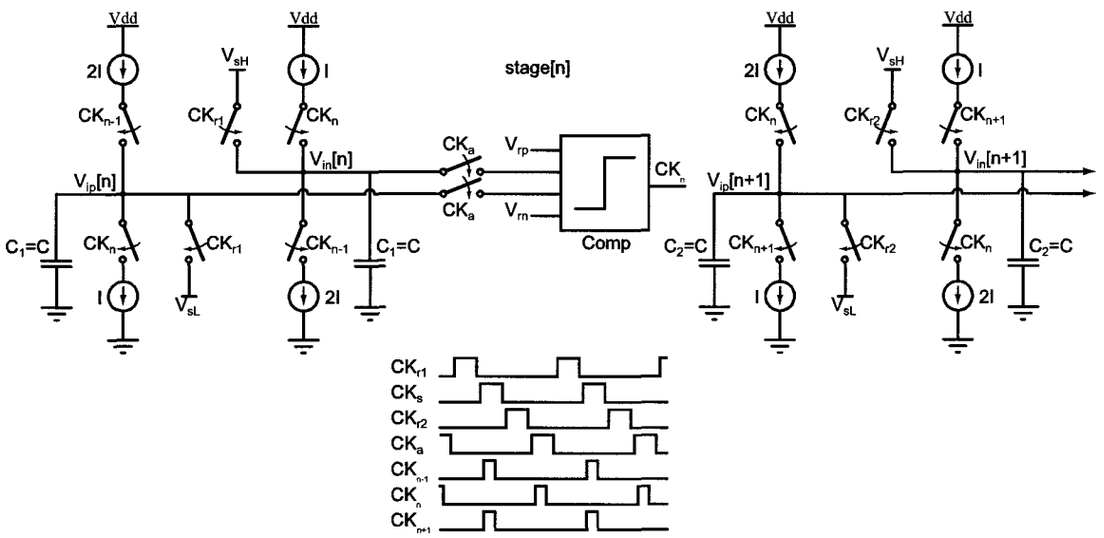

Figure 3.32: Fully differential schematic of the proposed current-charge-pump circuit for a pipelined ADC.

The prototype chip of the current-charge-pump circuit adopted a single ended design for the proof of concept. As we observe from the experimental results, the noise coupling from the supply and substrate significantly limits the ADC's performance. In a redesign, a fully differential version could be implemented and characterized. In this section, the schematic and operation of the fully differential current-charge-pump circuit is briefly described, another version of the fully differential design is also presented for comparison.

Fig. 3.32 shows the fully differential schematic of the proposed current-charge-pump circuit, which realizes the function of an MDAC in a pipelined stage. The switch control

clocks and the relative values of the capacitors and current sources are also illustrated in the schematic. Its operating principle is the same as the singled-ended version shown in Fig. 3.16. A differential difference comparator is needed to handle the differential input signals and the reference voltages from the DAC in a pipelined ADC stage. A low start voltage V_{sL} for the positive path and a high start voltage V_{sH} for the negative path are adopted so that the sampling of the positive path capacitor C_{1p} only involves charging and the negative path capacitor C_{1n} only involves discharging. In this way, the finite delay of the comparator only causes a fixed offset instead of the input signal sign-dependent offsets, as will be explained later in this section. To understand better how the circuit operates, we can write out the following equations assuming a 1.5bit stage,

$$\begin{aligned} V_{op} - V_{on} &= V_{ip}[n+1] - V_{in}[n+1] \\ &= 2[(V_{ip}[n] - V_{rp}) + (V_{rn} - V_{in}[n])] + V_{sL} - V_{sH} \\ &= 2[(V_{ip} - V_{in}) - (V_{rp} - V_{rn})] + V_{sL} - V_{sH} \end{aligned}$$

$$\text{For } V_{ip} - V_{in} < V_{cpb} - V_{cpt}$$

$$V_{op} - V_{on} = 2[(V_{ip} - V_{in}) - (V_{rp1} - V_{rn1})] + V_{sL} - V_{sH} \tag{3.33}$$

$$\text{For } V_{cpb} - V_{cpt} < V_{ip} - V_{in} < V_{cpt} - V_{cpb}$$

$$V_{op} - V_{on} = 2[(V_{ip} - V_{in}) - (V_{rp2} - V_{rn2})] + V_{sL} - V_{sH} \tag{3.34}$$

$$\text{For } V_{ip} - V_{in} > V_{cpt} - V_{cpb}$$

$$V_{op} - V_{on} = 2[(V_{ip} - V_{in}) - (V_{rp3} - V_{rn3})] + V_{sL} - V_{sH} \tag{3.35}$$

Table 3.4: Reference voltage and sub-ADC comparator threshold values, VDD = 1V, $V_{pp,diff} = 800mV$

V_{rp1}	300mV	V_{rn1}	700mV
V_{rp2}	400mV	V_{rn2}	600mV
V_{rp3}	500mV	V_{rn3}	500mV
V_{sH}	700mV	V_{sL}	300mV
V_{cpt}	550mV	V_{cpb}	450mV

where $V_{rp,1-3}$ and $V_{rn,1-3}$ are the reference voltages, V_{cpt} and V_{cpb} are the threshold voltage for the top and bottom comparators in the sub-ADC (not shown in schematic). In the case of a 1V supply voltage and $800mV_{pp,diff}$ signal range centered around VDD/2, the values for the variables in 3.35 are listed in Table 3.4. Similar to the standard MDAC, the offset of the sub-ADC comparators here can be tolerated up to $\pm V_{ref}/4$, or $\pm 50mV$ in the example above. Note that the output common mode of this circuit is not a big concern because the reset phase is built in before the sampling phase in each clock cycle.

A more straightforward way of implementing the MDAC based on the current charge-pumps is shown in Fig. 3.33. The main difference of this circuit is that it resets to V_{cm} before the sampling phase CK_s, instead of initializing the positive and negative path sampling capacitors to V_{sL} and V_{sH} respectively. In order to accommodate this change, the output capacitors need to be charged to achieve a larger than V_{cm} voltage or discharged otherwise. To realize a gain of 2 in the amplifying phase CK_a, two unit current source Is are used for both positive and negative paths at the output side, while only one unit current source I is on at the input side. The drawbacks of this circuit are that the logic to generate the switch control clocks are not as straightforward as the one in Fig. 3.32, and due to fi-

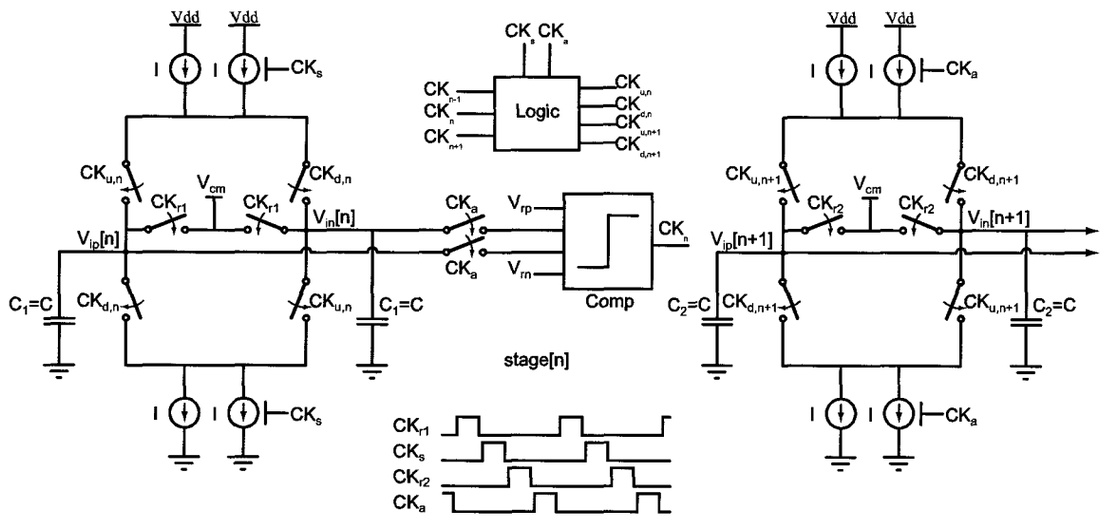

Figure 3.33: Fully differential schematic of the current-charge-pump circuit with output reset to V_{cm} before sampling. CK_{n-1} and CK_{n+1} are from previous and succeeding stage respectively.

nite comparator delay the output voltage experiences input sign dependent overshoots, as each capacitor can be charged (result in positive overshoot) or discharged(result in negative overshoot).

3.8.2 Alternative MDACs Avoiding Reference Buffers

The proposed current-charge-pump circuit replaces the traditional MDAC in a pipelined ADC stage, and big reference buffers are also avoided. The downside is that its accuracy is limited by the current source linearity. In this section, we present three alternative MDACs using the comparator based switched capacitor (CBSC) technique [18], while avoiding the big reference buffers. Pros and cons of these circuits are also briefly discussed.

Alternative MDAC with V_{ref} subtracted from V_{in}

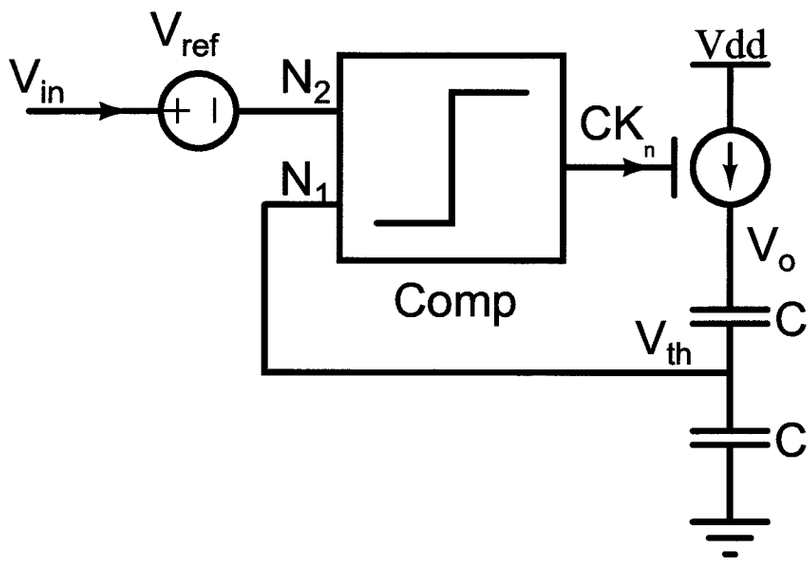

Figure 3.34: Alternative MDAC with V_{ref} subtracted from V_{in}, operation in the amplifying phase is shown.

Fig. 3.34 shows one of the solutions to achieve the MDAC transfer function without reference voltage driving a big capacitor. V_{in} is subtracted by V_{ref} before it is applied to the comparator input. During the amplifying phase, the current source charges the two capacitors connected in series until V_{th} at N_1 is equal to the voltage at N_2. If the two capacitors are identical and the initial voltages on them are 0, then:

$$\begin{aligned} V_o &= 2V_{th} \\ &= 2(V_{in} - V_{ref}) \end{aligned} \tag{3.36}$$

To realize the subtraction of V_{ref}, an offset voltage can be intentionally introduced to the

comparator. The drawback of the circuit is that the threshold voltage of the comparator is not fixed and is directly affected by V_{in}. This requires a comparator that can handle a large input common mode range and its finite delay independent of the threshold voltage.

Alternative MDAC with reference current injected into the comparator virtual ground node

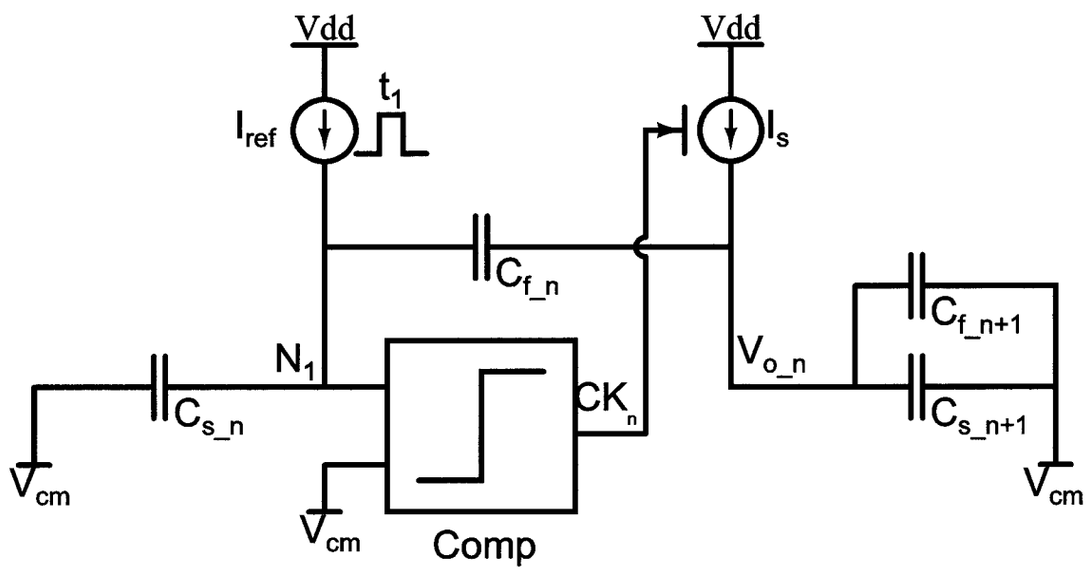

Figure 3.35: Alternative MDAC with reference current injected into the comparator virtual ground node, operation in the amplifying phase is shown.

To improve the design in Fig. 3.34, another MDAC is presented in Fig. 3.35. Here the threshold voltage of the comparator is fixed to V_{cm}. During the amplifying phase, a reference current is injected into the node N_1 for a certain amount of time $t_1(t_1 < T/2)$. Assuming each of the capacitor in Fig. 3.35 is equal to C, after applying the charge conser-

vation rule at N_1, we get the following equation at the end of the amplifying phase:

$$V_{o\_n} = 2(V_{i\_n} - \frac{3}{5}\frac{I_{ref}}{C}t_1) \tag{3.37}$$

where V_{i_n} is the voltage sampled onto C_{s_n} and C_{f_n} during the sampling phase. By tuning I_{ref} or t_1, an effective V_{ref} is subtracted from the circuit output. The downside of this approach is that the voltage at N_1 is settling during the amplifying phase, and it is also input signal dependent, thus the current source I_{ref} with finite output impedance is modulated by the voltage at N_1. As a result, the reference voltage has a signal dependent second-order nonlinearity.

Alternative MDAC with reference voltage sampled onto a separate capacitor

To further reduce the nonlinearity associated with V_{ref}, the reference voltage is sampled onto a separate capacitor, as shown in Fig. 3.36. A reference capacitor C_{ref} is added alongside the sampling capacitors, as illustrated in the succeeding stage in the schematic. During the sampling phase, the reference current source I_{ref} injects current onto C_{ref}, whose bottom plate is tied to a fixed voltage V_{cm}. During the amplifying phase, the top plate of C_{ref} is shorted to V_{cm}, along with the sampling capacitor C_s. Assuming all the capacitors are equal, with a value of C, the output voltage at the end of the amplifying phase is:

$$V_{o\_n} = 2V_{i\_n} - \frac{I_{ref}}{C}t_1 \tag{3.38}$$

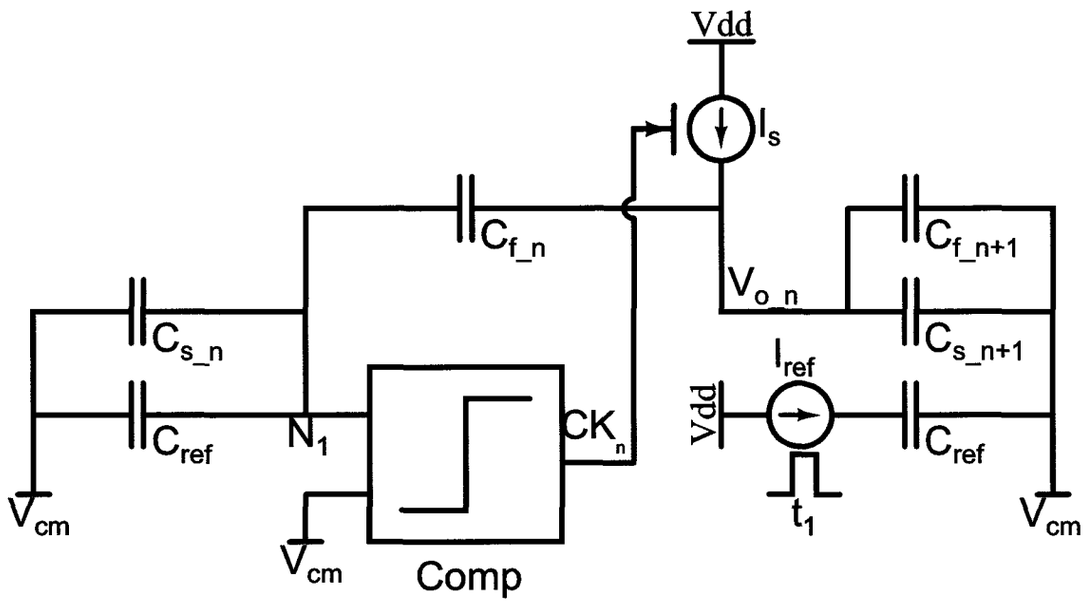

Figure 3.36: Alternative MDAC with reference voltage sampled onto a separate capacitor, operation in the amplifying phase is shown.

where V_{i_n} is the voltage sampled onto C_{s_n} and C_{f_n} during the sampling phase. Similar to the previous approach, I_{ref} or t_1 can be adjusted to realize the effective reference voltage V_{ref}. For this implementation, the reference voltage needs to be sampled during the sampling phase, but the sub-ADC output is not ready yet. To overcome this issue, both $+V_{ref}$ and $-V_{ref}$ can be sampled onto two separate C_{ref} capacitors in the case of a 1.5bit stage, then during the amplifying phase, the right reference capacitor is chosen based on the sub-ADC's decision. Another method is that a separate time slot is allocated between the sampling and amplifying phases, when the right reference current is chosen by the sub-ADC output to charge/discharge the capacitor C_{ref}.

3.9 Summary

In this chapter, a 1V 100MS/s 8bit pipelined ADC with an FOM of 237fJ/Conv. Step is demonstrated. This work has focused on an alternative to traditional MDAC to achieve high energy efficiency. This design utilizes a combination of current charge-pumps and an inverter based comparator to realize the function of a conventional MDAC. A second inverter based comparator is also designed for the sub-ADC path, so that the comparator is smaller, process scalable and has low offset. The proposed stage architecture avoids using the power hungry interstage OTAs and big reference buffers. The pipelined ADC stage is highly digital and does not involve the feedback circuit, thus it achieves high operation efficiency. Given that static interstage gain error can be calibrated in digital domain with minimal overhead, many opportunities open up to implement the pipelined ADC stage in alternative ways, in an effort to substantially reduce power consumption. For this proposed design, the operating speed is mainly limited by the signal-path comparator and the maximum resolution is restricted by the linearity of the charge-pump current source. Thus, the proposed architecture is more suitable for high speed and medium resolution applications, where it has a distinct advantage of high energy efficient operation. At the same time, further study is needed to achieve higher performance as it is a new approach to implement pipelined ADCs. Among others, enhanced current source linearity and a fully differential silicon implementation can be the next steps to make the design more mature.

This chapter also briefly touches on the possible fully differential implementation of the

current-charge-pump pipelined ADC, as well as several alternative MDACs for a pipelined ADC stage, without the need of big reference buffers.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

This thesis has focused on two important aspects of a pipelined ADC design. One is the supply voltage and the other is the power consumption. In both cases, we pushed to the limit and proposed a pipelined ADC operating from a 0.5V power supply and a highly efficient pipelined ADC without the need of signal path OTAs and big reference voltage buffers.

ITRS predicts that the supply voltage for low power operation will be down to 0.5V in about seven years (Fig. 1.5(b)) [9]. This is mainly driven by CMOS technology advancing and power reduction. In order for the ADC to be integrated onto the same digital die, a 0.5V pipelined ADC was investigated and designed using UMC 90nm digital CMOS technology. It operates at 10MS/s and has an 8 bit resolution. A cascaded sampling technique is used

to combat switch OFF leakage. An auxiliary S/H in the sub-ADC path allows eliminating of the front-end S/H stage. A two-stage 0.5V OTA with 50dB DC gain and 32MHz GBW is incorporated for the stage residue amplification. It is a true low voltage design, with no voltage boosting or special devices in the circuits. The measured peak SNDR is 48.1dB and peak SFDR is 57.2dB for a full-scale sinusoidal input. Maximal INL and DNL are 1.19 and 0.55 LSB, respectively. It consumes 2.4mW for 10MS/s operation and achieves an FOM of 1.15pJ/Conv. Step, which was the best among sub-1V pipelined ADCs.

In order to cope with the important issue of power consumption for the pipelined ADC, the traditional architecture of the pipelined ADC was reviewed and a new stage structure was proposed to avoid the using of power hungry residue amplifiers and big reference voltage buffers. Instead, current charge pump based circuit is employed to realize the stage transfer function. Two versions of inverter based comparators were designed for the signal path comparator and sub-ADC comparator. A 100MS/s and 8bit pipelined ADC was taped out to prove the concept. The prototype chip achieves a peak SNDR of 37.1dB and the peak SFDR is 46.7dB for a -1dBFS sinusoidal input. Maximal DNL and INL are 1LSB/-0.8LSB and 2LSB/-2.3LSB, respectively. The chip consumes 1.39mW at 100MS/s and 1V power supply. Its FOM is 237fJ/Conv. Step, which is the best compared with other 8bit ADCs of various types. This work is the first one that addresses the power consumption issue of the reference buffers by largely avoiding them, while most reported pipelined ADCs in the literature only focused on the design of the pipelined ADC itself.

4.2 Ideas for Future Work

In the ultra-low-voltage design domain, 0.5V sigma delta modulator has been proposed [44] and this thesis worked on 0.5V pipelined ADC design [11]. Other types of ADCs also need to be explored at ultra-low supply voltage, along with some other design issues that need to be further investigated.

A. Ultra-low supply successive approximation ADC, flash ADC, etc

Successive approximation and flash ADCs are two other major ADC types. The analog building blocks involved are similar to that of pipelined ADC. It is relatively straightforward to apply similar low voltage design techniques to operate successive approximation and flash ADCs under 0.5V supply voltage. Some detailed implementation issues might come up and need to be addressed.

B. High performance OTA at ultra-low supply voltage

When the supply voltage drops to 0.5V or even lower, the overdrive voltages for OTA input transistors and other transistors are squeezed to accommodate for desired common mode voltage and/or maximal output swing. Thus, the transistors are operating in moderate or even weak inversion, making the achievable OTA gain bandwidth considerably lower. Multi-stage OTA with pseudo differential pair input stage is one alternative to operate at low supply voltage, while maintaining reasonable overdrive voltage. The gain of the OTA

also starts decreasing when the transistors are pushed into linear region. Positive load impedance in parallel with negative impedance achieved by cross connected transistors could produce very high gain, but an accurate control loop is critical to tune the circuit to achieve high gain without triggering hysteresis.

C. Optimal supply voltage for analog circuits and reconfigurable design

While this work operates at a supply of 0.5V, analog circuits operating at other low voltages need to be analyzed. The tradeoff between power consumption and signal to noise ratio when scaling the power supply need to be looked into, both class A and class B circuits should be considered. In the subject of ADC design, reconfigurable supply voltage and operating frequency will make it more compatible with the digital processor, where voltage and frequency scaling are usually employed to optimize power consumption under different operating conditions.

D. Fully differential design of the charge pump based pipelined ADC

The design of a high efficient pipelined ADC without using a big reference buffer was introduced in this work, and a single ended version was implemented to prove the concept. The design suffers from noise coupling from digital circuits and other noisy sources, as indicated from the measurement results. A fully differential version needs to be developed. The current design can be naturally extended to operate differentially, but supporting build-

ing blocks, especially fully differential difference comparators for the signal path, need to be designed carefully in order not to compromise the resolution of the ADC.

E. Improved design of comparators and current sources

In the proposed approach, comparators and current sources are the main building blocks. The nonlinearity of the current source limits the achievable resolution of the ADC. Thus, a linear current source can be developed. Possibly a feedback circuit that senses the output of the current source and controls the body of the current biasing transistor can be investigated. For the comparator, effort can be focused on reducing its power consumption while achieving relatively low input referred offset. The inverter based comparator in the current design consumes considerable power during the offset calibration phase. The delay of the signal path comparator also needs to be input signal independent to achieve high resolution.

F. Alternative implementations to avoid using a big reference buffer

One of the drawbacks of the proposed structure is that its residue gain relies on the linearity of the two current source involved during the entire charging/discharging process. The third alternative scheme described in Section 3.8.2 can be further investigated, where it takes advantage of the comparator triggering point and charge conservation so that only the nonidealities after the input crosses the reference voltage is of concern. Other schemes mentioned in Section 3.8.2 are also worth more investigation.

G. Digital calibration of the pipelined ADC

While this work only involves offline static interstage gain calibration, static reference voltage calibration or even higher order nonidealities associated with current sources and comparators can be possibly calibrated in digital domain, as digital gates become cheaper and cheaper in advanced technologies. Efficient algorithms need to be studied to achieve fast convergence during digital background calibration.

Overall, the first work of the thesis proves the feasibility of ultra-low-voltage operation of the pipelined ADC, which serves as an early investigation for the near future low supply analog and mixed signal circuits. The second work addresses the issue of the power consumption associated with the reference buffers, which could possibly reduce the power consumption of the pipelined ADC dramatically. Eventually the dynamic power consumption will be dominating in the pipelined ADC. The authors hope the work done in this thesis could serve as stepping stones for further investigations.

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Appendix A

OTA Settling Consideration at Ultra Low Voltage

In this appendix, we will analyze the settling behavior of a typical two stage miller compensated OTA in a capacitive feedback configuration, and see its implication in the scenario of ultra-low supply voltage. Fig. A.1 shows the simplified OTA schematic used for the analysis, biasing circuitry is not shown here. Note that the first stage could also use a telescopic or folded cascode structure.

To see the settling behavior of the circuit shown in Fig. A.2, a step is applied at the input. In a real design, slewing effect usually comes into play and makes the output settling nonlinear. But on the other side, with proper amount of slewing, the linear settling section is largely reduced thus the error caused by it is relatively much smaller compared to the entire settling section. By taking into account slewing, the GBW requirement is calculated

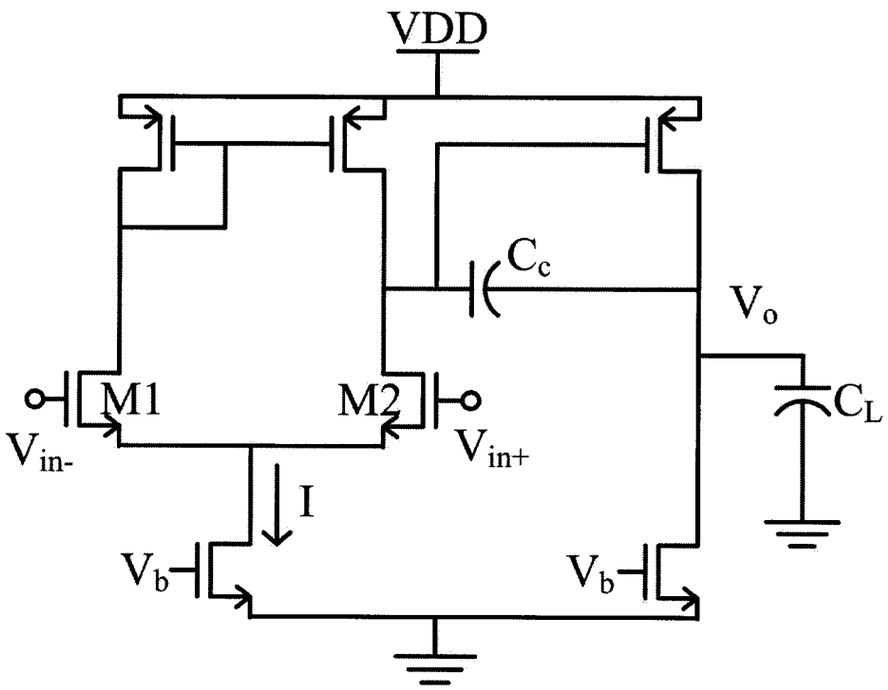

Figure A.1: A typical two stage miller compensated OTA.

below:

$$\frac{g_{m1}}{C_c} = GBW \tag{A.1}$$

$$g_{m1} = \frac{I}{V_{dsat}} \tag{A.2}$$

$$SR = \frac{I}{C_c} \tag{A.3}$$

$$SR = GBW \cdot V_{dsat} \tag{A.4}$$

$$\tau = \frac{1}{\beta \cdot GBW} \tag{A.5}$$

In the above equations, g_{m1} is the transconductance of the first stage input transistor

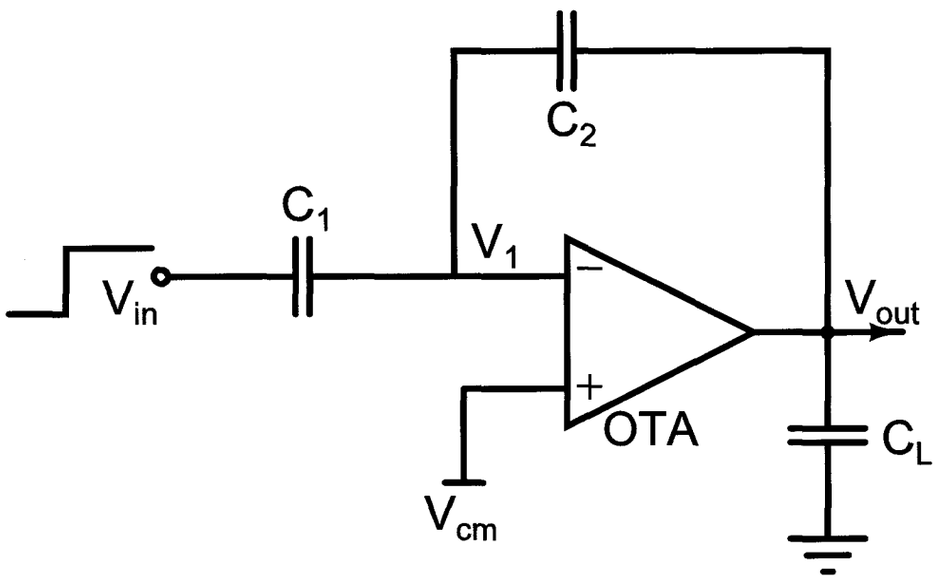

Figure A.2: OTA in a capacitive feedback configuration, step signal is applied at the input to analyze the output settling behavior.

M1/M2, I is the biasing current from the tail current source. SR stands for slew rate. The settling diagram is shown in Fig. A.3, OTA is slewing from time 0 to t_1, while from t_1 to T the circuit is settling. The following equation holds:

$$V_i = SR \cdot t_1 \tag{A.6}$$

$$\frac{V_f - V_i}{\tau} = SR \tag{A.7}$$

Note that at time instant t_1, the slope of the slewing curve is the same as that of settling

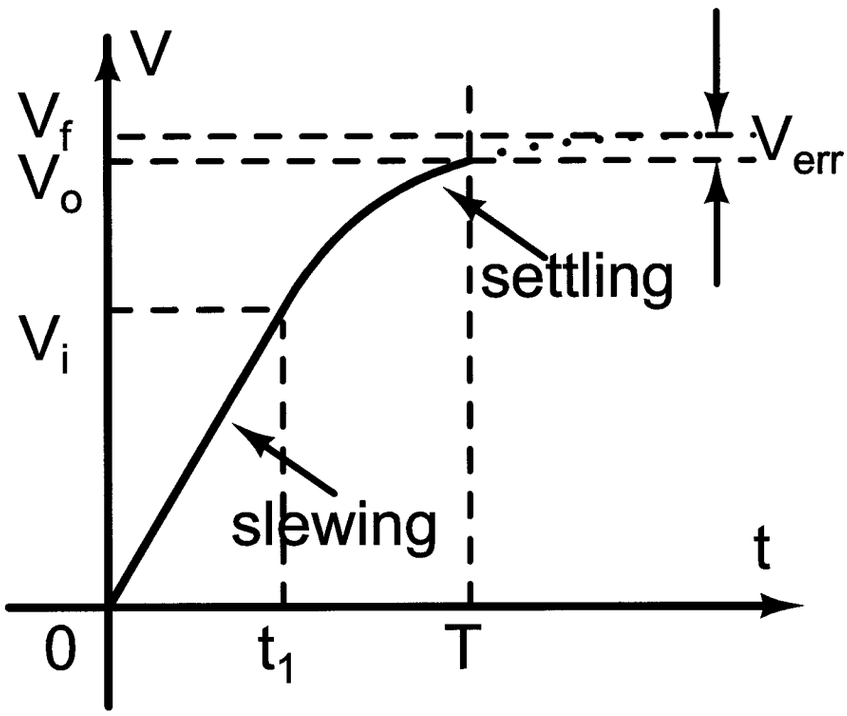

Figure A.3: OTA output slewing and linear settling.

curve, thus A.7 holds. From A.4 to A.7, we get:

$$\begin{aligned} t_1 &= \frac{V_f - SR \cdot \tau}{SR} \\ &= \frac{V_f}{GBW \cdot V_{dsat}} - \frac{1}{\beta \cdot GBW} \\ &= \frac{1}{GBW}\left(\frac{V_f}{V_{dsat}} - \frac{1}{\beta}\right) \end{aligned} \tag{A.8}$$

The equation is valid only when its solution is larger than 0. Or from another perspective, we observe that the OTA settling will be entirely linear when $V_{dsat} < \beta V_f$. In general,

output voltage in the linear settling part is governed by:

$$V_o = V_f + (V_i - V_f)e^{-\frac{T-t_1}{\tau}} \tag{A.9}$$

Where T is the available time for the circuit to settle. When A.8 is valid, output error voltage will be:

$$\begin{aligned} V_e &= V_f - V_o \\ &= (V_f - V_i)e^{-\frac{T-t_1}{\tau}} \\ &= (SR \cdot \tau)e^{-\frac{T-t_1}{\tau}} \\ &= \frac{V_{dsat}}{\beta}e^{(\frac{\beta V_f}{V_{dsat}} - T\cdot\beta\cdot GBW - 1)} \end{aligned} \tag{A.10}$$

Thus settling accuracy in terms of error voltage percentage is:

$$\begin{aligned} P_e &= \frac{V_e}{V_f} \\ &= \frac{V_{dsat}}{\beta V_f}e^{(\frac{\beta V_f}{V_{dsat}} - T\cdot\beta\cdot GBW - 1)} \\ &\approx \frac{V_{dsat}}{\beta V_f}e^{-T\cdot\beta\cdot GBW} \end{aligned} \tag{A.11}$$

This approximation holds in the case when a 0.5V power supply is used. At 0.5V, the available signal range of the OTA is about $\pm$150mV, with the output common mode set to 250mV. Thus maximum V_f should be within 150mV. V_{ds} of each transistor is about 120mV

which results in a 120x4=480mV voltage drop over four transistors when a folded cascode first stage is used. V_{dsat} is about 80mV to guarantee the ratio of V_{ds}/V_{dsat} is around 1.2-1.5 to get high output impedance without sacrificing voltage headroom. Assuming β =1/2 for a typical 1.5bit MDAC, we can simplify the expression in A.11. After rearranging A.11, the GBW requirement can be derived as:

$$\begin{aligned} GBW &= -\frac{1}{T\beta}(\ln\frac{P_e\beta V_f}{V_{dsat}} + 1 - \frac{\beta V_f}{V_{dsat}}) \\ &\approx -\frac{2}{T}\ln P_e \\ &\approx \frac{2}{T}\ln\frac{1}{P_e} \end{aligned} \tag{A.12}$$

In the case of a 0.5V supply voltage as described above, t_1 would be negative based on A.8, which means the circuit doesn't experience any slewing and thus we can't use A.12 to get the required GBW as we originally intended. The circuit shows only linear setting. This can be explained intuitively, since output swing V_f is very small, the initial slope of the linear settling equation is also small, thus it's not limited by the available biasing current and slewing is avoided. A.9 can be used directly to get the GBW requirement, where V_i and t_1 are equal to 0. For fully linear settling behavior, finite GBW only leads to fixed settling error, which is not signal dependent. This is beneficiary to ultra-low-voltage design but we need to be cautious that the linear settling is not entirely linear due to the moving bias point at the input of the OTA, which leads to slightly varying GBW as the circuit settles.