Digital Simulation using Xcelium

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Updated for Xcelium by Iain McNally

Digital Simulations Lab Instructions

For this lab you will need:

1. *A post-layout Verilog net list of the design*
   - obtained from place and route lab (wrap_qmults_final.v)

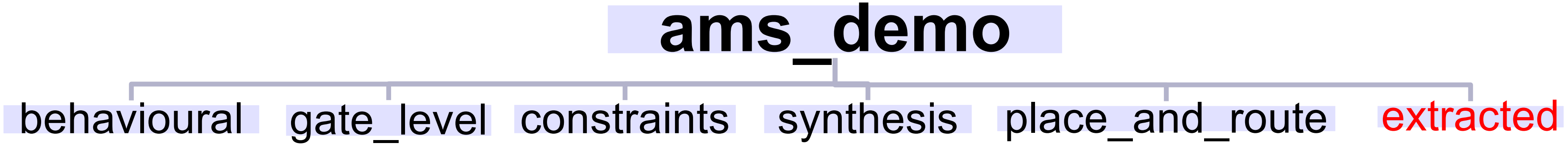
2. *A Standard Delay Format file of the design*
   - again, from place and route (wrap_qmults_func_max.sdf)

3. *A Verilog testbench*
   - the same as in synthesis lab (wrap_qmults_stim.sv)

Design Directory Management

1. Inside your design directory create a sub-directory called extracted

2. Copy the design files into extracted



ams_demo

behavioural gate_level constraints synthesis place_and_route extracted

```
cp place_and_route/wrap_qmults_final.v extracted/wrap_qmults.v

cp place_and_route/wrap_qmults_func_max.sdf extracted/

cp behavioural/wrap_qmults_stim.sv extracted/
```

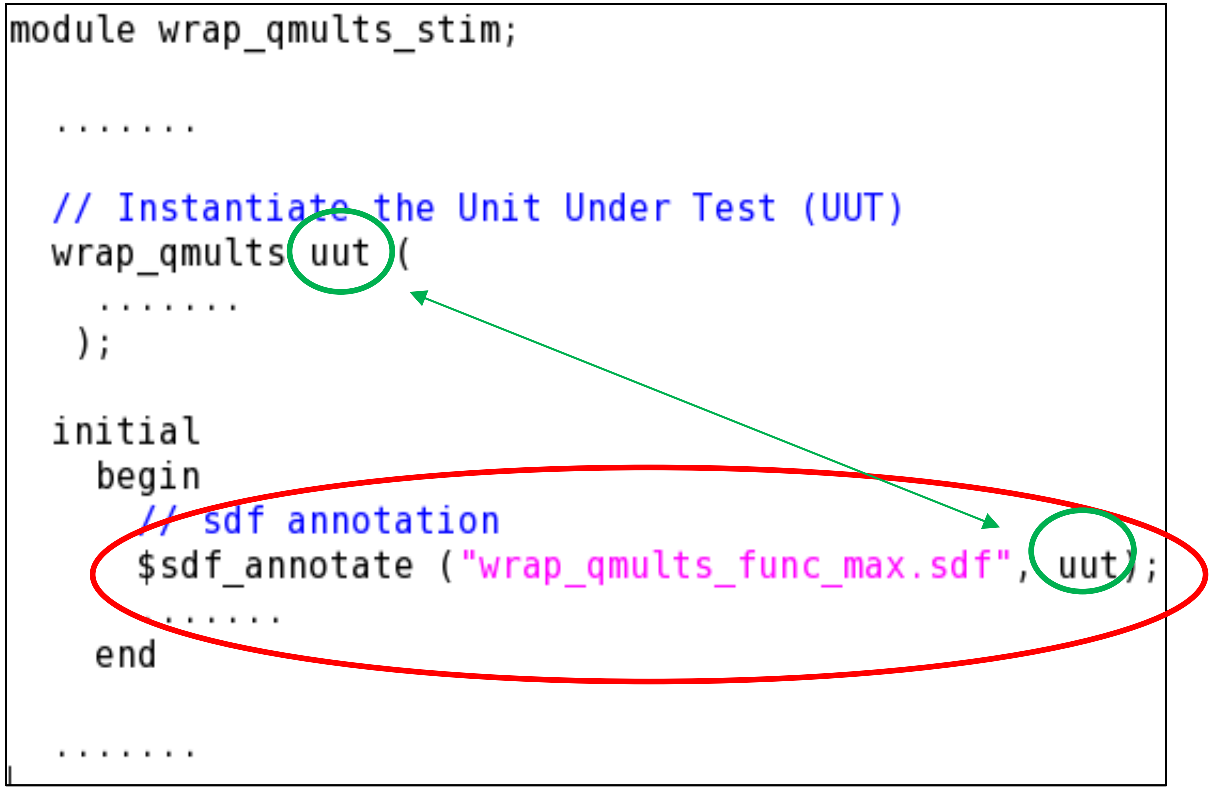
Introduction

- The simulator we are going to use in this lab is Cadence Xcelium (xmverilog)

- Before we run the simulation, there are some modifications you need to make …

SDF Annotation

- **In order to simulate your design with correct delays, you need to annotate the .sdf file, in the testbench:**



```
module wrap_qmults_stim;

  .......

  // Instantiate the Unit Under Test (UUT)
  wrap_qmults uut (
    .......
   );

  initial
    begin
      // sdf annotation
      $sdf_annotate ("wrap_qmults_func_max.sdf", uut);
      .......
    end

  .......
```

- **Make sure you annotate the .sdf for the right instance**

Timescale

- **xmverilog expects all modules to have timescales specified (whether or not any delays are used in the module).**
- **For the wrap_qmults.v Verilog file, we must set a default timescale using following xmverilog option:**

+xmtimescale+<*timeunit*>/<*timeprecision*>

Run Simulation

- Now you can simulate your design by following command:

```
xmverilog +naccess+r +xmtimescale+1ns/10ps -f
/opt/cad/designkits/ams/v410/verilog/c35b4/verilogin.inc
wrap_qmults_stim.sv wrap_qmults_final.v
```

- The circuit under test is a multiplier. Thus the functionality can be easily verified by observing the waves.