Minilab 2: Report

Erin Moon <limarshall@wisc.edu>

September 18, 2022

We were tasked with implementing a registered MAC, specified in the Minilab 2 slides. My implementation is extremely rudimentary; the datapath is expressed directly with SV signed arithmetic, and we simply hope the synthesizer does a good job for us. I did, however, split out individual intermediate products such that it would be easier to replace arithmetic with direct DSP instantiations or other FPGA-specific magic.

The state space of the MAC is given, ignoring sequential logic, by $\mathcal{S} = \{0,1\}^{\texttt{WIDTH\_AB}} \times \{0,1\}^{\texttt{WIDTH\_AB}} \times \{0,1\}^{\texttt{WIDTH\_C}}$, with

$$\operatorname{card} \mathcal{S} = 2^{2(\texttt{WIDTH\_AB})+\texttt{WIDTH\_C}} = 2^{32}$$

(for default parameters). While this is exhaustively enumerable in test, it is not particularly performant to do so, especially as MAC size increases; moreover, we don't need to know that *multiplication* works, as much as we need to know the sequential behavior of the unit is correct.

As such, my test plan has three main phases. First, I run a small number of randomized test vectors ($\sim 2^8$) through the MAC to test arithmetic, with all registers enabled; the `WrEn` mux is also tested. Secondly, I test disabling registers by deasserting `en` in a single case; and lastly, I test that an in-operation deassertion of `rst_n` resets all registers to the zero vector. Note that all checks are made via SystemVerilog assertions, rather than manual "self-checking" testbench error tracking.

Running vsim against `tpumac.sv`, `tpumac_tb.sv` produces no errors, warnings, nor assertions. I recorded coverage via `+cover=bcestf` passed to Questa `vlog` and `-coverage -coverstore ...` passed to `vsim`, merged the coverstore to a UCDB with `vcover`, and obtained an overall functional coverage on the DUT of

```
  ~/ece554/ece554_miniproject tux-134
» /cae/apps/data/mentor-2022/questasim/bin/vcover report -assert
↪  -code bcestf -annotate -instance='/tpumac_tb/dut'
↪  xwork/questa/coverout.ucdb
QuestaSim vcover 2021.2_2 Coverage Utility 2021.06 Jun 19 2021
Start time: 23:42:11 on Sep 18,2022
vcover report -assert -code bcestf -annotate
↪  -instance=/tpumac_tb/dut xwork/questa/coverout.ucdb
```

Coverage Report Summary Data by instance

```
================================================================================
=== Instance: /tpumac_tb/dut
=== Design Unit: work.tpumac
================================================================================
    Enabled Coverage  Bins Hits Misses  Coverage
    ----------------  ---- ---- ------  --------
    Branches             8    8      0   100.00%
    Statements          10   10      0   100.00%
    Toggles            200  200      0   100.00%


Total Coverage By Instance (filtered view): 100.00%
```