EHB-311E

Experiment-1

Name: Başar Demir

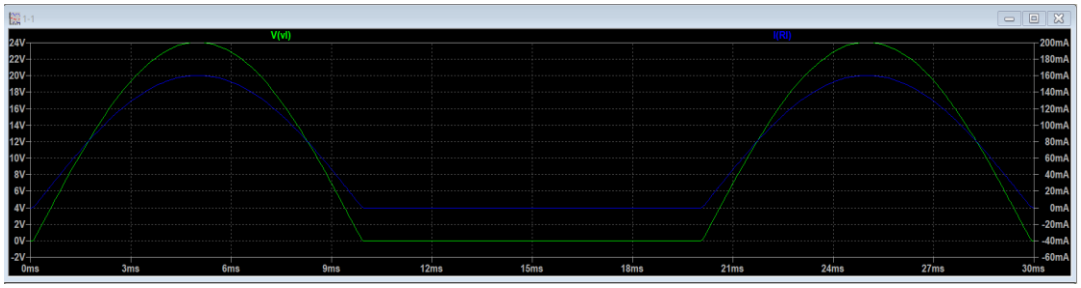
Student Number:150180080

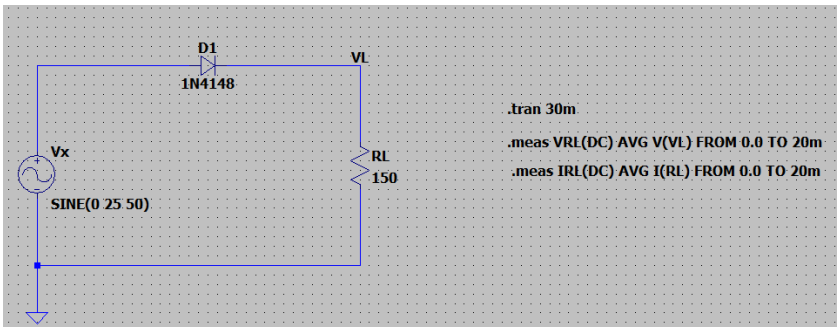
Part-1

In this circuit, diode prevents reverse current flow. Then, only positive voltage can pass through the diode, that is why it called half wave rectifier. It only allows to pass half of the voltage and current wave. Therefore, we use them for AC to DC transformation.

Difference of theoretical and measured result is occurred because of the diode. Diode cannot be ideal in real world, then it has resistance while using it.

	A_m	A_m / π	Measured
V(RL)	25V	7.95774715459	7.54179
I(RL)	25/150=0.166666A	0.05305164769	0.0502786



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SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-1.log
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-1.asc

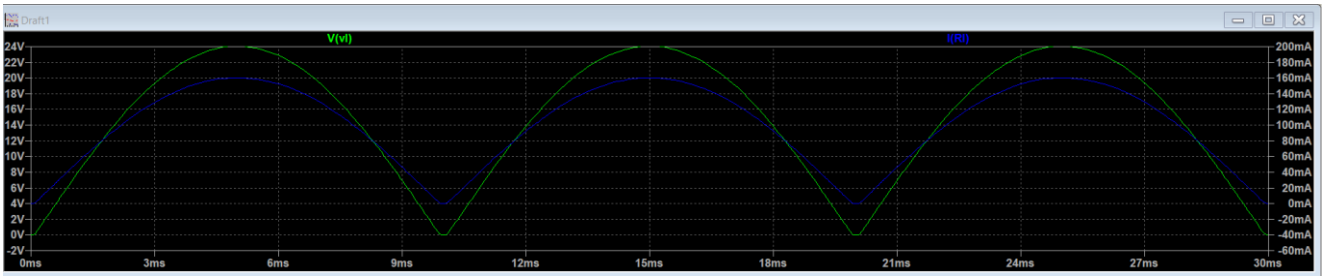
.OP point found by inspection.

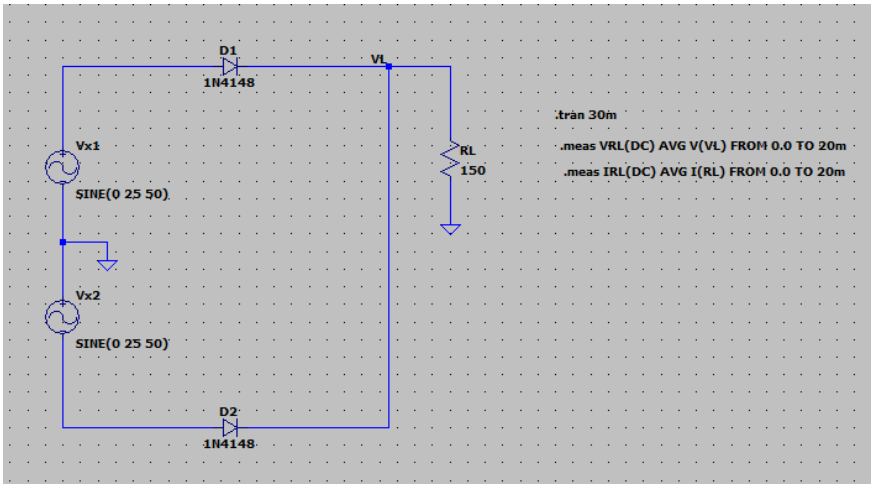
vrl(dc): AVG(v(vl))=7.54179 FROM 0 TO 0.02
irl(dc): AVG(i(rl))=0.0502786 FROM 0 TO 0.02


Date: Wed Nov 11 14:30:39 2020
Total elapsed time: 0.203 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2226
traniter = 2226
tranpoints = 1088
accept = 1070
rejected = 18
matrix size = 4
fillins = 0
solver = Normal
Matrix Compiler1: 118 bytes object code size  0.0/0.0/[0.0]
Matrix Compiler2: off  [0.0]/0.1/0.0
```

Part-2





SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-2.log

```
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-2.asc

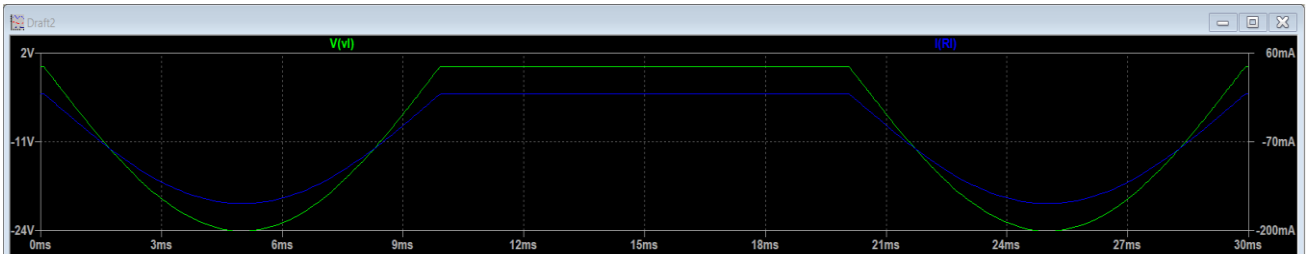
.OP point found by inspection.

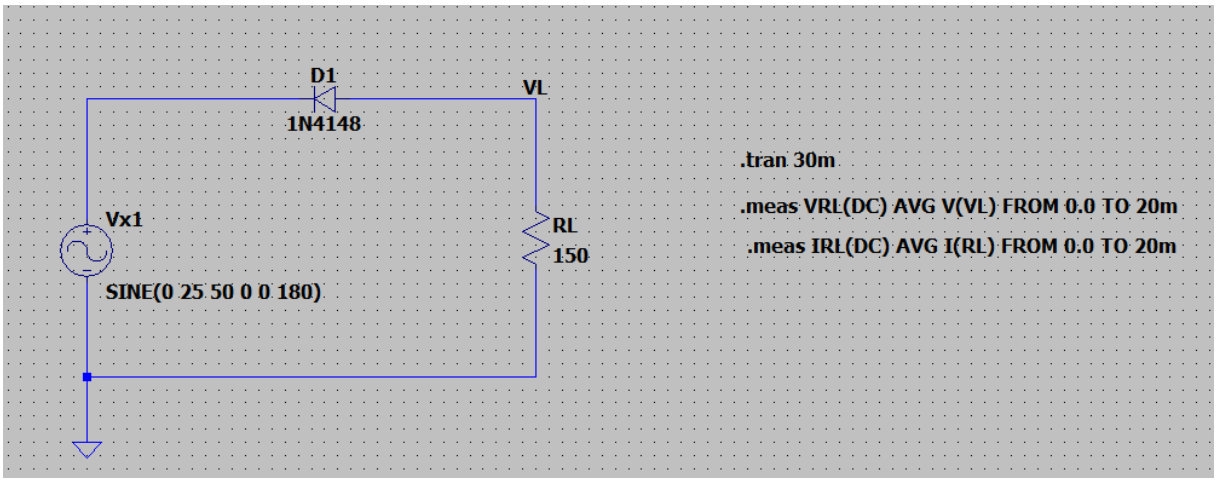
vrl(dc): AVG(v(vl))=15.0835 FROM 0 TO 0.02
irl(dc): AVG(i(rl))=0.100557 FROM 0 TO 0.02


Date: Wed Nov 11 14:31:58 2020
Total elapsed time: 0.164 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2314
traniter = 2314
tranpoints = 1116
accept = 1086
rejected = 30
matrix size = 7
fillins = 0
solver = Normal
Matrix Compiler1: 214 bytes object code size  0.1/0.1/[0.0]
Matrix Compiler2: 447 bytes object code size  0.1/0.1/[0.0]
```

Part-3





SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-3.log

```
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-3.asc

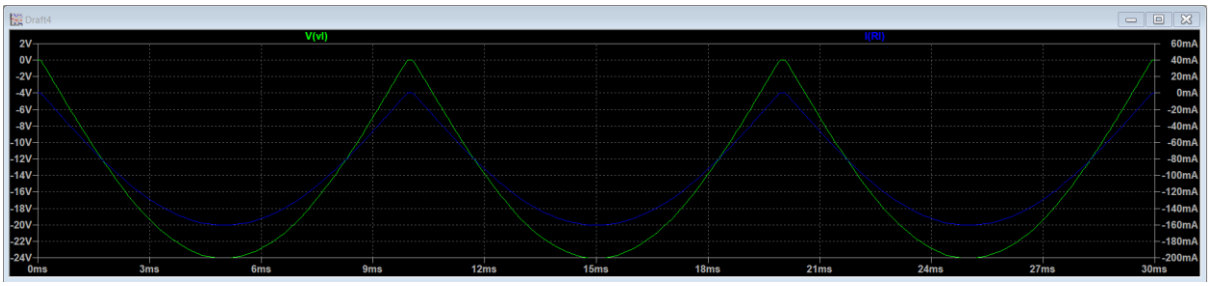
Direct Newton iteration for .op point succeeded.

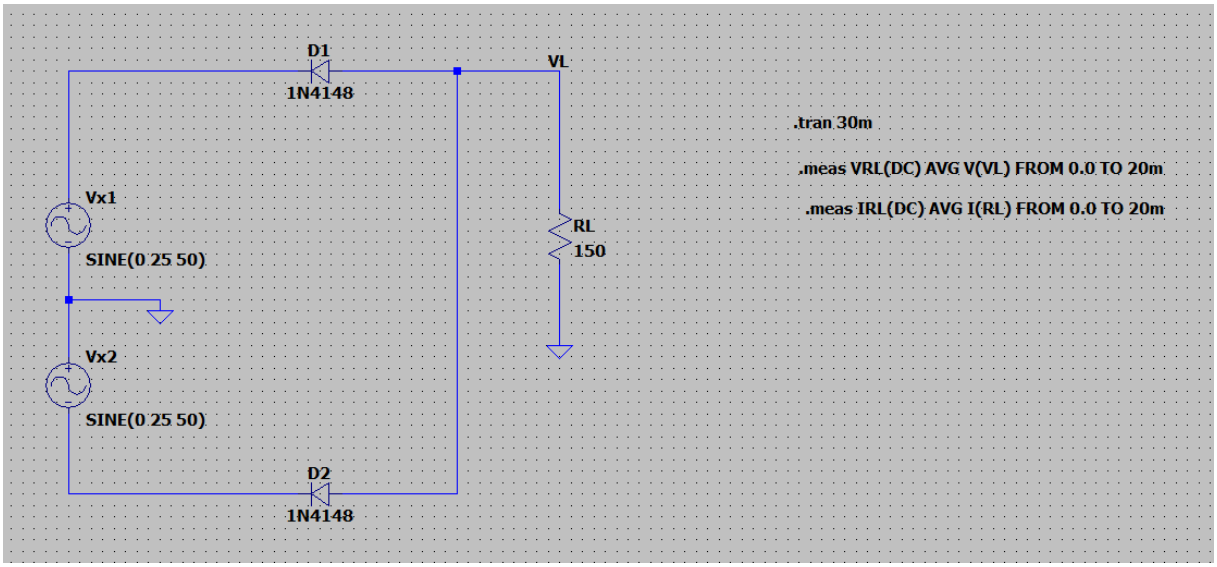
vrl(dc): AVG(v(vl))=-7.54179 FROM 0 TO 0.02
irl(dc): AVG(i(rl))=-0.0502786 FROM 0 TO 0.02


Date: Wed Nov 11 14:32:58 2020
Total elapsed time: 0.191 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2234
traniter = 2226
tranpoints = 1088
accept = 1070
rejected = 18
matrix size = 4
fillins = 0
solver = Normal
Matrix Compiler1:       6 opcodes  0.1/[0.0]/0.0
Matrix Compiler2: 248 bytes object code size  0.0/0.0/[0.0]
```

Part-4






```
Circuit: * C:\Users\BASAR-PC\Desktop\ele giriş lab\1-4.asc

.OP point found by inspection.

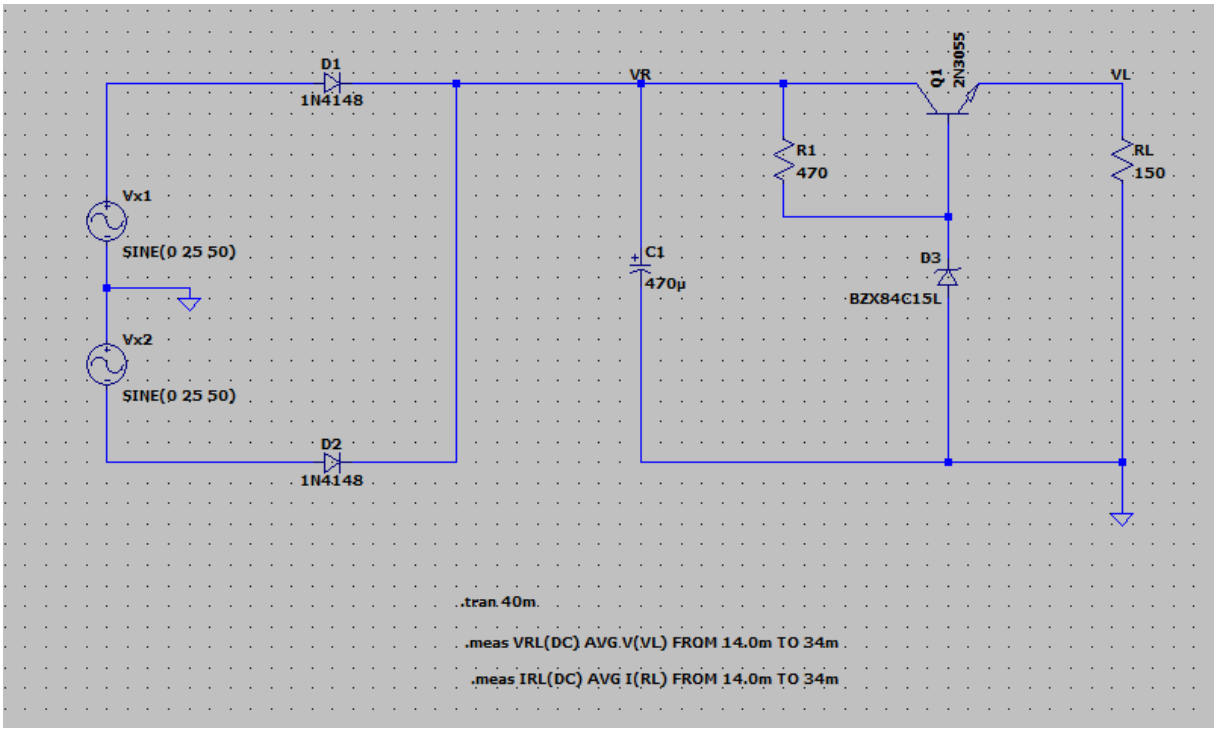
vrl(dc): AVG(v(vl))=-15.0835 FROM 0 TO 0.02
irl(dc): AVG(i(rl))=-0.100557 FROM 0 TO 0.02


Date: Wed Nov 11 00:13:31 2020
Total elapsed time: 0.232 seconds.

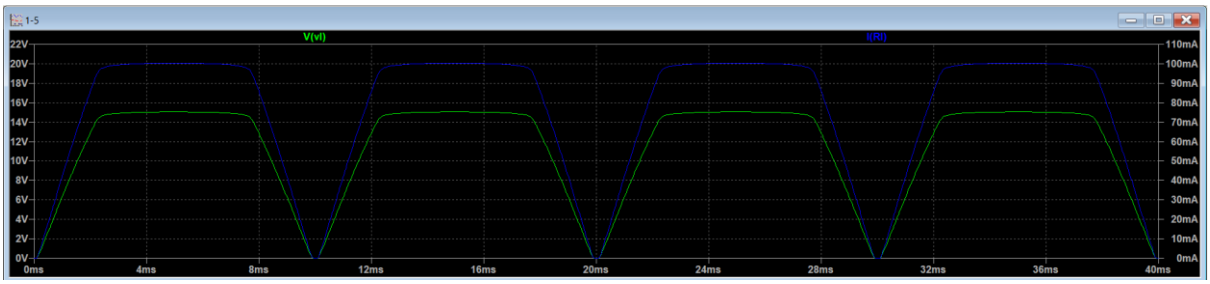
tnom = 27
temp = 27
method = modified trap
totiter = 2314
traniter = 2314
tranpoints = 1116
accept = 1086
rejected = 30
matrix size = 7
fillins = 0
solver = Normal
Matrix Compiler1: 196 bytes object code size  0.1/0.1/[0.0]
Matrix Compiler2: off  [0.1]/0.1/0.1
```

Part-5

This circuit has three parts that are rectifier, filter and regulator. Rectifier works as full wave such as second experiment. Then, we get dc voltage with waves. Capacitor reduces ripple of this wave. If we increase the capacitor size, it gives stronger support to reducing voltage waving but it takes more time to charge for first time. BJT and Zener diode provides keeping voltage output constant. At the end, we get constant DC voltage.



Simulation for C=0



SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-5.log

```
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-5.asc

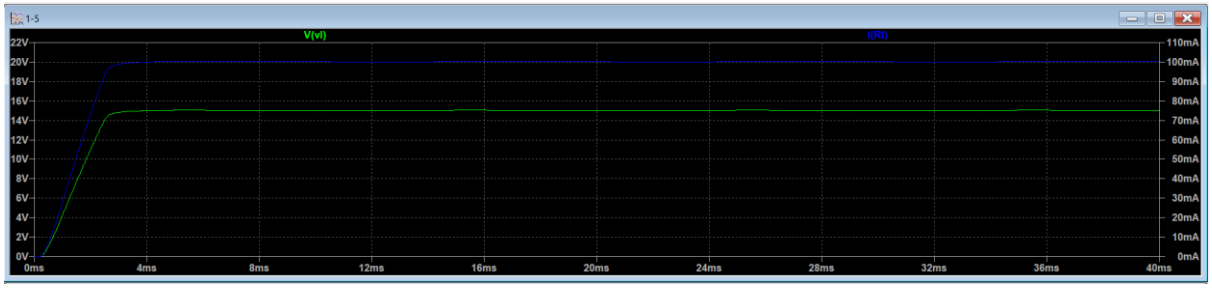
.OP point found by inspection.

vrl(dc): AVG(v(vl))=11.3862 FROM 0.014 TO 0.034
irl(dc): AVG(i(rl))=0.0759079 FROM 0.014 TO 0.034


Date: Wed Nov 11 13:36:02 2020
Total elapsed time: 0.142 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2682
traniter = 2682
tranpoints = 1246
accept = 1180
rejected = 66
matrix size = 13
fillins = 0
solver = Normal
Matrix Compiler1:      42 opcodes  0.1/[0.1]/0.1
Matrix Compiler2: off  [0.1]/0.1/0.1
```

Simulation for C= 470uF



SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-5.log

```
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-5.asc

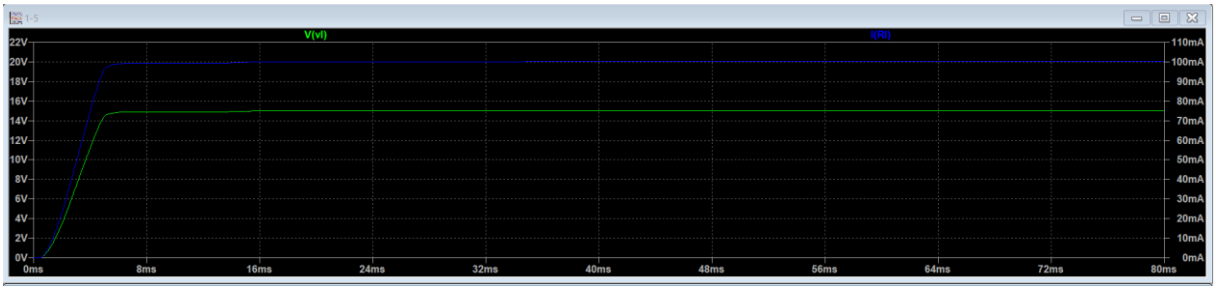
.OP point found by inspection.

vrl(dc): AVG(v(vl))=15.0257 FROM 0.014 TO 0.034
irl(dc): AVG(i(rl))=0.100172 FROM 0.014 TO 0.034


Date: Wed Nov 11 13:31:52 2020
Total elapsed time: 0.186 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2401
traniter = 2401
tranpoints = 1152
accept = 1122
rejected = 30
matrix size = 13
fillins = 0
solver = Normal
Matrix Compiler1: 736 bytes object code size  0.7/0.1/[0.1]
Matrix Compiler2: 993 bytes object code size  0.8/0.8/[0.1]
```

Simulation for C= 4700uF



SPICE Error Log: C:\Users\BASAR-PC\Desktop\lab1\1-5.log

```
Circuit: * C:\Users\BASAR-PC\Desktop\lab1\1-5.asc

.OP point found by inspection.

vrl(dc): AVG(v(vl))=15.0011 FROM 0.014 TO 0.034
irl(dc): AVG(i(rl))=0.100008 FROM 0.014 TO 0.034


Date: Wed Nov 11 14:58:02 2020
Total elapsed time: 0.151 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2875
traniter = 2875
tranpoints = 1319
accept = 1236
rejected = 83
matrix size = 13
fillins = 0
solver = Normal
Matrix Compiler1: 736 bytes object code size  0.2/0.1/[0.1]
Matrix Compiler2: 993 bytes object code size  0.1/0.1/[0.1]
```