

Basel Shbita

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EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA PH.D. STUDENT, COMPUTER SCIENCE

2018 - Present | Los Angeles, California, USA

Research Interests: Information Integration,
Artificial Intelligence, Knowledge Graphs,
Semantic Modeling, Machine Learning

TEL AVIV UNIVERSITY

BSC. ELECTRICAL ENGINEERING

2011 - 2015 | Tel Aviv, Israel

Specialization Areas: Computer Science,
Communications and Electronic Devices
magna cum laude. GPA: 93.33

ISRAEL ARTS AND SCIENCE ACADEMY

2007 - 2010 | Jerusalem, Israel

High-School Major in Computer Science,
Physics and Chemistry
cum laude

INTERNSHIPS

RESEARCH SCIENCE INSTITUTE

RESEARCH INTERN (COMPUTER SCIENCE)

2009 | Cambridge, MA, USA

Studied and practiced Statistical Natural
Language Processing, Automatic Speech
Recognition and Machine Learning.
Research hosted by HP Autonomy & MIT

AWARDS

TEL AVIV UNIVERSITY

FACULTY DEAN'S LIST OF OUTSTANDING
UNDERGRADUATE STUDENTS

2013 | Tel Aviv, Israel

"FREESCALE SEMICONDUCTOR ISRAEL"
EXCELLENCE SCHOLARSHIP

2013 | Tel Aviv, Israel

SKILLS

LANGUAGES

Arabic • Hebrew • English • Russian

PROGRAMMING

Proficient:

C++ • C • Python • Unix Shell & Bash

Experienced:

C# • MATLAB • VHDL • Assembly

Familiar:

Ruby on Rails • HTML • CSS • JavaScript

HOBBIES

Combined Martial Arts • Graphic Design
• Soccer • Music Production

EXPERIENCE

INFORMATION SCIENCES INSTITUTE

2018 - PRESENT

RESEARCH ASSISTANT

Aug 2018 – Present | Marina del Rey, California, USA

- Studying Data Extraction/Transformation, Artificial Intelligence and Machine Learning techniques to solve complex information integration problems

APPLE

2018

EMBEDDED FIRMWARE ENGINEER

Jan 2018 – June 2018 | Herzliya, Israel

- Designed, developed and implemented complex SW modules for Apple products

MELLANOX TECHNOLOGIES

2011 - 2017

SENIOR FIRMWARE ENGINEER & TEAM LEADER, SWITCH SILICON CORE DEPARTMENT

Apr 2017 – June 2017 | Tel Aviv, Israel

- Managed team of 5 engineers
- Led the 100GbE Switch Systems firmware development process and verification activities - an agile operation involving 16 engineers
- Developed a distributed functional testing environment, debug tools and performance testing in C++ in Unix for both Ethernet and InfiniBand fabrics in Data-Link and Network layers of the OSI (static and dynamic analysis)
- Conducted technical presentations to 50+ developers from various teams
- Awarded for excellence and ranked "Superior" (top 5% out of 3000)

TEAM LEADER FIRMWARE ENGINEER, SWITCH SILICON CORE DEPARTMENT

May 2015 – Mar 2017 | Tel Aviv, Israel

- Managed team of 3 engineers
- Contributed to end-to-end development for the company's 100GbE Switch products and led a full silicon bring-up process: Pre and Post-Silicon
- Conducted personal training, code reviews; defined coding-style and methodologies of software engineering for team of 30
- Optimized shared library cross-platform code, resulting in 40% reduction in project compilation time for 90+ department developers
- Supervised remote testing processes operating in China & USA
- Interviewed and effectively participated in the hiring of employees
- Represented company in the 2016 VSF Interoperability Event (TX, USA)

FIRMWARE ENGINEER, SWITCH SILICON CORE DEPARTMENT

Mar 2014 – Apr 2015 | Tel Aviv, Israel

- Achieved 2nd place in Hackathon; Project introduced simulation tool saving up to 50% time in development cycle & customer support
- Developed "Stress" tool that has become major tool for system production/screening, power measurements and debug process
- Created training-program for new employees and conducted daily technical and architectural guidance and coding assistance
- Represented company in the 26th IBTA Plugfest (NH, USA) & HVC15 (Haifa)

FIRMWARE STUDENT, SWITCH SILICON CORE DEPARTMENT

Oct 2011 – Feb 2014 | Tel Aviv, Israel

- Developed ANSI-C compiler-specific code to run on Switch Systems RISC
- Managed and optimized Python-based regression system
- Implemented cross-platform error-injection and functional-validity tool used by both departments of Switch Systems and Channel Adapters
- Collaborated with chip-design and software engineers to create a Post-Silicon Random Verification Environment for the 56GbE and EDR (100Gbps Infiniband) technologies