SPI Read timing diagram

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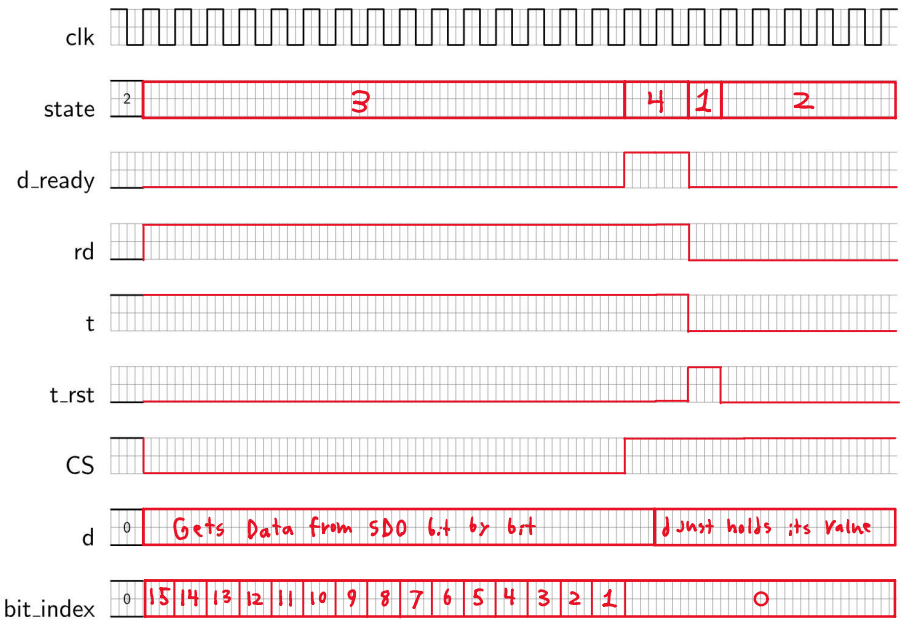

Timing diagram template

state of SPI read

data ready from SPI

read command from controller

timer done to SCLK

rst timer, set in states

SPI output

data from SPI bit

bit index of data
tracks which bit is active

This diagram assumes Ø delay.

input rd stays at 1 for an extra clock cycle to show the SPI FSM stays in state 4 until rd = Ø