User Guide for 8CBC2Flex interface board to GLIB test system

1. Introduction

The main purpose of this interface board is to connect to the 8CBC2Flex prototype on a flexible ZIF(Zero Insertion Force) FFC(Flexible Flat Connector). The signals from and to the prototype board have to be translated to the appropriate voltage levels and signalling formats. The interface board is also powering the prototype board and it has a probe connector to probe the signals from the Flex prototype.

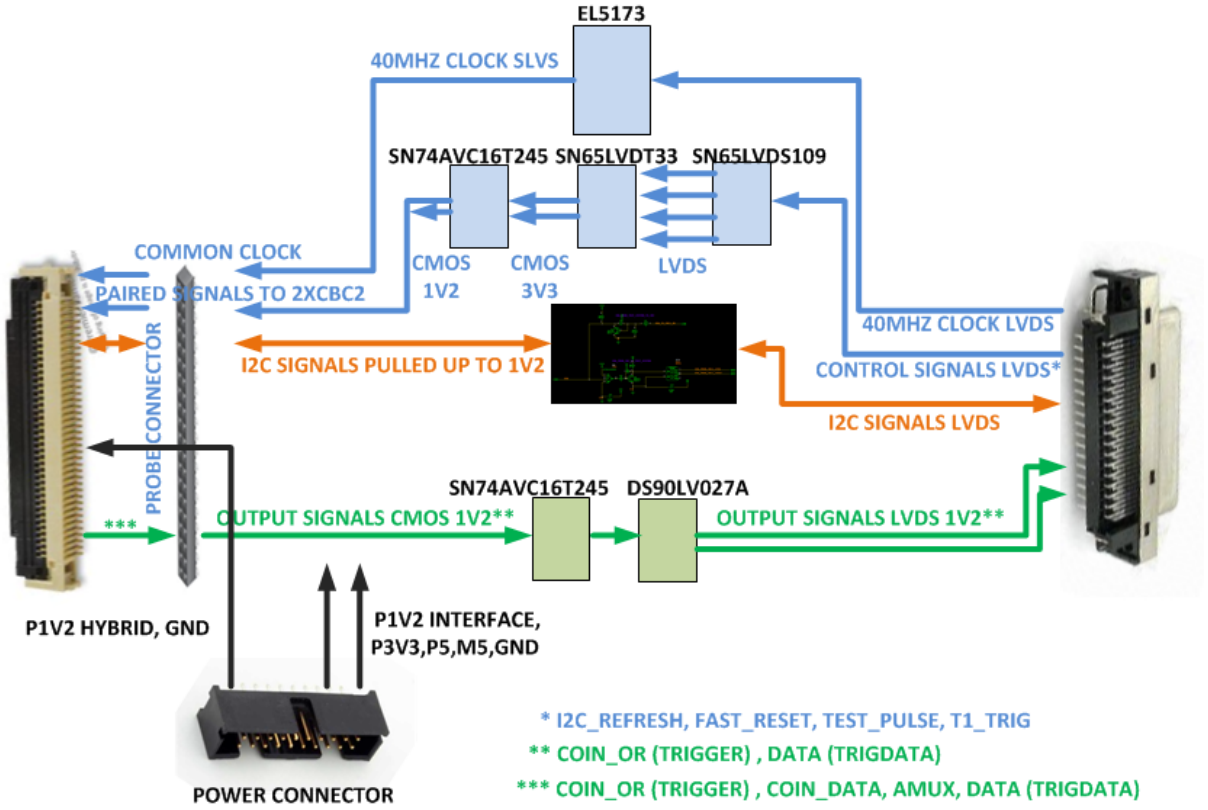

Figure 1: Block diagram of the interface board

2. Connectors

The interface board has 3 connectors. One power connector is for powering the interface board and the flex prototype. One FPC connector to connect the flex prototype and one VHDCI 68 pin connector to connect the FMC card from the GLIB test system.

The VHDCI connector has 4 GND connections 6 floating pairs (these pairs are allocated for the individual SDA bus per chip pairs, this is unused in this system). It's possible the mount termination resistor for these floating pairs to connect them to GND. All signals connected to VHDCI connector are LVDS signals.

PIN NO.	SIGNAL NAME	DESCRIPTION
1	CLKIN_40_LVDS	40 MHZ COMMON CLOCK TO CBC2
2	GND	
3	SCL_TO_CBC2_LVDS	COMMON I2C CLOCK TO CBC2
4	RESET_LVDS	COMMON RESET TO CBC2
5	I2C_REFRESH_LVDS_COMMON	I2C REFRESH CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S
6	TEST_PULSE_LVDS_COMMON	TEST PULSE CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S
7	FAST_RESET_LVDS_COMMON	FAST RESET CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S
8	T1_TRIGGER_LVDS_COMMON	L1 TRIGGER CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S
9	TRIGGER_CBC2_A_LVDS<0>	INDIVIDUAL SIGNAL FROM EACH CBC2
10	SDA_TO_CBC2_LVDS	COMMON I2C DATA BUS TO CBC2 (WARNING see note 1)
11	TRIGDATA_CBC2_A_LVDS<0>	INDIVIDUAL SIGNAL FROM EACH CBC2
12	TRIGGER_CBC2_B_LVDS<0>	INDIVIDUAL SIGNAL FROM EACH CBC2
13	SDA_FROM_CBC2_LVDS	COMMON I2C DATA BUS FROM CBC2
14	TRIGDATA_CBC2_B_LVDS<0>	INDIVIDUAL SIGNAL FROM EACH CBC2
15	CLK_DC_DC_LVDS	NOT USED ON THIS BOARD, TERMINATED ON 100OHMS
16	TRIGGER_CBC2_A_LVDS<1>	INDIVIDUAL SIGNAL FROM EACH CBC2
17	FLOATING	SDA_TO_CBC2_LVDS_DUMMY<0>
18	TRIGDATA_CBC2_A_LVDS<1>	INDIVIDUAL SIGNAL FROM EACH CBC2
19	TRIGGER_CBC2_B_LVDS<1>	INDIVIDUAL SIGNAL FROM EACH CBC2
20	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY<0>
21	TRIGDATA_CBC2_B_LVDS<1>	INDIVIDUAL SIGNAL FROM EACH CBC2
22	TRIGGER_CBC2_A_LVDS<2>	INDIVIDUAL SIGNAL FROM EACH CBC2
23	FLOATING	SDA_TO_CBC2_LVDS_DUMMY<1>
24	TRIGDATA_CBC2_A_LVDS<2>	INDIVIDUAL SIGNAL FROM EACH CBC2
25	TRIGGER_CBC2_B_LVDS<2>	INDIVIDUAL SIGNAL FROM EACH CBC2
26	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY<1>
27	TRIGDATA_CBC2_B_LVDS<2>	INDIVIDUAL SIGNAL FROM EACH CBC2
28	GND	
29	TRIGGER_CBC2_A_LVDS<3>	INDIVIDUAL SIGNAL FROM EACH CBC2
30	FLOATING	SDA_TO_CBC2_LVDS_DUMMY<2>
31	TRIGDATA_CBC2_A_LVDS<3>	INDIVIDUAL SIGNAL FROM EACH CBC2
32	TRIGGER_CBC2_B_LVDS<3>	INDIVIDUAL SIGNAL FROM EACH CBC2
33	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY<2>

34	TRIGDATA_CBC2_B_LVDS<3>	INDIVIDUAL SIGNAL FROM EACH CBC2
35	CLKIN_40_LVDS*	40 MHZ COMMON CLOCK TO CBC2 NEGATIVE NODE
36	GND	
37	SCL_TO_CBC2_LVDS*	COMMON I2C CLOCK TO CBC2 NEGATIVE NODE
38	RESET_LVDS*	COMMON RESET TO CBC2 NEGATIVE NODE
39	I2C_REFRESH_LVDS_COMMON*	I2C REFRESH CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S NEGATIVE NODE
40	TEST_PULSE_LVDS_COMMON*	TEST PULSE CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S NEGATIVE NODE
41	FAST_RESET_LVDS_COMMON*	FAST RESET CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S NEGATIVE NODE
42	T1_TRIGGER_LVDS_COMMON*	L1 TRIGGER CONNECTED TO FANOUT TO DRIVE 4 GROUPS OF 2CBC2-S NEGATIVE NODE
43	TRIGGER_CBC2_A_LVDS*<0>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
44	SDA_TO_CBC2_LVDS*	COMMON I2C DATA BUS TO CBC2 NEGATIVE NODE
45	TRIGDATA_CBC2_A_LVDS*<0>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
46	TRIGGER_CBC2_B_LVDS*<0>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
47	SDA_FROM_CBC2_LVDS*	COMMON I2C DATA BUS FROM CBC2 NEGATIVE NODE
48	TRIGDATA_CBC2_B_LVDS*<0>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
49	CLK_DC_DC_LVDS*	
50	TRIGGER_CBC2_A_LVDS*<1>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
51	FLOATING	SDA_TO_CBC2_LVDS_DUMMY*<0>
52	TRIGDATA_CBC2_A_LVDS*<1>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
53	TRIGGER_CBC2_B_LVDS*<1>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
54	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY*<0>
55	TRIGDATA_CBC2_B_LVDS*<1>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
56	TRIGGER_CBC2_A_LVDS*<2>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
57	FLOATING	SDA_TO_CBC2_LVDS_DUMMY*<1>
58	TRIGDATA_CBC2_A_LVDS*<2>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
59	TRIGGER_CBC2_B_LVDS*<2>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
60	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY*<1>
61	TRIGDATA_CBC2_B_LVDS*<2>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
62	GND	
63	TRIGGER_CBC2_A_LVDS*<3>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
64	FLOATING	SDA_TO_CBC2_LVDS_DUMMY*<2>
65	TRIGDATA_CBC2_A_LVDS*<3>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
66	TRIGGER_CBC2_B_LVDS*<3>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE
67	FLOATING	SDA_FROM_CBC2_LVDS_DUMMY*<2>
68	TRIGDATA_CBC2_B_LVDS*<3>	INDIVIDUAL SIGNAL FROM EACH CBC2 NEGATIVE NODE

Table 1: Pin assignment of VHDCI connector

Note 1: SDA_TO_CBC2_LVDS must be inverted polarity due to a hardware design issue.

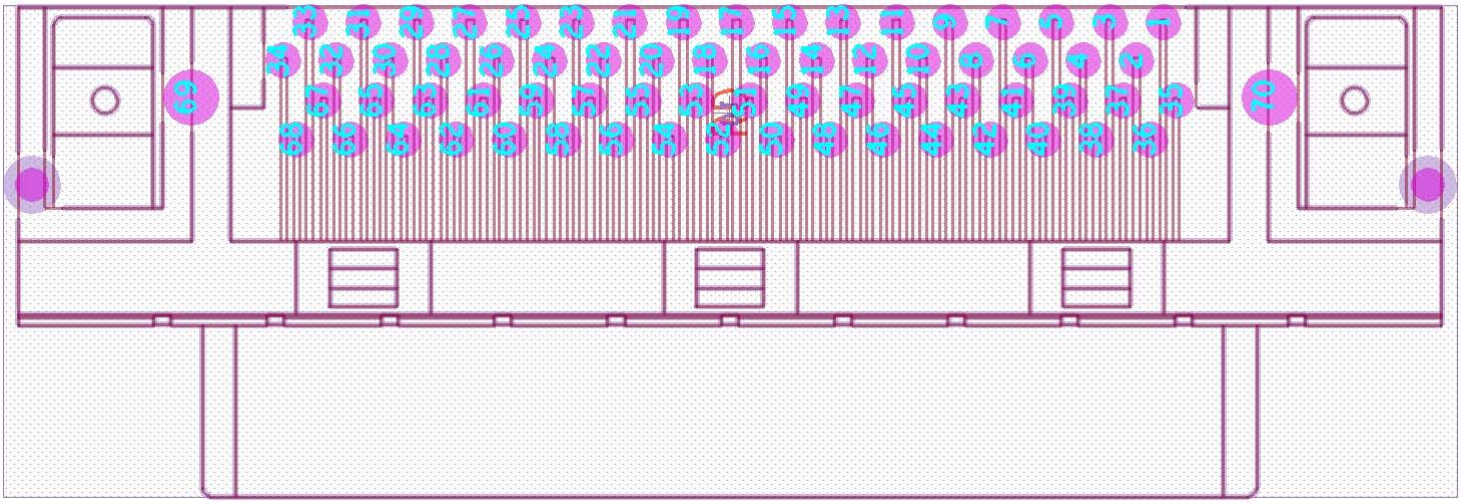

Figure 2: Pin layout of VHDCI 68 pin connector

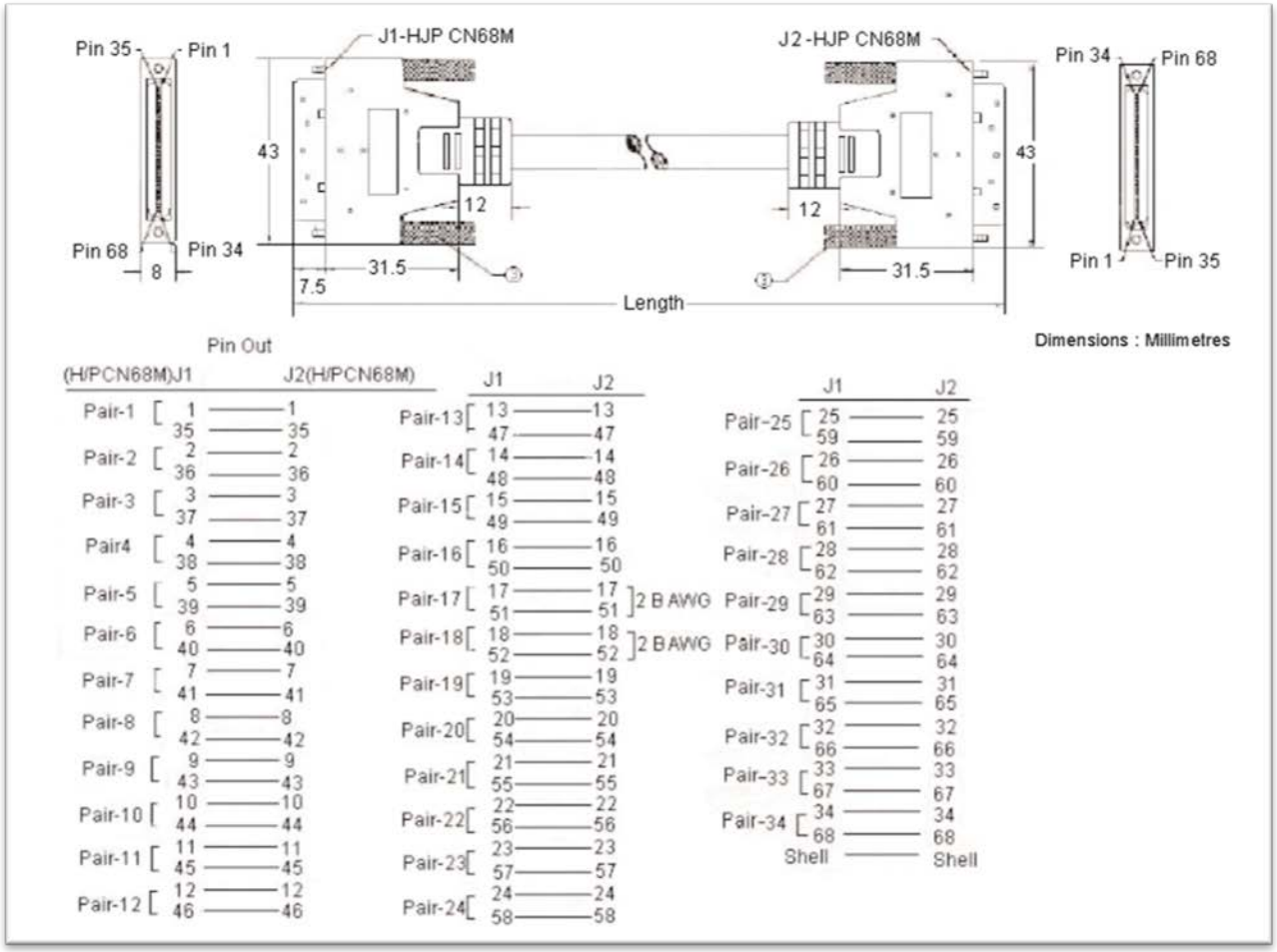

Figure 3: Standard VHDCI 68 Pin cable assignment

The power connector is a 20 pin Samtec right angle connector (find datasheets and part numbers in "ordered components XLS on sharepoint site.) It's mating connector is Molex 90142-0020 or similar connectors are also applicable.

Figure 4: Molex 20 pin mating power connector

Pin no.	Voltage
1	-5 V
3	+5 V
5;7	+3,3V
9;11;13;15	1,2V for 8CBC2 flex
17;19	1,2V for interface board
2;4;6;8;10;12;14;16;18;20	Common GND

Table 2: Pin assignment of Power connector on the PCB

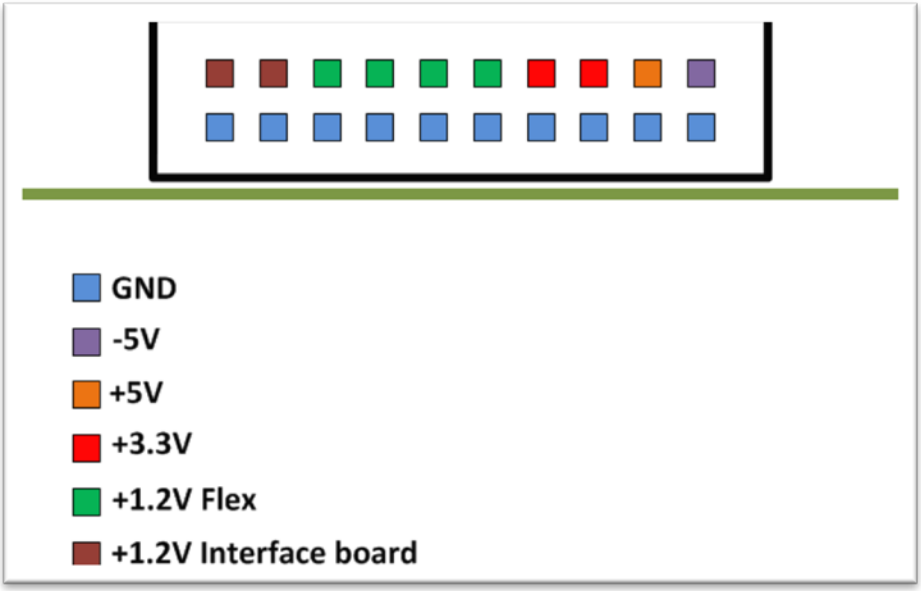

Figure 5: Pin assignment of power connector on the PCB

The FPC connector located on the bottom of the interface board. This connector is very fragile and only suitable for 20-25 cycles. Please read the instructions manual (uploaded to the sharepoint site) of the connector before connecting the flex prototype. The part number of the used connector is Molex 502790-8091.

Figure 6: The FPC connector

Pin no.	Signal name	Pin no.	Signal name
1	GND	41	GND
2	T1_TRIG_4	42	GND
3	FAST_RESET_4	43	CBC2_3_B_DATA
4	TEST_PULSE_4	44	CBC2_3_B_COIN_DATA
5	I2C_REFRESH_4	45	CBC2_3_B_AMUX
6	GND	46	CBC2_3_B_COIN_OR
7	T1_TRIG_3	47	GND
8	FAST_RESET_3	48	CBC2_3_A_DATA
9	TEST_PULSE_3	49	CBC2_3_A_COIN_DATA
10	I2C_REFRESH_3	50	CBC2_3_A_AMUX
11	GND	51	CBC2_3_A_COIN_OR
12	T1_TRIG_2	52	GND
13	FAST_RESET_2	53	CBC2_2_B_DATA
14	TEST_PULSE_2	54	CBC2_2_B_COIN_DATA

15	I2C_REFRESH_2	55	CBC2_2_B_AMUX
16	GND	56	CBC2_2_B_COIN_OR
17	T1_TRIG_1	57	GND
18	FAST_RESET_1	58	CBC2_2_A_DATA
19	TEST_PULSE_1	59	CBC2_2_A_COIN_DATA
20	I2C_REFRESH_1	60	CBC2_2_A_AMUX
21	GND	61	CBC2_2_A_COIN_OR
22	CBC2_4_B_DATA	62	GND
23	CBC2_4_B_COIN_DATA	63	CBC2_1_B_DATA
24	CBC2_4_B_AMUX	64	CBC2_1_B_COIN_DATA
25	CBC2_4_B_COIN_OR	65	CBC2_1_B_AMUX
26	GND	66	CBC2_1_B_COIN_OR
27	CBC2_4_A_DATA	67	GND
28	CBC2_4_A_COIN_DATA	68	CBC2_1_A_DATA
29	CBC2_4_A_AMUX	69	CBC2_1_A_COIN_DATA
30	CBC2_4_A_COIN_OR	70	CBC2_1_A_AMUX
31	GND	71	CBC2_1_A_COIN_OR
32	GND	72	GND
33	GND	73	CLK_40_N
34	P1V2	74	CLK_40_P
35	P1V2	75	GND
36	P1V2	76	SCLK
37	P1V2	77	SDA
38	P1V2	78	GND
39	P1V2	79	RESET
40	GND	80	GND

Table 3: Pin assignment of FPC connector

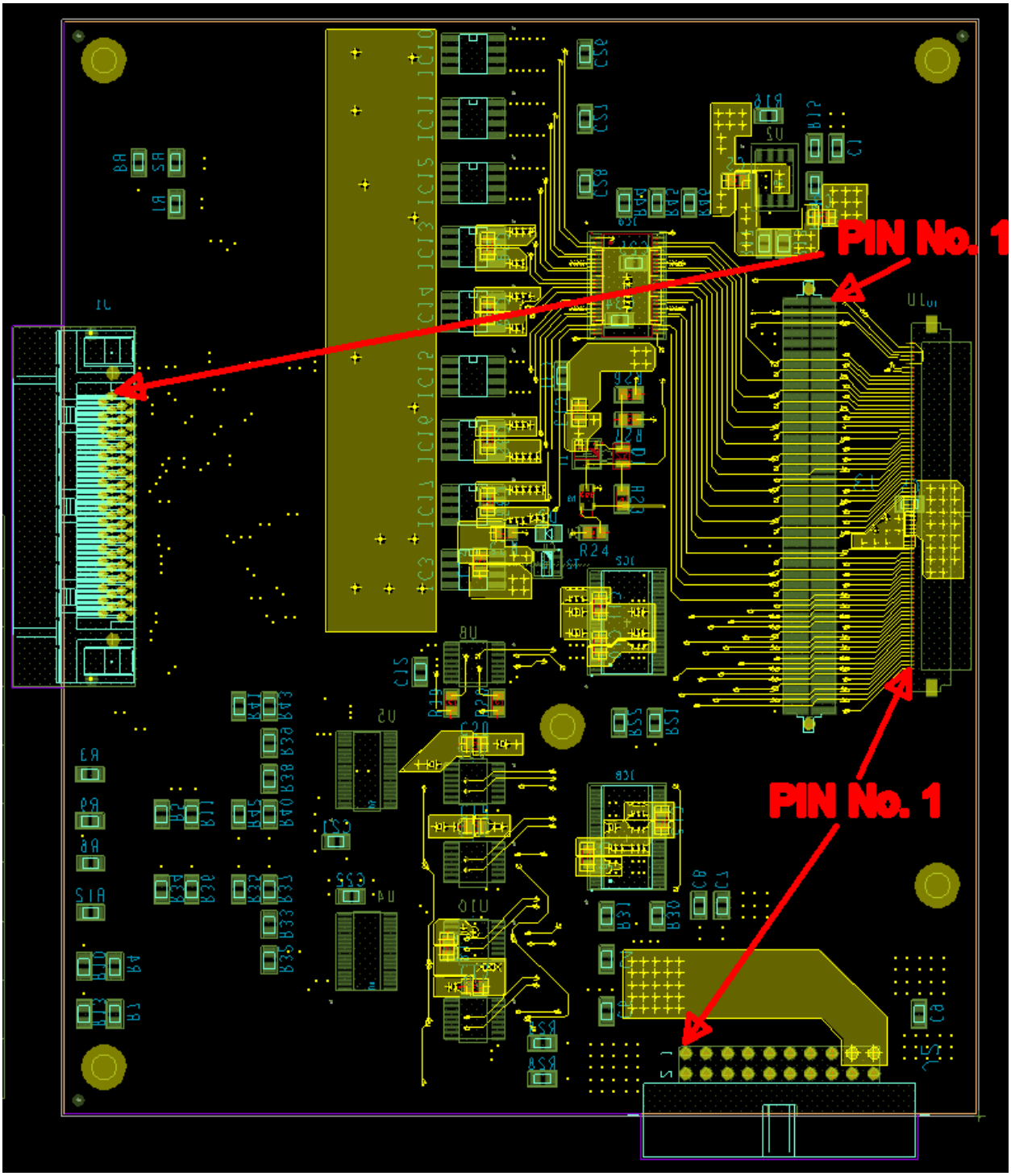

Figure 7: Pin no. 1 on connectors, bottom view

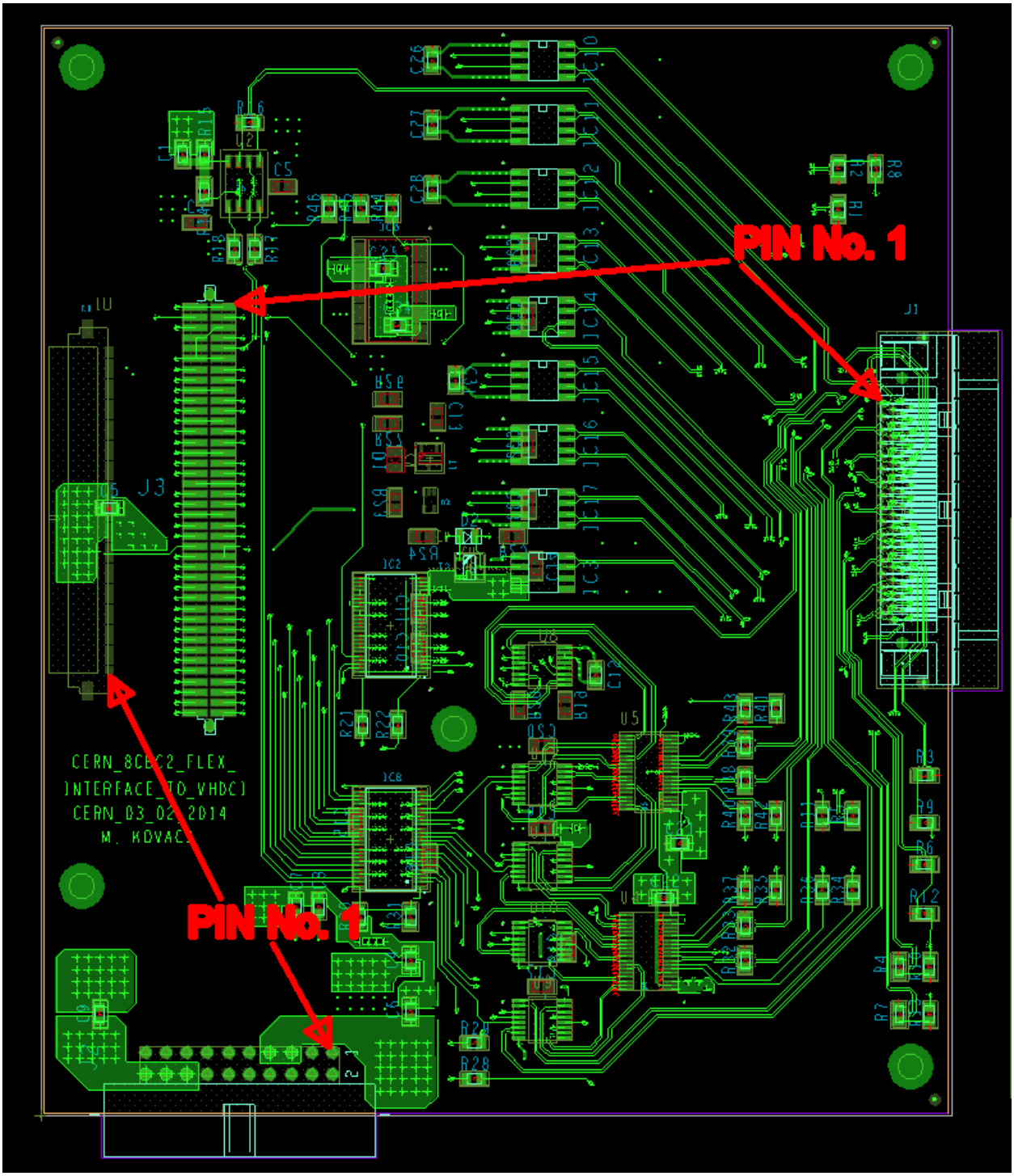

Figure 8: Connector pin no. 1, top view

Pin no.	Signal name	Pin no.	Signal name
1	GND	41	GND
2	GND	42	GND
3	SDA	43	CBC2_3_B_COIN_OR
4	RESET	44	CBC2_3_B_AMUX
5	GND	45	CBC2_3_B_COIN_DATA
6	SCLK	46	CBC2_3_B_DATA
7	CLK_40_P	47	GND
8	GND	48	P1V2_FLEX
9	CLK_40_N	49	GND
10	GND	50	CBC2_4_A_COIN_OR
11	GND	51	CBC2_4_A_AMUX
12	GND	52	CBC2_4_A_COIN_DATA
13	CBC2_1_A_COIN_OR	53	CBC2_4_A_DATA
14	CBC2_1_A_AMUX	54	GND
15	CBC2_1_A_COIN_DATA	55	CBC2_4_B_COIN_OR
16	CBC2_1_A_DATA	56	CBC2_4_B_AMUX
17	GND	57	CBC2_4_B_COIN_DATA
18	GND	58	CBC2_4_B_DATA
19	CBC2_1_B_COIN_OR	59	GND
20	CBC2_1_B_AMUX	60	I2C_REFRESH_1
21	CBC2_1_B_COIN_DATA	61	TEST_PULSE_1
22	CBC2_1_B_DATA	62	FAST_RESET_1
23	GND	63	T1_TRIG_1
24	GND	64	GND
25	CBC2_2_A_COIN_OR	65	I2C_REFRESH_2
26	CBC2_2_A_AMUX	66	TEST_PULSE_2
27	CBC2_2_A_COIN_DATA	67	FAST_RESET_2
28	CBC2_2_A_DATA	68	T1_TRIG_2
29	GND	69	GND
30	GND	70	I2C_REFRESH_3
31	CBC2_2_B_COIN_OR	71	TEST_PULSE_3
32	CBC2_2_B_AMUX	72	FAST_RESET_3
33	CBC2_2_B_COIN_DATA	73	T1_TRIG_3
34	CBC2_2_B_DATA	74	GND
35	GND	75	I2C_REFRESH_4
36	GND	76	TEST_PULSE_4
37	CBC2_3_A_COIN_OR	77	FAST_RESET_4
38	CBC2_3_A_AMUX	78	T1_TRIG_4
39	CBC2_3_A_COIN_DATA	79	GND
40	CBC2_3_A_DATA	80	GND

Table 4: Pin assignment of probe connector

3. Jumpers

Several jumpers are place on the board as 0805 size passive component pads. The purpose of these jumpers is to enable or disable functions of IC-s and to connect dummy signals to GND or terminate them.

Ref des.	Comment	Mount by default
R2	Mount 110 OHM resistor to terminate SDA_TO_CBC2_LVDS_DUMMY<0>	NO
R3	Mount 110 OHM resistor to terminate SDA_FROM_CBC2_LVDS_DUMMY<0>	NO
R4	Mount 110 OHM resistor to terminate SDA_TO_CBC2_LVDS_DUMMY<1>	NO
R5	Mount 110 OHM resistor to terminate SDA_FROM_CBC2_LVDS_DUMMY<1>	NO
R6	Mount 110 OHM resistor to terminate SDA_TO_CBC2_LVDS_DUMMY<2>	NO
R7	Mount 110 OHM resistor to terminate SDA_FROM_CBC2_LVDS_DUMMY<2>	NO
R8	Mount 0 OHM jumper and also for R2 to GND SDA_TO_CBC2_LVDS_DUMMY<0>	NO
R9	Mount 0 OHM jumper and also for R3 to GND SDA_FROM_CBC2_LVDS_DUMMY<0>	NO
R10	Mount 0 OHM jumper and also for R4 to GND SDA_TO_CBC2_LVDS_DUMMY<1>	NO
R11	Mount 0 OHM jumper and also for R5 to GND SDA_FROM_CBC2_LVDS_DUMMY<1>	NO
R12	Mount 0 OHM jumper and also for R6 to GND SDA_TO_CBC2_LVDS_DUMMY<2>	NO
R13	Mount 0 OHM jumper and also for R7 to GND SDA_FROM_CBC2_LVDS_DUMMY<2>	NO
R19	Output enable to pull U8 OE* to GND	YES
R20	Output enable to pull U8 OE to 3,3V	NO
R21	Output enable for IC2 (only enables 1OE*,pulls to GND)	YES
R28	Output enable to pull U9,U10,U11,U12 OE* to GND	YES
R29	Output enable to pull U9,U10,U11,U12 OE to 3,3V	NO
R30	Direction and output enable of IC 8 pulled to GND	YES
R34	Enable A outputs of U4, pulled to 3.3V	YES
R35	Enable C outputs of U4, pulled to 3.3V	YES
R36	Enable B outputs of U4, pulled to 3.3V	YES
R37	Enable D outputs of U4, pulled to 3.3V	YES
R40	Enable A outputs of U5, pulled to 3.3V	YES
R41	Enable C outputs of U5, pulled to 3.3V	YES
R42	Enable B outputs of U5, pulled to 3.3V	YES
R43	Enable D outputs of U5, pulled to 3.3V	YES
R44	Direction set for IC9 DIR A to B, pulled to 1,2V	YES
R46	Output enable for IC9 for all pins, pulled to GND	YES

Table 5: Ref des and functions of jumpers