Phase-2 DAQ Training Workshop
Preparing CBC for data taking [Chip calibration]

Sarah Seif El Nasr-Storey

CBC Chip Calibration :

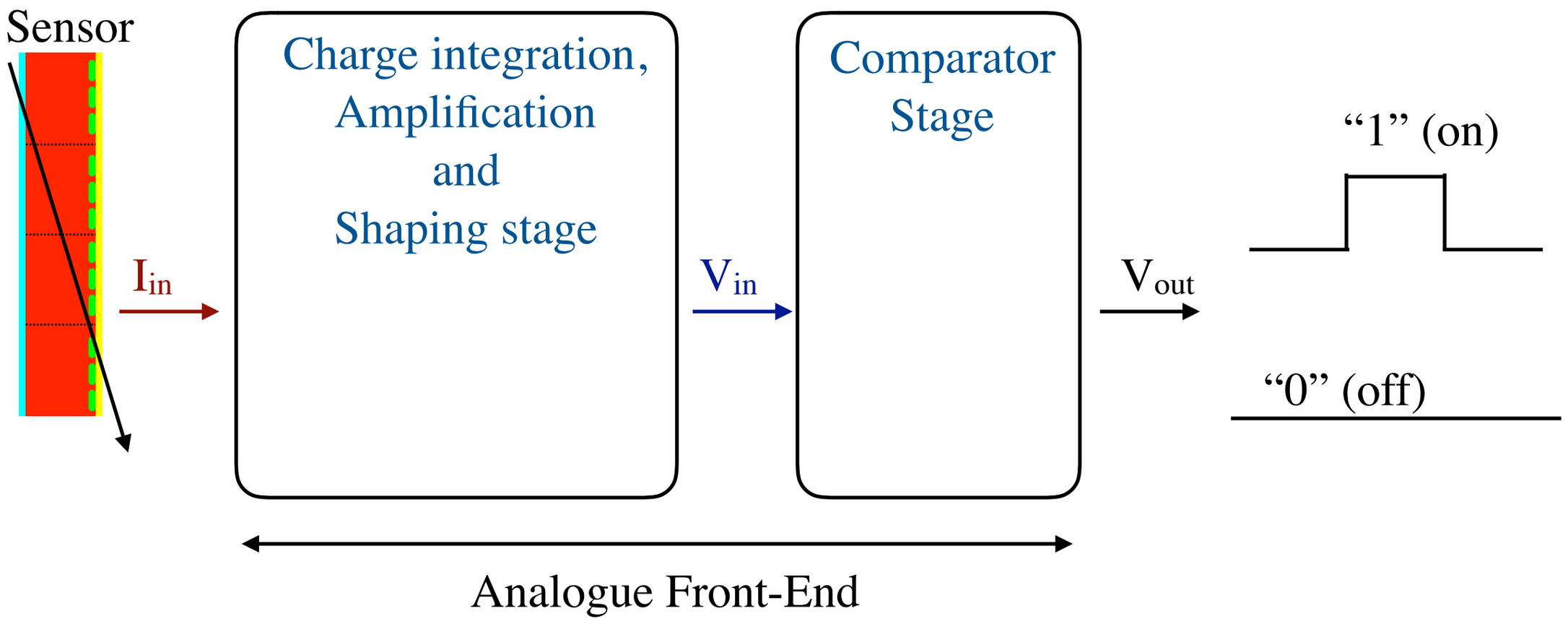
Before we start .. a few words on documentation!

- This talk is based on a (really) long list of talks/publications/resources available on the CBC2/ CBC3
  - Mark Raymond's list of **user manuals, progress talks, publications**
    - a good starting point when looking for information
  - the Ph2_ACF **git repository**
    - how things are actually done, default settings, documentation
  - **previous edition** of this workshop
  - **Kirika's talk from this morning's session**

CBC Chip Calibration :

Digital read-out of a silicon tracking detector

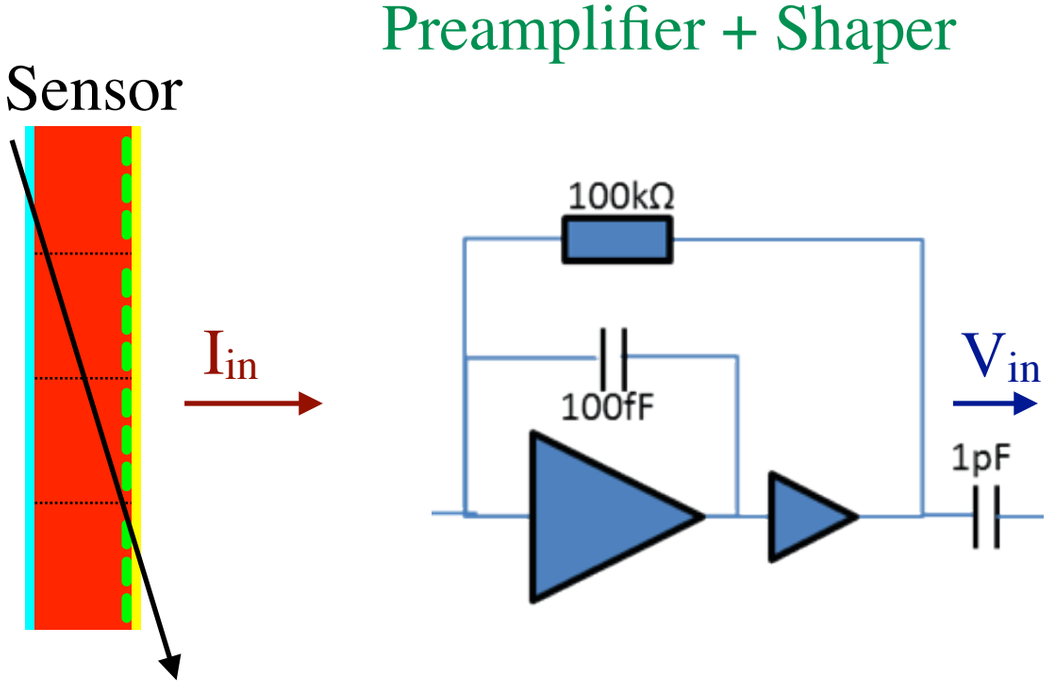
- Generic operation of a silicon tracking detector (sensor + read-out chip)
  - e-h pairs generated in the silicon by a particle crossing a particular channel
  - e-h collected by sensor, and generated current (I_{in}) transmitted to a channel of the read-out chip
  - each channel of the readout chip can make a decision on whether the signal is of interest or not
    - generates a binary signal based on the characteristics of the input signal (V_{in})



CBC Chip Calibration :

Analogue Front-end of CBC

- Preamplifier + Shaper : integrates signal from sensor channel ($I_{in} \rightarrow V_{in}$) and prelim. filtering.

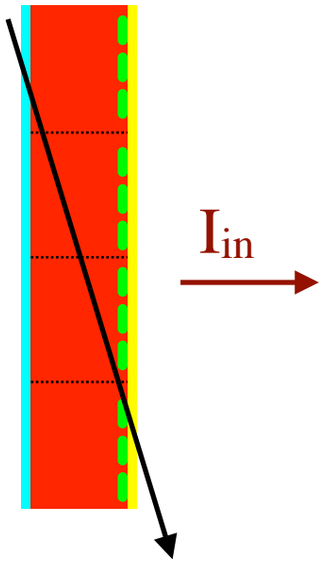


CBC Chip Calibration :

Analogue Front-end of CBC

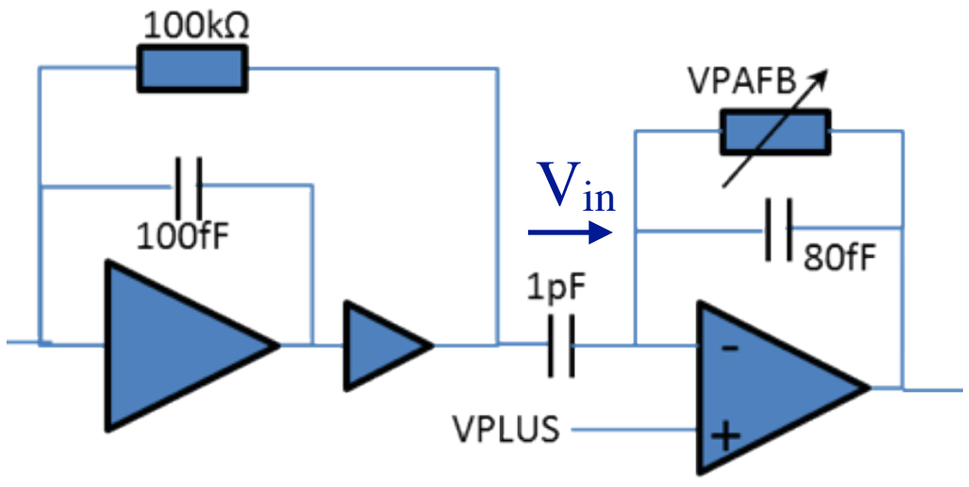
- Preamplifier + Shaper : integrates signal from sensor channel ($I_{in} \rightarrow V_{in}$) and prelim. filtering.
- Post-amplifier : produces final signal for the comparator ($V_{in} \rightarrow V_{out}$)

Sensor

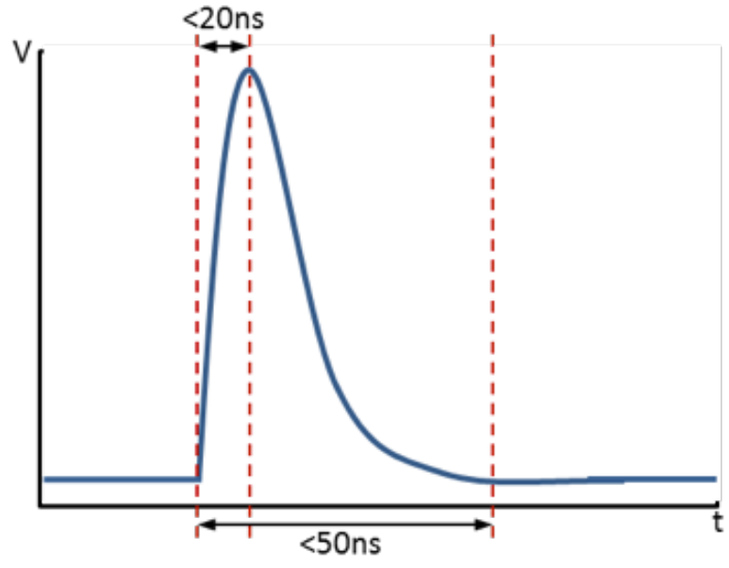


Preamplifier + Shaper

Postamplifier



CBC pulse shape

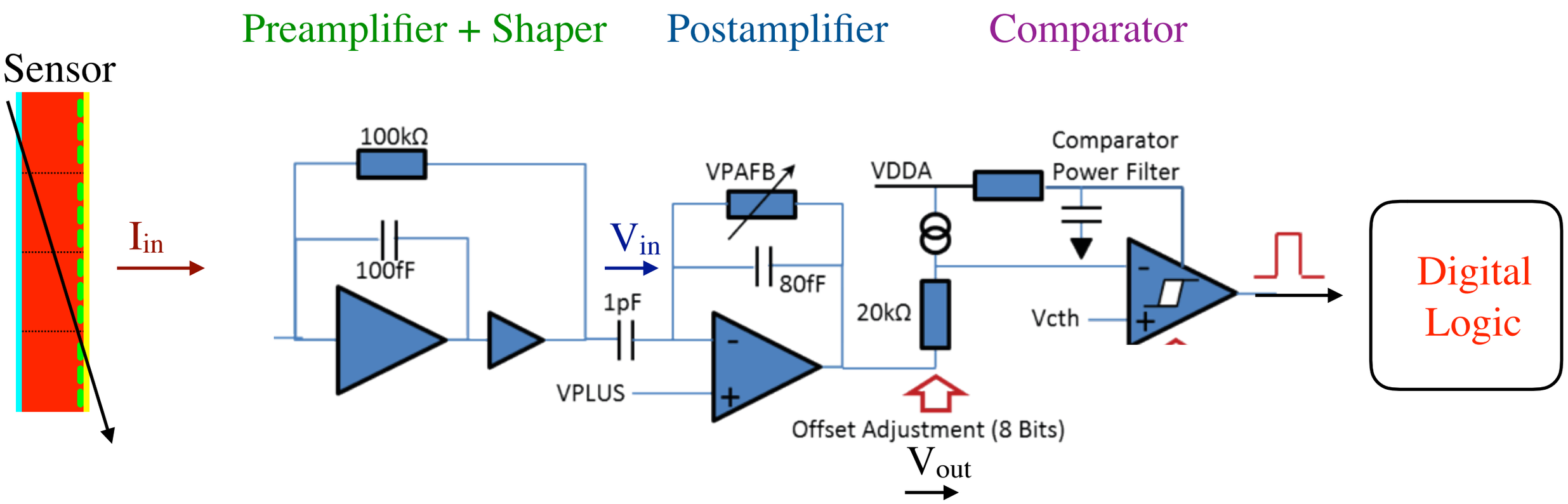


- Amplifier designed to have :
  - peaking time of less than 20 ns
  - return to DC baseline within 50 ns

CBC Chip Calibration :

Analogue Front-end of CBC

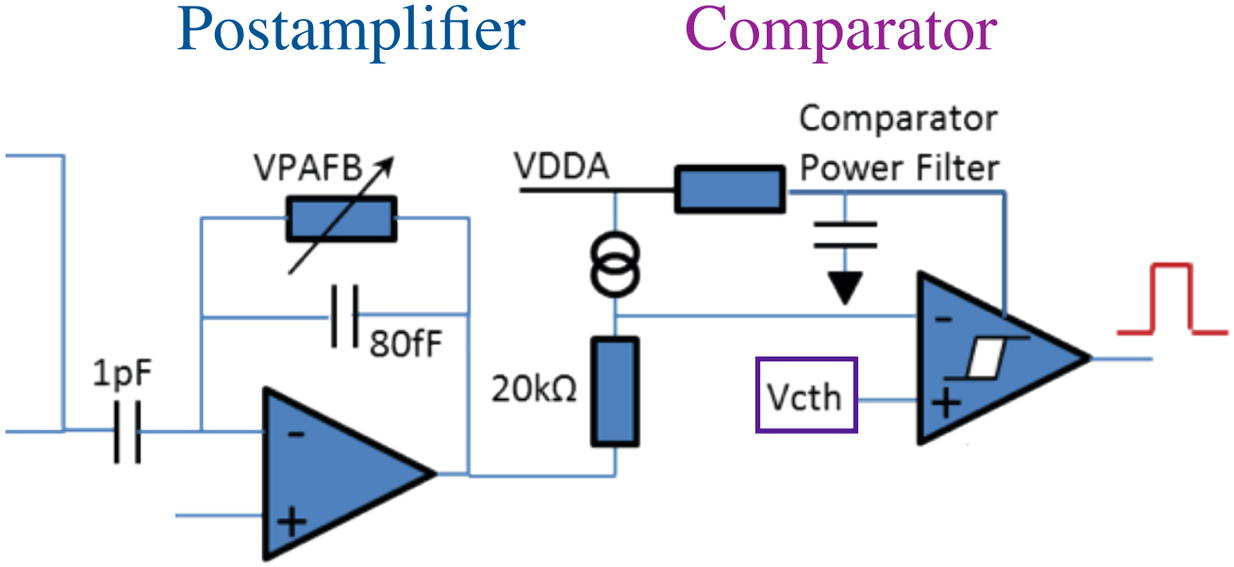
- Preamplifier + Shaper : integrates signal from sensor channel ($I_{in} \rightarrow V_{in}$) and prelim. filtering.
- Post-amplifier : produces final signal for the comparator ($V_{in} \rightarrow V_{out}$)
- Comparator : produces digital signal to feed logic circuitry of chip



CBC Chip Calibration :

I2C registers to control Amplification stage of CBC

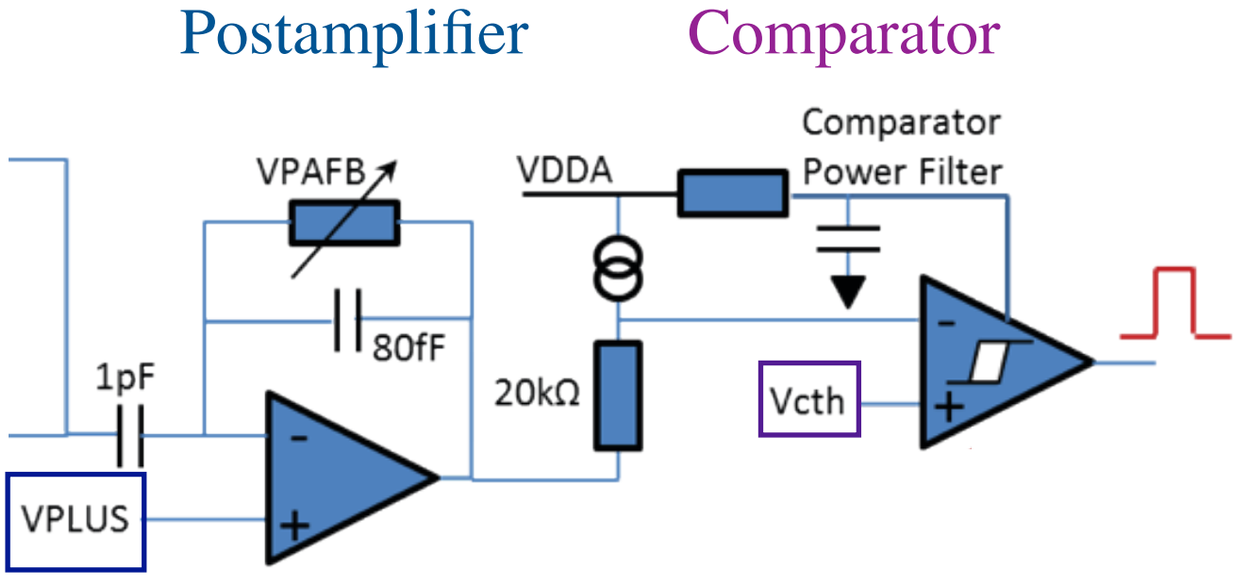
- V_{cth} : controls the comparator threshold.



CBC Chip Calibration :

I2C registers to control Amplification stage of CBC

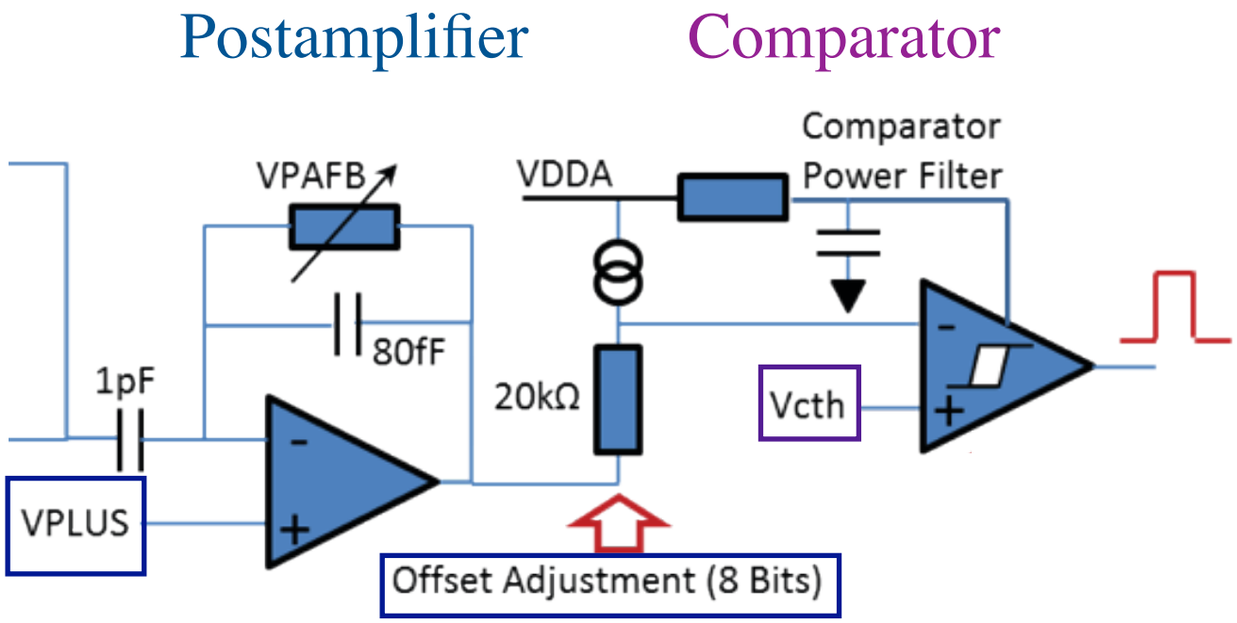
- V_{cth} : controls the comparator threshold.
- V_{plus} : controls the DC baseline of the post amplifier output signal (V_{out}).



CBC Chip Calibration :

I2C registers to control Amplification stage of CBC

- $\mathbf{V_{cth}}$: controls the comparator threshold.
- $\mathbf{V_{plus}}$: controls the DC baseline of the post amplifier output signal (V_{out}).
- $\mathbf{V_{offset}}$: fine tuning of the DC baseline of the post amplifier output signal (V_{out}).



N.B. : there are (many) more settings you can control on the analogue front-end, but these should not require changing from default values so will not be covered here.

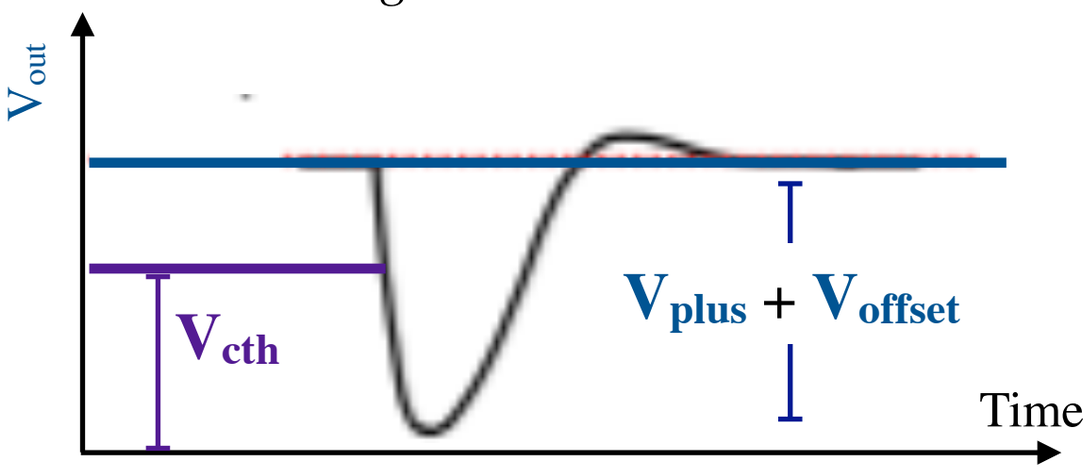
For a complete description of the analogue front-end please refer to the CBC2/CBC3 manuals and Mark Raymond's talks (links at the end of the presentation).

CBC Chip Calibration :

I2C registers to control Amplification stage of CBC : Electron Mode

- $\mathbf{V_{cth}}$: controls the comparator threshold.
- $\mathbf{V_{plus}}$: controls the DC baseline of the post amplifier output signal (V_{out}).
- $\mathbf{V_{offset}}$: fine tuning of the DC baseline of the post amplifier output signal (V_{out}).

Collecting Electrons :
Increasing Vcth → Reduces threshold



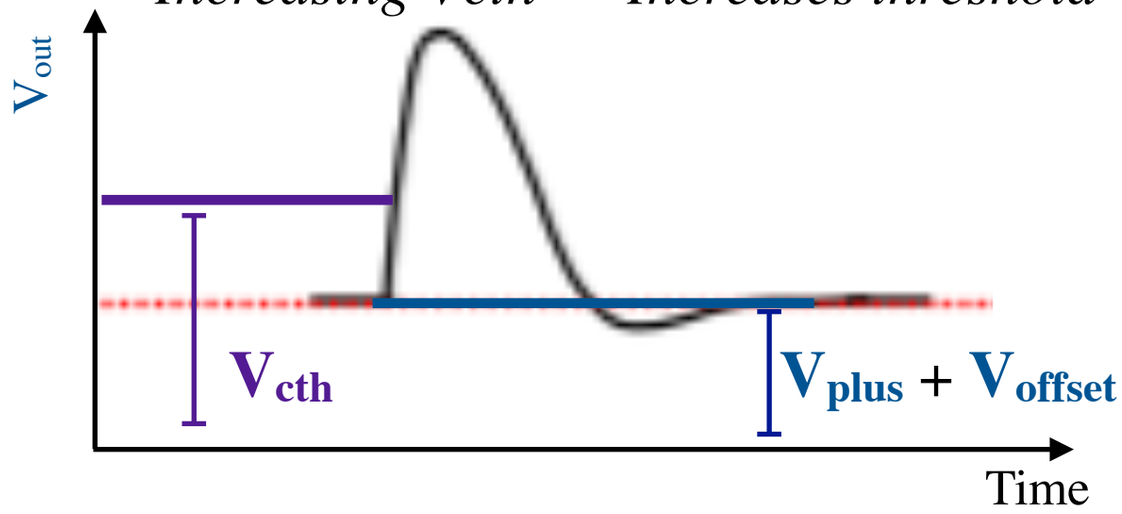
CBC Chip Calibration :

I2C registers to control Amplification stage of CBC : Hole Mode

- **V_{cth}** : controls the comparator threshold.
- **V_{plus}** : controls the DC baseline of the post amplifier output signal (V_{out}).
- **V_{offset}** : fine tuning of the DC baseline of the post amplifier output signal (V_{out}).

Collecting Holes:

Increasing Vcth → Increases threshold

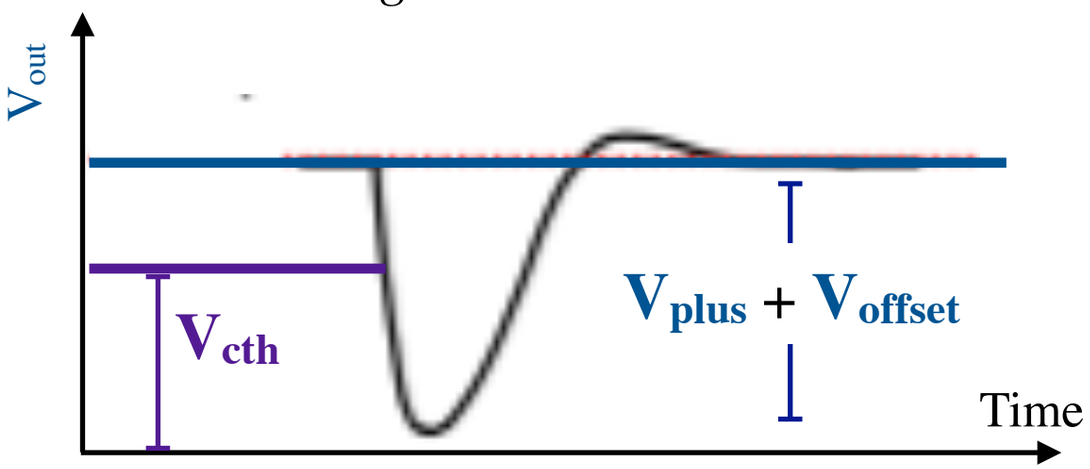


CBC Chip Calibration :

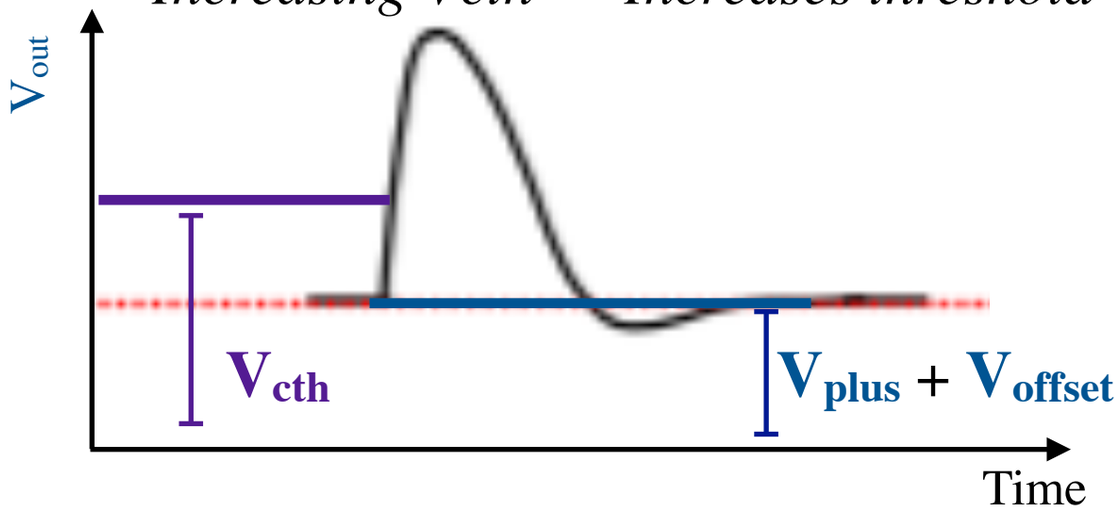
I2C registers to control Amplification stage of CBC

- V_{cth} : controls the comparator threshold [Global]
- V_{plus} : controls the DC baseline of the post amplifier output signal (V_{out}) [Global]
- V_{offset} : fine tuning of the DC baseline of the post amplifier output signal (V_{out}). [Per channel]

Collecting Electrons :
Increasing Vcth → Reduces threshold



Collecting Holes:
Increasing Vcth → Increases threshold



- V_{plus} and V_{offset} are generated in the same way on the CBCs - so same adjustment range on both
- V_{plus} should be chosen to accommodate expected dynamic range of signal
- V_{offset} should be not be too close to zero

V_{plus} + V_{offset} define the pedestal value on each channel

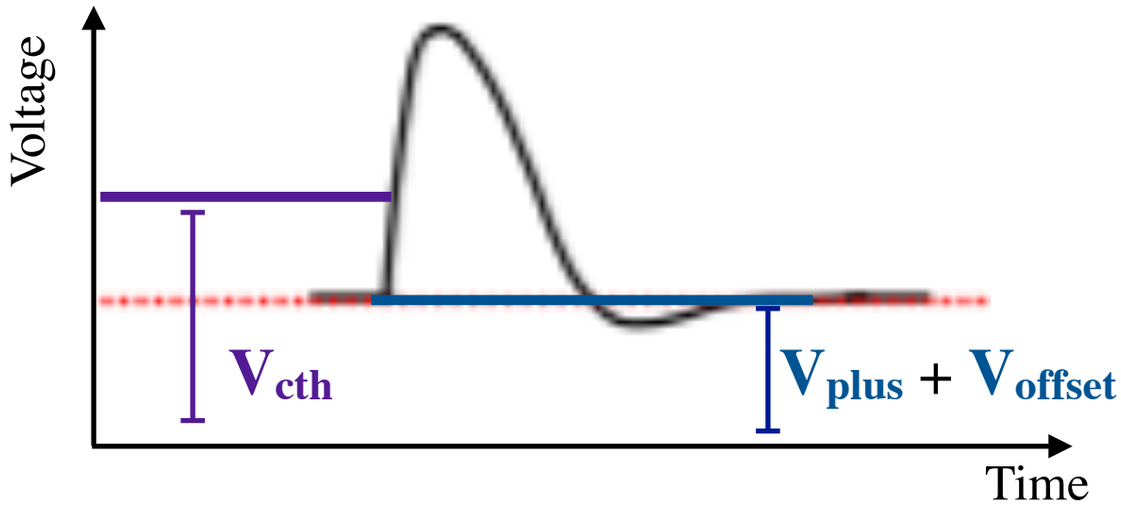
CBC Chip Calibration : Differences

Differences in Analogue Front-end of CBC2/CBC3

- V_{offset} : 8 bit DAC on CBC2 → 10 bit DAC on CBC3
  - access to finer grain tuning on CBC3
- New post-amp feedback bias scheme to address common mode noise observed in CBC2
  - second voltage (V_{plus2}) to generate the feedback control voltage for post-amp network [**should always be identical to V_{plus}**]
- Choice of n-on-p sensors made for outer tracker (i.e. collecting electrons not holes) therefore
  - only electron mode available in the CBC3

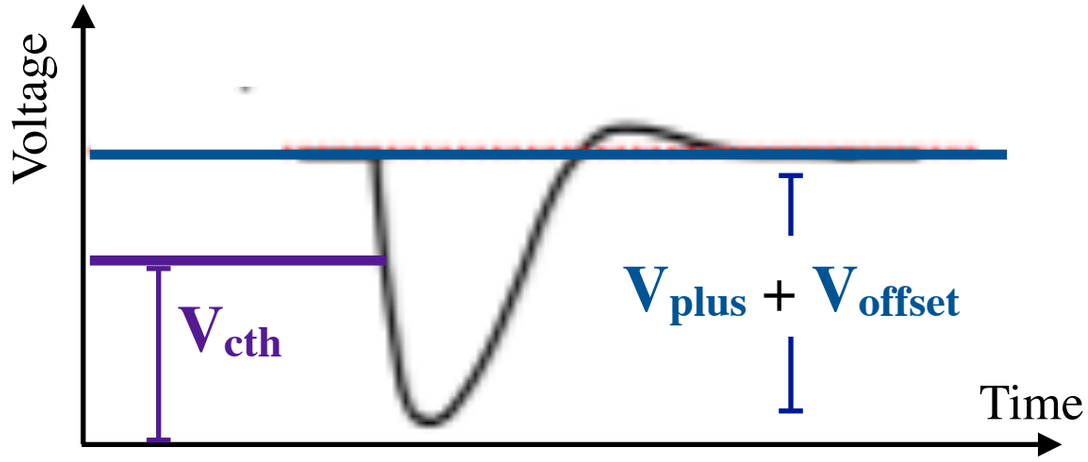
Collecting Holes

Valid for CBC2 only



Collecting Electrons

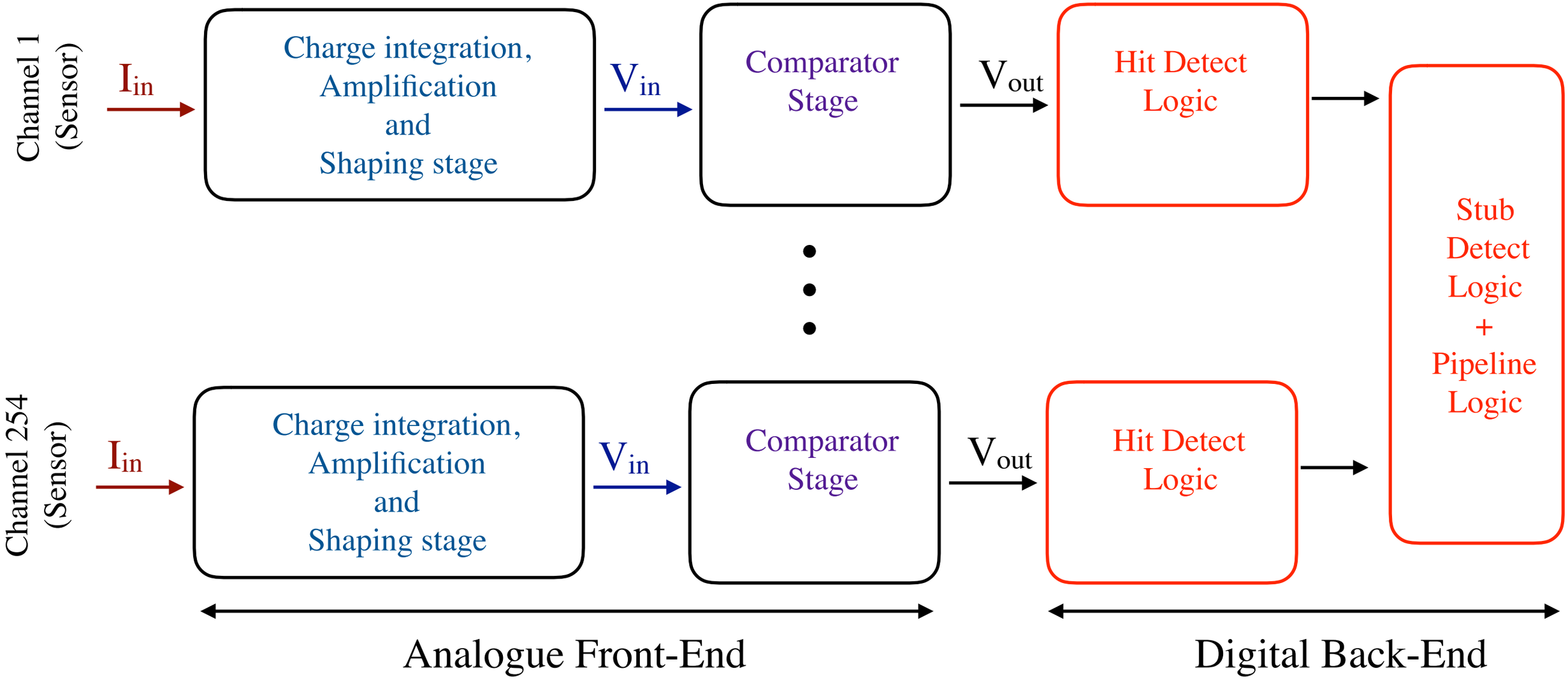
Valid for both CBC2 and CBC3



CBC Chip Calibration :

Basics of the Digital logic circuitry on the CBCs

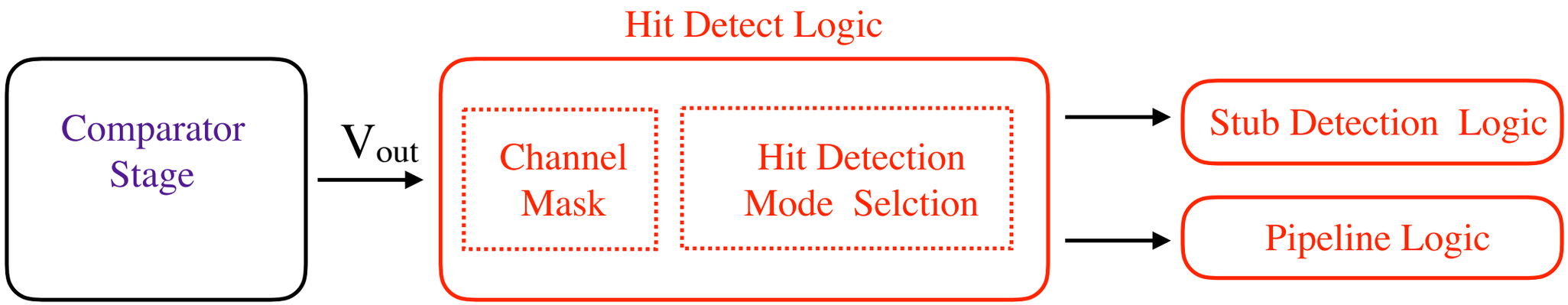
- CBC decides whether “hit” (signal in sensor channel) or stub has occurred by examining the outputs of the (binary) comparator stages :
  - all logic synchronized with 40 MHz external clock
  - hit detection logic to identify hits in sensor channels
  - stub detection logic to correlate hits between the two sensor layers on a 2S module and generate stubs (track primitive for L1)



CBC Chip Calibration :

Checklist : prepare CBC for data taking

- Configuring the CBC for data taking requires :



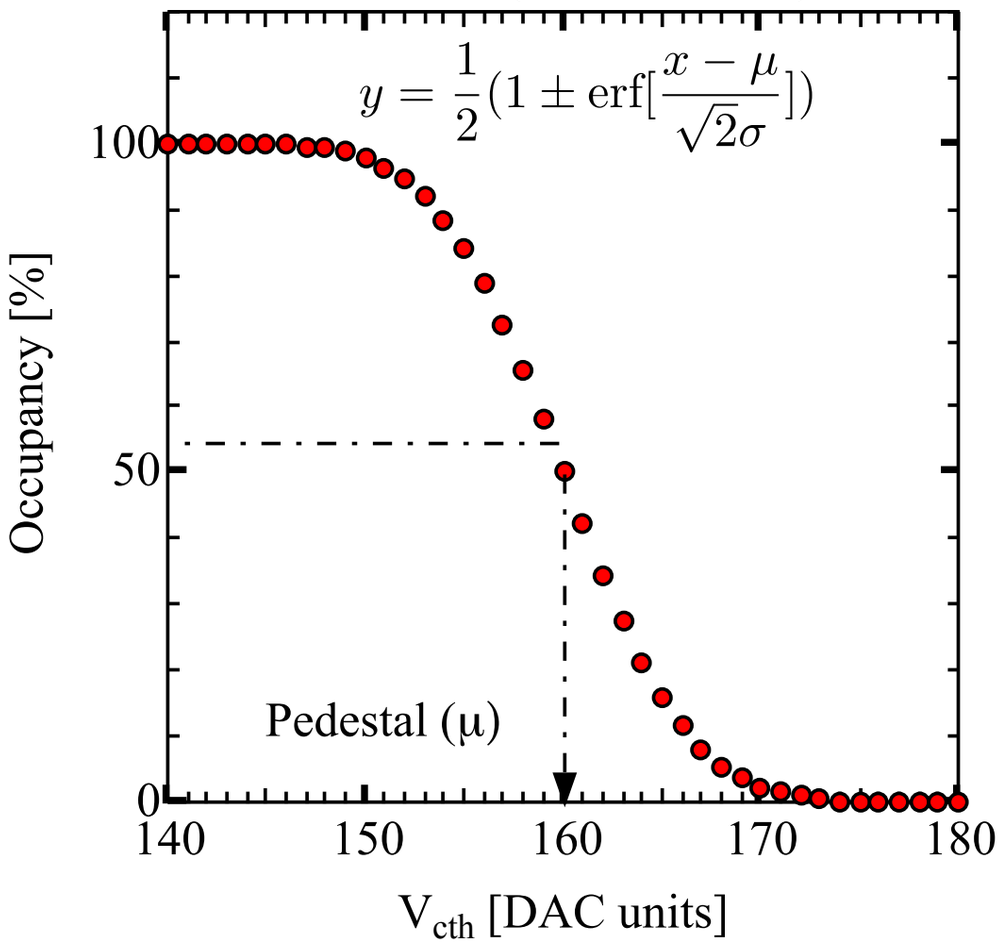
- Uniform sensitivity across the 254 channels of each CBC (i.e. uniform pedestals)
  - might require masking out noisy channels from the hit detection logic
- Selecting the hit detection mode most appropriate to your test
- Selecting appropriate data latency for your particular set-up (will be dependent on cable lengths, external trigger system)
- Selecting appropriate stub latency

CBC Chip Calibration :

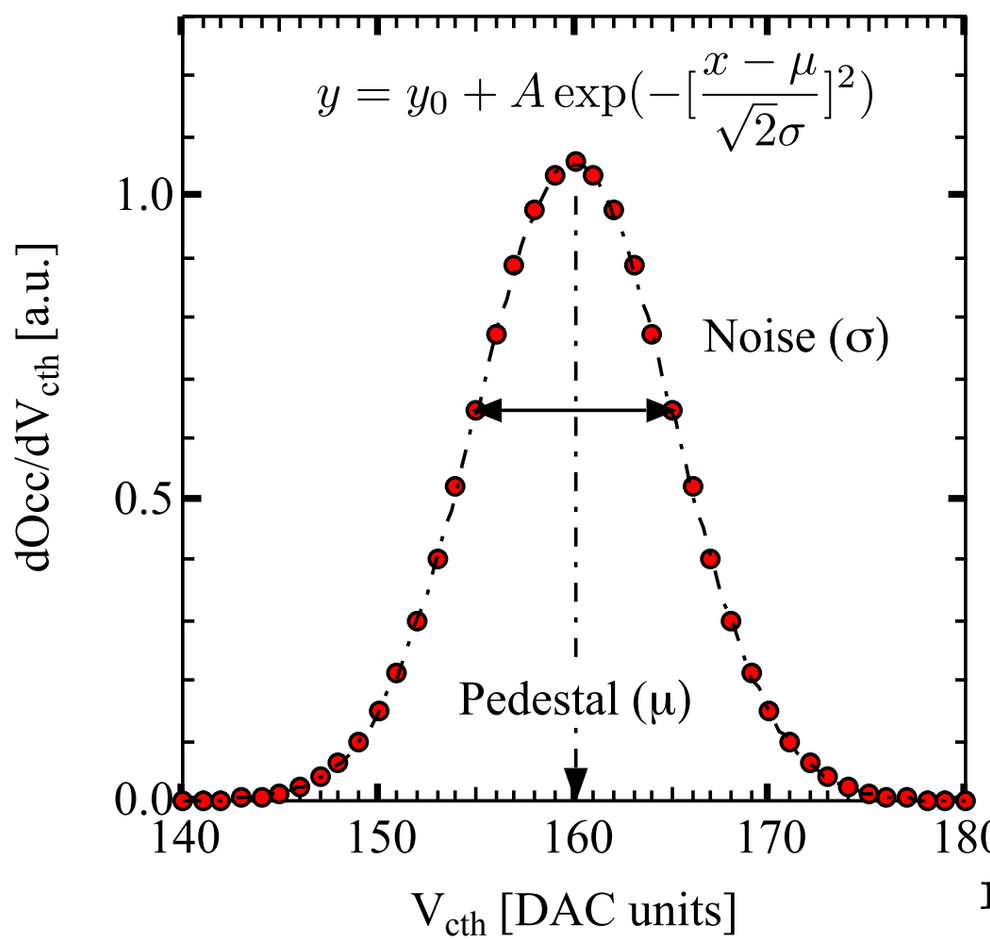
Preparing CBC for data taking : Uniform pedestals.

- Minimize the variation in the pedestal values across the CBC's 254 channels
- Binary read-out! So the analogue performance must be *inferred* from a channel's S-curve :
  - occupancy [hit count/number of triggers] per channel as a function of $\mathbf{V_{cth}}$
  - pedestal defined as $\mathbf{V_{cth}}$ corresponding to 50% occupancy [mean of the differentiated s-curve]
  - noise defined as the width of the S-curve in $\mathbf{V_{cth}}$ units [width of the differentiated s-curve]

S-curve (hole mode)



differentiate

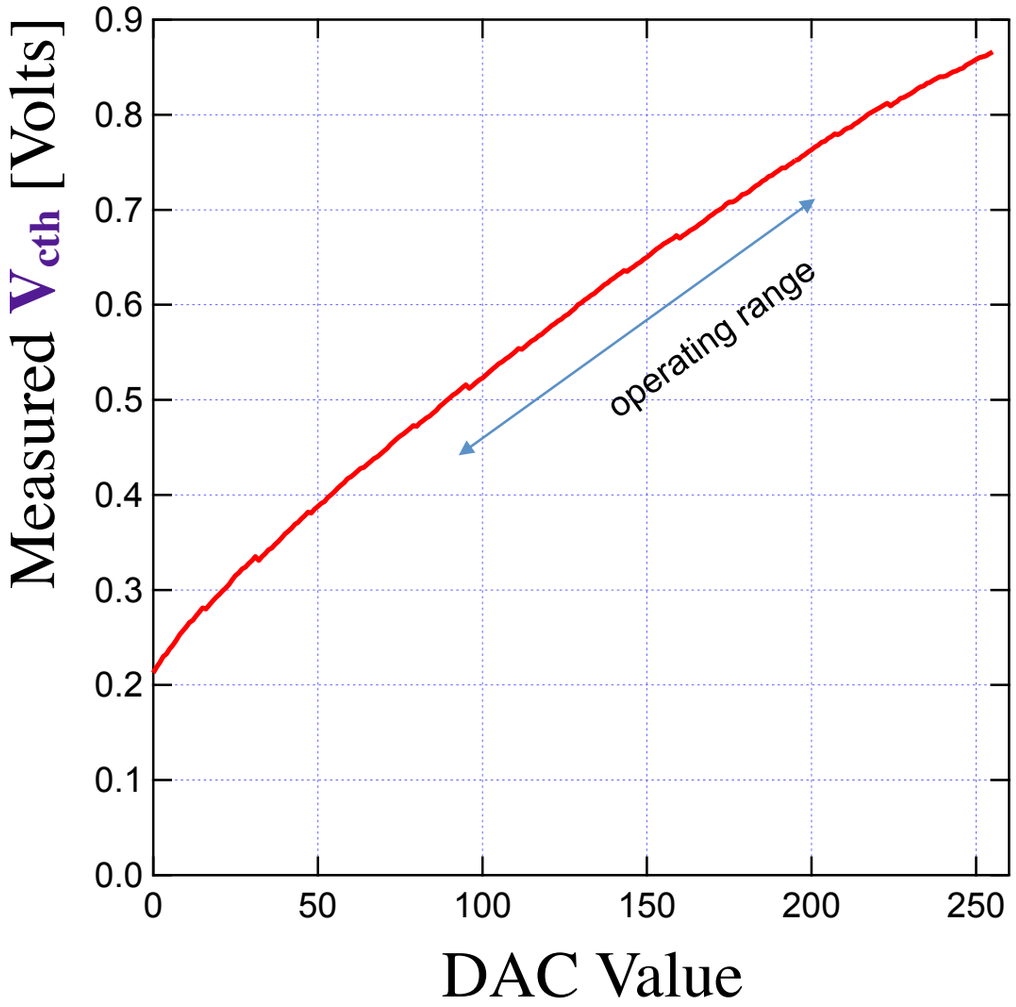


CBC Chip Calibration : Procedure

Offset tuning procedure for CBC2 : Things to remember

- CBC2 does not like being operated in high occupancy conditions :
  - perform tuning in groups of 32 channels (i.e. in test pulse groups)
    - all other channels set to maximum threshold

- Discontinuities present in measured V_{cth} at certain DAC settings
  - identified as kinks/steps in Vcth DAC scan [0x20 , 0x40 , 0x80]
  - avoid those values when choosing target V_{cth} value in scan : e.g. 0x78 , 0x84

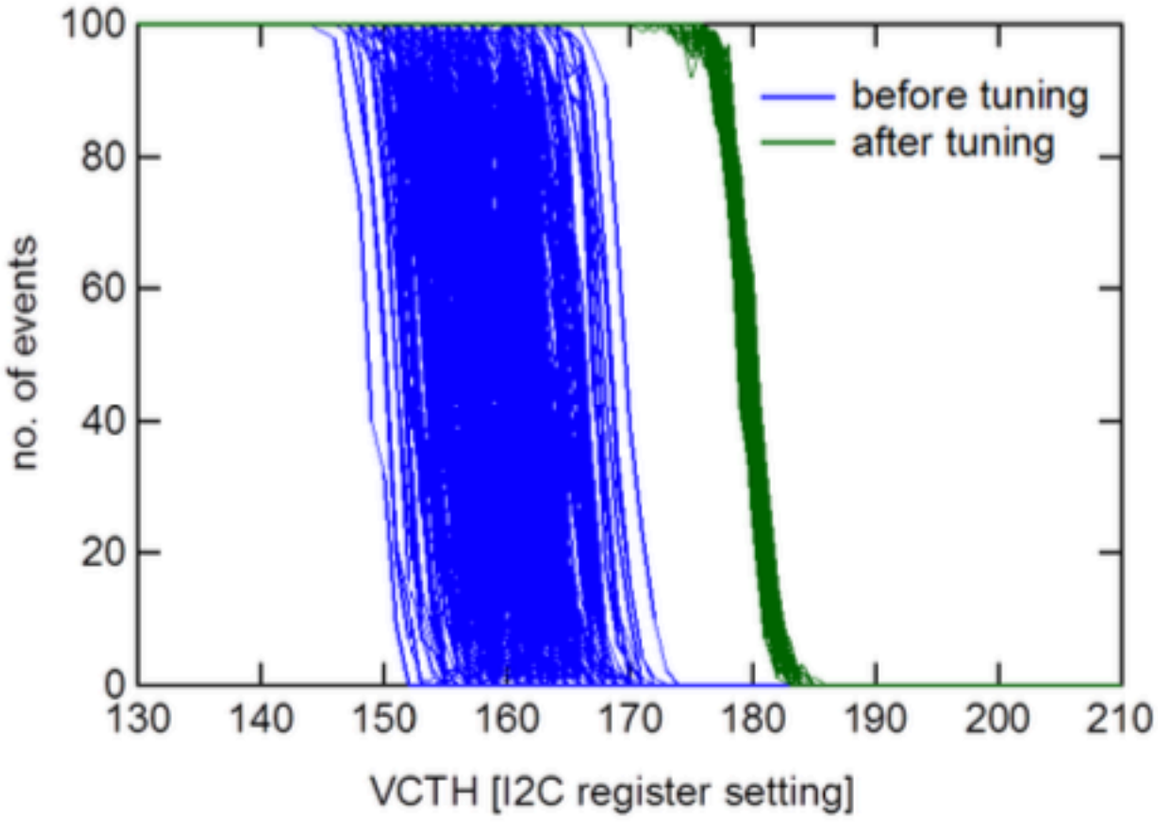


CBC Chip Calibration : Procedure

Offset tuning procedure for CBC2

- Goal : bring all channels' pedestals into alignment

Measured S-curves [σ_{Vcth} = 10 V_{cth} units (~10 mV) to σ_{Vcth} = 0.22 V_{cth} units (~ 0.5 mV)]

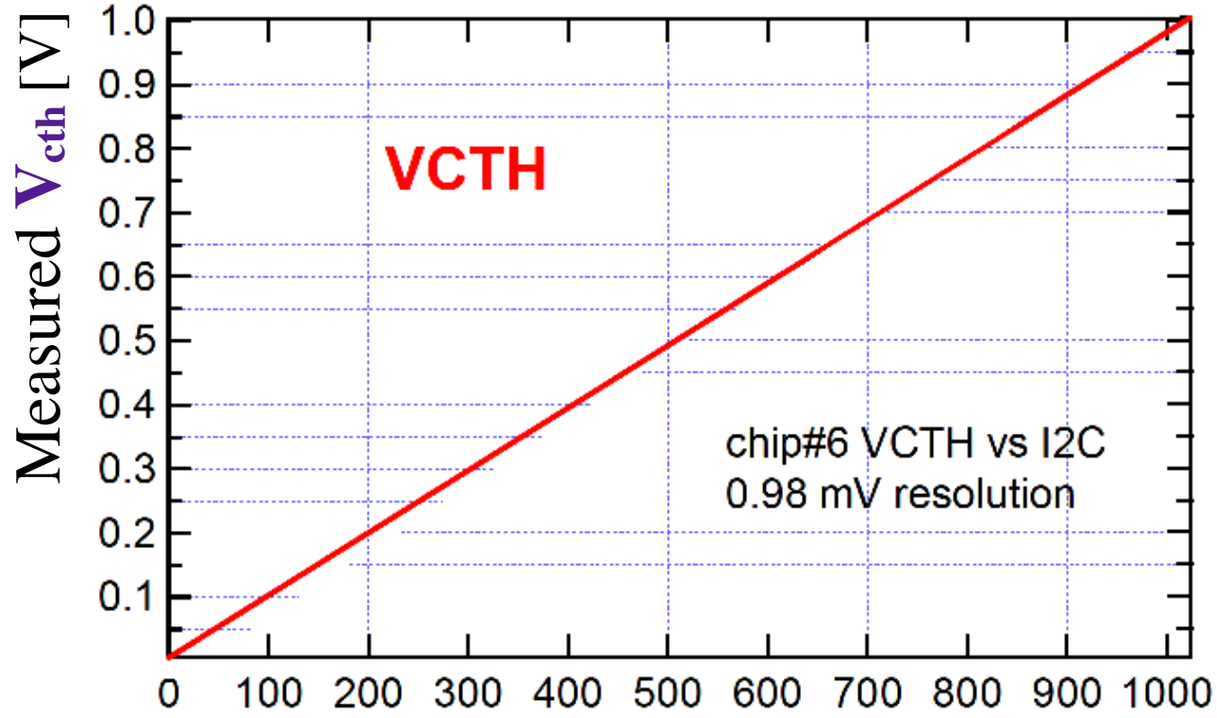


- Tuning procedure designed to avoid discontinuities in V_{cth}
- Two-step tuning procedure to tune all pedestals to a target V_{cth} value on all channels in a test group
  - V_{plus} scan : for a fixed value of V_{offset} , locate V_{plus} value for which occupancy ~50%
  - V_{offset} scan : for the found value of V_{plus}, tune each channel's V_{offset} to ensure occupancy is 50%.

CBC Chip Calibration : Procedure

Offset tuning procedure for CBC3 : Things to remember

- V_{cth} now generated by a 10-bit resistor ladder DAC
  - nicely linear and monotonous

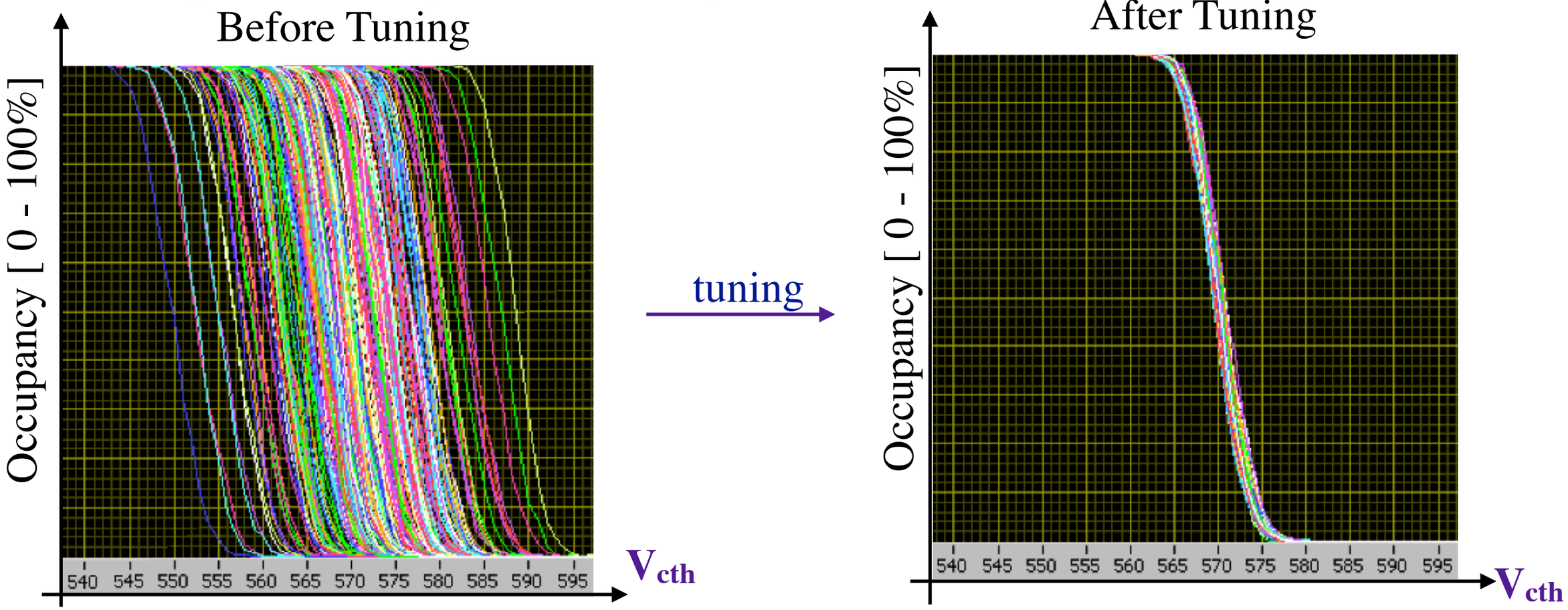


- Improved performance when acquiring S-curves on all 254 channels simultaneously
  - some distortion still present - possible it will improve when chips are bump-bonded
  - bare chips/wire bonded chips still require tuning to be performed on test groups

CBC Chip Calibration : Procedure

Offset tuning procedure for CBC3

- Goal : bring all channels' pedestals into alignment

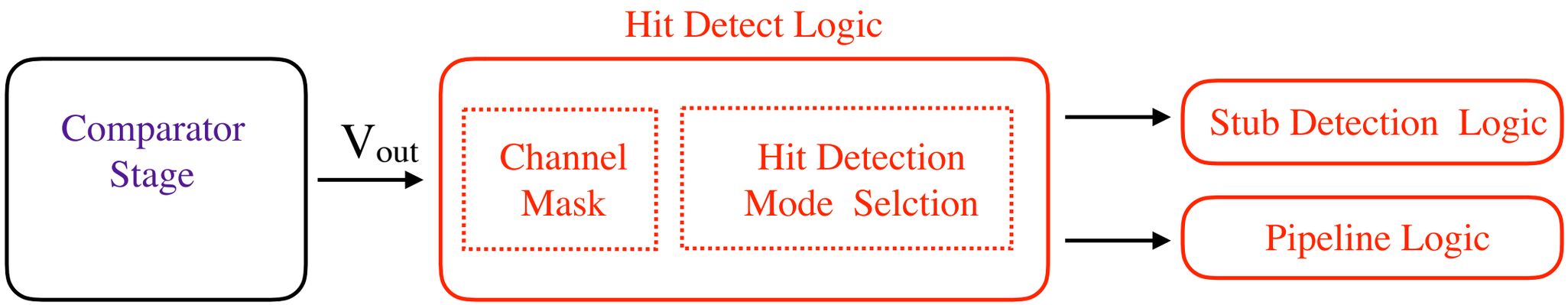


- Two-step tuning procedure to tune all pedestals to a target V_{plus} value on all channels in a test group :
  - V_{plus} [4 bit DAC , 281 - 750 mV] set to the (default) mid-range value of 500 mV.
  - V_{cth} scan : measure S-curves on channels in test group for a fixed value of V_{offset} [e.g. mid-range 0x80]. Set V_{cth} on all channels to average midpoint of all S-curves.
  - V_{offset} scan : tune each channel's V_{offset} so that occupancy is 50% [should be close to midrange value of 0x80]

CBC Chip Calibration :

Checklist : prepare CBC for data taking

- Configuring the CBC for data taking requires :



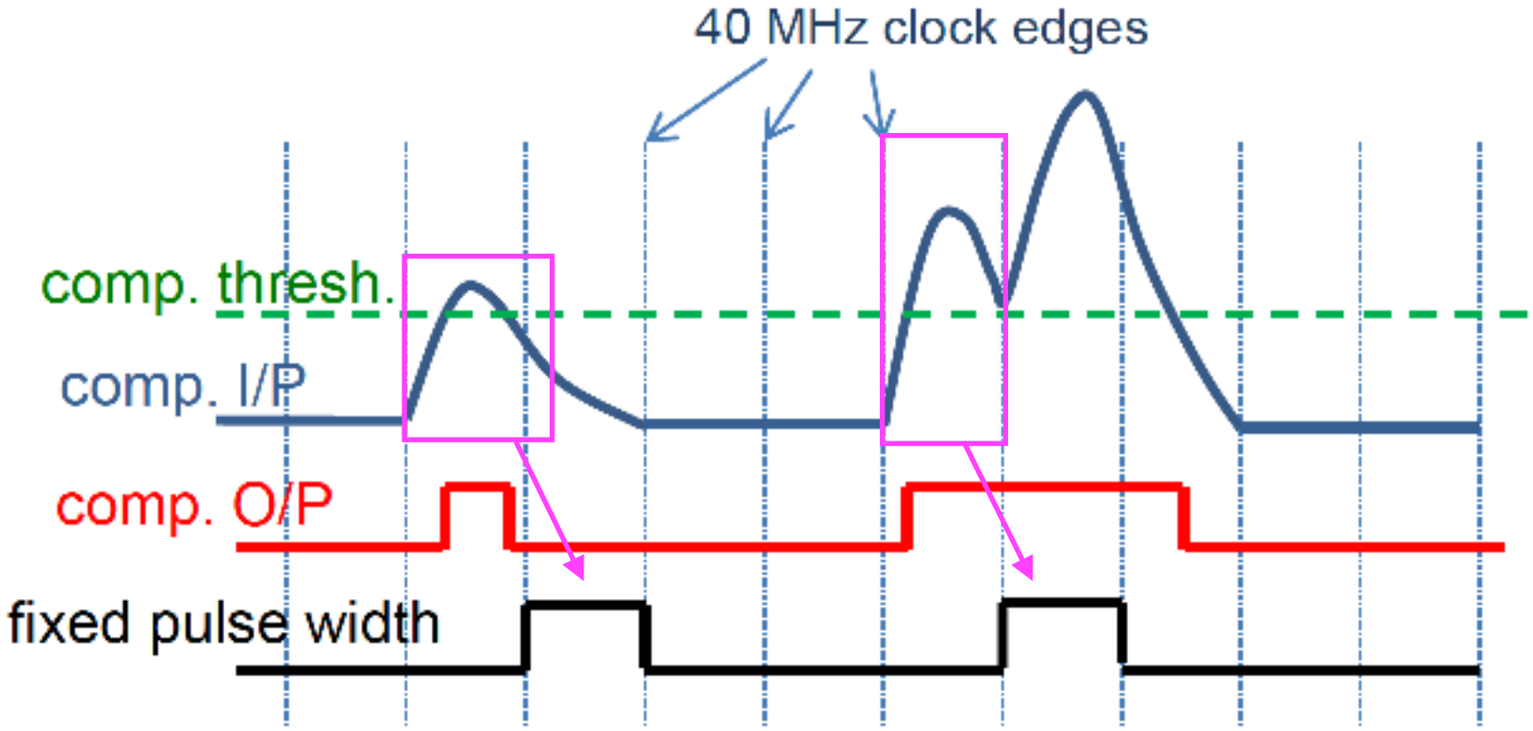
☑Uniform sensitivity across the 254 channels of each CBC (i.e. uniform pedestals)

  - might require masking out noisy channels from the hit detection logic
- Selecting the hit detection mode most appropriate to your test
- Selecting appropriate data latency for your particular set-up (will be dependent on cable lengths, external trigger system)
- Selecting appropriate stub latency

CBC Chip Calibration :

Preparing CBC for data taking : Fixed Pulse Width Hit Detection

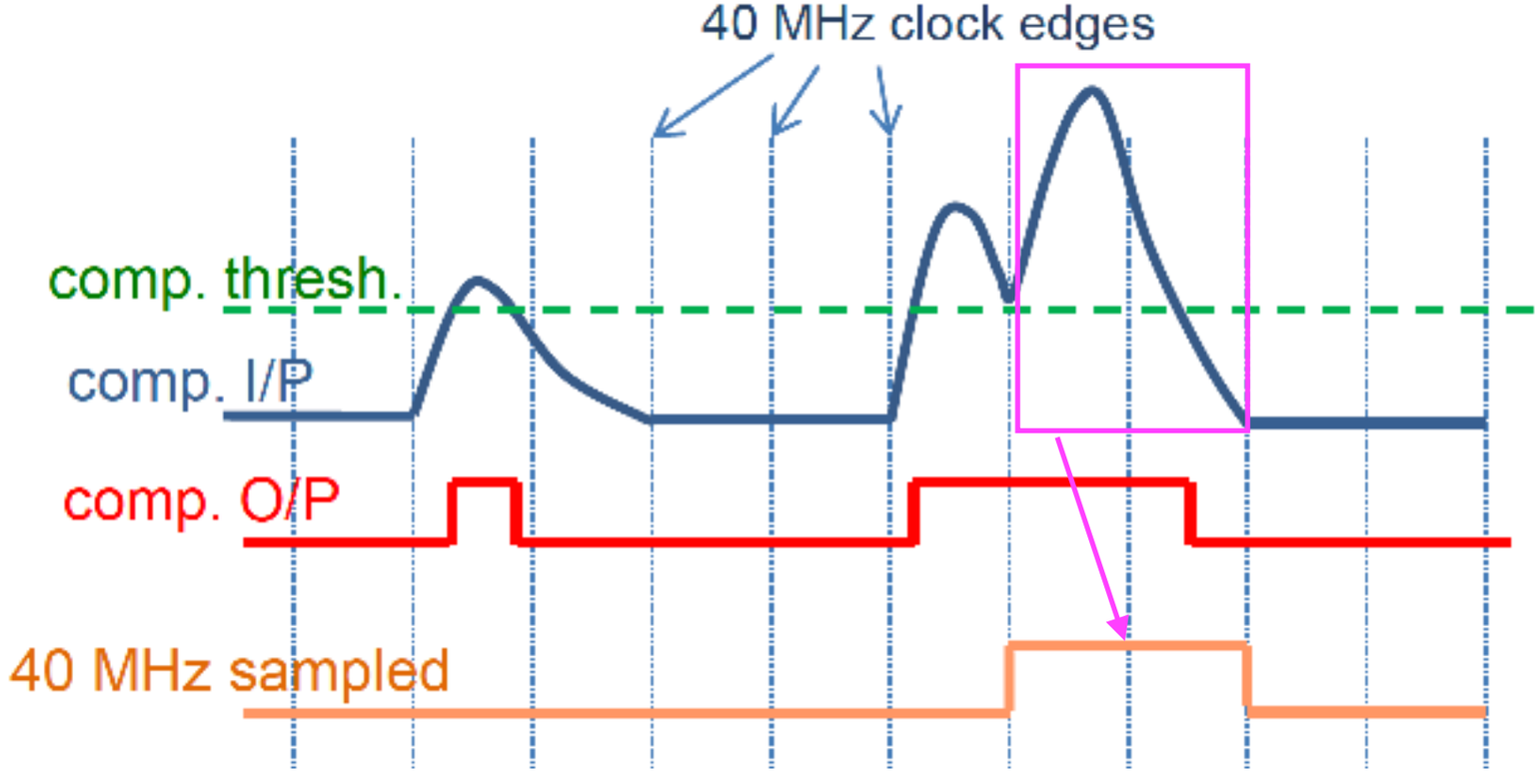
- Available on both the CBC2 and the CBC3 [Single Hit Detect Mode in User manual for CBC2 (default)]
  - output from comparator latched for one clock cycle (25 ns)
  - hits in consecutive clock cycles can be identified provided the signal on the channel goes below V_{cth} for each hit (i.e. comparator output returns to zero)



CBC Chip Calibration :

Preparing CBC for data taking : 40 MHz Sampled Hit Detection

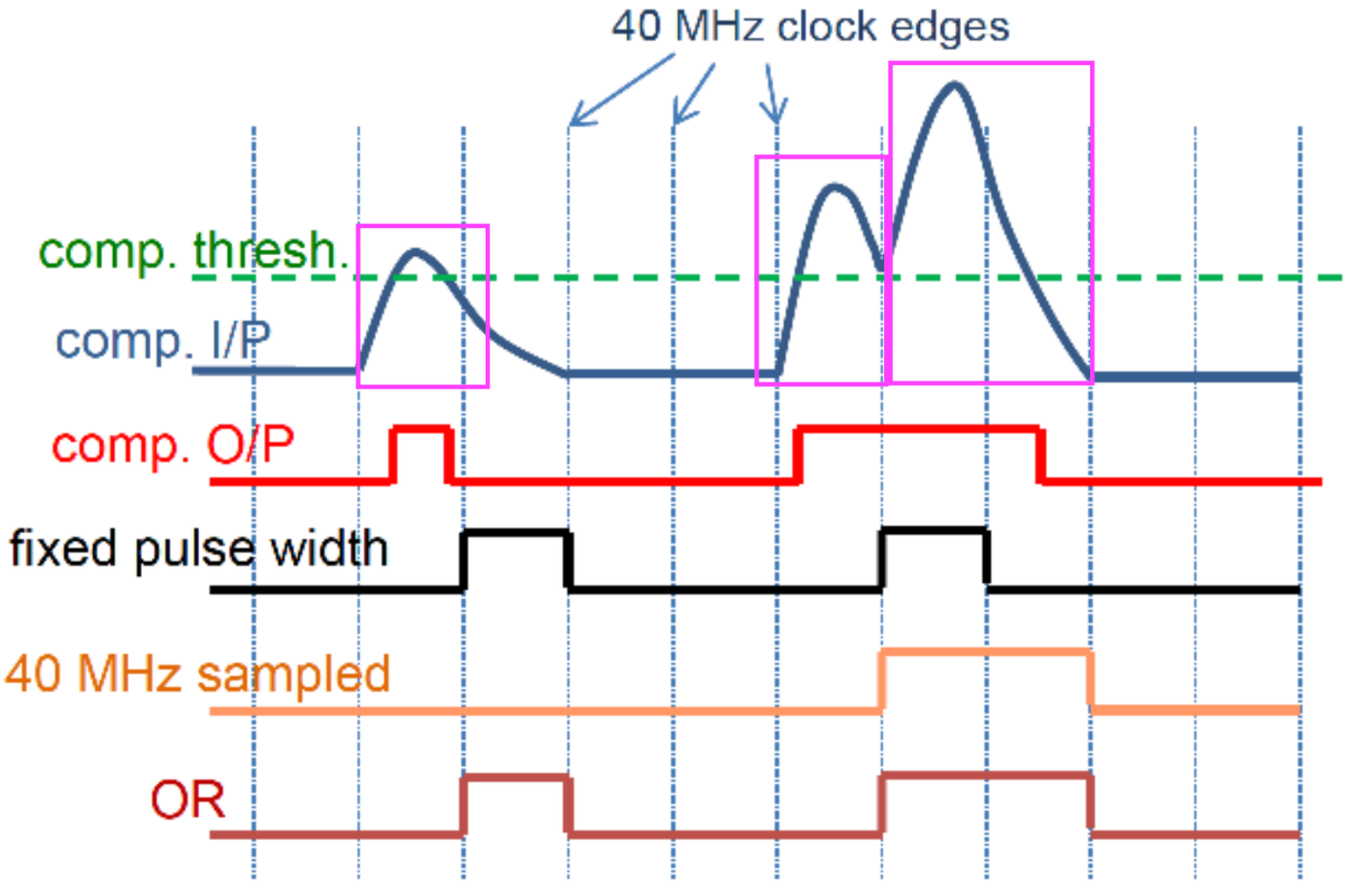
- Available on both the CBC2 and the CBC3 [Variable Hit Detect Mode in User manual for CBC2]
  - comparator output sampled using the CBCs internal 40 MHz clock
  - only comparator outputs that are high on the rising edge of the clock are identified
  - output returns to zero on the first rising clock edge following the comparators return to zero
  - hits in consecutive clock cycles are captured even if comparator output never goes below zero



CBC Chip Calibration :

Preparing CBC for data taking : Logical OR Hit Detection

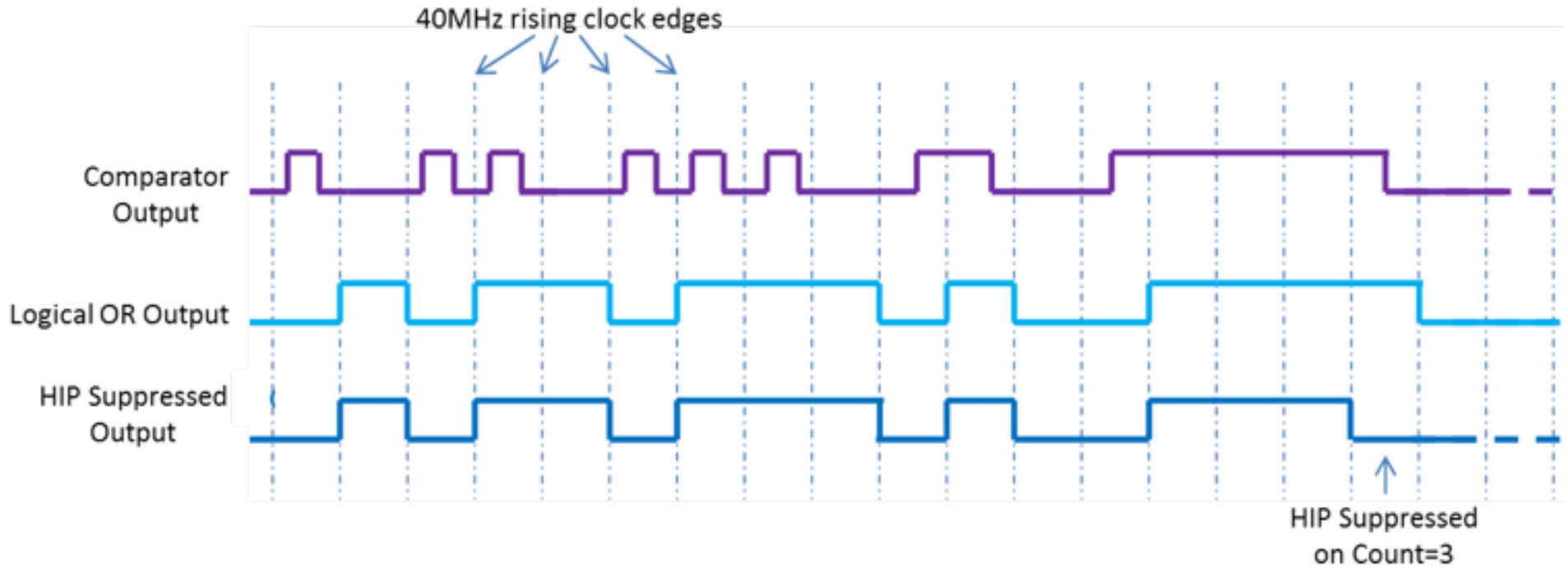
- Only implemented on the CBC3
  - combines the results from the Fixed Pulse and 40 MHz sampled outputs
    - catch everything mode - detect piled-up pulses without introducing inefficiency due to smaller signals.



CBC Chip Calibration :

Preparing CBC for data taking : HIP suppression Hit Detection

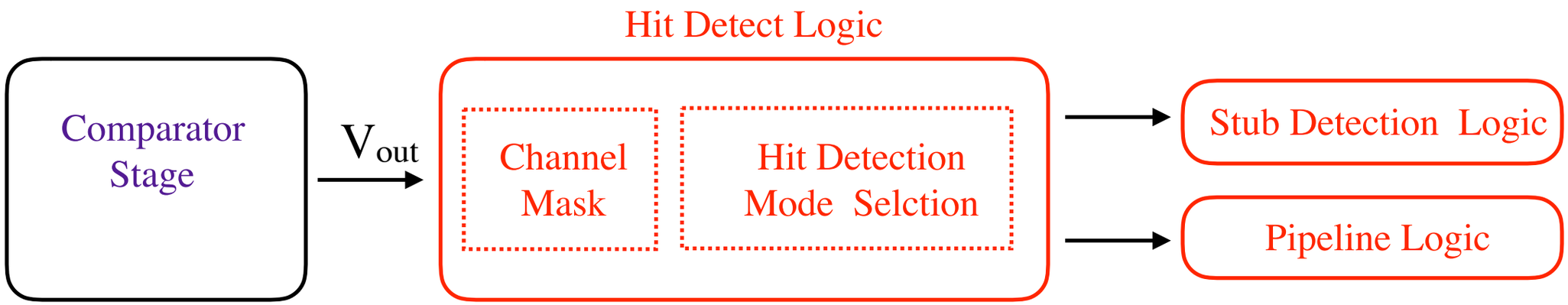
- Only implemented on the CBC3
  - designed to suppress the detection of highly ionizing particles
  - can be applied to either the 40 MHz sampled output or the Logical OR output of each channel
  - checks the length of the pulse again a pre-programmed number of clock cycles
  - forces the output to return to zero if that number of clock cycles is exceeded



CBC Chip Calibration :

Checklist for preparing CBC for data taking

- Configuring the CBC for data taking requires :



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- might require masking out noisy channels from the hit detection logic

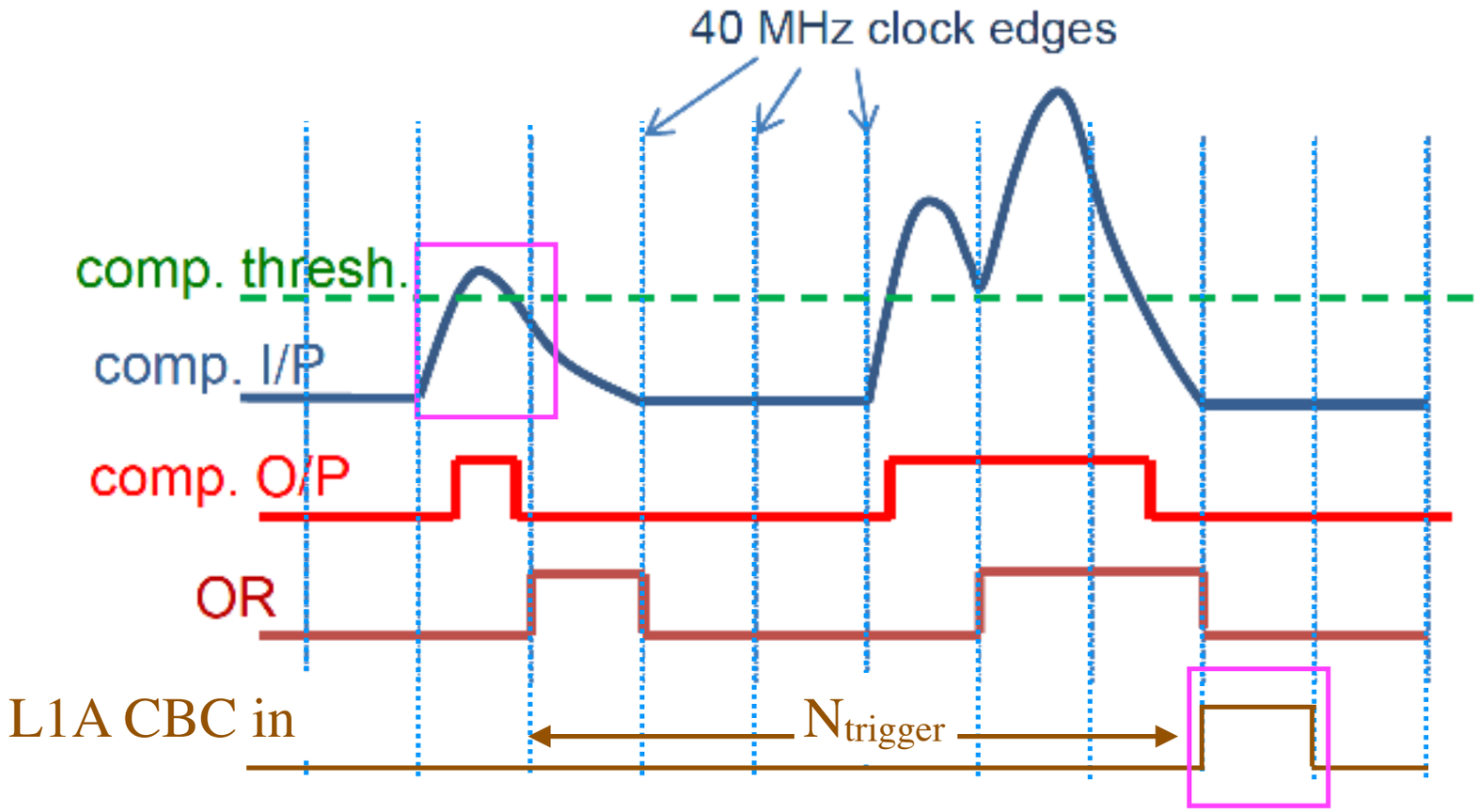
☑ Selecting the hit detection mode most appropriate to your test

- Selecting appropriate data latency for your particular set-up (will be dependent on cable lengths, external trigger system)
- Selecting appropriate stub latency

CBC Chip Calibration :

Preparing CBC for data taking : trigger latency.

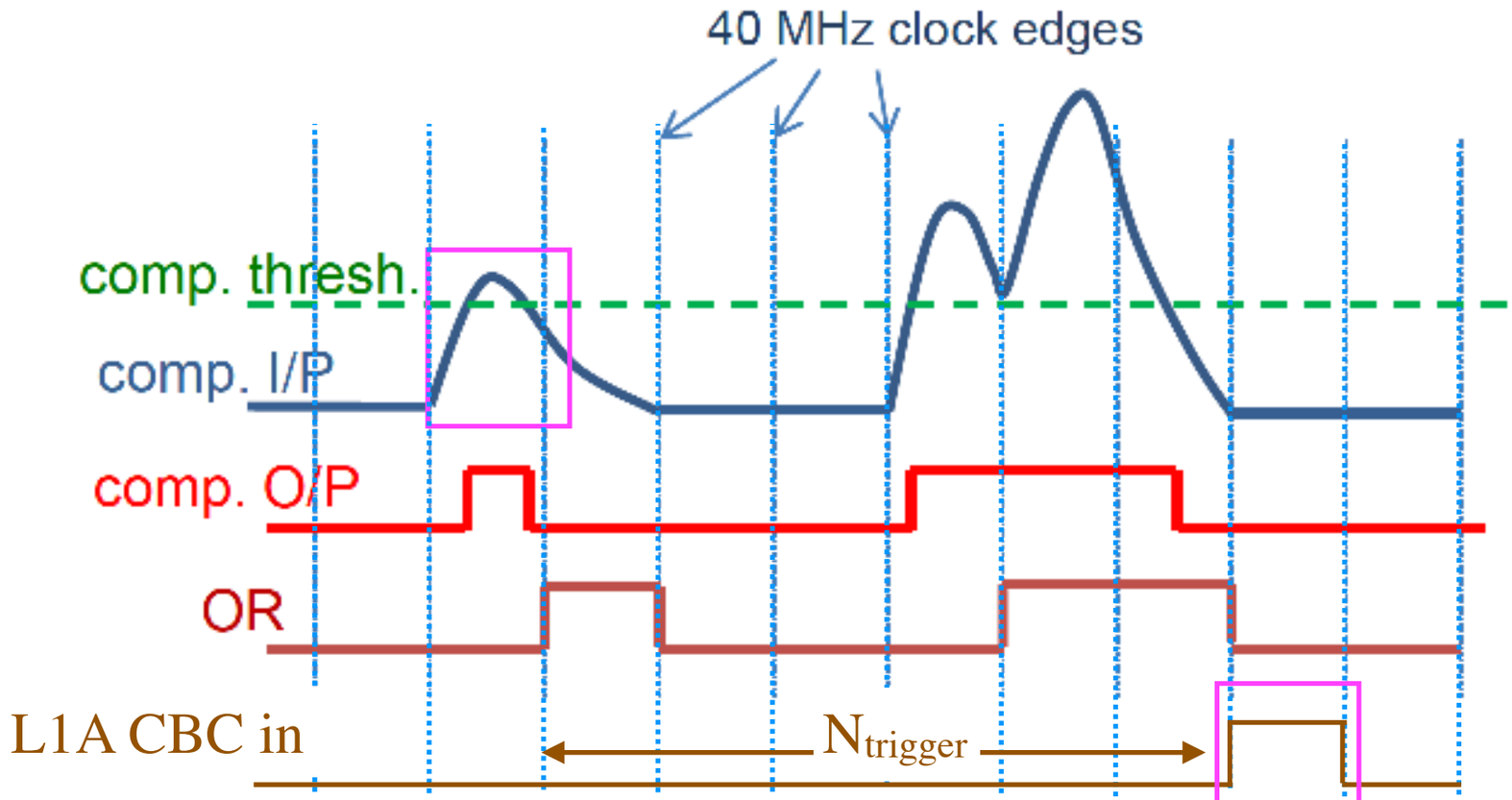
- Expect a delay between detecting signal on the CBC and the trigger (e.g. L1A) arriving



CBC Chip Calibration :

Preparing CBC for data taking : trigger latency.

- Expect a delay between detecting signal on the CBC and the trigger (e.g. L1A) arriving
  - internally, the trigger latency is controlled by the pipeline control logic of the chip
    - Write Counter in pipeline starts counting from 0 when the CBC is initialized
    - Trigger Counter only begins counting $N_{trigger}$ clock cycles after initialization of the Write counter
      - this defines a position in RAM to read data from when an external trigger is received



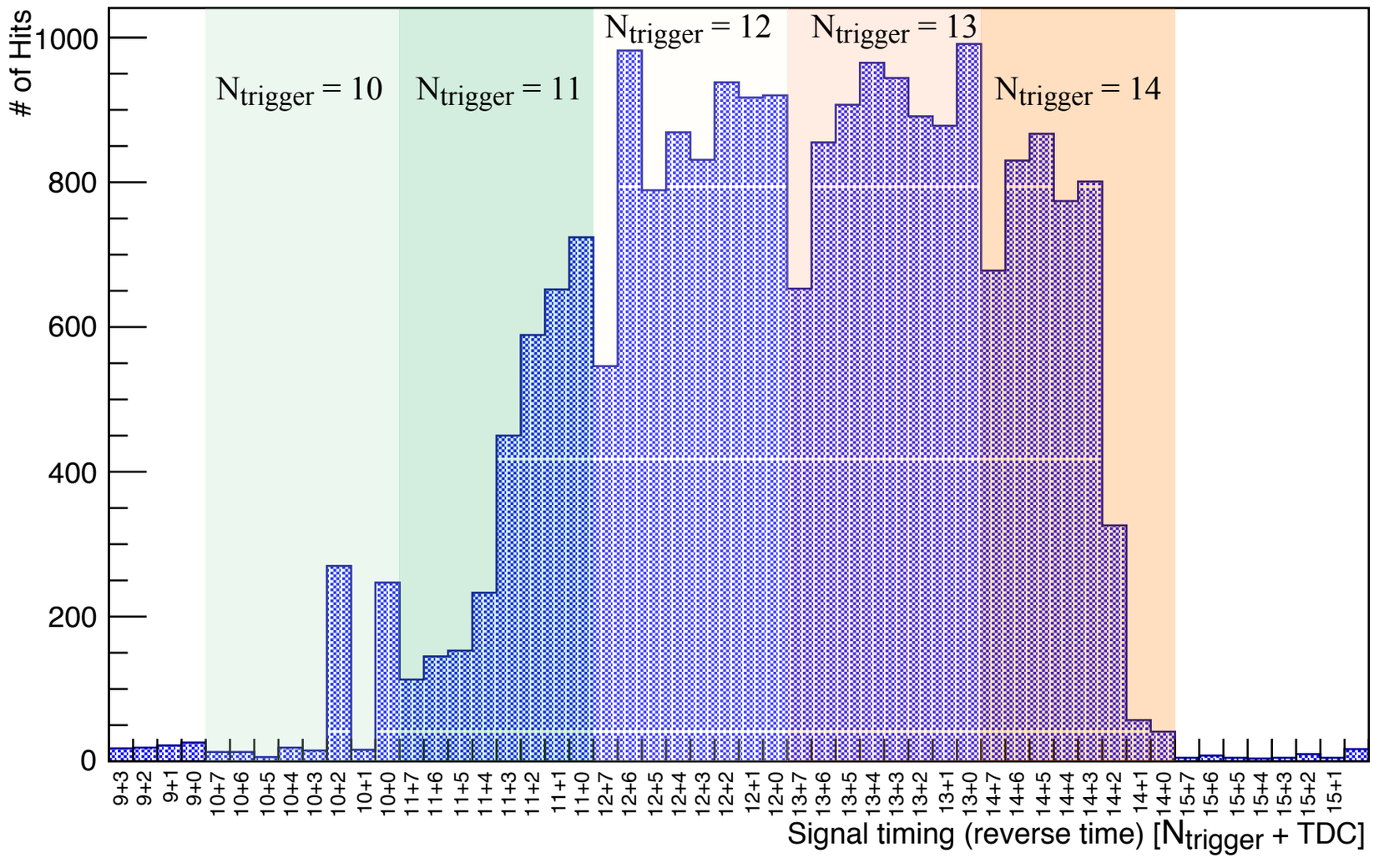
N.B. offset between trigger and write counter checked constantly by latency check circuitry

error bit set if this deviates from the configured value

CBC Chip Calibration :

Trigger Latency Tuning Procedure : CBC2

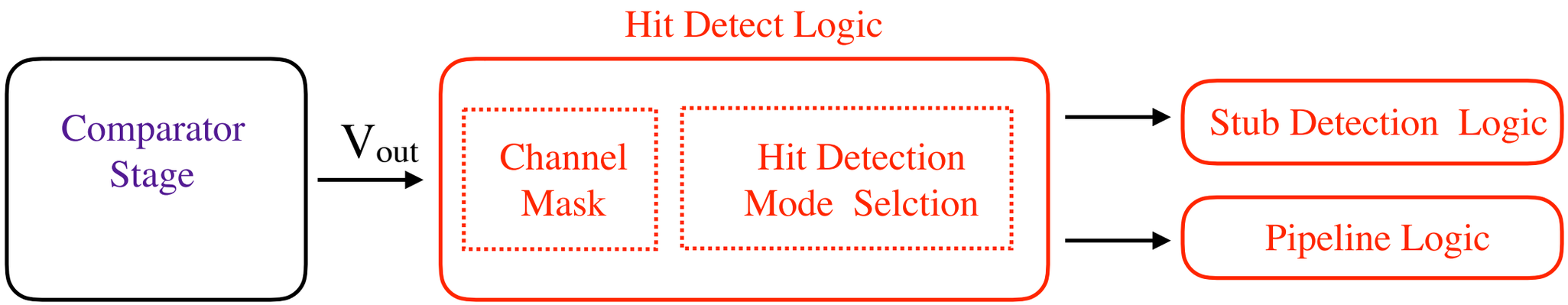
- Identifying the trigger latency ($N_{trigger}$ clock cycles delay) in the set-up used for test beams of the CBC2 in the CERN North Area :
  - $N_{trigger}$ is scanned using the trigger latency control register in the CBC
  - the TDC phase measures the time of arrival of the trigger signal at the back end (BE) with respect to the 40 MHz clock edge using a 3 bit counter (0-7) counting at 320 MHz
  - $N_{trigger}$ chosen to maximize hit detection efficiency.



CBC Chip Calibration :

Checklist for preparing CBC for data taking

- Configuring the CBC for data taking requires :



☑ Uniform sensitivity across the 254 channels of each CBC (i.e. uniform pedestals)

- might require masking out noisy channels from the hit detection logic

☑ Selecting the hit detection mode most appropriate to your test

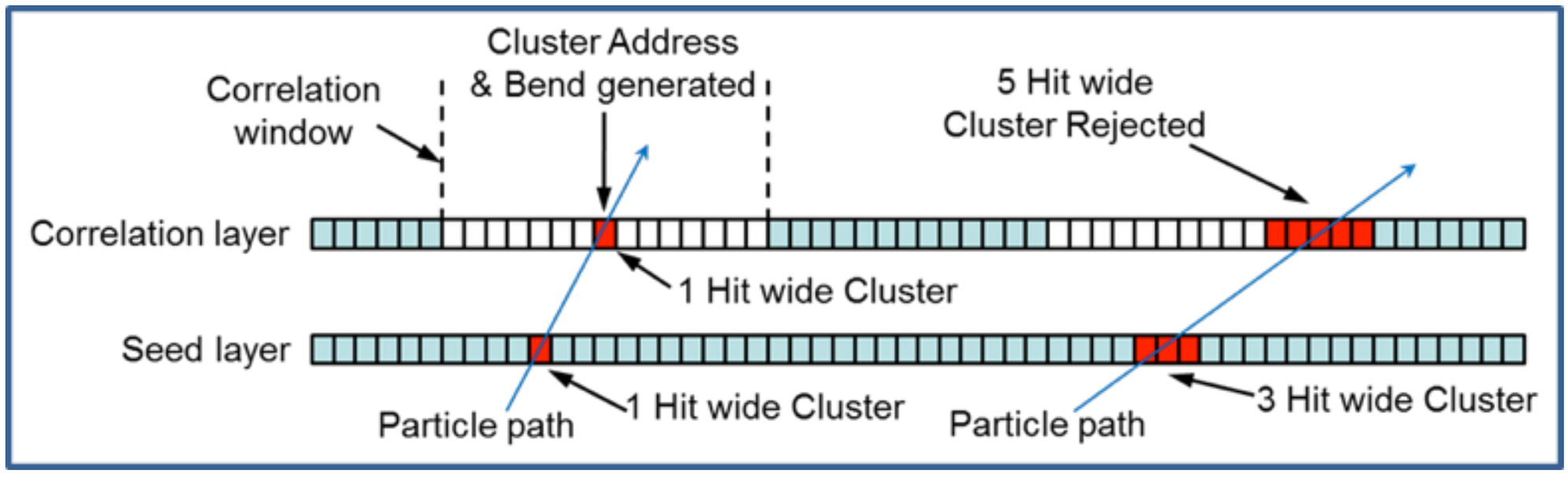
☑ Selecting appropriate data latency for your particular set-up (will be dependent on cable lengths, external trigger system)

- Selecting appropriate stub latency

CBC Chip Calibration :

Preparing CBC for data taking : stub latency.

- Stub finding logic in the CBCs :
  - initial stage that rejects wide clusters on both sensor layers
    - for valid cluster on bottom (seed) sensor logic looks for hits in a coincidence window on the top (correlation) sensor
      - if a hit is found in the correlation layer then a valid stub is found in the central strip of the seed layer

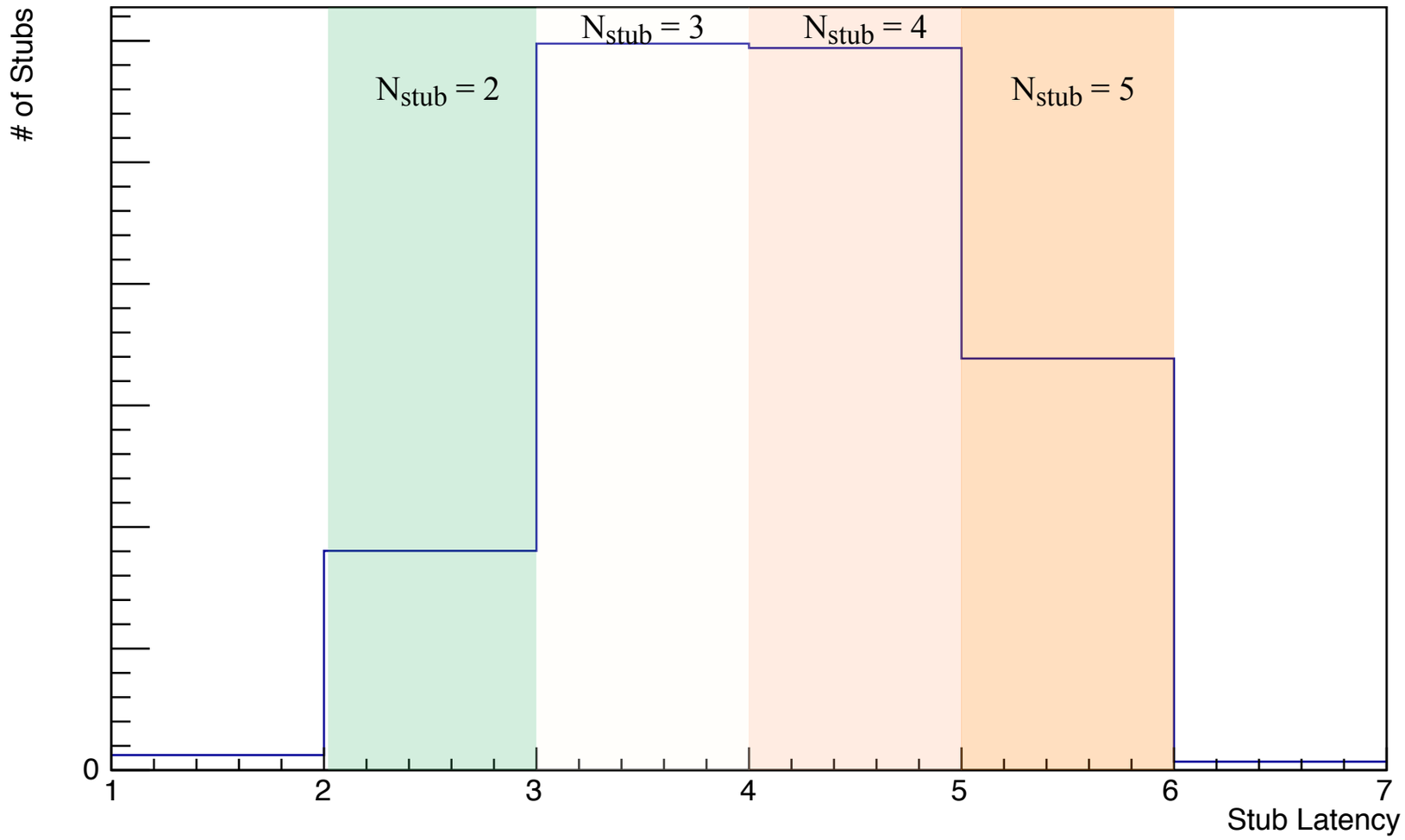


- CBC2 : simple OR of all valid stubs is output at 40 MHz.
- CBC3 : the stub gathering logic outputs on 5 dedicated SLVS lines all the stub information at 320 MHz
  - a maximum of 3 stubs can be output on a given clock edge (bunch crossing)
  - stub data packet consists of : sync bit + error bits + hit OR + stub bend(s) + address(es)

CBC Chip Calibration :

Preparing CBC for data taking : stub latency.

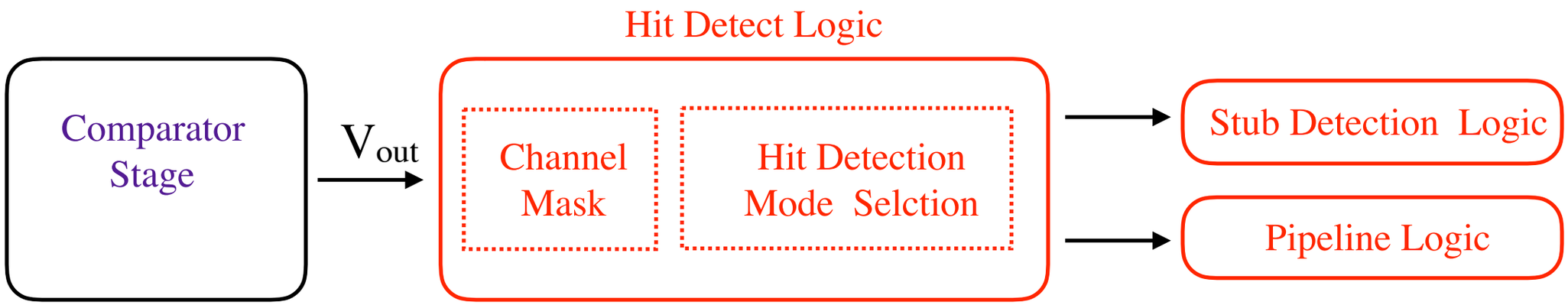
- Expect a delay between (hit/triggered) data and stub data arriving at the back-end of the DAQ system
  - delay is defined in the back-end FPGA as the stub latency N_{stub}
    - firmware needs to know this value in order to perform data matching between the triggered and stub data
  - N_{stub} chosen to maximize number of stubs found in data



CBC Chip Calibration :

Checklist for preparing CBC for data taking

- Configuring the CBC for data taking requires :



☑Uniform sensitivity across the 254 channels of each CBC (i.e. uniform pedestals)

- might require masking out noisy channels from the hit detection logic

☑Selecting the hit detection mode most appropriate to your test

☑Selecting appropriate data latency for your particular set-up (will be dependent on cable lengths, external trigger system)

☑Selecting appropriate stub latency

Details on Firmware and Middleware implementation …..

after the break!