

EEEN202 Lab 3 Sequential Logic: Counters

Section 3

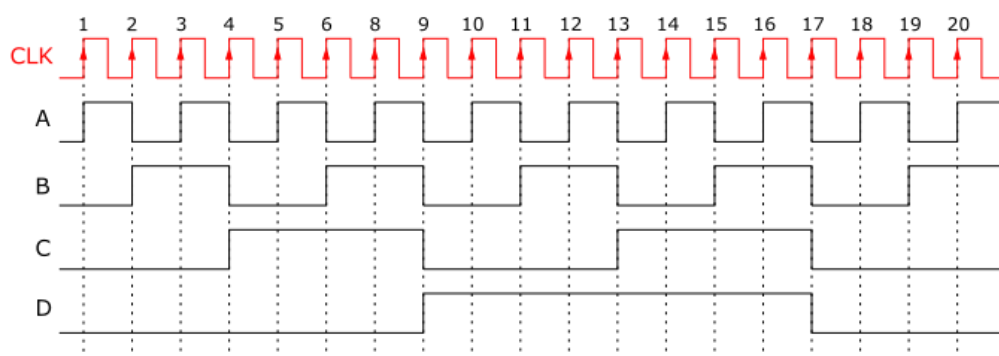
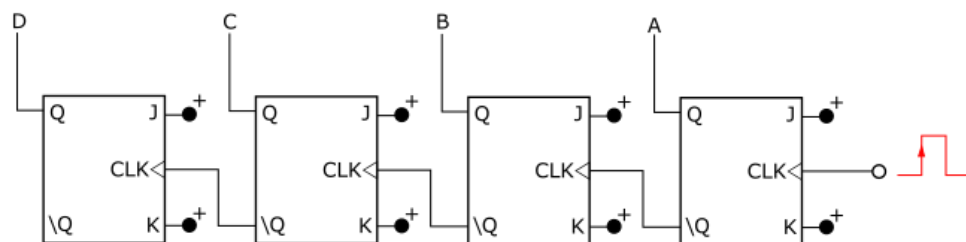
3.1 – J-K FF

Initial state: Enable: 1, Reset: 0, Clear: 0, J = 1, K = 1, Q = 0

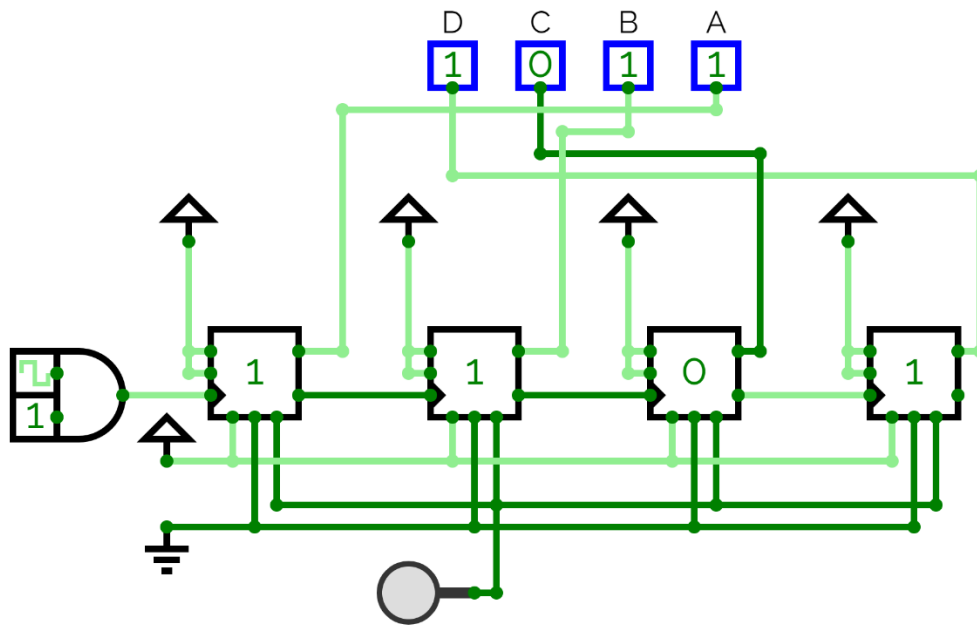
J	K	Q after CLK pulse	Resulting FF
0	0	0	0
0	1	0	0
1	0	1	1
1	1	0	0

- (i) The FF transitions off LO to HI pulse i.e., it's a rising edge FF
- (ii) When enable goes LO, the FF stops operating. The current state of the FF persists
- (iii) When Preset goes HI, nothing changes. If Reset goes HI whilst Preset = HI, the FF transitions to the set state, or FF = 1
- (iv) When Clear/K goes HI, and Q = 1, FF transitions and Q = 0 and /Q = 1. If /Q = 1, then nothing changes

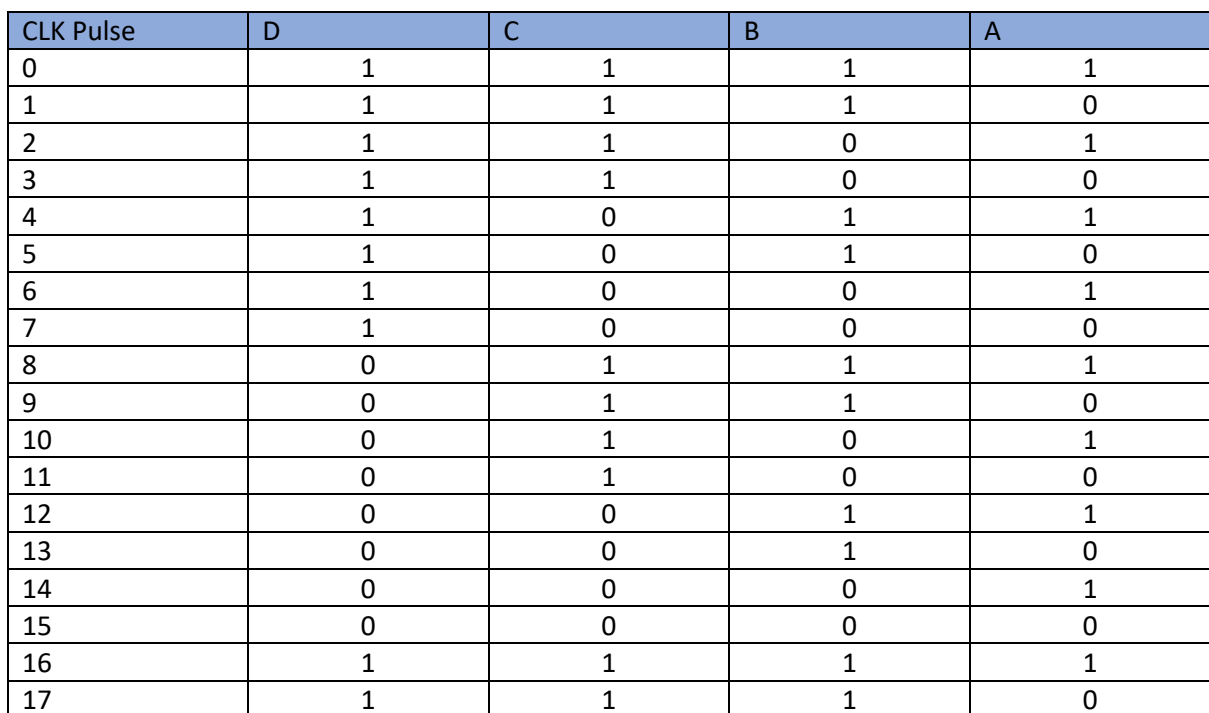
3.2 – 4 Bit asynchronous counter using rising edge J-K FF + 3.3 – Timing diagram



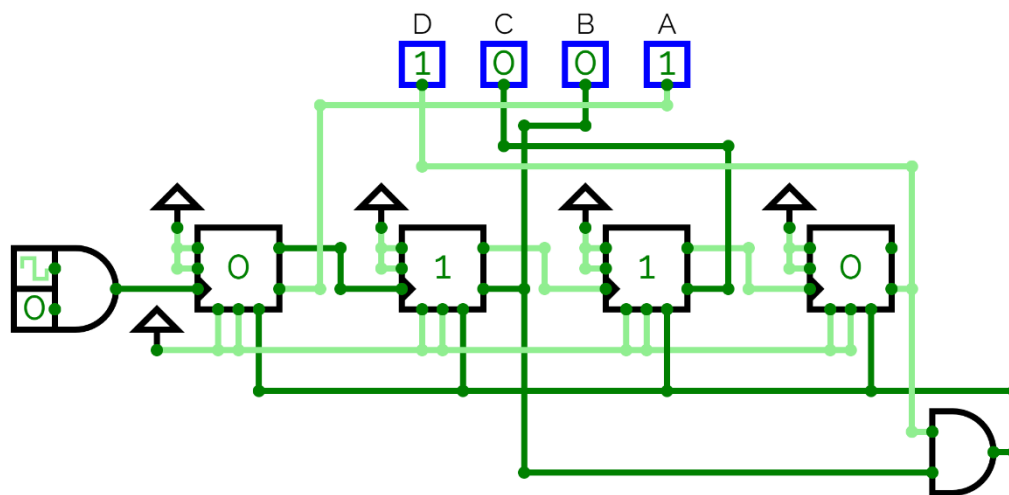
3.4 – Circuitverse and table



CLK Pulse	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0
17	0	0	0	1


$$f_{out} = \frac{CLK}{MOD}$$

3.7 – MOD 10 counter



Section 4

4.1 – J-K edge-triggered flip-flop

Inputs before nth CLK pulse		Outputs after nth CLK pulse	
J	K	Q	\bar{Q}
0	0	0	1
0	1	0	1
1	0	1	0
1	1	0	1

4.2

Set line (active low): when pulled to LO, Q of all the FF's gets locked to HI i.e., pulsing the CLK of the first FF does nothing. Pulsing LO sets Q of all FF's to HI, but does not lock it

Clear line (active low): when pulled to LO, Q of all the FF's gets locked to LO. Pulsing LO sets Q of all the FF's to LO.

4.3

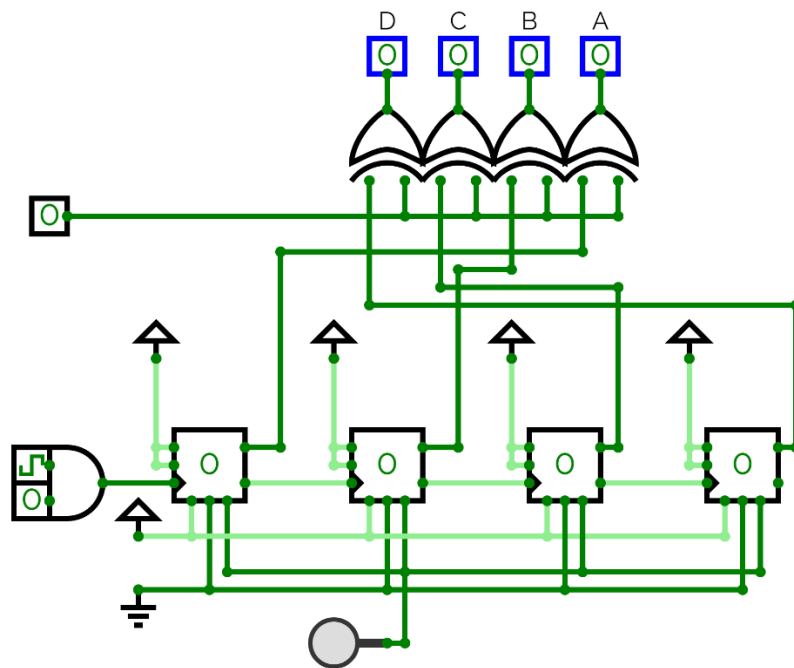
(i) MOD 12 counter: NAND gate with inputs from D and C

(ii) MOD 10 counter: NAND gate with inputs from D and B

4.4

(i) Down counter: take the \bar{Q} output or use a NOT gate for each output

(ii) Flexible counter: have an XOR gate for each output of an up counter. One input is the output of an FF and the other is tied to a switch. When turned on, the XOR turns into NOT gate, turning the up counter into a down counter. Circuitverse example:



Section 5

5.(i) – 50hz to 1hz converter (Circuitverse sim)

MOD 50 counter using the reset AND gate as the output

