Name _____

ECEN202 Test 2, 80 points total.
5 June 2019
Closed Book. Please staple any additional pages to this test, and add your name to all pages.

1) The AT89C51AC3 is 'binary compatible' with which popular microcontroller? ***(1pt)***

2) ***2A - 2D, 1 point each.***
A) What high-level computer architecture makes use of a shared data and program memory?

B) What high-level computer architecture makes use of separate data and program memories?

C) Which of the architectures from questions 2A and 2B does the 8051 employ?

D) What does CISC stand for, and is the 8051 an example of a CISC system?

3) In a standard 8051, how many clock cycles result in one machine cycle? ***(1pt)***

4) A) Given a 40 MHz crystal, find the time (in μs) required for one machine cycle. ***(2pt)***

B) Given a 12 MHz crystal, find the time (in μs) required for one machine cycle. ***(2pts)***

5) A) In a CPU, what does ALU stand for? ***(1pt)***

B) In the 8051, what is an alternative name for Register A? ***(1pt)***

C) How many bits is Register A? ***(1pt)***

D) What register holds the address of the next instruction to be executed? ***(1pt)***

6) A) What is 0d16 in hexadecimal? ***(1pt)***

B) What is a larger numerical value: 0d128 or 0xFF? ***(1pt)***

C) What is a smaller numerical value: 0b10000000 of 0xFF? ***(1pt)***

D) Circle or underline the lower nibble of this 8051 byte: 0b10101010 ***(1pt)***

7) A) On the 8051, what does the NOP instruction do? ***(1pt)***

B) On the 8051, what does the INC instruction do? ***(1pt)***

8) Multiple choice (circle one of a-d): On the 8051, when MOV A,B is called, which of the following occurs? ***(1pt)***

a) The contents of B are moved to A, with B's contents being cleared after this operation.

b) The contents of a A are moved to B, with A's contents being cleared after this operation.

c) The contents of B are moved to A, with B's contents being retained after this operation.

d) The contents of a A are moved to B, with A's contents being retained after this operation.

9) Multiple choice (circle one of a-d): On the 8051, which of the following instructions is directly associated with a subroutine call? ***(1pt)***

a) LJMP

b) SJMP

c) ACALL

d) INC

10) In a hex file, what is the role of the checksum, and (in an 8051 hex file) how is it calculated? ***(1pt)***

11) a) How many register banks does the 8051 have? ***(1pt)***

b) By default, which register bank is occupied by the 8051's stack? ***(1pt)***

c) When looking at the 8051's memory map, what does SFR stand for? ***(1pt)***

d) ***(1pt)*** What addressing mode is used by the following instruction? **`MOV A, R7`**

12) a) What instruction is used to add data to the stack? ***(1pt)***

b) What instruction is used to remove data from the stack? ***(1pt)***

c) What register (containing the last used location of the staack) is incremented/decremented by the instructions in (12a) and (12b)? ***(1pt)***

13) Timer mode information and details about the TMOD register are provided. Write code that sets Timer 0 to Mode 1 and Timer 1 to Mode 3. Assume that TMOD holds other values that must not be overwritten. ***(3pts)***

	Mode name
MODE 0	13-bit timer mode: 8 bits of THx and 5 bits of TLx
MODE 1	16-bit timer mode. TLx counts 0-255; on overflow, this adds 1 to THx
MODE 2	8-bit timer mode. TLx auto-reloads with THx value.
MODE 3	“Split timer” mode: THx is one 8-bit timer, and TLx is another.

TMOD.7	TMOD.6	TMOD.5	TMOD.4	TMOD.3	TMOD.2	TMOD.1	TMOD.0
GATE When 1, timer only counts when TR1 bit is high and there is an external interrupt at INT0	C/T When 0, Timer1 serves as XTAL-driven delay generator (timer); When 1, Timer1 counts external events	M1 Timer 1 Mode bit 1 (see figure below for more info.)	M0 Timer 1 Mode bit 0 (see figure below for more info.)	GATE When 1, timer only counts when TR0 bit is high and there is an external interrupt at INT1	C/T When 0, Timer0 serves as XTAL-driven delay generator (timer); When 1, Timer0 counts external events	M1 Timer 0 Mode bit 1 (see figure below for more info.)	M0 Timer 0 Mode bit 0 (see figure below for more info.)

Timer 0 Mode Select Bit

M10	M00	Operating mode
0	0	Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).
0	1	Mode 1: 16-bit Timer/Counter.
1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL0) (2)
1	1	Mode 3: TL0 is an 8-bit Timer/Counter

TH0 is an 8-bit Timer using Timer 1’s TR0 and TF0 bits.

14) ***(3pts)*** Information about the TCON register is provided below. Assume that TCON holds other values that must not be overwritten. Write code that sequentially fulfils the following three steps:
Step 1: Stop Timer 0.
Step 2: Clear Timer 0’s overflow flag.
Step 3: Start Timer 0.

TCON.7	TCON.6	TCON.5	TCON.4	TCON.3	TCON.2	TCON.1	TCON.0
TF1 Timer 1 Overflow Flag 1 when overflow occurs. Must be cleared in software; auto. cleared when leaving ISR	TR1 Timer 1 run bit 1: Start timer 0: Stop timer (Software controlled)	TF0 Timer 0 Overflow Flag 1 when overflow occurs. Must be cleared in software; auto. cleared when leaving ISR	TR0 Timer 0 run bit 1: Start timer 0: Stop timer (Software controlled	IE1 Ext. interrupt1 edge flag. 1: external interrupt occurred. 0: External interrupt processed. (Hardware controlled; no need to edit this)	IT1 Interrupt1 trigger type select bit. 1: Interrupt occurs on the falling edge of INT1. 0: Interrupt occurs on INT1’s level being LOW.	IE0 Ext. interrupt0 edge flag. 1: external interrupt occurred. 0: External interrupt processed. (Hardware controlled; no need to edit this)	IT0 Interrupt0 trigger type select bit. 1: Interrupt occurs on the falling edge of INT1. 0: Interrupt occurs on INT1’s level being LOW.

15) ***(3pts)*** Using information about the TMOD and TCON registers provided above, write code that sequentially fulfils the following steps. Assume that your registers begin in a zeroed out state.
Step 1: Set Timer 1 as a counter in Mode 2.
Step 2: Clear the TH1 register (TH1 = register that holds counter values)
Step 3: Start Timer 1

16) Briefly describe the role, function, and use of a watchdog timer. ***(2pts)***

17) Briefly describe the advantages of an interrupt-driven approach compared to a blocking/ polling approach. ***(2pts)***

18) a) In relation to interrupts, what does ISR stand for? ***(1pt)***

b) What timer condition triggers a Timer-related interrupt? ***(1pt)***

c) What two pin states can be used to trigger an external interrupt? ***(1pt)***

d) On the 8051, INT0 and INT1 are what type of interrupt? ***(1pt)***

19) ***(2pt)*** 8051 assembly language programs often contain variations of the following code. Briefly explain the point of the ORG and LJMP instructions as they relate to interrupt vector tables.

```
ORG 0000H
LJMP MAIN

//ISR CODE HERE

ORG 0030H
MAIN:
//MORE CODE HERE, INCLUDING CONFIG CODE
```

21) ***(5pts)*** Fill in the blanks with 8051 assembly language code that fulfils the behaviour described in the comments. Each blank (5 blanks total) has a corresponding comment that should be realised in code. Details about the IEN0 register are below. Consult prior pages' details about other registers.

IEN0.7 EA Enable all interrupts 1: interrupts may be enabled individually 0: All interrupts are disabled.	IEN0.6 EC PCA interrupt enable When 1, PCA interrupt is enabled.	IEN0.5 ET2 Timer 2 Overflow Interrupt Enable When 1, Timer 2 interrupt is enabled.	IEN0.4 ES Serial Port interrupt enable bit. When 1, serial port interrupt is enabled.	IEN0.3 ET1 Timer 1 Overflow Interrupt Enable When 1, Timer 1 interrupt is enabled.	IEN0.2 EX1 External interrupt 1 enable bit. When 1, External Interrupt 1 is enabled.	IEN0.1 ET0 Timer 0 Overflow Interrupt Enable When 1, Timer 0 interrupt is enabled.	IEN0.0 EX0 External interrupt 0 enable bit. When 1, External Interrupt 0 is enabled.

```
ORG 0000H
LJMP MAIN

;— ISR: Interrupt 1, toggles LED when new interrupt arrives.

_____________ ;directive to place ISR code at INT1 vector table
              ;location (0013H)

_____________ ;Toggle Port 1 pin 3 (CPL instruction)

_____________ ;Instruction to reset PC and clear interrupt flags

;Set up interrupts at ROM location past vector table
ORG 0030H
MAIN:

_____________ ;In TCON, set Interrupt 1 to falling edge triggered

_____________ ;In IEN0, enable all interrupts and INT1. You may
              ;assume that IEN0 is initially zeroed out.

IDLE: SJMP IDLE ;Other code could go here. Idle main CPU for now.
END
```

22) Why do we need to call PSIDLE when using the ADC in precision mode? ***(1pt)***

23) ***(2pts)*** Write assembly language code that fulfils the following steps. Write one line of code per step.

ADCON.7 Mnemonic: *n/a* (Unused)	ADCON.6 Mnemonic: *PSIDLE (pseudo idle mode)* (1: Convert in CPU idle mode) (0: Convert without idling CPU)	ADCON.5 Mnemonic: *ADEN (Enable/ Standby mode)* (1: ADC enabled) (0: low-power standby mode)	ADCON.4 Mnemonic: *ADEOC (End of conversion), can generate an interrupt* (1: result ready to be read, set by HW, must be cleared in software)	ADCON.3 Mnemonic: *ADCSST (Start & Status)* *(1: Start an ADC conversion* *0: Cleared by HW after conversion complete)*	ADCON.2:0 Mnemonic: *SCH2:0 (Selection of channel to convert)*

Step 1) From standby mode, enable the ADC.
Step 2) Using ORL, begin a conversion; all 10 bits of the conversion will be needed, so CPU noise must be minimised.

24) ***(1pt)*** Multiple choice. Circle one of A-D. Which of the following is not true about the AT89C51AC3?

A) It has three 16 bit timers

B) It has two 10-bit ADCs

C) It has two external interrupt pins

D) It has one watchdog timer

25) The initial contents of Register A are 0b11001100. What are the contents of register A after the execution of an ORL instruction against A with an operand of 0b00110011? ***(2pt)***

26) The initial contents of Register A are 0b11111111. What are the contents of register A after the execution of an ANL instruction against A with an operand of 0b00100000? ***(2pt)***

27) The A register has an initial value of 0b00000100
What are the register's contents after executing the following code? ***(2pt)***

```
RR A
RR A
ANL A, #10000011B
```

28) A) Sketch a basic design for a 4 bit flash converter that will convert voltages in the input range 0 – 8 V. ***(3pts)***
B) Indicate the resistor values that you will use to create the desired reference voltages. ***(2pts)***
C) What will be the binary output code for an input voltage of 3.4 V ? ***(2pts)***

29) A thermocouple (temperature sensor) has an output of 0 to 46 mV over a measuring range of 0 – 800 degrees C.

A) Calculate by how much the output of a 12 bit A/D converter with a 0 – 5 V input range would change over the full input range of the thermocouple. ***(3pts)***
B) What would be the temperature resolution of this system? ***(2pts)***
C) Would this be a practical system, why or why not? ***(1pts)***
D) What would be the resolution if a 16 bit A/D was used? ***(2pts)***
E) What can be done to improve this situation? ***(1pt)***