EEEN202 Lab 2 Sequential Logic: Latches & Flip-flops

Section 3

3.1 – Basic NAND SC latch

SET	CLEAR	Q	$\bar{Q}$	Latch State
1	1	1	0	SET
0	1	1	0	SET
1	1	1	0	SET
1	0	0	1	CLEAR
1	1	0	1	CLEAR
0	0	1	1	UNDEF

Limitations of the basic SC latch

1. If both inputs are set to LO, then the SC latch becomes unstable, and the output is undefined (as the latch tries to SET and CLEAR simultaneously
2. The SC latch is asynchronous, meaning it can't be controlled by a clock

3.2 – Enabling a line

(i) AND Gate

A	E	X
0	0	0
1	0	0
0	1	0
1	1	1

(ii) Boolean expression:

When E = 0:

$$X = A \cdot 0 = 0$$

When E = 1:

$$X = A$$

(iii) Setting a clock on A

E	X
0	0
1	1 or 0 (dependent on current clock signal)

(iv) When E = 0, the output is 0. When E = 1, the output changes from 1 – 0 depending on current signal from the clock. Essentially, E acts a switch that either blocks or allows the clock source to output through the AND gate

(v) NAND truth table

A	E	X
0	0	1
1	0	1
0	1	1

1	1	0

(vi) Boolean expression:

When E = 0:

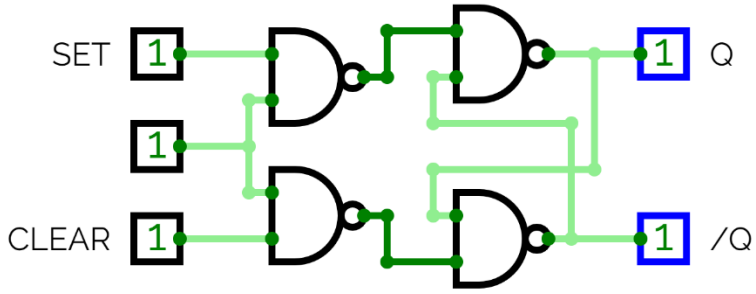
$$X = \overline{A \cdot 0} = 1$$

When E = 1:

$$X = \bar{A}$$

(vii) When E = 0, the output is 1. When E = 1, the output changes from 0 – 1 depending on current signal from the clock like before. However, the NAND gate acts as an inverter while E = 1, so the output is out of phase with the input

(viii) Adding NAND gate enabled input



E	SET	CLEAR	Q	$\bar{Q}$	Latch state
0	0	0	0	1	CLEAR
0	1	0	0	1	CLEAR
0	0	0	0	1	CLEAR
0	0	1	0	1	CLEAR
0	1	0	0	1	CLEAR
0	1	1	0	1	CLEAR
1	0	0	0	0	CLEAR
1	1	0	1	0	SET
1	0	0	1	0	SET
1	0	1	0	1	CLEAR
1	1	0	1	0	SET
1	1	1	1	1	UNDEF

(ix)

E is now required to be HI for the latch to operate. When E = 0, the latch remains in whatever state it was before

(x)

The inputs are now active HI i.e., they change when the inputs change on a high input

Section 4

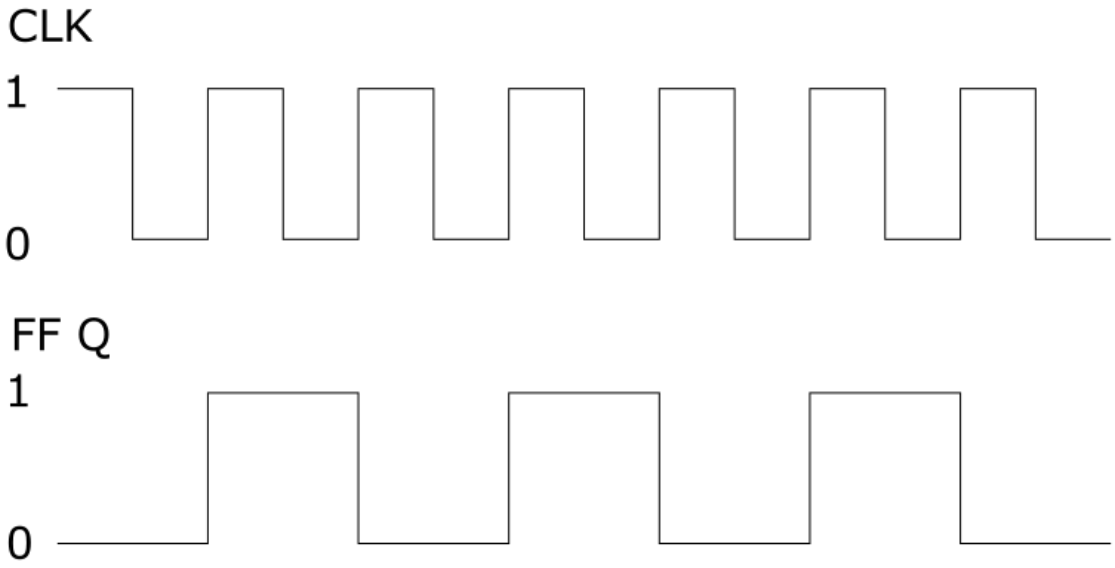
4.1 – Edge-triggered D Flip-flop

While the state only toggles on the rising edge (LO -> HI) of the clock, the input set and reset switches can be flipped any time, meaning their operation is asynchronous. However, flipping one of the switches during the CLK HI pulse doesn't change the state until the next HI, therefore the flip-flop inputs are only sensitive during the edge.

The oscilloscope shows that the outputs (yellow line) only change on the rising edge of the clock input (blue line)

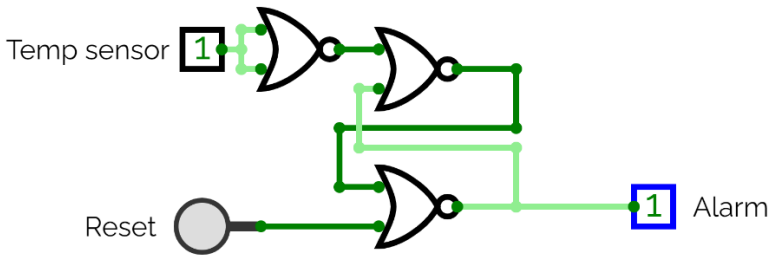
4.2 – JK edge-triggered flip-flop

Inputs before nth CLK pulse		Outputs after nth CLK pulse	
J	K	Q	$\bar{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	0	1



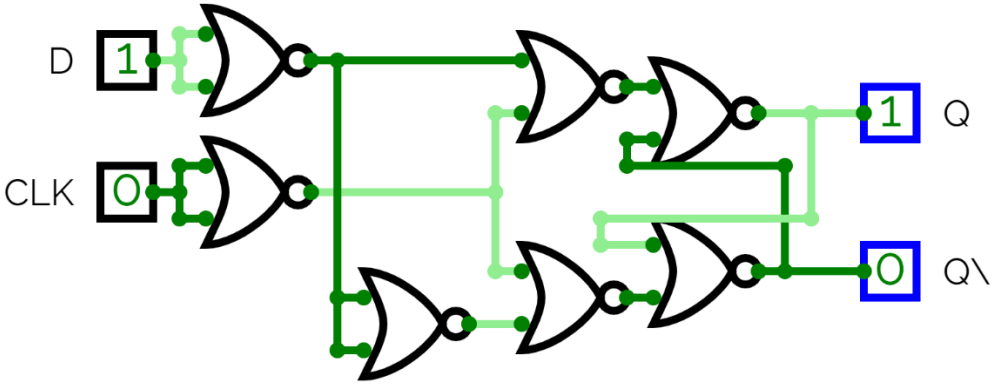
4.3 – NOR gate alarm

74HCT02 Alarm circuit diagram



Section 5

5.1 – D FF using NOR gates



5.2

5.3