BLG222E Computer Organization

Project 3

Due Date: 15.05.2019

Design a **hardwire-control unit** for the following architecture. Use the structure that you have designed in project #2.

Instruction format

There are two types of instructions as described below.

(1) Instructions with address reference has the format shown in Figure 1:

- The OPCODE is a 5-bit field (See Table 1 for the definition).
- The REGSEL is a 2-bit field (See left side of Table 2 for the definition).
- The ADDRESSING MODE is a 1-bit field (See Table 3 for the definition).
- The ADDRESS is 8 bits

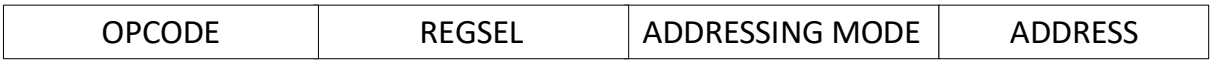

Figure 1: Instructions with an address reference

(2) Instructions without address reference has the format shown in Figure 2:

- The OPCODE is a 5-bit field (See Table 1 for the definition).
- DESTREG is a 3-bit field which specifies the destination register (See right side of Table 2 for the definition).
- SRCREG1 is a 3-bit field which specifies the first source register (See right side of Table 2 for the definition).
- SRCREG2 is a 3-bit field which specifies the second source register (See right side of Table 2 for the definition).

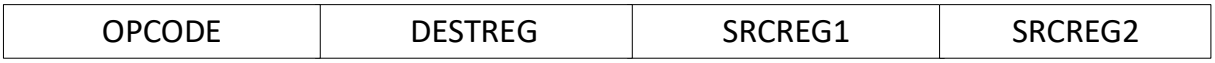

Figure 2: Instructions without an address reference

Table 1: OPCODE field and SYMBols for opertions and their descriptions

OPCODE (HEX)	SYMB	ADDRESSING MODE	DESCRIPTION
0x00	ADD	N/A	DESTREG ← SRCREG1 + SRCREG2
0x01	SUB	N/A	DESTREG ← SRCREG2 - SRCREG1
0x02	DEC	N/A	DESTREG ← SRCREG1 - 1
0x03	INC	N/A	DESTREG ← SRCREG1 + 1
0x04	BRA	IM	PC ← Value
0x05	BEQ	IM	IF Z=1 THEN PC ← Value
0x06	BNE	IM	IF Z=0 THEN PC ← Value
0x07	LSL	N/A	DESTREG ← LSL SRCREG1
0x08	LSR	N/A	DESTREG ← LSR SRCREG1
0x09	LD	IM, D	Rx ← Value (Value is described in Table 3)
0x0A	ST	D	Value ← Rx
0x0B	MOV	N/A	DESTREG ← SRCREG1
0x0C	NOT	N/A	DESTREG ← NOT SRCREG1
0xOD	OR	N/A	DESTREG ← SRCREG1 OR SRCREG2
0x0E	AND	N/A	DESTREG ← SRCREG1 AND SRCREG2

Table 2:REGSEL (Left) and DESTREG/SRCREG1/SRCREG2 (Right) select the register of interest for a particular instruction

REGSEL	REGISTER
00	R3
01	R2
10	R1
11	R0

DESTREG/SRCREG1/SRCREG2	REGISTER
000	R3
001	R2
010	R1
011	R0
100	AR
101	SP
110	PC
111	PC

Table 3: Addressing modes

ADDRESSING MODE	MODE	SYMB	Value
0	Direct	D	M[AR]
1	Immediate	IM	ADDRESS Field

Example Code:

The code given below adds data that are stored at M[A0]+M[A1]+M[A2]+M[A3]+M[A4] and stores the total at M[A5]. It is written as a loop that iterates 5 times.

```
        ORG 0x20          # Write the program starting from the address 0x20
        LD R0 IM 0x05     # R0 is used for iteration number
        LD R1 IM 0x00     # R1 is used to store total
        LD R2 IM 0xA0
        MOV AR R2          # AR is used to track data adrress: starts from 0xA0
LABEL:  LD R2 D           # R2 <- M[AR] (AR = 0xA0 to 0xA4)
        INC AR AR         # AR <- AR + 1 (Next Data)
        ADD R1 R1 R2      # R1 <- R1 + R2 (Total = Total + M[AR])
        DEC R0 R0         # R0 <- R0 – 1 (Decrement Iteration Counter)
        BNE IM LABEL      # Go back to LABEL if Z=0 (Itertaion Counter > 0)
        INC AR AR         # AR <- AR + 1 (Total will be written to 0xA5)
        ST  R1 D          # M[AR] <- R1 (Store Total at 0xA5)
```