30.11.2023

Field Effect Transistors (FETs)

1. They are unipolar devices — Operation depends on only one type of charge-carriers (free electrons or holes).

2. It means FET has majority charge-carriers (No minority carriers)
Majority charge-carrier devices

3. FETs are preferred devices for most switching applications. (No stored minority charge has to be removed from the junction area)

4. FETs are voltage-controlled devices. (BJTs are current-controlled devices)
(Field)

5. Drift Transport of majority charge-carriers.

Reasons for popularity of FETs:

1. Operation of FETs is very simple.

2. Fabrication of FETs requires few steps.

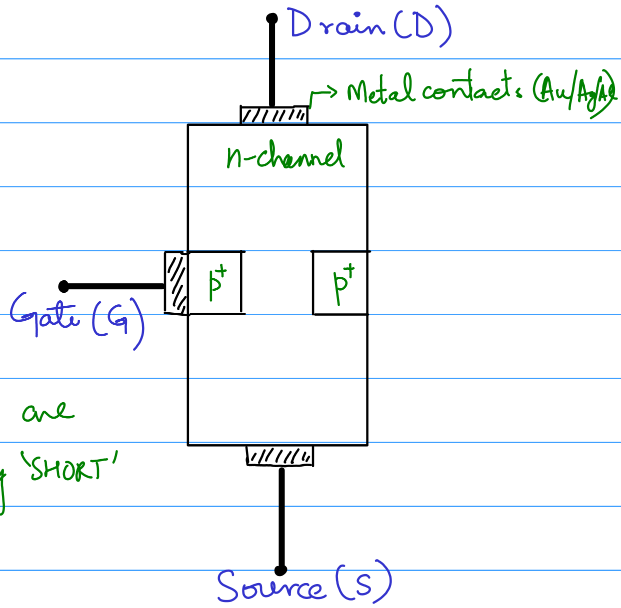
3. FET requires $\frac{1}{5}$th space as compared to BJTs.
(High density of the devices on the chip).

Types of FETs:

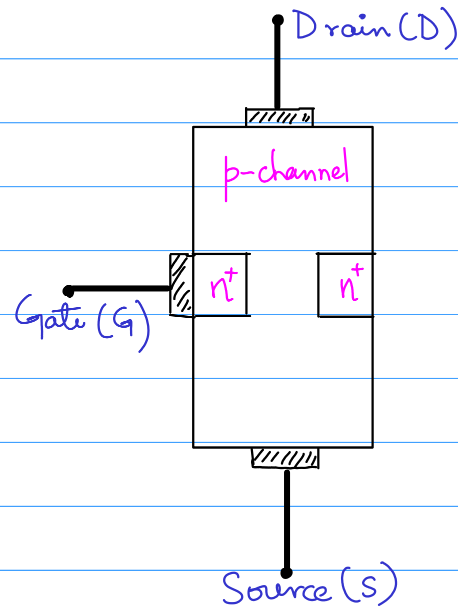
1. Junction Field effect transistor (JFETs) or simply FETs

2. Metal-Oxide Semiconductor field effect transistors (MOSFETs)

JFETs :



n-channel JFET



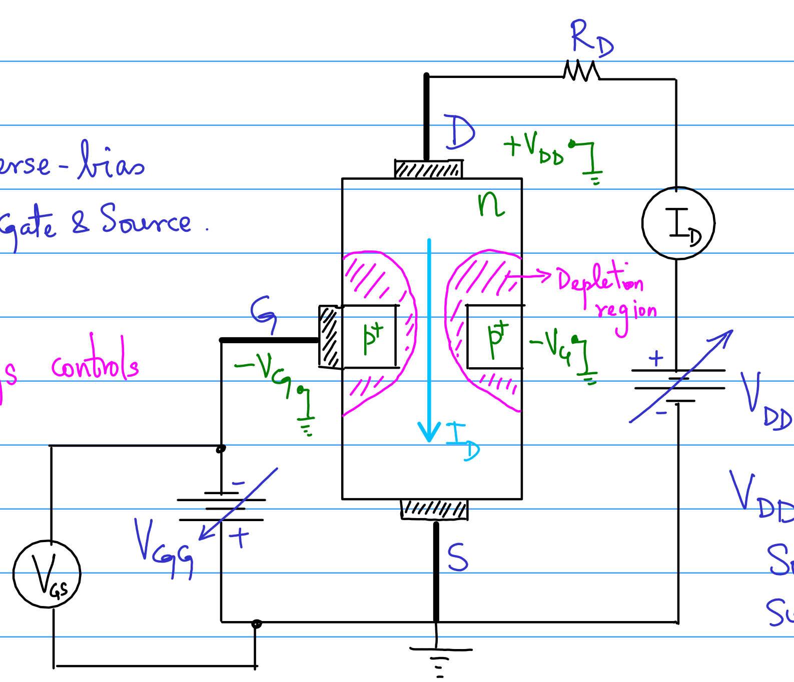
p-channel JFET

Both gates are internally 'SHORT'

Basic Operation :

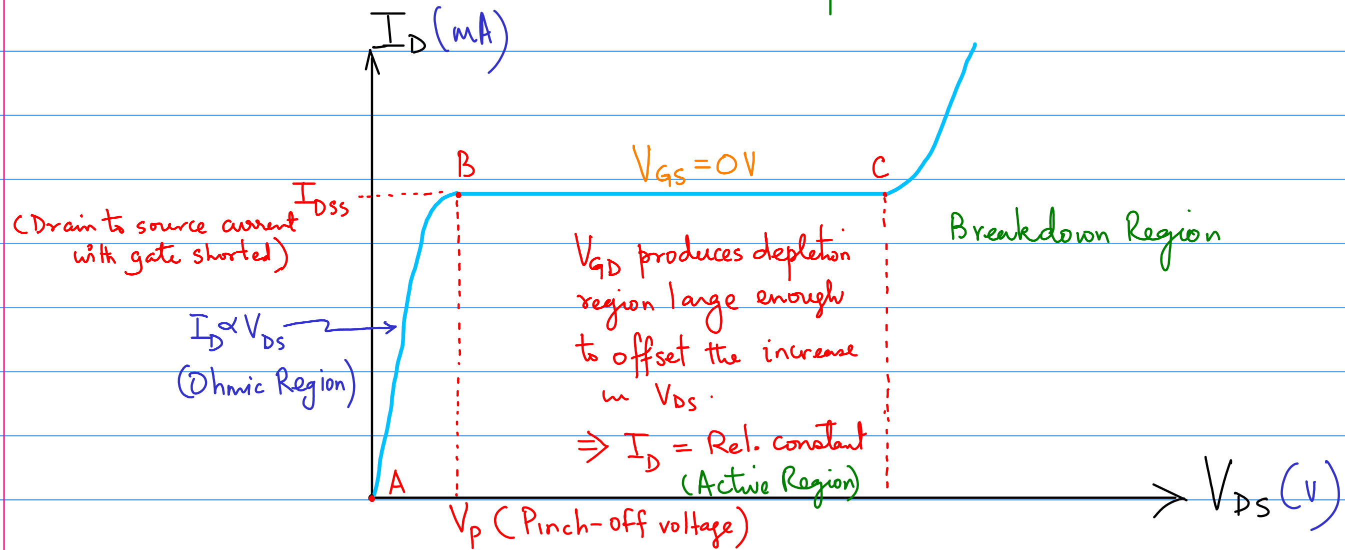
V_{GG} = Sets reverse-bias between Gate & Source.

Effectively V_{GS} controls channel width (or, resistance to I_D)

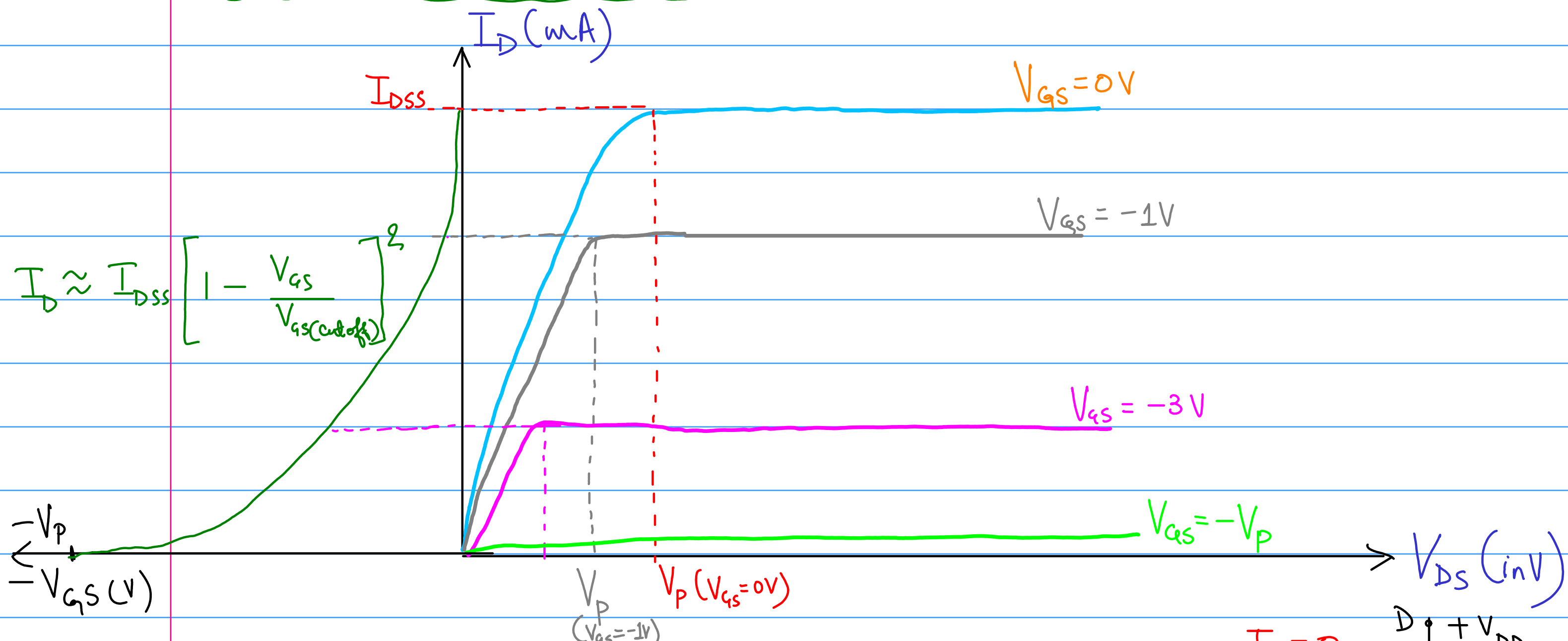


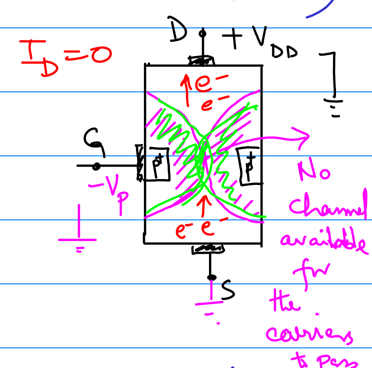
V_{DD} provides Drain to Source voltage and supplies I_D.

JFET characteristics and parameters:



Full-Characteristics Curves:





$$\boxed{V_{GS(cut\text{-}off)} = -V_p \qquad \text{where } I_D = 0}$$

A JFET transfer characteristic curve is expressed approximately as:

$$\boxed{I_D \approx I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(cut\text{-}off)}}\right)^2}$$

Input Resistance and Capacitance:

- We have seen that JFETs operates with its Gate–Source junction in reverse biased.

$\Rightarrow$ High input resistance: Advantage of JFETs over BJTs.

here $R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right|$

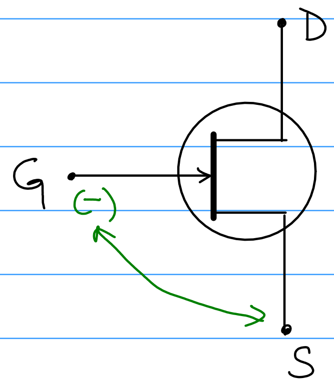
Also, the input capacitance C_{iss} is a result of JFET operating in reverse-bias pn junction. Typically, $C_{iss} =$ pF.

AC Drain to Source Resistance:

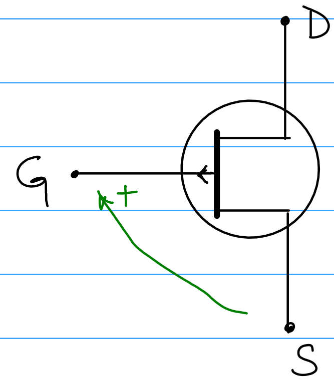
$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

Circuit Symbols:

Gate–Source is in Reverse bias



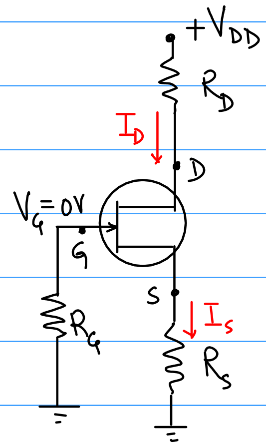
n-channel JFETs



p-channel JFETs

Biasing of JFET :

(a) Self - Biasing



$I_S = I_D$

$$V_{GS} = V_G - V_S = 0V - I_D R_S = -I_D R_S$$

$$\Rightarrow \boxed{V_{GS} = -I_D R_S}$$

Also, $V_D = V_{DD} - I_D R_D$

Hence, $V_{DS} = V_D - V_S = V_{DD} - I_D R_D - I_D R_S = V_{DD} - I_D(R_D + R_S)$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

$$\Rightarrow I_D = \frac{V_{DD}}{R_D + R_S} - \frac{V_{DS}}{R_S + R_D}$$

$$\Rightarrow I_D = \left(\frac{-1}{R_S + R_D}\right) \cdot V_{DS} + \frac{V_{DD}}{R_S + R_D}$$

$$\Rightarrow Y = MX + C$$

Voltage-Divider Bias Ckt: