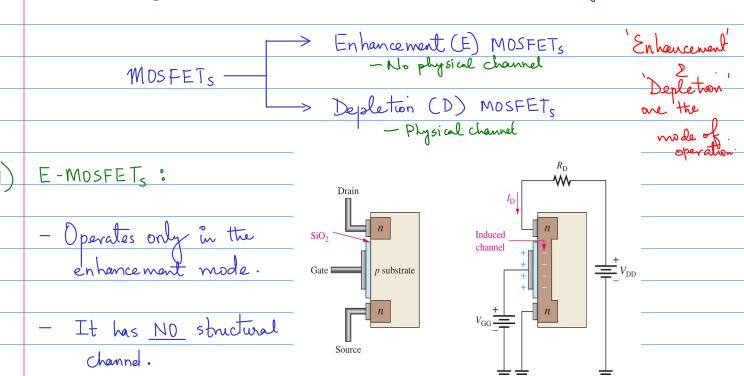
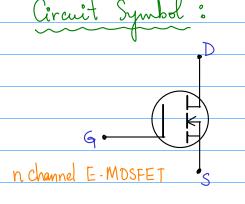
The MOSFETs

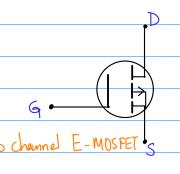
- No p-n junction in the device structure.
- The gate (G) is insulated from the channel by a Silicondioxide



- The substrate extends completely to the SiOz layer.
- When Vgs > Vgs(Threshold), a channel is induced by creating a then layer of negative changes in the substrate region adjacent to SiO2 layer.

(a) Basic construction





(b) Induced channel $(V_{GS} > V_{GS(th)})$

Broken lines

Symbolize absonce

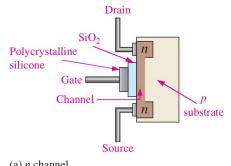
of physical

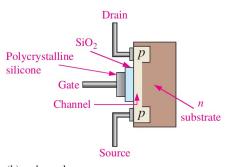
channel in

E-MOSFETs.

D-MOSFET:

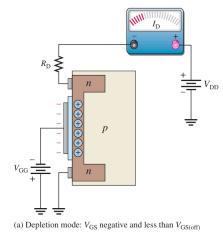
- Physical Channel is present.
- Can be operated in either depletion or enhancement mode.

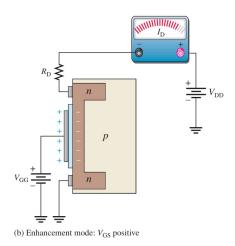




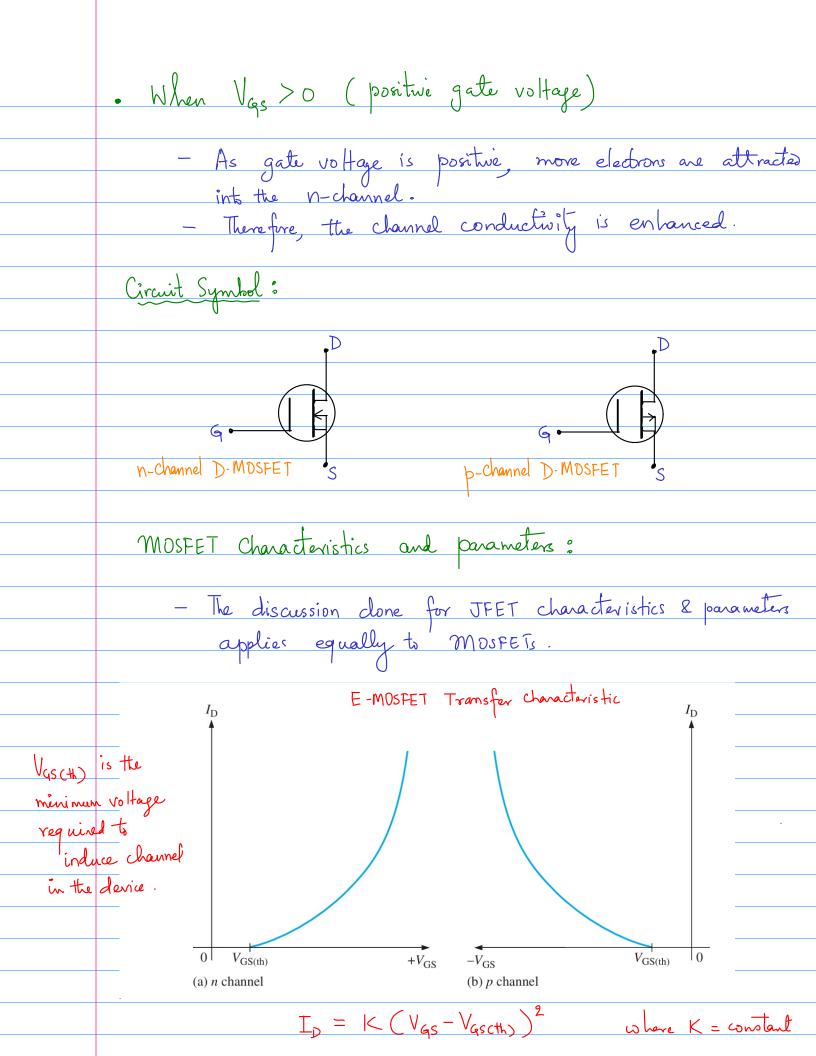
(a) n channel

- (b) p channel
- VGS = negative (Depletion mode of speration) Vgs = positive (Enhancement mode of operation
- · Visualize the gate as one plate of a parallel-plate copacitor and channel as the other plate. The SiOz is an insulating layer.

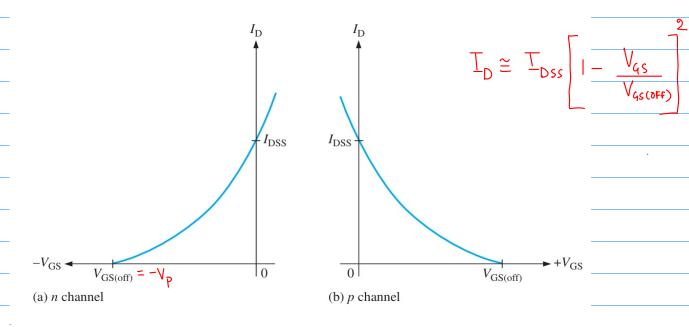




- When Vgs < 0 (Negative gate-voltage)
 - the electrons in n-channel are repelled leaving tre ions
 - as a consequence the n-channel is depleted with mobile charge carriers.
 - therefore, the channel conductivity decreases.
 - At sufficient negative gate 5 source voltage (Vascor) the channel is completely depleted with mobile change carriers. > In=0
 - Similar to n-channel JFET, the n-channel D-MOSFET LD Grand Vas



D-MOSFET Transfer Characteristic



MOSFET Biasing:

(a) Voltage-Divider Bias:

