Indian Institute of Information Technology Vadodara (Gandhinagar Campus)

End Semester Examination | Semester-I | Autumn 2021-22

Course: EC100 Basic Electronic Circuits

Full Marks: 80 **Date: 07/04/2022** **Time: 11:35 AM-1:15 PM**

Instructions:

1. Attempt part **(a)** OR **(b)** of **Q2** and **Q7**. All other questions are compulsory.
2. Only scientific calculators are allowed to be used.
3. Each question carries ten marks.

Q1. For the given input waveform to the diode circuit shown in Fig. 1, draw the output waveform.

Q2. **(a)** The energy level diagrams of the isolated *p*-type and *n*-type doped silicon are shown in Fig. 2(a) and 2(b), respectively. ***(i)*** Draw the equilibrium energy-level diagram when they are physically joined. ***(ii)*** Show the directions of diffusion and drift currents. ***(iii)*** Calculate the value of built-in potential.

OR

(b) Find the value of V_{out} in the circuit shown in Fig. 9. Assume the given Op-Amps are ideal, *i.e.*, $A_{OL} = \infty$.

Q3. Calculate the value of dc current gain β_{DC} of the given bipolar junction transistor in Fig. 3.

Q4. Sketch an ideal family of output characteristics for the circuit shown in Fig. 4. The characteristics should be sketched for the base current $I_B = 5\mu A$ to $25\mu A$ with the increments of $5\mu A$. Assume $\beta_{DC} = 100$ and that collector-emitter voltage V_{CE} does not exceed the breakdown region. Label the saturation and active regions of operation. Draw the dc load line for $V_{CE(cut\,off)} = 30V$ and collector resistance $R_C = 4.7k\Omega$. Indicate the operation point for each of the curves in the family.

Q5. Determine how much the operating point (Q-point) for the circuit in Fig. 5 will change over a temperature range where β_{DC} increase from 100 to 200. [Assume base-emitter voltage $|V_{BE}| = 0.7V$]

Q6. For the given voltage amplifier circuit in Fig. 6, (*i*) draw the dc equivalent circuit and determine ac-emitter resistance r'_e, (*ii*) draw the ac equivalent circuit using a π-model of transistor and determine the voltage gain A_V, (*iii*) determine the minimum value for the emitter by-pass capacitor for the amplifier to operate over a frequency range of 200 Hz to 10 kHz.

Q7. **(a)** Determine the critical frequencies associated with the low-frequency response of the BJT amplifier in Fig. 7. What is the dominant critical frequency? Show it on the A_V (dB) versus *f* curve.

OR

(b) ***(i)*** Explain Pinch-off in an *n*-channel JFET with proper diagram. Why does the drain current (I_D) become almost constant at Pinch-off ? What is the impact on the depletion layer if we increase V_{DS} after pinch-off for a specific value of V_{GS}? ***(ii)*** The device parameters for *n*-channel JFET are: Maximum drain current I_{DSS} = 15 mA; Pinch-off voltage $|V_p| = |V_{GS(off)}| = 4$V . Calculate the I_D for V_{GS} = 0 V, −2 V and −4 V.

Q8. For the given input waveform to the operational amplifier shown in Fig.8, draw the output waveform.

Please turn-over for the figures.

Fig. 1

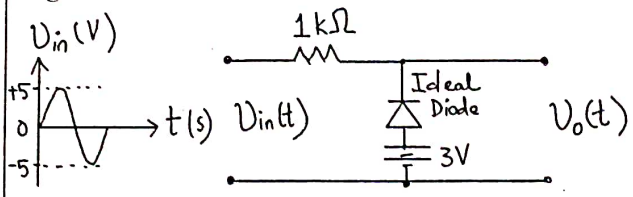

Fig. 2(a)

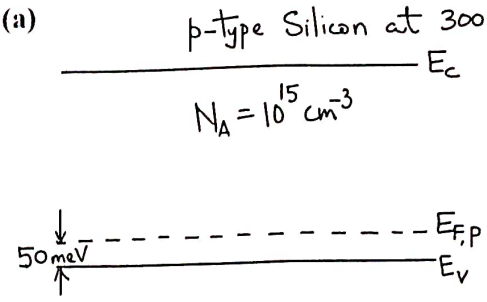

Fig. 2(b)

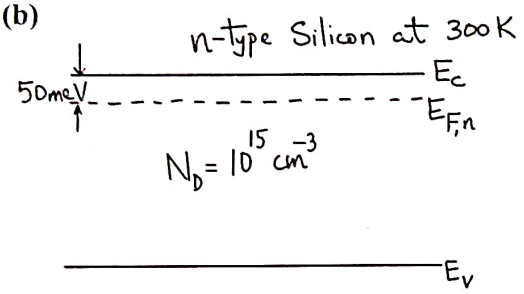

Fig. 3

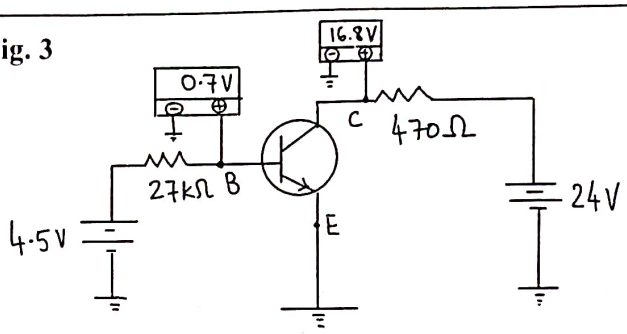

Fig. 4

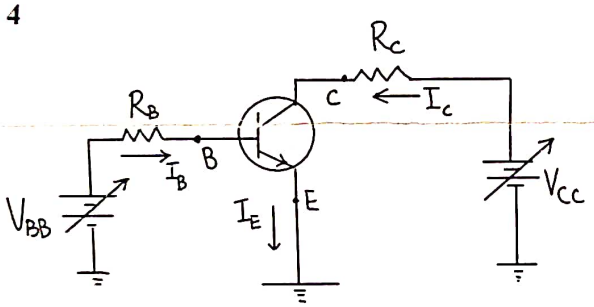

Fig. 5

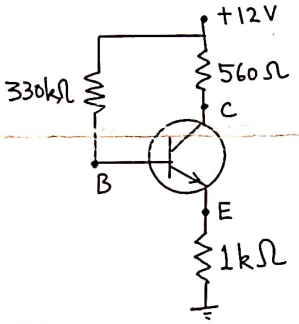

Fig. 6

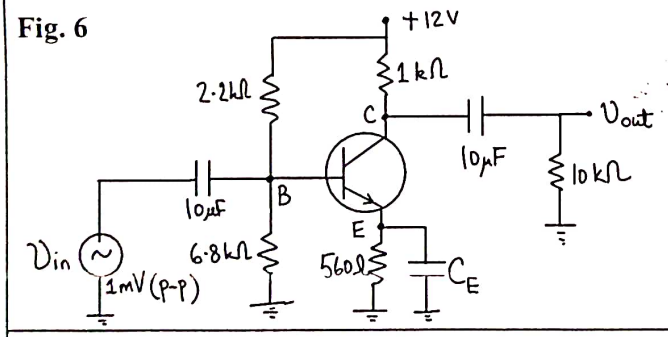

Fig. 7

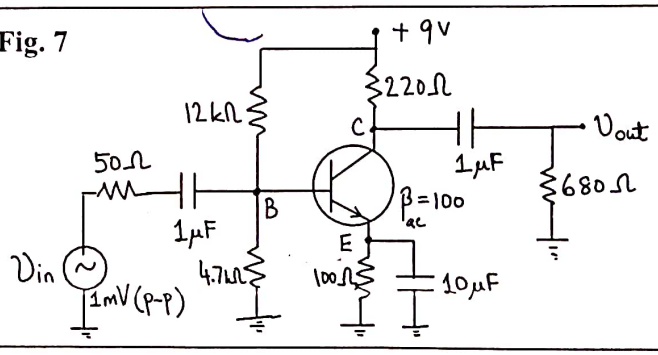

Fig. 8

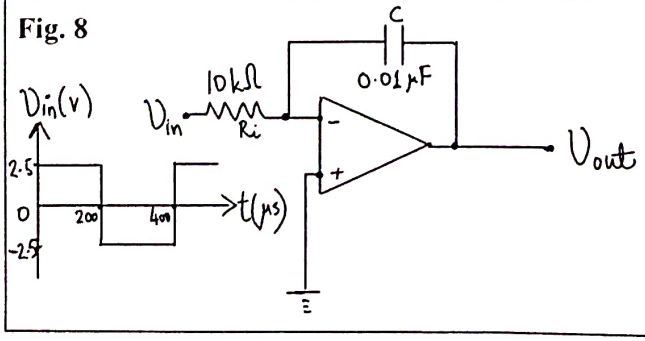

Fig. 9