MPM3610A

21V/1.2A DC/DC Module Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3610A is a synchronous rectified, step-down module converter with built-in power MOSFETs, inductor, and two capacitors. It offers a very compact solution, requires only 5 external components to achieve a 1.2A continuous output current with excellent load and line regulation over a wide input supply range and provides fast load transient response.

Full protection features include over-current protection and thermal shut-down.

MPM3610A eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3610A is available in a space-saving QFN20 (3mmx5mmx1.6mm) package.

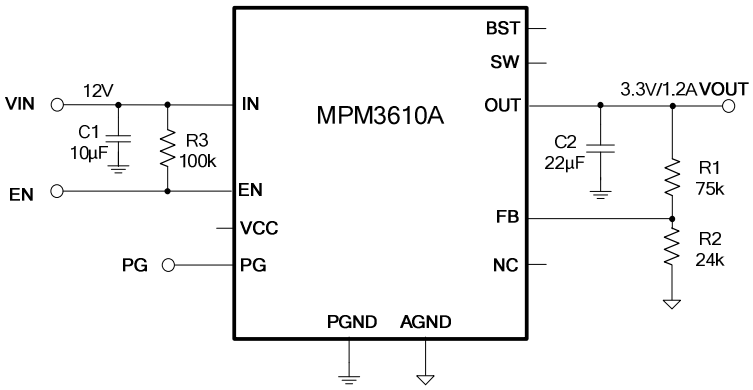
FEATURES

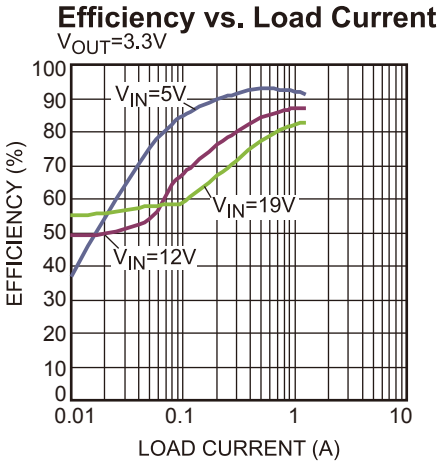
- 4.5V-to-21V Operating Input Range
- 1.2A Continuous Load Current
- 90mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Integrated Inductor
- Integrated VCC and Bootstrap Capacitors
- Power Save Mode at Light Load
- Power Good Indicator
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in QFN20 (3x5x1.6mm) Package
- Total solution size 6.7mm x7.3mm

APPLICATIONS

- Industrial Controls
- Medical and Imaging Equipment
- Telecom and Networking Applications
- LDO Replacement
- Space and Resource-limited Applications

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3610AGQV	QFN-20 (3mmx5mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPM3610AGQV–Z);

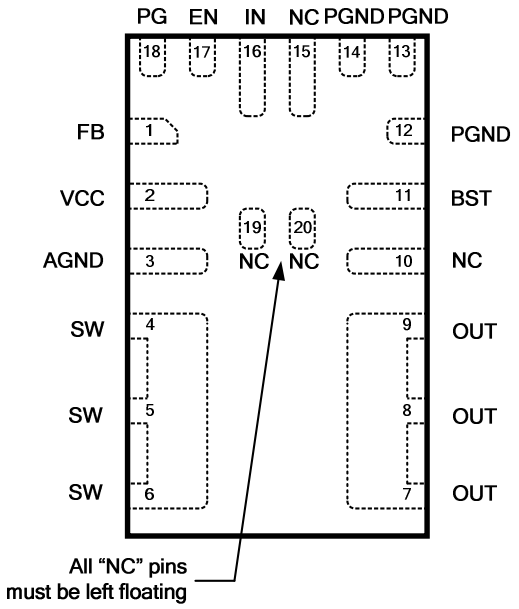
TOP MARKING

MPYW
3610
ALLL
M

MP: MPS prefix:
Y: year code;
W: week code:
3610A: first five digits of the part number;
LLL: lot number;
M: module;

PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 28V
V_{SW} .....
-0.3V (-5V for <10ns) to 28V (30V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins..... -0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....2.7W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 21V
Output Voltage V_{OUT}.....0.8V to V_{IN}*D_{MAX}(5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-20 (3mmx5mmx1.6mm)	46	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to page 14, Enable control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) In practical design, the minimum V_{OUT} is limited by minimum on time, 50ns on time is commonly recommended for calculating to give some margin. For output voltage setting above 5.5V, please refer to the application information on page 17.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Vin=12V, T_J=-40°C to +125°C[7], typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_s	V_{EN} = 0V, T_J =+25°C		6.5	8	μA
		V_{EN} = 0V, T_J =-40°C to +125°C		6.5	9	μA
Supply Current (Quiescent)	I_q	V_{FB} = 1V, T_J =+25°C		0.3	0.39	mA
		V_{FB} = 1V, T_J =-40°C to +125°C		0.3	0.44	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		90		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		40		mΩ
Inductor DC Resistance	L_{DCR}			60		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit	I_{LIMIT}	Under 40% Duty Cycle	2.3	3		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V, T_J =+25°C	1600	2000	2400	kHz
		V_{FB}=0.75V, T_J =-40°C to +125°C	1500	2000	2500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}=200mV		0.3		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV, T_J =+25°C	78	83	88	%
		V_{FB}=700mV, T_J =-40°C to +125°C	77	83	89	%
Minimum On Time[8]	T_{ON_MIN}			30		ns
Feedback Voltage	V_{FB}	T_J =25°C	786	798	810	mV
		T_J =-40°C to +125°C	782	798	814	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}	T_J =+25°C	1.2	1.4	1.6	V
		T_J =-40°C to +125°C	1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN\_FALLING}$	T_J =+25°C	1.05	1.25	1.4	V
		T_J =-40°C to +125°C	1	1.25	1.45	V
EN Input Current	I_{EN}	V_{EN}=2V, T_J =+25°C	2	2.3	2.6	μA
		V_{EN}=2V, T_J =-40°C to +125°C	1.8	2.3	2.8	μA
Power Good Rising Threshold	PG_{VTH-Hi}	T_J =+25°C	0.86	0.9	0.95	V_{FB}
Power Good Falling Threshold	PG_{VTH-LO}	T_J =+25°C	0.78	0.83	0.88	V_{FB}
Power Good Rising Delay	PG_{TD_RSING}	T_J =+25°C	15	35	55	μs
		T_J =-40°C to +125°C	10	35	60	μs
Power Good Falling Delay	$PG_{TD\_FALLING}$	T_J =+25°C	40	80	125	μs
		T_J =-40°C to +125°C	30	80	135	μs
Power Good Sink Current Capability	V_{PG}	Sink 1mA			0.4	V
Power Good Leakage Current	$I_{PG-LEAK}$	V_{PG}=6V			1	μA

ELECTRICAL CHARACTERISTICS*(continued)*

Vin=12V, T_J=-40°C to +125°C, typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$	T_J =+25°C	3.7	3.9	4.1	V
		T_J =-40°C to +125°C	3.65	3.9	4.15	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$		600	675	750	mV
VCC Regulator	V_{CC}	T_J =+25°C	4.75	4.9	5.05	V
		T_J =-40°C to +125°C	4.7	4.9	5.1	V
VCC Load Regulation		I_{CC}=5mA		1.5	3	%
Soft-Start Time	t_{SS}	V_{OUT} from 10% to 90%, T_J =+25°C	0.8	1.6	2.4	ms
		V_{OUT} from 10% to 90%, T_J =-40°C to +125°C	0.6	1.6	2.6	ms
Thermal Shutdown (8)	T_{SD}			150		°C
Thermal Hysteresis (8)	T_{SD_HYS}			20		°C

Notes:

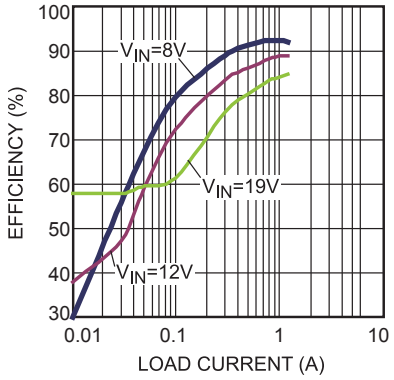
7) Not tested in production. Guaranteed by over-temperature correlation.

8) Guaranteed by Characterization.

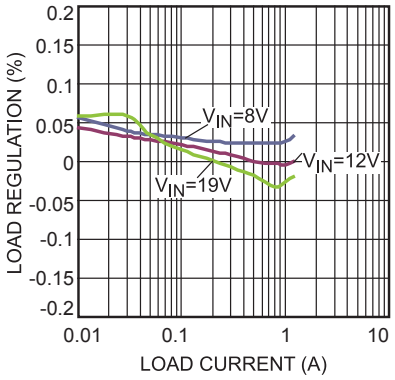
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

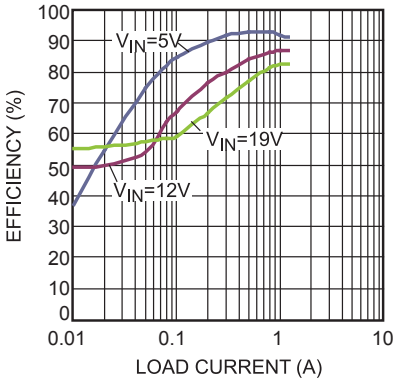
Efficiency vs. Load Current
V_{OUT}=5V



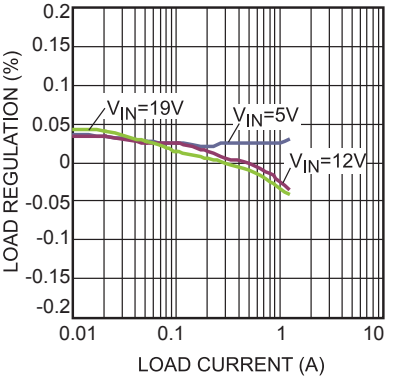
Load Regulation
V_{OUT}=5V



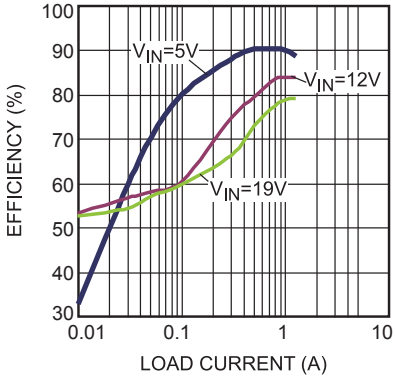
Efficiency vs. Load Current
V_{OUT}=3.3V



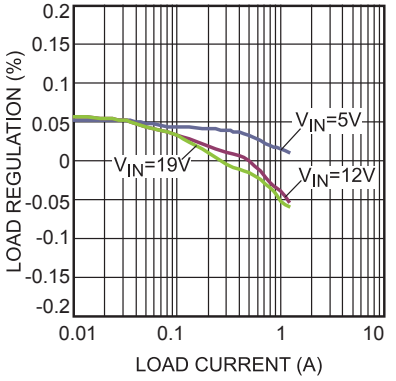
Load Regulation
V_{OUT}=3.3V



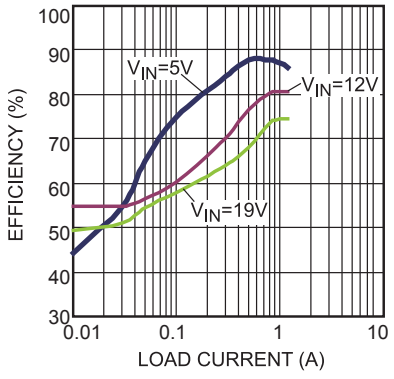
Efficiency vs. Load Current
V_{OUT}=2.5V



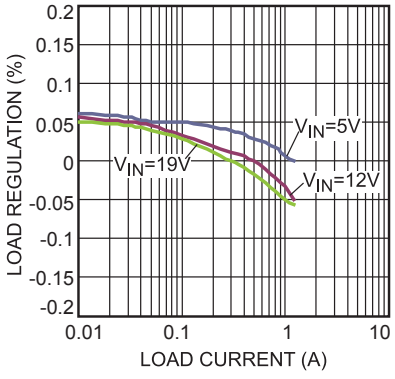
Load Regulation
V_{OUT}=2.5V



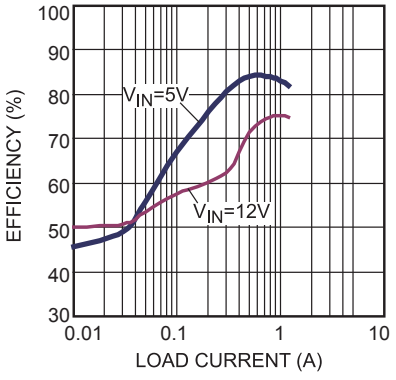
Efficiency vs. Load Current
V_{OUT}=1.8V



Load Regulation
V_{OUT}=1.8V



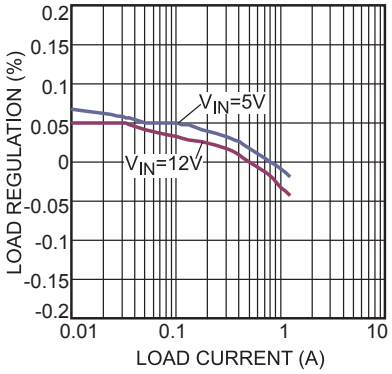
Efficiency vs. Load Current
V_{OUT}=1.2V



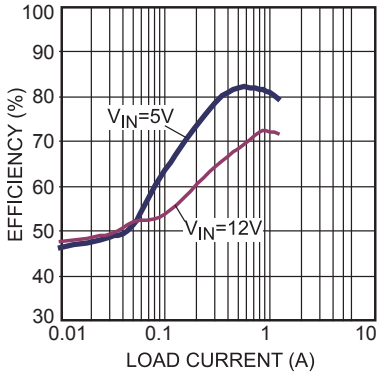
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

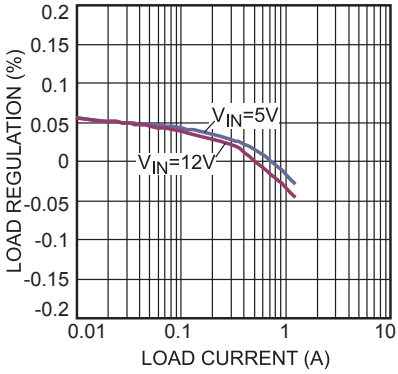
Load Regulation
V_{OUT}=1.2V



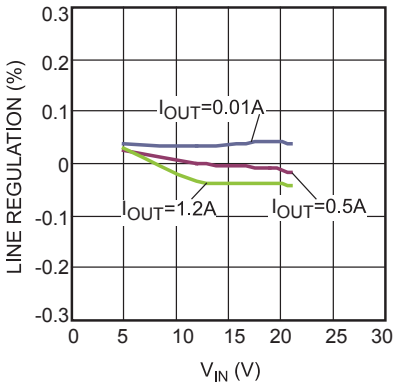
Efficiency vs. Load Current
V_{OUT}=1V



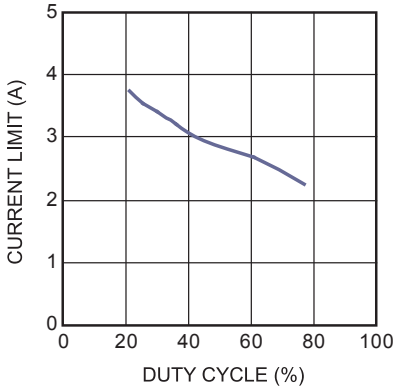
Load Regulation
V_{OUT}=1V



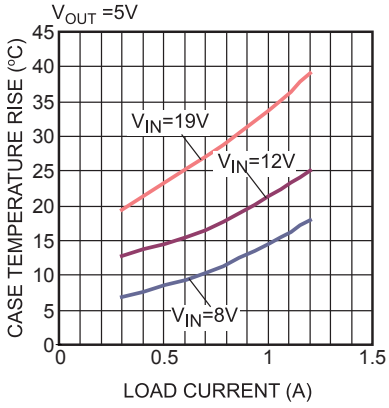
Line Regulation
V_{IN}=5V to 21V, V_{OUT}=3.3V



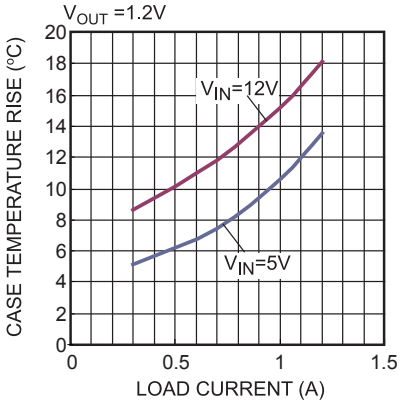
Inductor Peak Current Limit vs. Duty Cycle



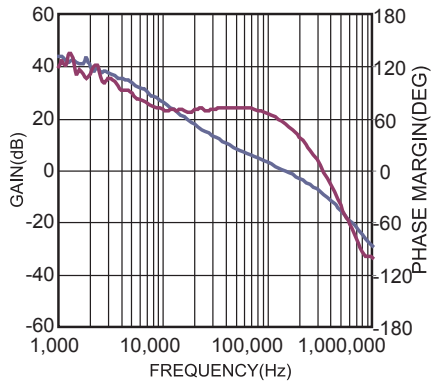
Case Temperature Rise vs. Load Current
V_{OUT} =5V



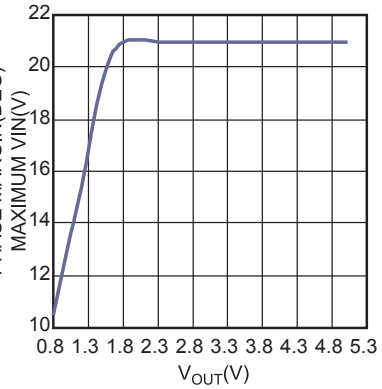
Case Temperature Rise vs. Load Current
V_{OUT} =1.2V



Bode Plot
I_{OUT} =1.2A



Maximum VIN vs. VOUT

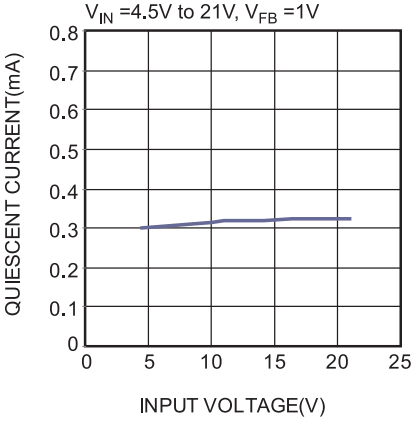


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

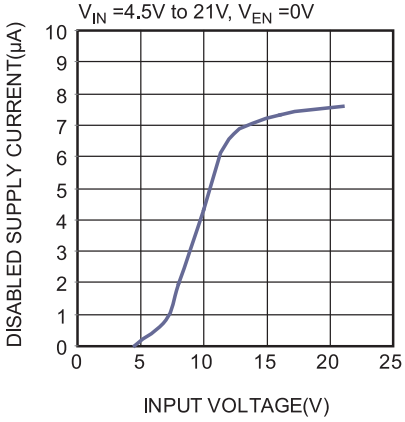
Quiescent Current vs. Input Voltage

V_{IN} =4.5V to 21V, V_{FB} =1V



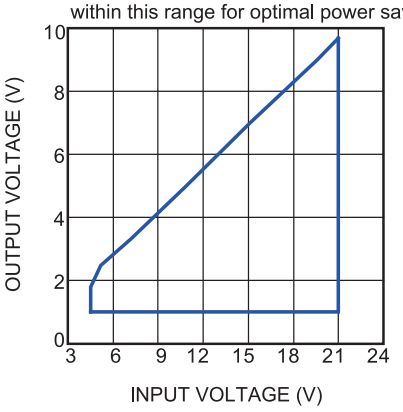
Disabled Supply Current vs. Input Voltage

V_{IN} =4.5V to 21V, V_{EN} =0V



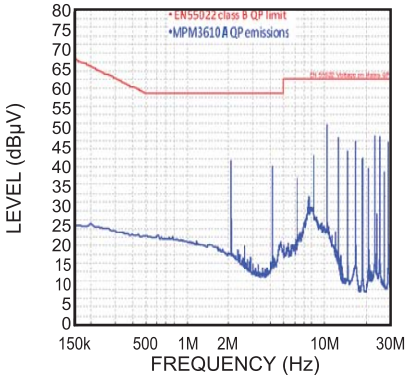
Power Save Mode Range

Recommend operating the device within this range for optimal power save mode



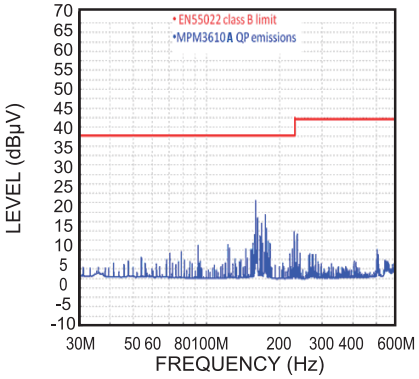
Conduction-EMI

I_{OUT}=1A



Radiated-EMI

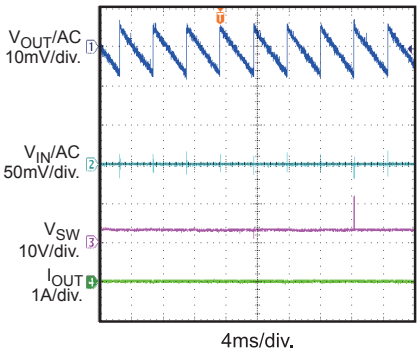
I_{OUT}=1A



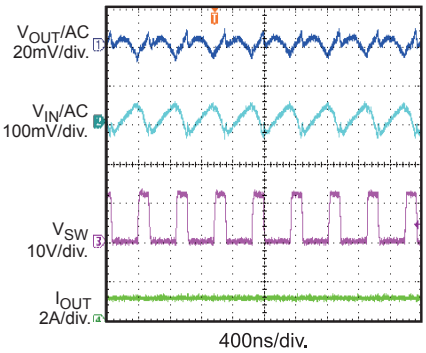
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

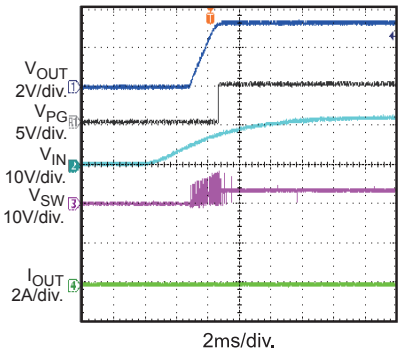
Input/Output Ripple
I_{OUT} = 0A



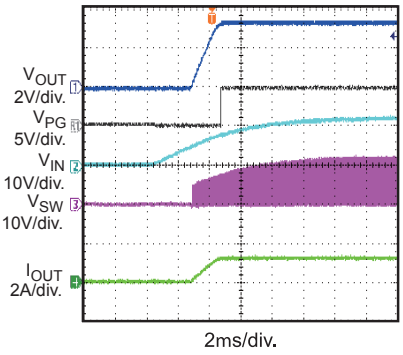
Input/Output Ripple
I_{OUT} = 1.2A



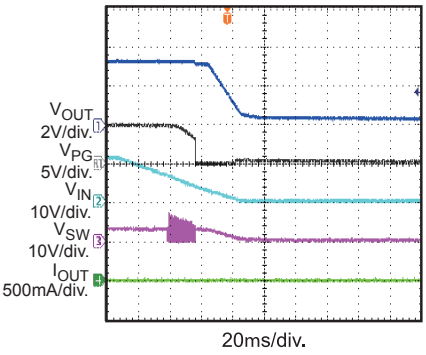
Startup through Input Voltage
I_{OUT} = 0A



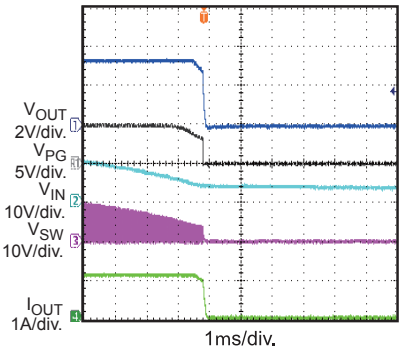
Startup through Input Voltage
I_{OUT} = 1.2A



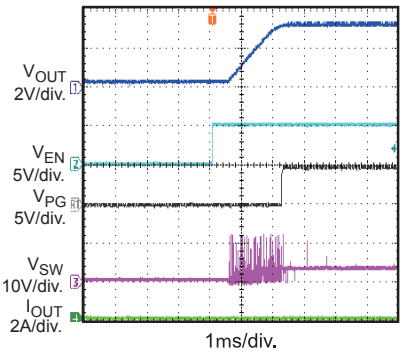
Shutdown through Input Voltage
I_{OUT} = 0A



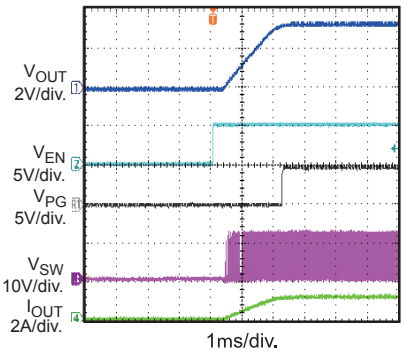
Shutdown through Input Voltage
I_{OUT} = 1.2A



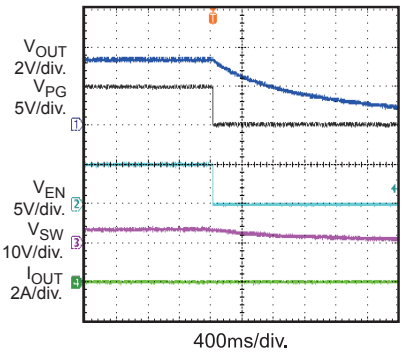
Startup through Enable
I_{OUT} = 0A



Startup through Enable
I_{OUT} = 1.2A



Shutdown through Enable
I_{OUT} = 0A

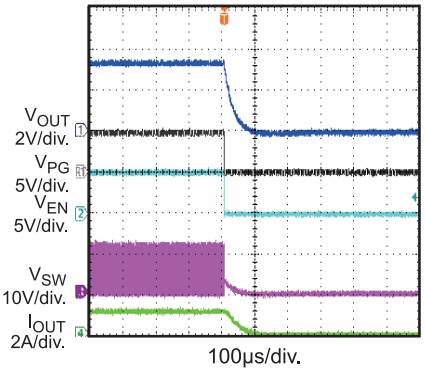


TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

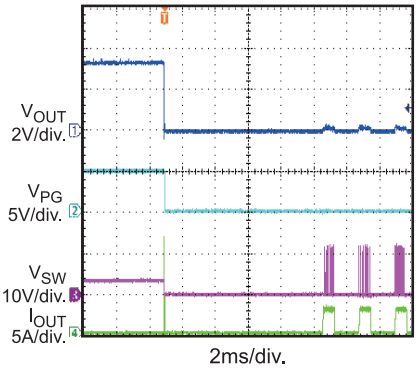
Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Shutdown through Enable

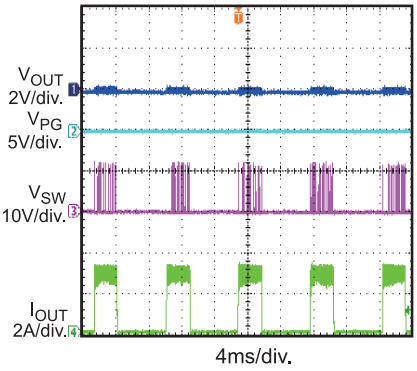
I_{OUT} = 1.2A



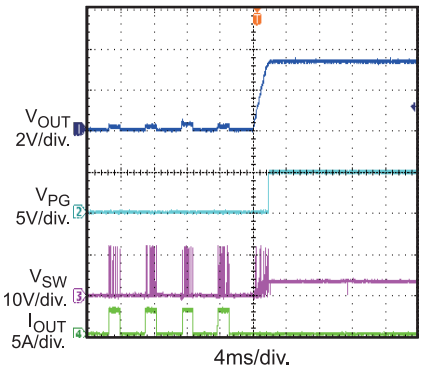
Short Circuit Entry



Short Circuit Steady State

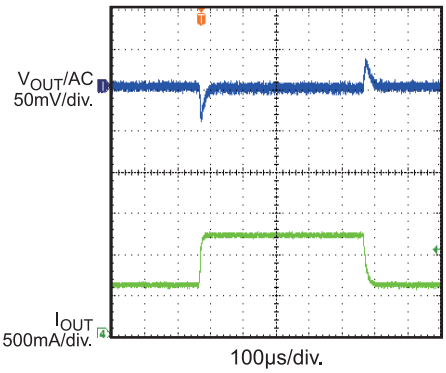


Short Circuit Recovery



Load Transient Response

0.6A to 1.2A



PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	Feedback. Connect to the tap of an external resistor divider from the output to AGND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short circuit fault. Place the resistor divider as close to the FB pin as possible. Avoid placing vias on the FB traces.
2	VCC	Internal 5V LDO output. Internal circuit integrates LDO output capacitor, so there is no need to add external capacitor.
3	AGND	Analog Ground. Reference ground of logic circuit. AGND is internally connected to PGND. There is no need to add external connections to PGND.
4, 5, 6	SW	Switch Output. Large copper plane is recommended on pin 4, 5 and 6 for better heat sink.
7, 8, 9	OUT	Power Output. Connect the load to this pin. Output capacitor is needed.
10, 15, 19, 20	NC	DO NOT CONNECT. Pin must be left floating.
11	BST	Bootstrap. Bootstrap capacitor is integrated internally. External connection is not needed.
12, 13, 14	PGND	Power Ground. Reference ground of the power device. PCB layout requires extra care. For best results, connect to PGND with copper and vias.
16	IN	Supply Voltage. The IN pin supplies power to internal MOSFET and regulator. The MPM3610A operates from a +4.5V to +21V input rail. Requires a low-ESR, and low-inductance capacitor to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
17	EN	Pull the EN pin high to enable the module. Leave it floating or connecting it to GND will disable the module.
18	PG	Power Good Indicator. The PG pin is an open-drain output. Connect PG pin to VCC or other voltage source through a pull up resistor (e.g. 100kΩ). The detail PG behavior is on Power Good Indicator Section in OPERATION.

FUNCTIONAL BLOCK DIAGRAM

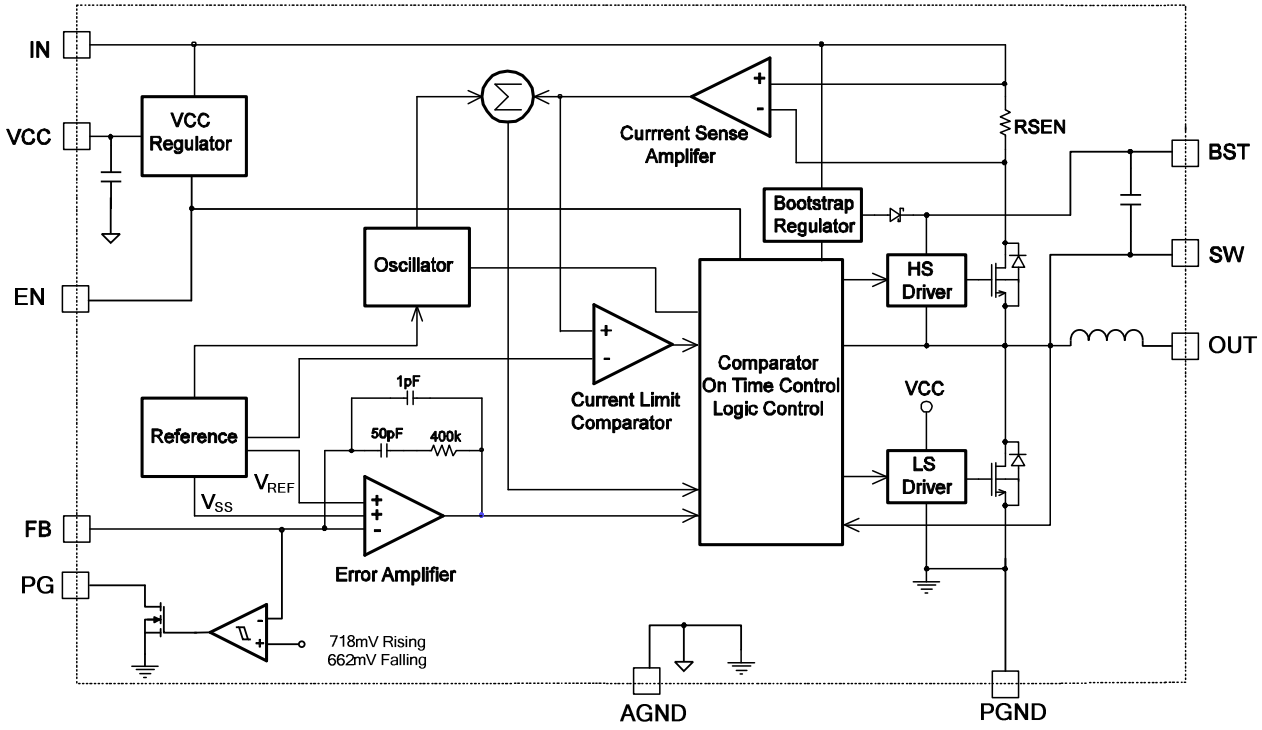


Figure 1: Functional Block Diagram

OPERATION

The MPM3610A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, integrated inductor and two capacitors. It offers a very compact solution that achieves a 1.2A continuous output current with excellent load and line regulation over 4.5V to 21V input supply range.

The MPM3610A has three working modes: AAM (Advanced Asynchronous Modulation, similar as PFM) mode, DCM (Discontinues-Conduction Mode) and CCM (Continues-Conduction Mode). The device will operate from AAM mode, DCM to CCM with the load current increasing. In some particular condition the device will not enter AAM mode in light load condition, refer to "Power Save Mode Range" curve on page 8.

AAM Control Operation

In the light load condition, MPM3610A works in AAM mode. Refer to Figure 2, the V_{AAM} is an internal fixed voltage when input and output voltages are fixed. V_{COMP} is the error amplifier output which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked, thus the MPM3610A skips some pulses and achieves the light load power save. Refer to AN032 for more detail.

The internal clock resets every time when V_{COMP} is higher than V_{AAM}. At the same time the HS-FET(High-Side MOSFET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light load feature in this device is optimized for 12V input applications.

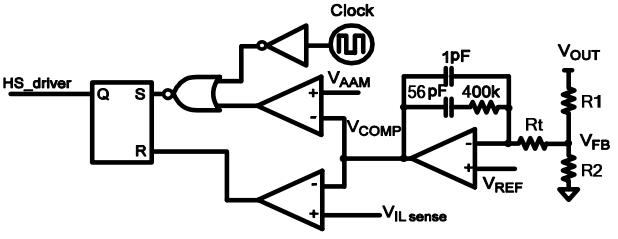


Figure 2: Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} voltage ramps up with the increasing of the output current, when its minimum value exceeds V_{AAM}, the device will enter DCM. In this mode the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}, after a period of dead time, the LS-FET (Low-Side MOSFET) will turn on and remain on until the inductor current value decreases to zero. The device will repeat the same operation in every clock cycle to regulate the output voltage.

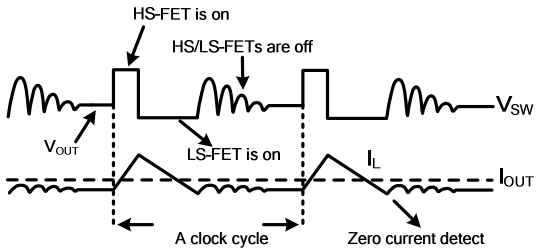


Figure 3: DCM Control Operation

CCM Control Operation

The device will enter CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}, after a period of dead time, the LS-FET will turn on and remain on until the next clock cycle starts. The device will repeat the same operation in every clock cycle to regulate the output voltage.

If within 83% of one PWM period, $V_{ILsense}$ does not reach the value set by V_{COMP}, the HS power MOSFET is forced off.

Internal V_{CC} Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. When V_{IN} is less than 4.9V, the output decreases, and the part integrates internal decoupling capacitor. No need add external VCC output capacitor.

Error Amplifier

The error amplifier compares the FB pin voltage to the internal 0.798V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The MPM3610A UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.9V while its falling threshold is 3.225V.

Enable Control

EN is a control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 870kΩ resistor from EN to GND allows EN to be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 4. Connecting the EN input pin through a pull up resistor to the voltage on the V_{IN} pin limits the EN input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 6.5V) \div 100\mu A = 55k\Omega$.

Connecting the EN pin directly to a voltage source without any pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

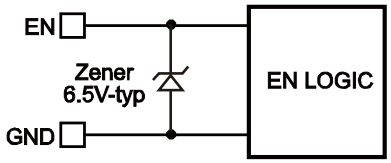


Figure 4: 6.5V Zener Diode Connection

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.6ms(V_{OUT} from 10% to 90%).

Pre-Bias Startup

The MPM3610A has been designed for monotonic startup into pre-biased output voltage. If the output is pre-biased to a certain voltage during startup, the voltage on the soft-start capacitor will be charged. When the soft-Start capacitor's voltage exceeds the sensed output voltage at the FB pin, the part starts to turn on high side and low side power switches sequentially. Output voltage starts to ramp up following with soft-start slew rate.

Power Good Indicator

The MPM3610A has power good (PG) output used to indicate whether the output voltage of the module is ready or not. The PG pin is an open drain output. Connect PG pin to VCC or other voltage source through a pull up resistor (e.g. 100kΩ). When the input voltage is applied, the PG pin is pulled down to GND before internal V_{SS}>1V. After V_{SS}>1V, when V_{FB} is above 90% of V_{REF}, the PG pin will be pulled high after 35μs delay time. During normal operation, the PG pin will be pulled low when the V_{FB} drops below 83% of V_{REF} after 80μs delay.

When UVLO or OTP happens, the PG pin will be pulled low immediately; When OC(Over current) happens, the PG pin will be pulled low when V_{FB} drops below 83% of V_{REF} after 80μs delay.

Since MPM3610A doesn't implement dedicate output over voltage protection, the PG won't response to output over voltage condition.

Over-Current-Protection and Hiccup

The MPM3610A has a cycle-by-cycle over-current limiting control. When the inductor current peak value exceeds internal "peak" current limit threshold, the HS-FET will turn off and the LS-FET will turn on and remains on until the inductor current falls below the internal "valley" current limit threshold. The "valley" current limit circuit is employed to decrease the

operation frequency after the "peak" current limit threshold is triggered. Meanwhile, the output voltage drops until V_{FB} is below the Under-Voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MPM3610A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and greatly reduces the average short circuit current to alleviate thermal issues and protect the converter. The MPM3610A exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon's temperature exceeds 150°C, the whole chip is shut down. When the temperature drops below its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (Figure 5). If (V_{BST}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V voltage across C4.

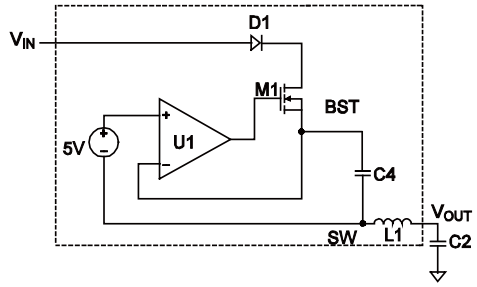


Figure 5: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and V_{EN} exceeds its thresholds, the chip starts. The reference block starts first, generating stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} low, V_{EN} low and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Additional RC Snubber Circuit

Additional RC snubber circuit can be chosen to damp the device's spike and ringing voltage to get better EMI performance.

The power dissipation of the RC snubber circuit can be simply estimated by the formula below:

$$P_{Loss} = f_S \times C_S \times V_{IN}^2$$

Where f_S is the switching frequency; C_s is the snubber capacitor; V_{IN} is the input voltage.

For efficiency consideration, the value of C_S should not be set too large. Commonly a 5.6Ω R_S and a 330pF C_S is recommended to generate the RC snubber circuit.

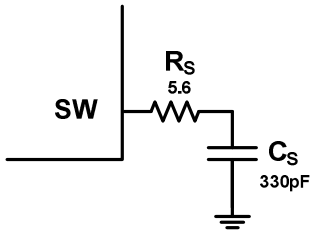


Figure 6: Additional RC Snubber Circuit

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). Choose R1 refer to Table 1, R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.798V} - 1}$$

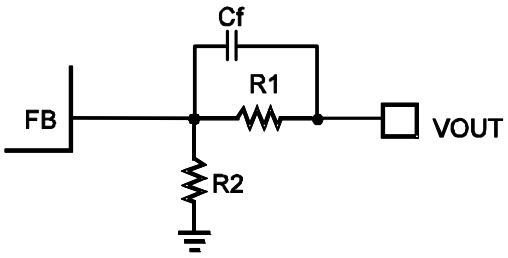


Figure 7: Feedback Network

Table 1 lists the recommended feedback network parameters for common output voltages.

Table 1: Recommended Parameters For Common Output Voltages

		Small Solution Size(C_{IN}=10µF/0805/25V, C_{OUT}=22µF/0805/16V)					Low V_{OUT} Ripple(C_{IN}=10µF/0805/25V, C_{OUT}=2X22µF/0805/16V)				
V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV)(9)	Load Transient (mV)(10)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV) (9)	Load Transient (mV) (10)
21	5	115	22	NS	17.6	119	40.2	7.68	NS	9.4	74
	3.3	102	32.4	NS	12.4	73	62	19.6	NS	7	50
	2.5	102	47.5	5.6	10	48	62	29.4	5.6	5.2	31
19	5	115	22	NS	16.4	116	40.2	7.68	NS	8.8	72
	3.3	102	32.4	NS	11.4	73	62	19.6	NS	6.6	51
	2.5	102	47.5	5.6	9.8	51	62	29.4	5.6	5	33
16	5	115	22	NS	15.6	116	40.2	7.68	NS	7.8	69
	3.3	102	32.4	NS	10.6	72	62	19.6	NS	6	53
	2.5	102	47.5	5.6	9.6	52	62	29.4	5.6	4.8	36
	1.8	102	82	5.6	8.6	41	62	49.9	5.6	4	30
14	5	115	22	NS	14.8	110	40.2	7.68	NS	7.4	65
	3.3	102	32.4	NS	10.2	72	40.2	12.7	NS	5.6	41
	2.5	75	34.8	5.6	9.4	46	40.2	18.7	5.6	4.6	34
	1.8	102	82	5.6	8.4	42	62	49.9	5.6	4.2	31
	1.5	158	180	5.6	7.2	44	62	69.8	5.6	3.6	30
12	5	100	19.1	NS	13.8	93	34	6.49	NS	6.4	56
	3.3	75	24	NS	9.4	61	40.2	12.7	NS	5.2	40
	2.5	75	34.8	5.6	9	51	40.2	18.7	5.6	4.4	34
	1.8	102	82	5.6	7.8	47	47	37.4	5.6	4	29
	1.5	158	180	5.6	6.6	57	47	53.6	5.6	3.4	27
	1.2	158	316	5.6	6.2	51	75	147	5.6	3	32

Table 1: Recommended Parameters For Common Output Voltages *(continued)*

		Small Solution Size(C_{IN}=10µF/0805/25V, C_{OUT}=22µF/0805/16V)						Low V_{OUT} Ripple(C_{IN}=10µF/0805/25V, C_{OUT}=2X22µF/0805/16V)				
V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV) (9)	Load Transient (mV) (10)		R1 (kΩ)	R2 (kΩ)	C_f (pF)	V_{OUT} Ripple (mV) (9)	Load Transient (mV) (10)
10	5	100	19.1	NS	13.2	77		34	6.49	NS	6.2	47
	3.3	75	24	NS	8.4	58		40.2	12.7	NS	4.8	40
	2.5	75	34.8	5.6	8.2	51		40.2	18.7	5.6	4	34
	1.8	75	59	5.6	7.2	40		47	37.4	5.6	3.6	30
	1.5	102	115	5.6	6	46		47	53.6	5.6	3.2	28
	1.2	102	205	5.6	5.4	45		62	124	5.6	2.8	32
	1	102	402	5.6	4.8	41		82	324	5.6	2.6	36
8	5	100	19.1	NS	9.2	76		34	6.49	NS	5	48
	3.3	75	24	NS	7.6	57		40.2	12.7	NS	3.8	38
	2.5	75	34.8	5.6	7	48		40.2	18.7	5.6	3.4	33
	1.8	75	59	5.6	6.4	42		47	37.4	5.6	3	32
	1.5	75	84.5	5.6	5.4	44		47	53.6	5.6	2.8	29
	1.2	75	147	5.6	5	38		47	93.1	5.6	2.6	26
	1	75	294	5.6	4.6	35		56	221	5.6	2.2	29
5	3.3	75	24	NS	6	57		40.2	12.7	NS	3.4	40
	2.5	75	34.8	5.6	5.8	52		40.2	18.7	5.6	3.2	32
	1.8	75	59	5.6	5.2	47		47	37.4	5.6	2.8	31
	1.5	62	69.8	5.6	5	41		47	53.6	5.6	2.4	30
	1.2	62	124	5.6	4.6	37		47	93.1	5.6	2.2	29
	1	62	243	5.6	4.4	37		47	187	5.6	2	27

Notes:

9) The output voltage ripple is tested at 1.2A output current.
10) Load transient from 0.6A to 1.2A, slew rate =0.8A/µs.

Normally output voltage is recommended to be set from 0.8V to 5.5V. Actually it can be set larger than 5.5V. Output voltage ripple will be larger in this case due to larger inductor ripple current. Additional output capacitor is needed to reduce the output ripple voltage.

When output voltage is high, the chip's heat dissipation become more important, please refer to PC Board layout guidelines on page 18 to achieve better thermal effect.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 10µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. L_1=1μH for MPM3610A.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3610A internal compensation is optimized for a wide range of capacitance and ESR values.

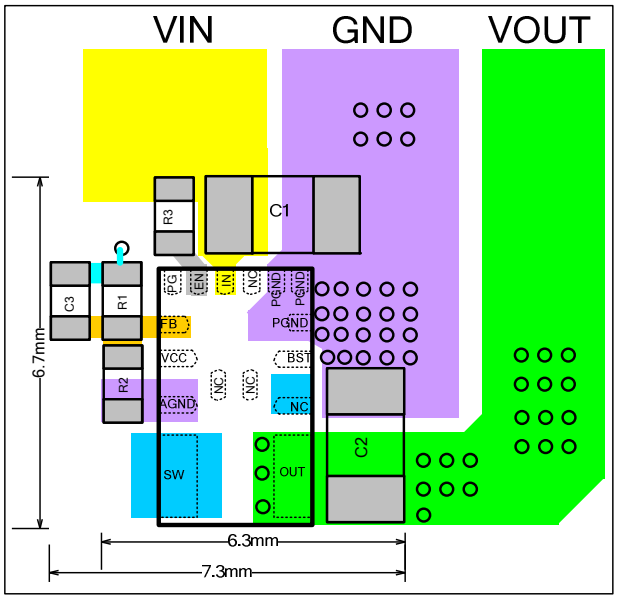
PC Board Layout (11)

PCB layout is very important to achieve stable operation especially for input capacitor placement. For best results, follow these guidelines:

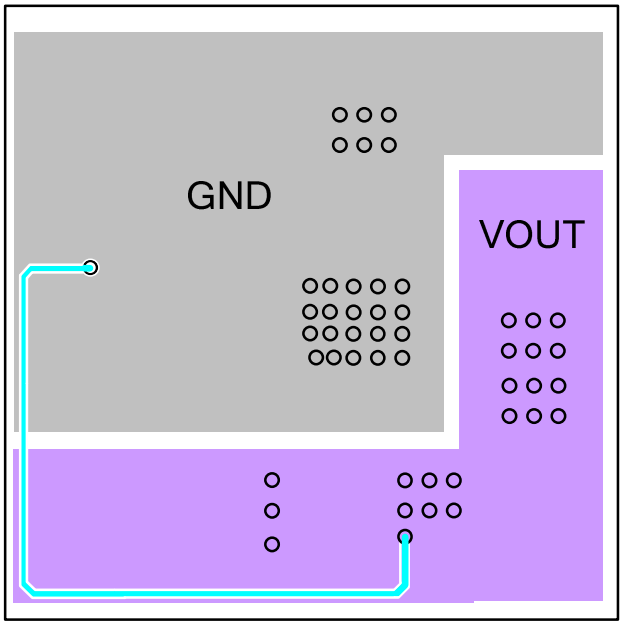
1. Use large ground plane directly connect to PGND pin. Add vias near the PGND pin if bottom layer is ground plane.
2. The high current paths (PGND, IN and OUT) should have short, direct and wide traces. Place the ceramic input capacitor close to IN and PGND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.
3. The external feedback resistors should be placed next to the FB pin.
4. Keep the feedback network away from the switching node.

Notes:

11) The recommended layout is based on Typical Application Circuits section on page 20.



Top Layer



Bottom Layer

Figure 8: Recommend PC Board Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	1.2A

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS(12)

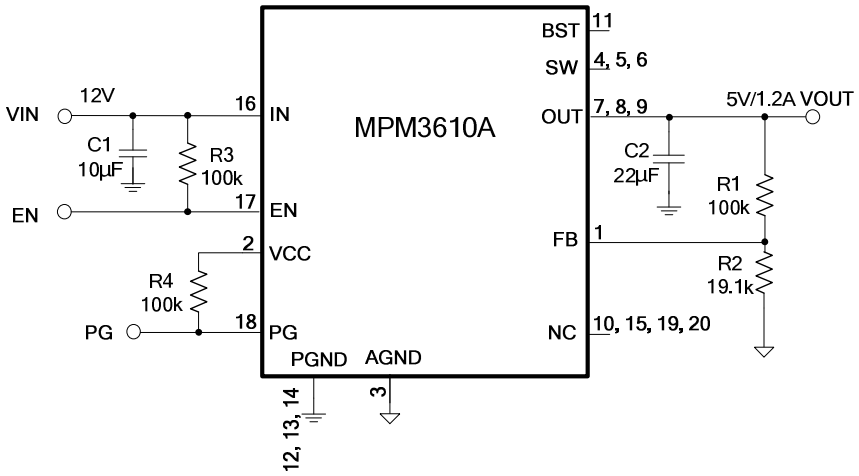


Figure 9: Vo=5V, Io=1.2A

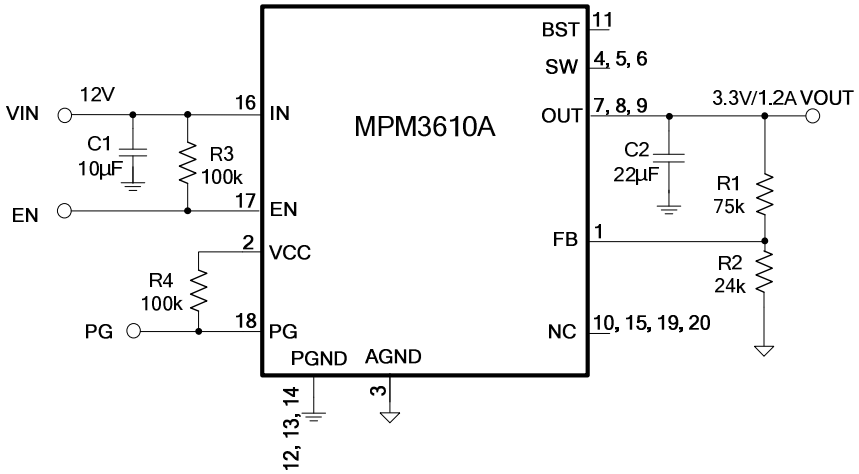


Figure 10: Vo=3.3V, Io=1.2A

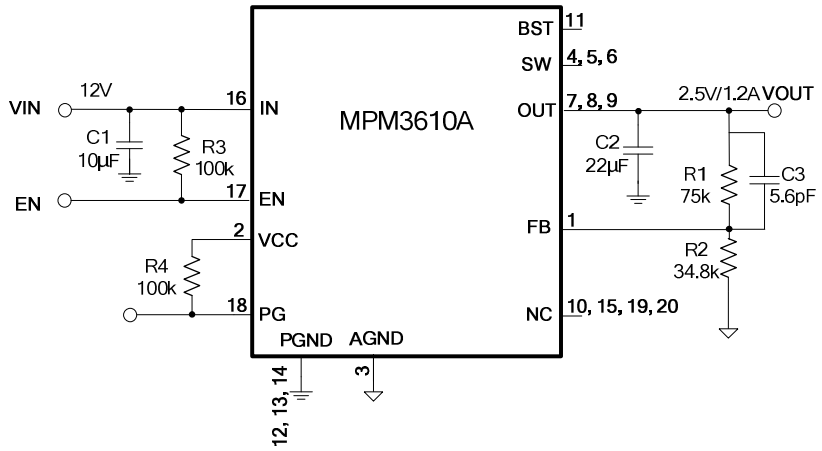


Figure 11: Vo=2.5V, Io=1.2A

TYPICAL APPLICATION CIRCUITS(*continued*)

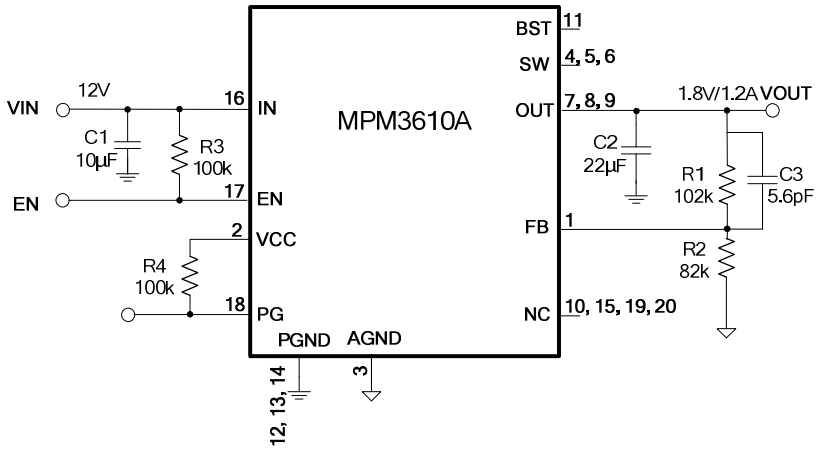


Figure 12: Vo=1.8V, Io=1.2A

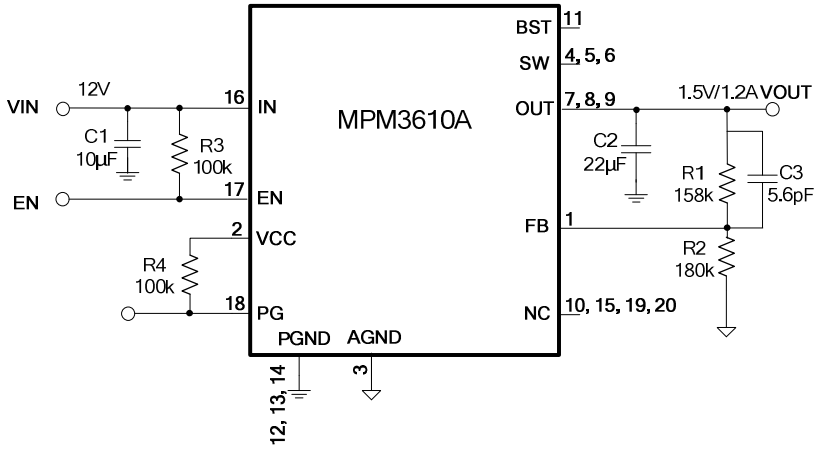


Figure 13: Vo=1.5V, Io=1.2A

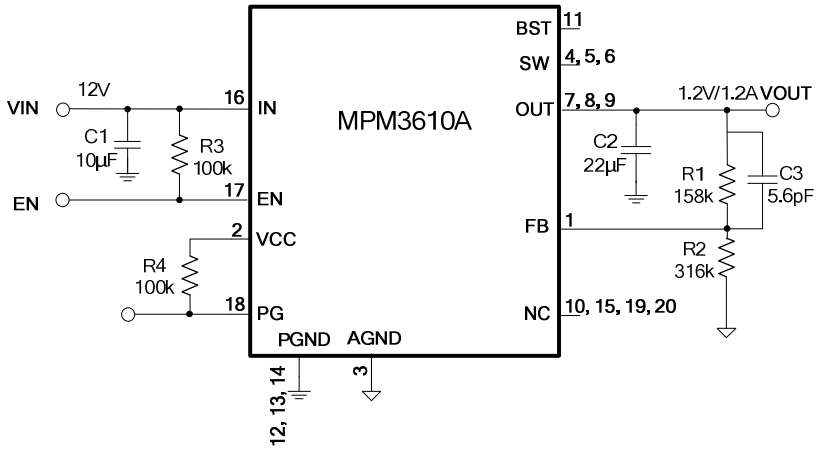


Figure 14: Vo=1.2V, Io=1.2A

TYPICAL APPLICATION CIRCUITS (*continued*)

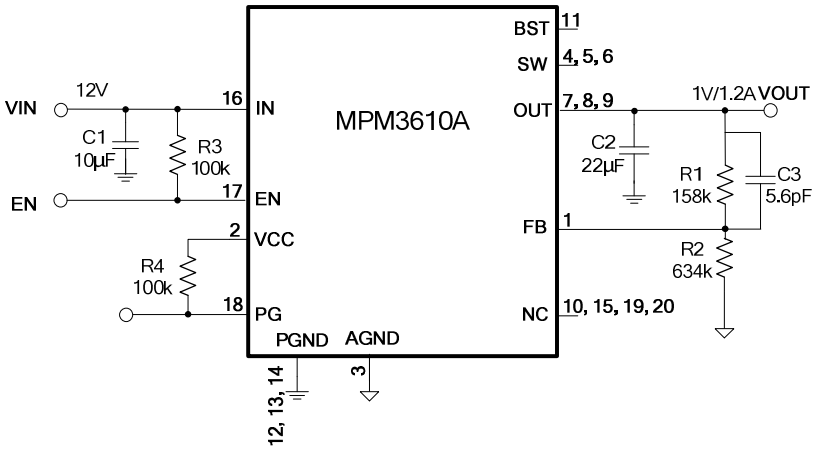


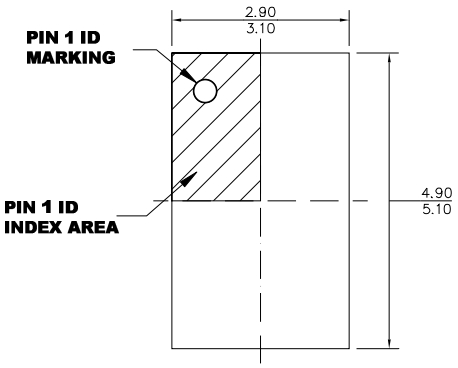
Figure 15: Vo=1V, Io=1.2A

Notes:

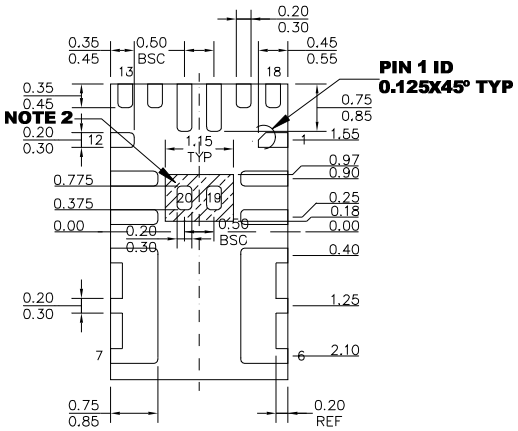
12) In $12V_{IN}$ to $1V_{OUT}$ application condition, the HS-FET's on time is close to minimum on time, the SW may have a little jitter, even so the output voltage ripple is smaller than 15mV.

PACKAGE INFORMATION

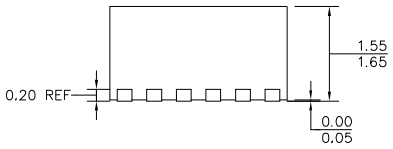
QFN-20 (3mmx5mmx1.6mm)



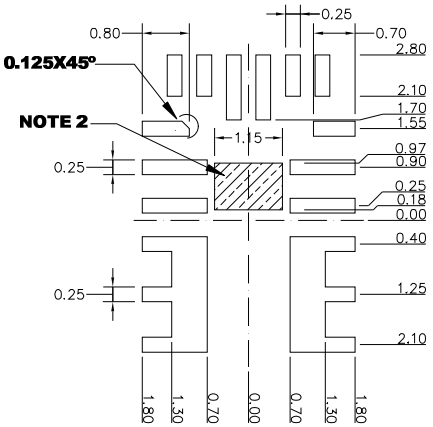
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.