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Gates SR Latch Truth Table:

Blue – inputs , Yellow – outputs

CLK	S	R	Qt	Qt+1	NotQt+1
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	Forbidden	Forbidden
1	1	1	1	Forbidden	Forbidden

Diagrams:

Main:
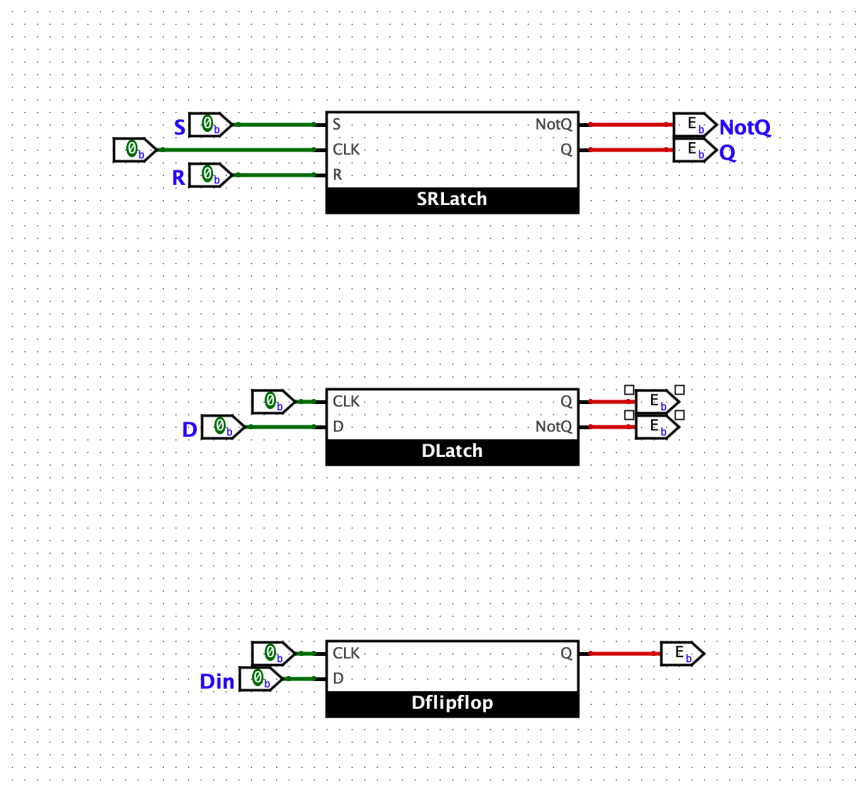
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SR Latch:

S
CLK
R
E_b NotQ
E_b Q

D Latch:

CLK
D
E_b Q
E_b NotQ

D Flipflop:

CLK
D
Q1
CLK Q
D NotQ
DLatch
CLK Q
D NotQ
DLatch
E_b Q

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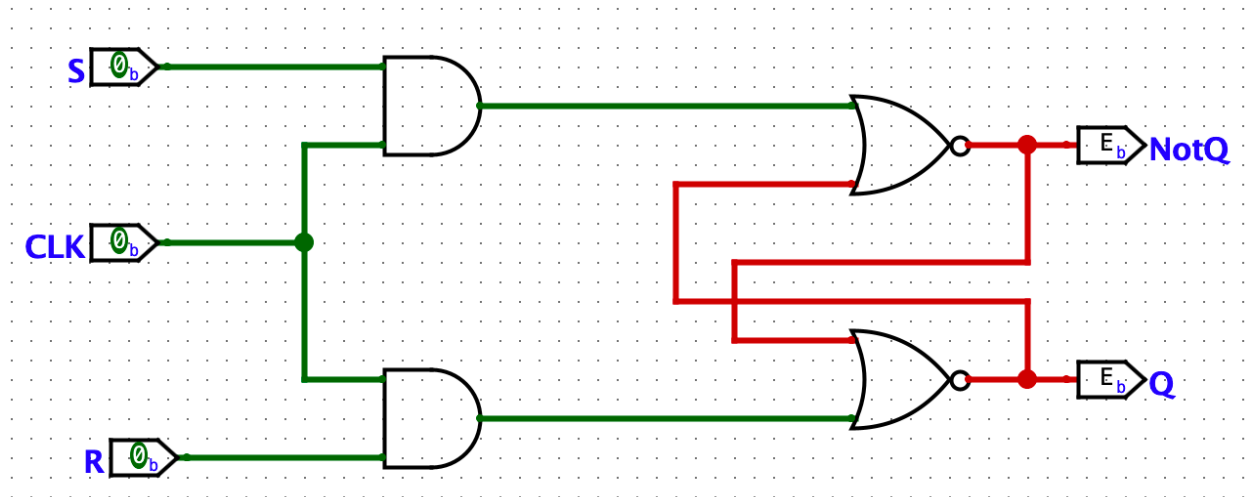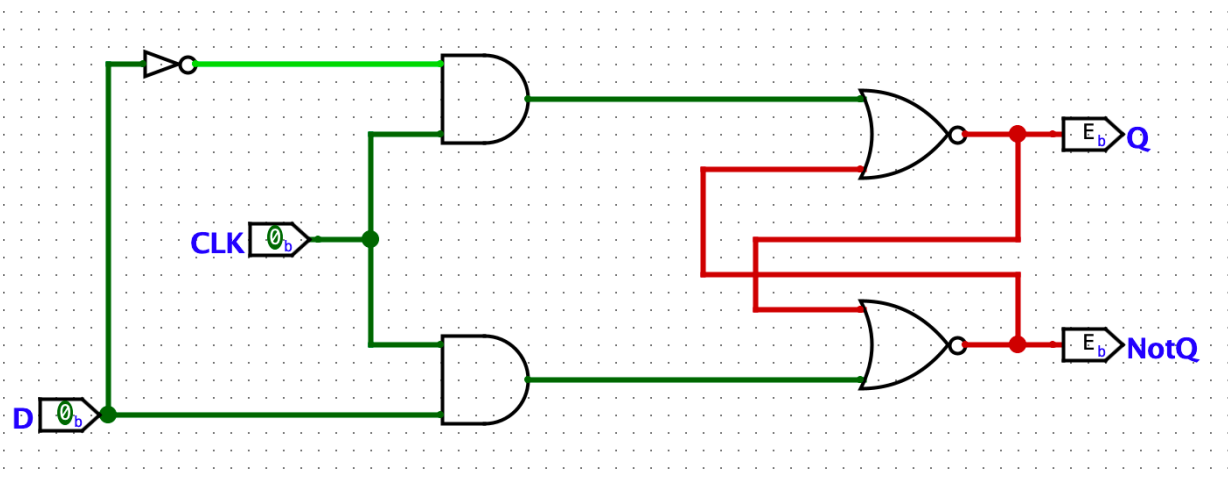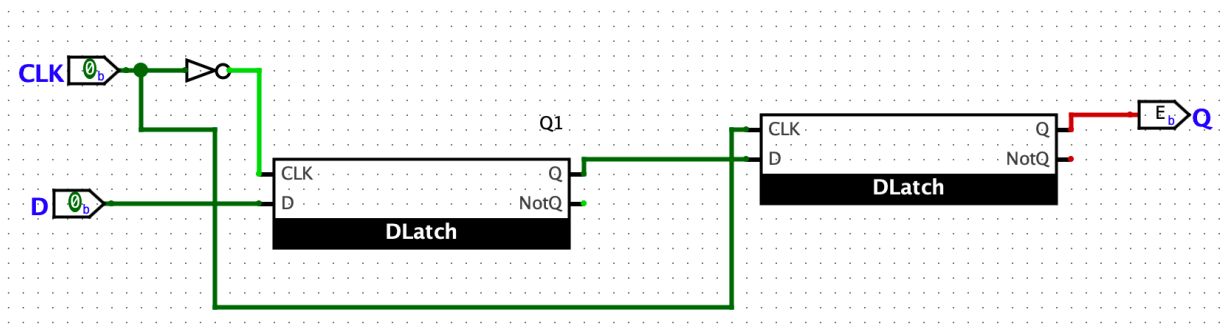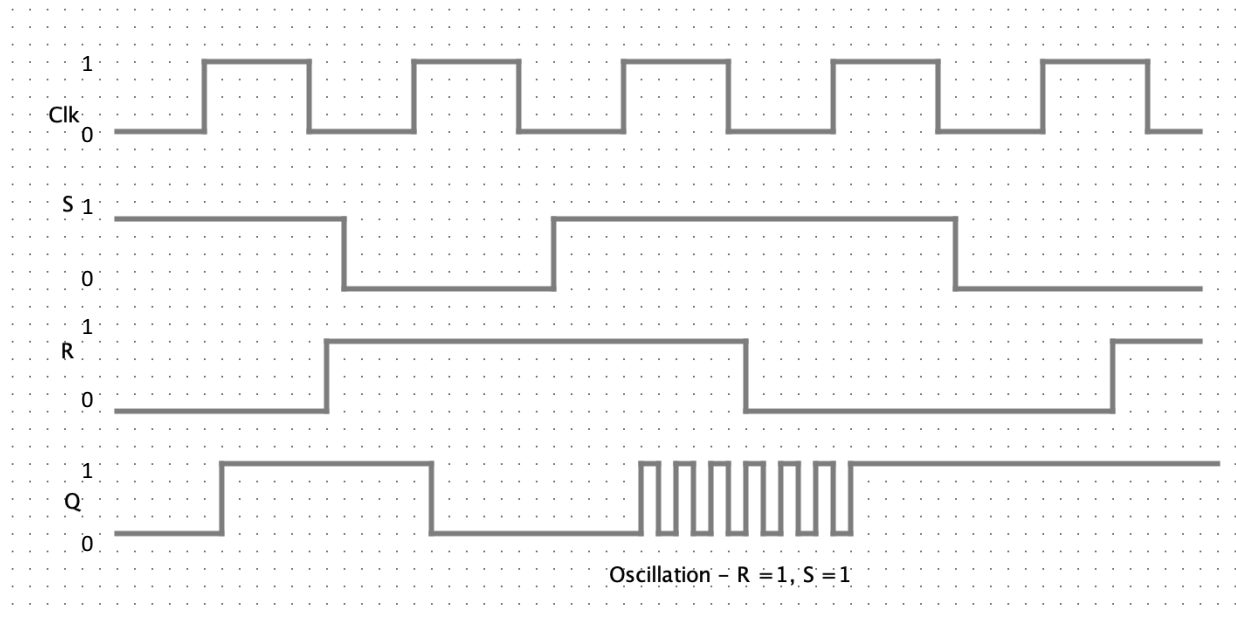
Wave Diagrams:

SR Latch:

The circuit works whenever the clock is at 1not as it changes from 0 to 1, making it pulse-triggered. When the clock is 0, while S and are changing, Q does not change. When the clock is 1, S is 1 and R is 0 then Q becomes 1. When the clock is 1, S is 0 and R is 1 then Q becomes 0. When the clock is 1, S is 1 and R is 1 then Q becomes an oscillating state (forbidden state).

D Flipflop:
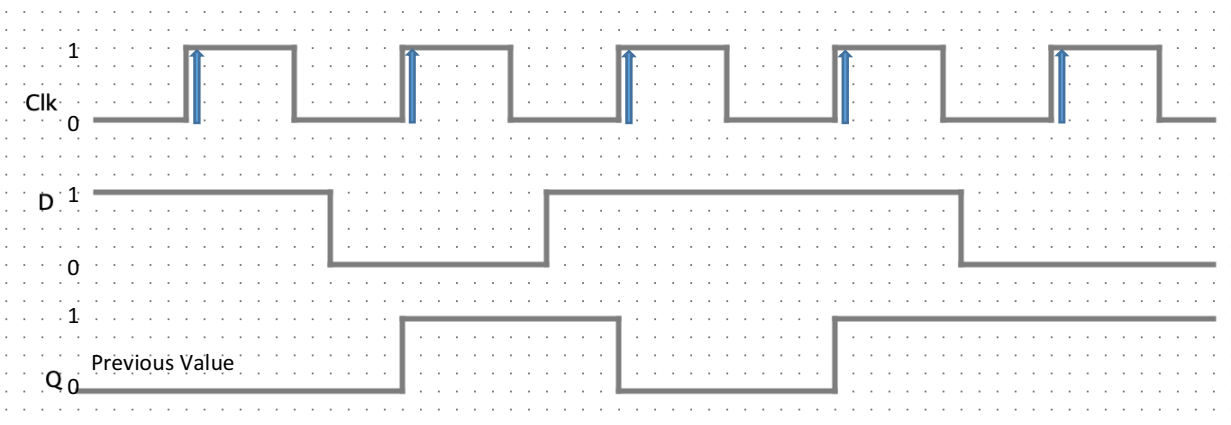
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Whenever the clock goes from 0 to 1, the first latch and Q1 takes the value of D. This value then gets outputted when the clock goes from 0 to 1; hence, making it positive edge-triggered. Right at the edge of when the clock changes from 0 to 1, the value gets outputted.