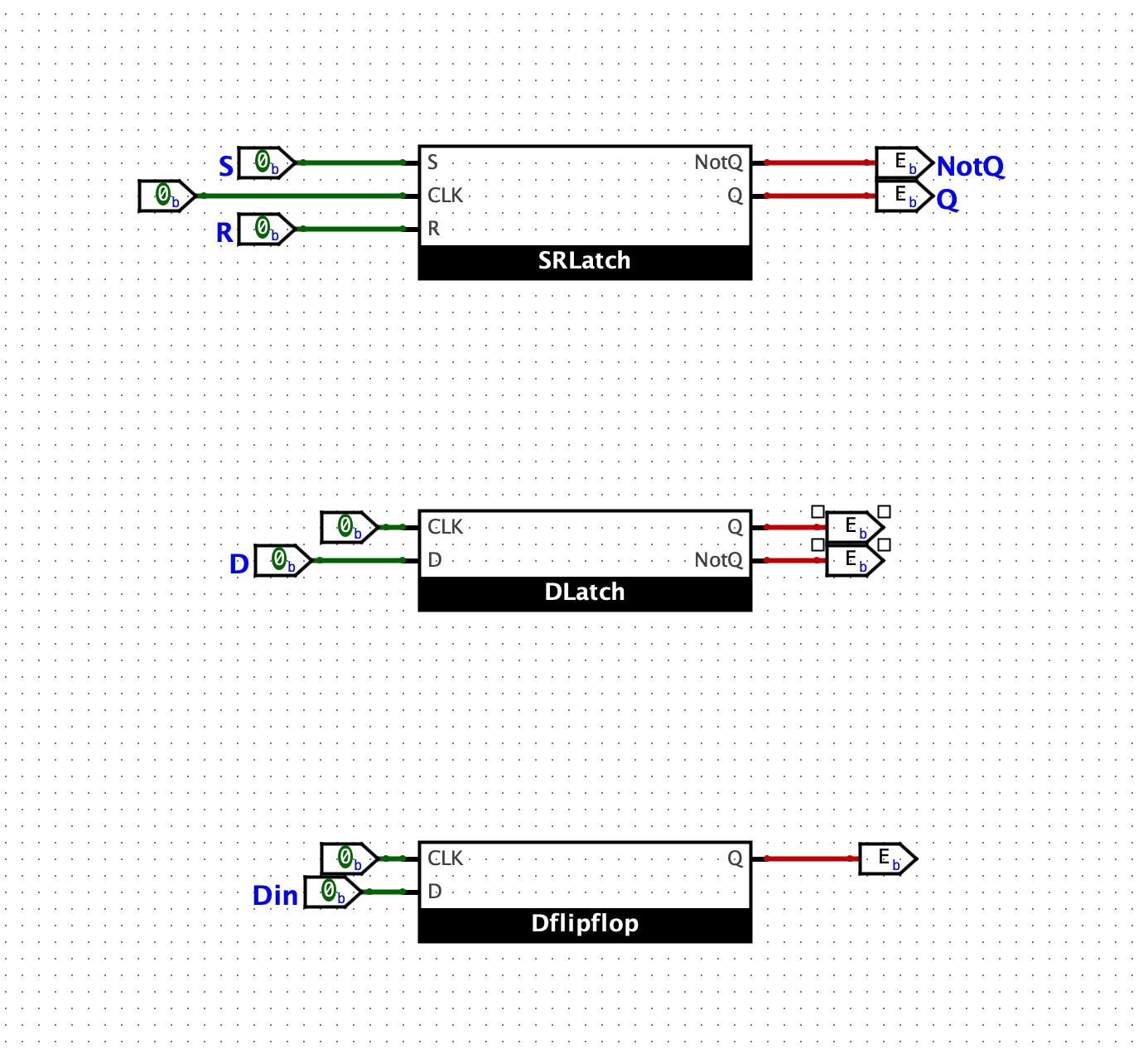
**Gates SR Latch Truth Table:**

Blue – inputs , Yellow – outputs

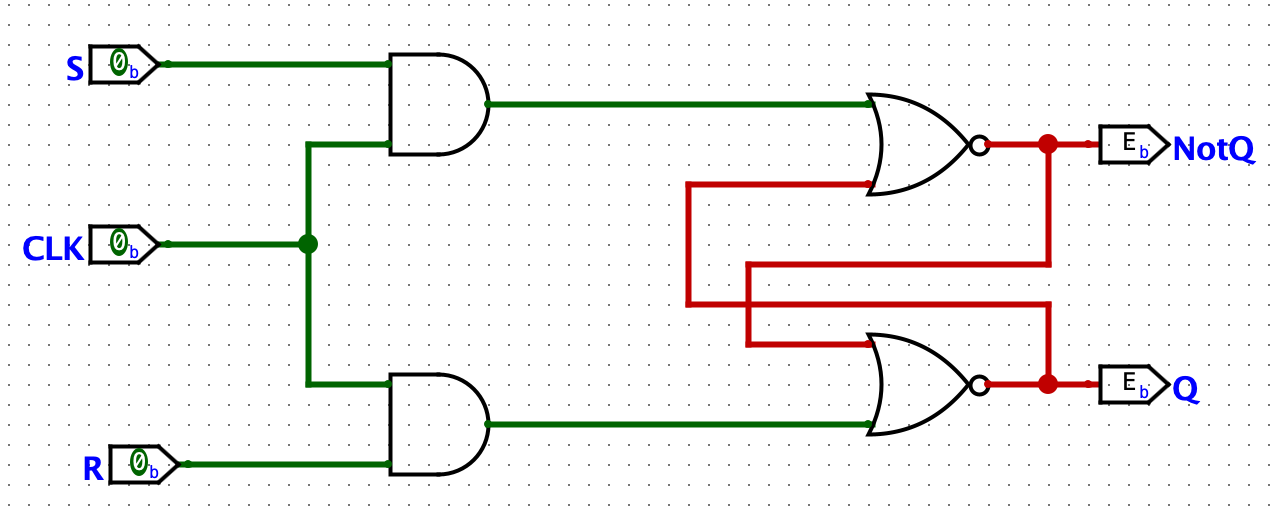
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CLK | S | R | Qt | Qt+1 | NotQt+1 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | Forbidden | Forbidden |
| 1 | 1 | 1 | 1 | Forbidden | Forbidden |

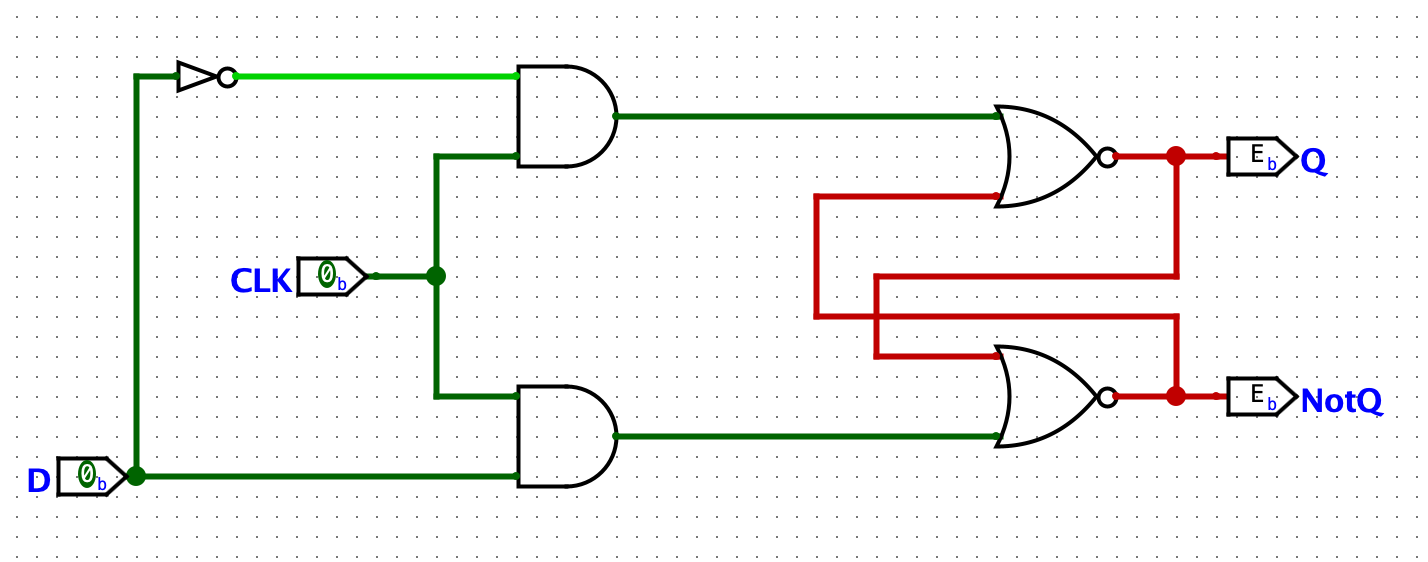
**Diagrams:**

**Main:**

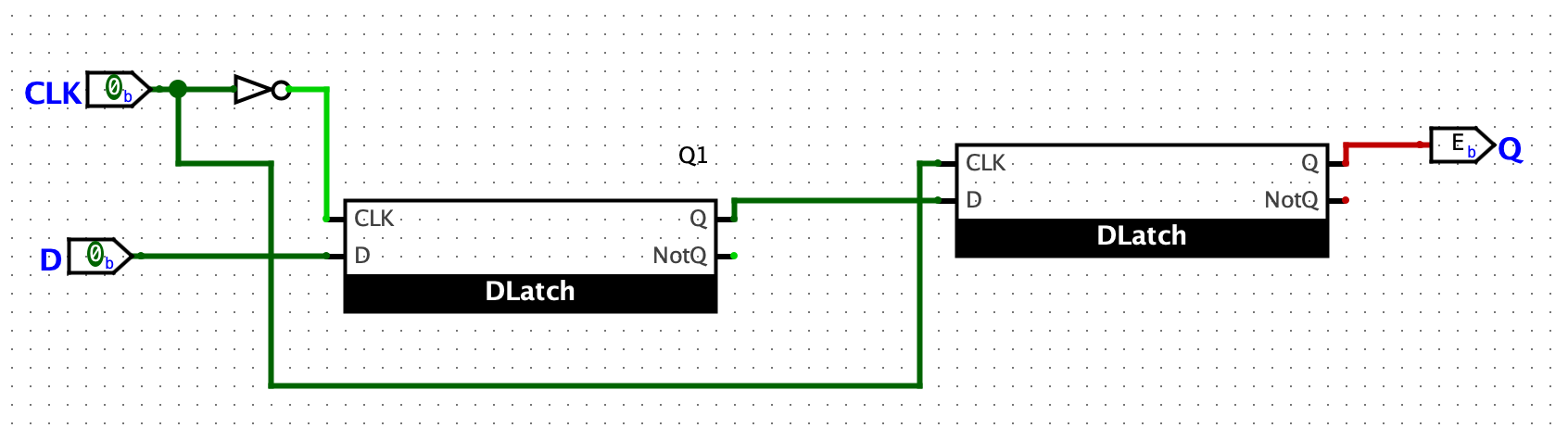


**SR Latch:**

****

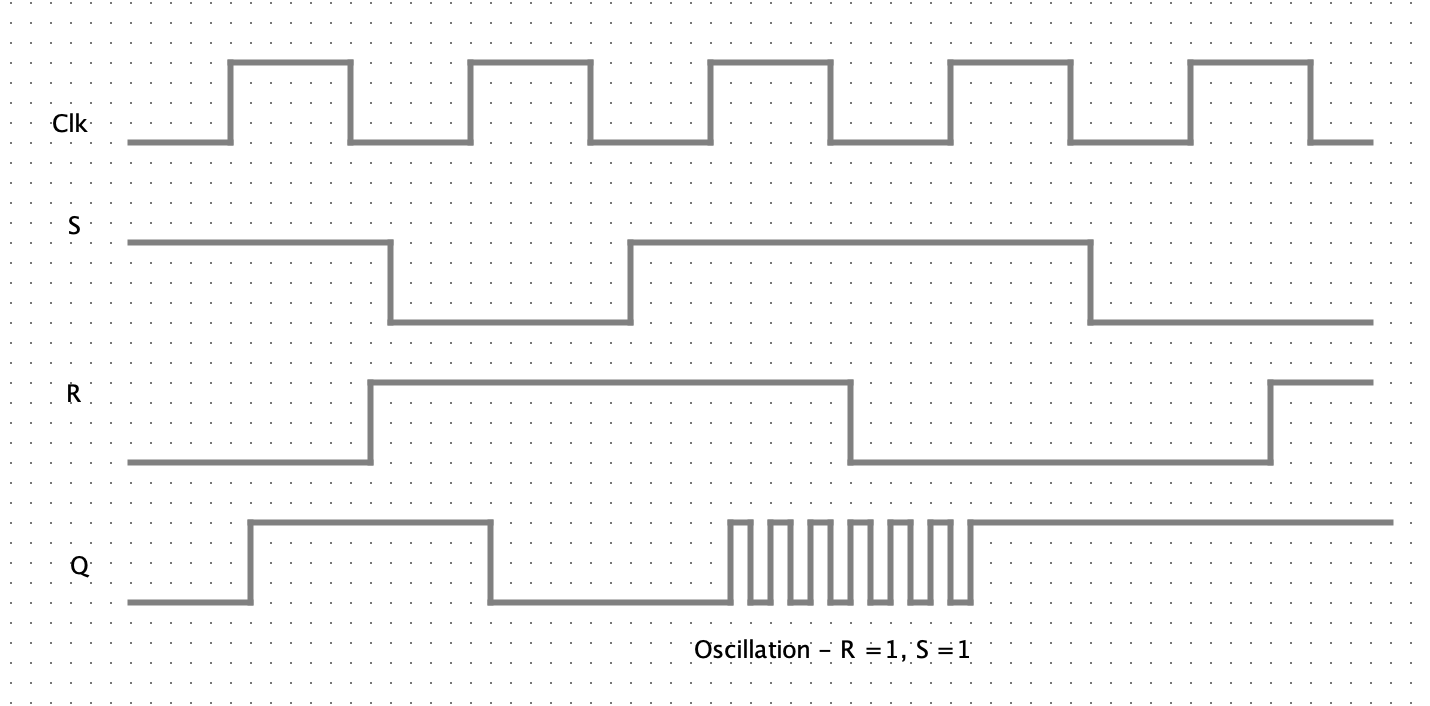
**D Latch:**

**D Flipflop:**

****

**Wave Diagrams:**

**SR Latch:**

****

0

0

0

0

1

1

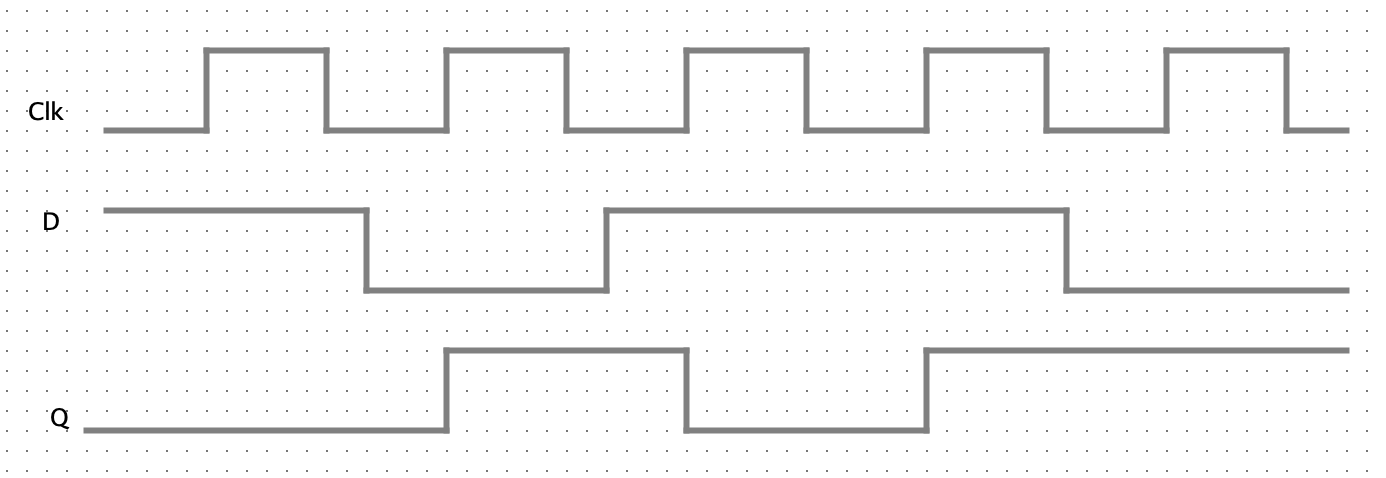
1

1

The circuit works whenever the clock is at 1not as it changes from 0 to 1, making it pulse-triggered. When the clock is 0, while S and are changing, Q does not change. When the clock is 1, S is 1 and R is 0 then Q becomes 1. When the clock is 1, S is 0 and R is 1 then Q becomes 0.

When the clock is 1, S is 1 and R is 1 then Q becomes an oscillating state (forbidden state).

**D Flipflop:**

****

0

0

0

1

1

1

Previous Value

Whenever the clock goes from 0 to 1, the first latch and Q1 takes the value of D. This value then gets outputted when the clock goes from 0 to 1; hence, making it positive edge-triggered. Right at the edge of when the clock changes from 0 to 1, the value gets outputted.