Fast Layout-Oblivious Tensor-Matrix Multiplication with BLAS

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Abstract. The tensor-matrix product is a basic tensor operation that is required by various tensor methods such as the ALS or the HOSVD. This paper presents flexible high-performance algorithms for the modeq tensor-matrix multiplication that computes the product according to the the Loops-over-gemms (LOG) approach with gemm being the general matrix multiply Our algorithms can process dense tensors with any linear tensor layout, arbitrary tensor order and dimensions all of which can be runtime variable. We discuss different tensor slicing methods with parallelization strategies and propose six variations of a base algorithm which calls a gemv, gemm and/or a gemm_batch with subtensors or tensor slices. Their performance is quantified for a set of tensors with various shapes and tensor order. The best-performing version attains a median performance of 1.37 double precision Tflops/s on an Intel Xeon Gold 6248R processor using Intel's MKL. We show that the performance is only slightly affected by the tensor layout and the median performance is between [?] and [?] Tflops/s for a range of linear tensor formats. Our fastest version of the tensor-matrix multiplication is on average at least 14.05% and up to 3.79 x faster than other state-of-the-art implementations, including Libtorch and Eigen.

1 Introduction

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Tensor computations are found in many scientific fields such as computational 26 neuroscience, pattern recognition, signal processing and data mining [7,14]. Ten-27 sors representing large amount of multidimensional data are decomposed and 28 analyzed with the help of basic tensor operations [8,9]. The decomposition and 29 analysis led to the development and analysis of high-performance kernels for tensor contractions. In this work, we present and analyze a high-performance 31 algorithm for the tensor-matrix multiplication that is used in many numerical 32 algorithms such as the alternating least squares method [8,9]. It is a compute-33 bound tensor operation and has the same arithmetic intensity as a matrix-matrix multiplication which can almost reach the practical peak performance of a computing machine. 36

There has been three main approaches for implementing tensor contractions. The Transpose-Transpose-gemm-Transpose (TGGT) approach reorganizes (flattens) tensors in order to perform a tensor contraction with an optimized

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matrix-matrix multiplication (gemm) implementation [2,16]. Implementations of a more recent method (GETT) are based on high-performance gemm-like algorithms [1,12,17]. A different method is the LOG approach in which BLAS are utilized with multiple tensor slices or subtensors if possible [10,13,15]. Implementations of the LOG and TTGT approaches are in general easier to maintain and faster to port than GETT implementations which might need to adapt vector instructions or blocking parameters according to a processor's micro-architecture.

Our work is motivated by the fact that LOG-based implementations of the tensor-matrix and tensor-vector multiplication are similar. To our best knowledge, we are the first to combine the approach in [3] with the findings in [10] and to propose fast in-place tensor-matrix multiplication algorithms that are layout-oblivious. Our algorithms compute the tensor-matrix product in parallel using OpenMP together with highly efficient gemm or gemm_batch implementations. They support dense tensors with any order, dimensions and any linear tensor layout including the first- and the last-order storage formats for any contraction mode all of which can be runtime variable. Input and output tensors do not need to be transposed or flattened into two-dimensional matrices. The parallel versions of the recursive base algorithm execute fused loops in parallel and are able to fully utilize a processors compute units. Despite, the generality of our approach, every proposed algorithm can be implemented with less than 100 lines of C++ code where the complexity is hidden by the BLAS implementation and the corresponding selection of subtensors or tensor slices. We have provided an open and free reference C++ implementation of all algorithms and a python interface for convenience. While we have used Intel's MKL for our benchmarks, the user is free to choose any other library that provides the BLAS interface.

The following analysis quantifies the impact of the tensor layout, the tensor slicing method and parallel execution of slice-matrix multiplications with varying contraction modes. The runtime measurements of our implementations are compared with those presented in [12,17] including Libtorch and Eigen. In summary, the main findings of our work are:

- A tensor-matrix multiplication can be implemented by an in-place algorithm with 1 gemv and 7 gemm calls supporting all combinations of contraction mode, tensor order and dimensions for any linear tensor layout.
- Our algorithm with variable loop fusion and parallel slice-matrix multiplications is on average 17% faster than a single batched gemm call when the contraction and leading dimensions are greater than 256.
- All our proposed algorithms are layout oblivious and achieve at least a median throughput of [?] for any linear tensor layout.
- Our LOG-based tensor-times-matrix implementation are in general faster than TTGT- and GETT-based implementations that have been described in [12,17] including actively developed libraries such as Libtorch and Eigen. Using symmetrically shaped tensors, an average speedup of [?] x to [?] x for single and double precision floating point computations can be achieved.

The remainder of the paper is organized as follows. Section 2 presents related work. Section 3 introduces the terminology used in this paper and defines the

tensor-vector multiplication. Algorithm design and methods for parallel execution is discussed in Section 4. Section 5 describes the test setup and discusses the benchmark results in Section 6. Conclusions are drawn in Section 7.

$_{88}$ 2 Related Work

The authors in [13] discuss the efficient tensor contractions with highly optimized BLAS. Based on the LOG approach, they define requirements for the use of GEMM for class 3 tensor contractions and provide slicing techniques for tensors. The slicing recipe for the class 2 categorized tensor contractions contains a short description with a rule of thumb for maximizing performance. Runtime measurements cover class 3 tensor contractions.

The work in [10] presents a framework that generates in-place tensor-matrix multiplication according to the LOG approach. The authors present two strategies for efficiently computing the tensor contraction applying GEMMs with tensors. They report a speedup of up to 4x over the TTGT-based MATLAB tensor toolbox library discussed in [2]. Although many aspects are similar to our work, the authors emphasize the code generation of tensor-matrix multiplications using high-performance GEMM's.

The authors of [17] present a tensor-contraction generator TCCG and the GETT approach for dense tensor contractions that is inspired from the design of a high-performance GEMM. Their unified code generator selects implementations from generated GETT, LoG and TTGT candidates. Their findings show that among 48 different contractions 15% of LoG based implementations are the fastest. However, their tests do not include the tensor-vector multiplication where the contraction exhibits at least one free tensor index.

Using also the GETT approach, the author presents in [12] a runtime flexible tensor contraction library. He describes block-scatter-matrix algorithm which uses a special layout for the tensor contraction. The proposed algorithm yields results that feature a similar runtime behavior to those presented in [17].

3 Background

Notation An order-p tensor is a p-dimensional array [11] where tensor elements are contiguously stored in memory. We write a, \mathbf{a} , \mathbf{A} and $\underline{\mathbf{A}}$ in order to denote scalars, vectors, matrices and tensors. If not otherwise mentioned, we assume $\underline{\mathbf{A}}$ to have a tensor order that is greater than 2. The p-tuple \mathbf{n} with $\mathbf{n} = (n_1, n_2, \ldots, n_p)$ will be referred to as a dimension tuple with $n_r > 1$. We will use round brackets $\underline{\mathbf{A}}(i_1, i_2, \ldots, i_p)$ or $\underline{\mathbf{A}}(\mathbf{i})$ to denote a tensor element where $\mathbf{i} = (i_1, i_2, \ldots, i_p)$ is a multi-index. A subtensor is denoted by $\underline{\mathbf{A}}'$ and references elements of a tensor $\underline{\mathbf{A}}$. They are specified with p index ranges and form a selection grid. In this work, the index range shall either address all indices of a given mode or a single element that are given by single indices i_r with $1 \le r \le p$. Elements n'_r of a subtensor's dimension tuple \mathbf{n}' are therefore n_r if all indices of mode r are selected and 1 otherwise. We will annotate subtensors using only

their non-unit modes such as $\underline{\mathbf{A}}'_{u,v,w}$ where $n_u > 1, n_v > 1$ and $n_w > 1$ and $1 \le u \ne v \ne w \le p$. It is sufficient to only provide non-unit modes as the remaining single indices correspond to the loop induction variables of the following algorithms. A subtensor is called a slice $\underline{\mathbf{A}}'_{u,v}$ if the full range selection of $\underline{\mathbf{A}}$ occurs with only two modes. A fiber $\underline{\mathbf{A}}'_u$ is a tensor slice with only one dimension greater than 1.

Linear Tensor Layouts We use a layout tuple $\pi \in \mathbb{N}^p$ to encode all linear tensor layouts including the first-order or last-order layout. They contain permuted tensor modes whose priority is given by their index. For instance, the first- and last-order storage formats are given by $\pi_F = (1, 2, ..., p)$ and $\pi_L = (p, p-1, ..., 1)$. An inverse layout tuple π^{-1} is defined by $\pi^{-1}(\pi(k)) = k$. Given a layout tuple π with p modes, the π_r -th element of a stride tuple is given by $w_{\pi_r} = \prod_{k=1}^{r-1} n_{\pi_k}$ for $1 < r \le p$ and $w_{\pi_1} = 1$. Tensor elements of the π_1 -th mode are contiguously stored in memory.

The location of tensor elements is determined by the tensor layout and the layout function. For a given tensor layout and stride tuple, a layout function $\lambda_{\mathbf{w}}$ maps a multi-index to a scalar index with $\lambda_{\mathbf{w}}(\mathbf{i}) = \sum_{r=1}^{p} w_r(i_r - 1)$. With $j = \lambda_{\mathbf{w}}(\mathbf{i})$ being the relative memory position of an element with a multi-index \mathbf{i} , reading from and writing to memory is accomplished with j and the first element's address of \mathbf{A} .

Non-Modifying Flattening and Reshaping The flattening operation $\varphi_{r,q}$ transforms an order-p tensor $\underline{\mathbf{A}}$ to another order-p' view $\underline{\mathbf{B}}$ that has different a shape \mathbf{m} and layout $\boldsymbol{\tau}$ tuple of length p' with p' = p - q + r and $1 \leq r < q \leq p$. It is related to the tensor unfolding operation as defined in [8, p.459] but neither changes the element ordering nor copies tensor elements. Given a layout tuple $\boldsymbol{\pi}$ of $\underline{\mathbf{A}}$, the flattening operation $\varphi_{r,q}$ is defined for contiguous modes $\hat{\boldsymbol{\pi}} = (\pi_r, \pi_{r+1}, \dots, \pi_q)$ of $\boldsymbol{\pi}$. Let j = 0 if $k \leq r$ and j = q - r otherwise for $1 \leq k \leq p'$. Then the resulting layout tuple $\boldsymbol{\tau} = (\tau_1, \dots, \tau_{p'})$ of $\underline{\mathbf{B}}$ is given by $\tau_r = \min(\boldsymbol{\pi}_{r,q})$ and $\tau_k = \pi_{k+j} + s_k$ if $k \neq r$ where $s_k = |\{\pi_i \mid \pi_{k+j} > \pi_i \wedge \pi_i \neq \min(\hat{\boldsymbol{\pi}}) \wedge r \leq i \leq p\}|$. Elements of the corresponding shape tuple \mathbf{m} are given by $m_{\tau_r} = \prod_{k=r}^q n_{\pi_k}$ and $m_{\tau_k} = n_{\pi_{k+j}}$ if $k \neq r$.

The reshaping operation ρ transforms an order-p tensor $\underline{\mathbf{A}}$ to another order-p tensor $\underline{\mathbf{B}}$ with different shape \mathbf{m} and layout $\boldsymbol{\tau}$ tuples of length p. In this work, it permutes the shape and layout tuple simultaneously without changing the element ordering and without copying tensor elements. The operation ρ uses a permutation tuple $\boldsymbol{\rho} = (\rho_1, \dots, \rho_p)$ to only modify shape and layout tuples. Elements of the resulting shape tuple \mathbf{m} and the layout tuple $\boldsymbol{\tau}$ are given by $m_r = n_{\rho_r}$ and $\tau_r = \pi_{\rho_r}$, respectively.

Tensor-Matrix Multiplication (TTM) Let $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ be order-p tensors with shapes $\mathbf{n}_a = (n_1, \dots, n_q, \dots, n_p)$ and $\mathbf{n}_c = (n_1, \dots, n_{q-1}, m, n_{q+1}, \dots, n_p)$. Let $\underline{\mathbf{B}}$ be a matrix of shape $\mathbf{n}_b = (m, n_q)$. A mode-q TTM is denoted by $\underline{\mathbf{C}} = \underline{\mathbf{A}} \times_q \underline{\mathbf{B}}$

where an element of \mathbf{C} is given by

$$\underline{\mathbf{C}}(i_1, \dots, i_{q-1}, j, i_{q+1}, \dots, i_p) = \sum_{i_q=1}^{n_q} \underline{\mathbf{A}}(i_1, \dots, i_q, \dots, i_p) \cdot \mathbf{B}(j, i_q)$$
(1)

with $1 \leq i_r \leq n_r$ and $1 \leq j \leq m$. The mode q is the contraction mode of the TTM with $1 \leq q \leq p$. The tensor-matrix multiplication generalizes the computational aspect of the two-dimensional case $\mathbf{C} = \mathbf{B} \cdot \mathbf{A}$ if p = 2 and q = 1. Its arithmetic intensity is equal to that of a matrix-matrix multiplication and is not memory-bound. In the following, we assume that the tensors $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ have the same tensor layout π . Elements of matrix $\underline{\mathbf{B}}$ can stored in either the column-major or row-major format.

4 Algorithm Design

4.1 Sequential Algorithm

The sequential baseline algorithm for Eq. 1 can be implemented with a single C++ function that supports tensors with arbitrary order, dimensions and any linear tensor layout. It consists of nested recursion with a control flow that is akin to algorithm 1 in [4] consisting of two if statements with an else branch. The body of the first if statement contains a recursive call that skips the iteration over the dimension n_q when $r = \hat{q}$ with $\pi_r = q$ and $\hat{q} = \pi_q^{-1}$ where π^{-1} is the inverse layout tuple. The second if statement contains multiple recursive calls for the modes $1 \le r \ne \hat{q} \le p$ with different multi-indices. The else branch is the base case and consists of two loops that compute a fiber-matrix product. The outer loop iterates with j over the dimension m of $\underline{\mathbf{C}}$ and $\underline{\mathbf{B}}$. The inner loop iterates with i_q over the dimension n_q of $\underline{\mathbf{A}}$ and $\underline{\mathbf{B}}$ computing an inner product.

4.2 Baseline Algorithm with Contiguous Memory Access

The baseline algorithm accesses elements of $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ non-contiguously whenever $\pi_1 \neq q$. Matrix \mathbf{B} is contiguously accessed if i_q or j is incremented with unitsteps depending on the storage format of $\underline{\mathbf{B}}$. The access pattern can be improved by reordering tensor elements according to the storage format. However, copy operations reduce the overall throughput of the operation [15].

A better approach is to access tensor elements according to the tensor layout using the tensor layout tuple π as proposed in [4]. The modified algorithm 1 contiguously accesses memory for $\pi_1 \neq q$ and p>1. Each recursion level adjusts only one multi-index element i_{π_r} with a stride w_{π_r} in line 5. With increasing recursion level and decreasing r, indices are incremented with smaller step sizes as $w_{\pi_r} \leq w_{\pi_{r+1}}$. The condition of the second if statement in line 4 is changed from $r \geq 1$ to r > 1. In this way, the mode- π_1 loop with index i_{π_1} and the minimum stride w_{π_1} are included in the base case which contains three loops performing a slice-matrix multiplication. The loop ordering are adjusted according to the

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tensor_times_matrix(\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{n}, \mathbf{i}, m, q, \hat{q}, r)
 1
              if r = \hat{q} then
 2
                     tensor_times_matrix(A, B, C, n, i, m, q, \hat{q}, r - 1)
              else if r > 1 then
 4
                     for i_{\pi_r} \leftarrow 1 to n_{\pi_r} do
 5
                        tensor_times_matrix(\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{n}, \mathbf{i}, m, q, \hat{q}, r - 1)
 6
              else
 7
                     for j \leftarrow 1 to m do
 8
                             for i_q \leftarrow 1 to n_q do
 9
                                    \begin{array}{l} \mathbf{for} \ i_{\sigma_1} \leftarrow 1 \ \mathbf{to} \ n_{\pi_1} \ \mathbf{do} \\ & \quad \underline{\mathbf{C}}(i_1,...,i_{q-1},j,i_{q+1},...,i_p) \ \textbf{+=} \ \underline{\mathbf{A}}(i_1,...,i_q,...,i_p) \cdot \mathbf{B}(j,i_q) \end{array}
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Algorithm 1: Modified baseline algorithm with contiguous memory access for the tensor-matrix multiplication. The tensor order must be greater than one and for the contraction mode $1 \le q \le p$ and $\pi_1 \ne q$ must hold. The algorithm needs to be initially called with r = p where **n** is the shape tuple of $\underline{\mathbf{A}}$ and m is the q-th dimension of \mathbf{C} .

tensor and matrix layout. The inner-most loop increments i_{π_1} and contiguously accesses tensor elements of $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$. The second loop increments i_q with which elements of $\underline{\mathbf{B}}$ are contiguously accessed if $\underline{\mathbf{B}}$ is stored in the row-major format. The third loop increments j and could be placed as the second loop if $\underline{\mathbf{B}}$ is stored in the column-major format.

While spatial data locality is improved by adjusting the loop ordering, the temporal data locality of tensors $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ differ. Note that slice $\underline{\mathbf{A}}'_{\pi_1,q}$ is accessed m times, fiber $\underline{\mathbf{C}}_{\pi_1}$ is accessed $\mathbf{n}(q)$ times and element $\underline{\mathbf{B}}(j,i_q)$ is accessed $\mathbf{n}(\pi_1)$ times. While the specified fiber of $\underline{\mathbf{C}}$ can fit into first or second level cache, slice elements of $\underline{\mathbf{A}}$ are unlikely to fit in the local caches if the slice size $n_{\pi_1} \times n_q$ is large leading to higher cache misses and suboptimal performance. Optimized tiling for better temporal data locality has been discussed in [6] which suggests to use existing high-performance BLAS implementations for the base case.

4.3 BLAS-based Algorithms with Tensor Slices

Algorithm 1 is the starting point for the BLAS-based algorithm which computes the tensor-matrix product with a gemm routine. Besides the illustrated algorithm, we have identified seven other cases where a single gemm call suffices to compute the tensor-matrix product even if the tensor order p>2. In summary, there are eight cases with a single gemm call using different arguments which are listed in table 1. The list of gemm calls supports all linear tensor layout and has no limitation on tensor order and contraction mode. The arguments of gemm are chosen depending on the tensor order p, tensor layout π and contraction mode p except for the CBLAS_ORDER which is CblasRowMajor.

Case	Order p	Layout π	$\mathrm{Mode}\; q$	Routine	T	M	N	K	A	LDA	В	LDB	LDC
1	1	-	1	gemv	-	m	n_1	-	В	n_1	<u>A</u>	-	-
2	2	(1, 2)	1	gemm	В	n_2	m	n_1	A	n_1	В	n_1	\overline{m}
3	2	(1, 2)	2	gemm	-	m	n_1	n_2	В	n_2	$\underline{\mathbf{A}}$	n_1	n_1
4	2	(2, 1)	1	gemm	-	m	n_2	n_1	В	n_1	$\underline{\mathbf{A}}$	n_2	n_2
5	2	(2, 1)	2	gemm	В	n_1	m	n_2	<u>A</u>	n_2	В	n_2	m
6	> 2	any	π_1	gemm	В	\bar{n}_q	m	n_q	<u>A</u>	n_q	В	n_q	m
7	> 2	any	π_p	gemm	-	m	\bar{n}_q	n_q	В	n_q	<u>A</u>	\bar{n}_q	\bar{n}_q
8	> 2	any	$\pi_2,,\pi_{p-1}$	gemm*	-	m	n_{π_1}	n_q	В	n_q	<u>A</u>	w_q	w_q

Table 1. Eight gemv and gemm cases for the mode-q tensor-matrix multiplication. Arguments T, M, N, etc. of the BLAS are chosen with respect to the tensor order p, layout π and contraction mode q where T specifies if \mathbf{B} is transposed. gemm* denotes multiple gemm calls with different tensor slices. Argument \bar{n}_q for case 6 and 7 is given by $\bar{n}_q = 1/n_q \prod_{r=1}^p n_r$. Matrix \mathbf{B} has the row-major format.

Case 1 (p=1): The tensor-vector product $\underline{\mathbf{A}} \times_1 \mathbf{B}$ can be computed with a gemv operation $\mathbf{a}^T \cdot \mathbf{B}$ where $\underline{\mathbf{A}}$ is an order-1 tensor, i.e. a vector \mathbf{a} of length n_1 .

Case 2-5 (p=2): If $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ are order-2 tensors, i.e. a matrix \mathbf{A} with dimensions n_1 and n_2 , then a single gemm suffices to compute the tensor-matrix product. If \mathbf{A} and \mathbf{C} have the column-major format with $\pi = (1,2)$, gemm either executes $\mathbf{C} = \mathbf{A} \cdot \mathbf{B}^T$ for q=1 or $\mathbf{C} = \mathbf{B} \cdot \mathbf{A}$ for q=2. Note that gemm interprets \mathbf{C} and \mathbf{A} as matrices using the reshaping operation ρ with $\rho = (2,1)$ in row-major format even though both are stored column-wise. If \mathbf{A} and \mathbf{C} have the row-major format with $\pi = (2,1)$, gemm either executes $\mathbf{C} = \mathbf{B} \cdot \mathbf{A}$ for q=1 or $\mathbf{C} = \mathbf{A} \cdot \mathbf{B}^T$ for q=2. Note that the transposition of \mathbf{B} is necessary for the cases 2,5 and independent of the chosen storage format.

Case 6-7 (p > 2): If the order of $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ is greater than 2 and if the contraction mode q is equal to π_1 (case 6), a single gemm with the depicted parameters executes $\mathbf{C} = \mathbf{A} \cdot \mathbf{B}^T$ and computes a tensor-matrix product $\underline{\mathbf{C}} = \underline{\mathbf{A}} \times_{\pi_1} \mathbf{B}$ for any storage layout of $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$. Tensors $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ are flattened with $\varphi_{2,p}$ to row-major matrices \mathbf{A} and \mathbf{C} . Matrix \mathbf{A} has $\bar{n}_{\pi_1} = \bar{n}/n_{\pi_1}$ rows and n_{π_1} columns while matrix \mathbf{C} has the same number of rows and m columns. If $\pi_p = q$ (case 7), Tensors $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ are flattened with $\varphi_{1,p-1}$ to column-major matrices \mathbf{A} and \mathbf{C} . Matrix \mathbf{A} has n_{π_p} rows and $\bar{n}_{\pi_p} = \bar{n}/n_{\pi_p}$ columns while matrix \mathbf{C} has m rows and the same number of columns. A single gemm executes $\mathbf{C} = \mathbf{B} \cdot \mathbf{A}$ and computes the tensor-matrix product $\underline{\mathbf{C}} = \underline{\mathbf{A}} \times_{\pi_p} \mathbf{B}$ for any storage layout of $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$. Note that in all cases no copy operation is performed in order to compute the desired contraction, see subsection 3.

Case 8 (p > 2): If the tensor order is greater than 2 with $\pi_1 \neq q$ and $\pi_p \neq q$, the modified baseline algorithm 1 is used to successively call $\bar{n}/(n_q \cdot n_{\pi_1})$ times gemm with different tensor slices of $\underline{\mathbf{C}}$ and $\underline{\mathbf{A}}$ in the base case. Each gemm computes one slice $\underline{\mathbf{C}}'_{\pi_1,q}$ of the tensor-matrix product $\underline{\mathbf{C}}$ using the corresponding tensor slices $\underline{\mathbf{A}}'_{\pi_1,q}$ and the matrix $\underline{\mathbf{B}}$. The matrix-matrix product $\mathbf{C} = \underline{\mathbf{B}} \cdot \underline{\mathbf{A}}$ is performed

by interpreting both tensor slices as row-major matrices **A** and **C** which have the dimensions (n_q, n_{π_1}) and (m, n_{π_1}) , respectively.

4.4 BLAS-Based Algorithms with Subtensors

Case 8 can be optimized by selecting larger subtensors instead of tensor slices which might lead to a better processor utilization. Larger subtensors can be used by selecting additional mergeable modes that still allow the subtensor to be flattened into a matrix without reordering tensor elements using the description provided in section 3, see also lemma 4.1 in [10]. The maximum number of mergeable modes is $\hat{q} - 1$ with $\hat{q} = \boldsymbol{\pi}^{-1}(q)$ and the corresponding modes are $\pi_1, \pi_2, \ldots, \pi_{\hat{q}-1}$. Applying flattening $\varphi_{1,q-1}$ and reshaping ρ with $\rho = (2,1)$ on a subtensor of $\underline{\mathbf{A}}$ with dimensions $n_{\pi_1}, \ldots, n_{\pi_{\hat{q}-1}}, n_q$ yields a row-major matrix \mathbf{A} with shape $(n_q, \prod_{r=1}^{\hat{q}-1} n_{\pi_r})$. This is done analogously for $\underline{\mathbf{C}}$ resulting in a row-major matrix with shape $(m, \prod_{r=1}^{\hat{q}-1} n_{\pi_r})$. This description supports all linear tensor layouts and generalizes lemma 4.2 in [10].

Algorithm 1 needs a minor modification for calling gemm flattened subtensors instead of tensor slices. The modified algorithm must therefor omit the first \hat{q} modes $\pi_{1,\hat{q}} = (\pi_1, \dots, \pi_{\hat{q}})$ including $\pi_{\hat{q}} = q$. This is done by only iterating over modes larger than \hat{q} in the non-base case. The conditions in line 2 and 4 are changed to $1 < r \le \hat{q}$ and $\hat{q} < r$, respectively. The single indices of the subtensors $\underline{\mathbf{A}}'_{\pi_{1,\hat{q}}}$ and $\underline{\mathbf{C}}'_{\pi_{1,\hat{q}}}$ are given by the loop induction variables that belong to the π_r -th loop with $\hat{q} + 1 \le r \le p$.

4.5 Parallel BLAS-based Algorithms

The following paragraphs discuss three parallel approaches for the eighth case. Cases 1 to 7 already call a multi-threaded gemm and cannot be further optimized.

Sequential Loops and Multithreaded gemm One straight forward approach is to use algorithm 1 as it is and to sequentially call a multi-threaded gemm in the base case of the algorithm as described in subsection 4.4. This is beneficial if $q=\pi_{p-1}$, the inner dimensions n_{π_1},\ldots,n_q are large or the outer-most dimension n_{π_p} is smaller than the available processor cores. However, if the above conditions are not met, the processor cores might not be fully utilized where each multi-threaded gemm is executed with small subtensors. We will refer to this algorithm version as <code>seq-loops,par-gemm></code> that is executable with subtensors or tensor slices.

Parallel Loops and Single- or Multithreaded gemm A more advanced version of the above algorithm executes a single-threaded gemm in parallel including all available (free) modes which depend on the slicing. If subtensors are used, all $\pi_{\hat{q}+1}, \ldots, \pi_p$ modes are free. In case of tensor slices, only π_1 and $\pi_{\hat{q}}$ are free modes. The corresponding maximum degree of parallelism for both cases are $\prod_{r=\hat{q}+1}^p n_{r_r}$ and $\prod_{r=1}^p n_r/(n_{\pi_1}n_{\pi_{\hat{q}}})$, respectively.

Using tensor slices for the multiplication, $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ are flattened twice with $\varphi_{\pi_{\hat{q}+1},\pi_p}$ and $\varphi_{\pi_2,\pi_{\hat{q}-1}}$. The resulting tensor is of order 4 with dimensions n_{π_1} , \hat{n}_{π_2} , n_q , \hat{n}_{π_4} where $\hat{n}_{\pi_2} = \prod_{r=2}^{\hat{q}-1} n_{\pi_r}$ and $\hat{n}_{\pi_4} = \prod_{r=\hat{q}+1}^p n_{\pi_r}$. In this way the treerecursion has been transformed in two loops. The outer loop iterates over \hat{n}_{π_4} while the inner loop iterates over \hat{n}_{π_2} calling gemm with slices $\underline{\mathbf{A}}'_{\pi_1,q}$ and $\underline{\mathbf{C}}'_{\pi_1,q}$. Both loops are parallelized using omp parallel for together with the collapse(2) and the num_threads clause which specifies the thread number.

In case of the general subtensor-matrix approach, both tensors are flattened twice with $\varphi_{\pi_{\hat{q}+1},\pi_p}$ and $\varphi_{\pi_1,\pi_{\hat{q}-1}}$. The resulting tensor is of order 3 with dimensions $\hat{n}_{\pi_1}, n_q, \hat{n}_{\pi_4}$ where $\hat{n}_{\pi_1} = \prod_{r=1}^{\hat{q}-1} n_{\pi_r}$ and $\hat{n}_{\pi_4} = \prod_{r=\hat{q}+1}^p n_{\pi_r}$. The corresponding algorithm consists of one loops which iterates over \hat{n}_{π_4} calling single-threaded gemm with multiple subtensors $\underline{\mathbf{A}}'_{\pi',q}$ and $\underline{\mathbf{C}}'_{\pi',q}$ with $\pi' = (\pi_1, \dots, \pi_{\hat{q}-1})$. Both algorithm variants will be referred to as $\operatorname{par-loops, seq-gemm}$ which

Both algorithm variants will be referred to as <par-loops,seq-gemm> which can be used with subtensors or tensor slices. Note that <seq-loops,par-gemm> and <par-loops,seq-gemm> are opposing versions where either gemm or the free loops are performed in parallel. The all-parallel version <par-loops,par-gemm> executes available loops in parallel where each loop thread executes a multi-threaded gemm with either subtensors or tensor slices.

Multithreaded gemm_batch The next version of the base algorithm is a modified version of the general subtensor-matrix approach that calls a single batched gemm for the eighth case. The subtensor dimensions and remaining gemm arguments remain the same. The library implementation is responsible how subtensor-matrix multiplications are executed and if subtensors are further divided into smaller subtensors or tensor slices. This version will be referred to as the <gemm_batch> variant.

5 Experimental Setup

Computing System The experiments have been carried out on an Intel Xeon Gold 6248R processor with a Cascade micro-architecture. The processor consists of 24 cores operating at a base frequency of 3 GHz for non-AVX512 instructions. With 24 cores and a peak AVX-512 boost frequency of 2.5 GHz, the processor achieves a theoretical data throughput of ca. 1.92 double precision TFlops/s We measured a peak performance of 1.78 double precision Tflops/s using the likwid performance tool.

The source code has been compiled with GCC v10.2 using the highest optimization level -03 and -march=native, -pthread and -fopenmp. Loops within for the eighth case have been parallelized using GCC's OpenMP v4.5 implementation. We have used the GEMV and GEMM implementation of the 2024.0 Intel MKL and its own threading library mkl_intel_thread together with the threading runtime library libiomp5.

If not otherwise mentioned, both tensors $\underline{\mathbf{A}}$ and $\underline{\mathbf{C}}$ are stored according to the first-order linear tensor layout with $\boldsymbol{\pi}=(1,\ldots,p)$ whereas matrix \mathbf{B} has the row-major storage format. The benchmark results of each function are the average of 10 runs.

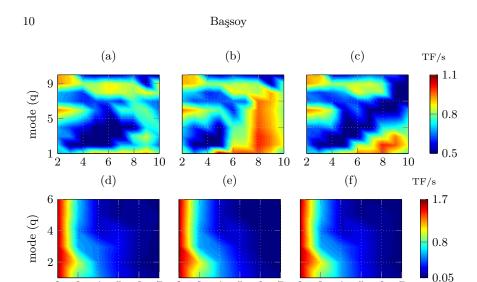


Fig. 1. Performance maps in double-precision Tflops/s of the proposed tensor-times-matrix algorithms with varying tensor orders p and contraction modes q. Tensors are asymmetrically-shaped on the upper plots and symmetrically-shaped on the lower plots. In (a) and (d) function <code>sgemm_batch></code> is executed, in (b) and (e) <code>spar-loops,seq-gemm></code> with tensor slices, in (c) and (f) <code>spar-loops,seq-gemm></code> with subtensors.

4 5 6 7

order (p)

2 3

4 5 6 7 2

order (p)

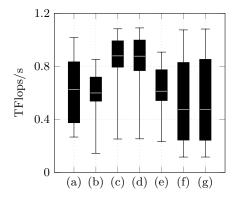
 $2 \quad 3 \quad 4 \quad 5 \quad 6 \quad 7$

order (p)

Tensor Shapes We have used asymmetrically-shaped and symmetrically-shaped tensors in order to cover many possible use cases. The dimension tuples of both shape types are organized within two three-dimensional arrays with which tensors are initialized. The dimension array for the first shape type contains $720 = 9 \times 8 \times 10$ dimension tuples where the row number is the tensor order ranging from 2 to 10. For each tensor order 8 tensor instances with increasing tensor size is generated. The second set consists of $336 = 6 \times 8 \times 7$ dimensions tuples where the tensor order ranges from 2 to 7 and has 8 dimension tuples for each order. Each tensor dimension within the second set is 2^{12} , 2^{8} , 2^{6} , 2^{5} , 2^{4} and 2^{3} . A detailed explanation of the tensor shape setup is given in [3,4].

6 Results and Discussion

Slicing Methods We have first analyzed the two slicing methods by benchmarking function
par-loops,seq-gemm> and <gemm-batch> using asymmetrically (top) and symmetrically (bottom) shaped tensors. Fig. 1 contains six filled contour plots (performance maps) in which
par-loops,seq-gemm> either uses subtensors or tensor slices and <gemm-batch> loops over subtensors only. Each point within the performance map represents a mean value that has been averaged over tensor sizes for a tensor order.



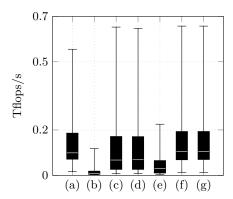
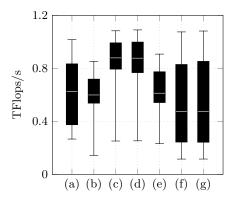


Fig. 2. Box plots visualizing performance statics in double-precision Tflops/s of the proposed tensor-times-matrix algorithms for the 8-th case. Tensors are asymmetrically-shaped on the left plot and symmetrically-shaped on the right plot. In (a) function version <code><gemm_batch></code> is executed, in (b) and (e) <code><seq-loops,par-gemm></code>, in (c) and (f) <code><par-loops,seq-gemm></code>, in (d) and (g) <code><par-loops,par-gemm></code>, Functions (b,c,d) and (e,f,g) are executed with tensor slices or subtensors, respectively.

For asymmetrically shaped tensors, function $\operatorname{spar-loops,seq-gemm}$ with tensor slices performs on average 18% better than with subtensors. Surprisingly, $\operatorname{spar-loops,seq-gemm}$ with tensor slices is on average 11% faster than Intel's $\operatorname{gemm_batch}$ routine and reaches almost 1.1 Tflops/s for non-edge cases with q>2 and p>6. This suggests that the Intel's implementation might not divide subtensors into smaller blocks. With symmetrically shaped tensors, the performance maps of $\operatorname{spar-loops,seq-gemm}$ with tensor slices and $\operatorname{sgemm-batch}$ are almost identical with a median performance of 221.52 and 236.21 Gflops/s. Moreover, the slicing method does minimally affect the runtime behavior of $\operatorname{spar-loops,seq-gemm}$. In contrast to the performance maps with asymmetrically shaped tensors, all functions almost reach the attainable peak performance of 1.7 Tflops/s when p=2. This can by the fact that both dimensions are equal or larger than 4096 which lets gemm operate under optimal conditions.

Parallelization Methods Applying the first setup configuration with asymmetrically-shaped tensors, we have analyzed the effects of the blocking and parallelization strategy. The LB-PN version processes tensors with different storage formats, namely the 1-, 2-, 9- and 10-order layout. The performance behavior is almost the same for all storage formats except for the corner cases $q = \pi_1$ and $q = \pi_p$. Even the performance drop for q = p - 1 is almost unchanged. The standard deviation from the mean value is less than 10% for all storage formats. Given a contraction mode $q = \pi_k$ with 1 < k < p, a permutation of the inner and outer tensor dimensions with their respective indices π_1, \ldots, π_{k-1} and π_{k+1}, \ldots, π_p does influence the runtime where the LB-PN version calls GEMV with the values w_m and n_m . The same holds true for the outer layout tuple.



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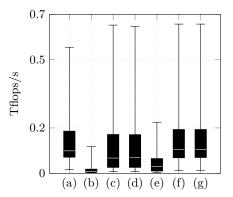


Fig. 3. Box plots visualizing performance statics in double-precision Tflops/s of a tensor-times-matrix algorithm for linear k-order tensor formats. The algorithm loops over single-threaded gemm with tensor slices with asymmetrically-shaped tensors on the left plot and with subtensors with symmetrically-shaped tensors on the right plot. Box plot number k denotes the utilized k-order storage.

Comparison with other Approaches The following comparison includes three state-of-the-art libraries that implement three different approaches. The library TCL (v0.1.1) implements the (TTGT) approach with a high-perform tensor-transpose library HPTT which is discussed in [17]. TBLIS (v1.0.0) implements the GETT approach that is akin to BLIS's algorithm design for matrix computations [12]. The tensor extension of EIGEN (v3.3.90) is used by the Tensorflow framework and performs the tensor-vector multiplication in-place and in parallel with contiguous memory access [1]. TLIB denotes our library that consists of sequential and parallel versions of the tensor-vector multiplication. Numerical results of TLIB have been verified with the ones of TCL, TBLIS and EIGEN.

Fig. ?? illustrates the average single-precision Gflops/s with asymmetricallyand symmetrically-shaped tensors in the first-order storage format. The runtime behavior of TBLIS and EIGEN with asymmetrically-shaped tensors is almost constant for varying tensor sizes with a standard deviation ranging between 2% and 13%. TCL shows a different behavior with 2 and 4 Gflops/s for any order $p \geq 2$ peaking at p = 10 and q = 2. The performance values however deviate from the mean value up to 60%. Computing the arithmetic mean over the set of contraction modes yields a standard deviation of less than 10% where the performance increases with increasing order peaking at p=10. TBLIS performs best for larger contraction dimensions achieving up to 7 Gflops/s and slower runtimes with decreasing contraction dimensions. In case of symmetrically-shaped tensors, TBLIS and TCL achieve up to 12 and 25 Gflops/s in single precision with a standard deviation between 6% and 20%, respectively. TCL and TBLIS behave similarly and perform better with increasing contraction dimensions. EIGEN executes faster with decreasing order and increasing contraction mode with at most 8 Gflops/s at p=2 and q>2.

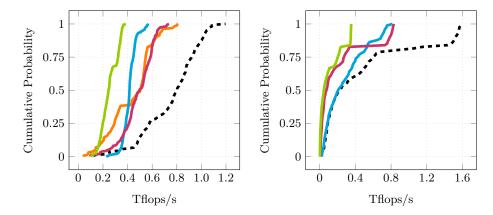


Fig. 4. Cumulative performance distributions of tensor-times-matrix algorithms in double-precision Tflops/s. Each distribution line belongs to a library: tlib (---), tcl (----), tblis (-----), libtorch (------), eigen (---------). Libraries have been tested with asymmetrically-shaped (left plot) and symmetrically-shaped tensors (right plot).

Fig. ?? illustrates relative performance maps of the same tensor-vector multiplication implementations. Comparing TCL performance, TLIB-SB-PN achieves an average speedup of 6x and more than 8x for 42% of the test cases with asymmetrically shaped tensors and executes on average 5x faster with symmetrically shaped tensors. In comparison with TBLIS, TLIB-SB-PN computes the tensor-vector product on average 4x and 3.5x faster for asymmetrically and symmetrically shaped tensors, respectively.

7 Conclusion and Future Work

Based on the LOG approach, we have presented in-place and parallel tensor-vector multiplication algorithms of TLIB. Using highly-optimized DOT and GEMV routines of OpenBLAS, our proposed algorithms is designed for dense tensors with arbitrary order, dimensions and any non-hierarchical storage format. TLIB's algorithms either directly call DOT, GEMV or recursively perform parallel slice-vector multiplications using GEMV with tensor slices and fibers.

Our findings show that loop-fusion improves the performance of TLIB's parallel version on average by a factor of 5x achieving up to 34.8/15.5 Gflops/s in single/double precision for asymmetrically shaped tensors. With symmetrically shaped tensors resulting in small contraction dimensions, the results suggest that higher-order slices with larger dimensions should be used. We have demonstrated that the proposed algorithms compute the tensor-vector product on average 6.1x and up to 12.6x faster than the TTGT-based implementation provided by TCL. In comparison with TBLIS, TLIB achieves speedups on average of 4.0x and at most 10.4x. In summary, we have shown that a LOG-based tensor-vector multiplication

implementation can outperform current implementations that use a TTGT and GETT approaches.

In the future, we intend to design and implement the tensor-matrix multiplication with the same requirements also supporting tensor transposition and subtensors. Moreover, we would like to provide an in-depth analysis of LOG-based implementations of tensor contractions with higher arithmetic intensity.

Project and Source Code Availability TLIB has evolved from the Google
Summer of Code 2018 project for extending Boost's uBLAS library with tensors.
Project description and source code can be found at https://github.com/bassoy/ttv.
The sequential tensor-vector multiplication of TLIB is part of uBLAS and in the
official release of Boost v1.70.0.

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441 References

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