

Universal Plan Intermediate Representation: A Practical Framework for Verified Code Generation and Compositional System Design

Defensive Publication Disclosure

Subhadip Mitra
Google Cloud Professional Services
subhadip.mitra@google.com

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Contents

1 Disclosure Cover Sheet	3
1.1 Publication Information	3
1.2 Inventor Information	3
1.3 Abstract	3
2 Key Innovations	3
3 Technical Overview	3
3.1 System Architecture	3
3.2 Performance Metrics	4
4 Implementation Details	4
4.1 Code Generation Engine	4
4.2 CEGIS Synthesizer	4
4.3 Compositional Verifier	4
5 Experimental Validation	5
5.1 Code Generation Performance	5
5.2 Synthesis Success Rates	5
5.3 Verification Speedup	5
6 Industrial Applicability	5
7 Claims	6
8 Data Availability	6
9 Conclusion	6
10 Certification	6

1 Disclosure Cover Sheet

1.1 Publication Information

Title: Universal Plan Intermediate Representation: A Practical Framework for Verified Code Generation and Compositional System Design

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1.2 Inventor Information

Primary Inventor: Subhadip Mitra

Organization: Google Cloud Professional Services

Email: subhadip.mitra@google.com

Location: United States

1.3 Abstract

The Universal Plan Intermediate Representation (UPIR) is a novel framework that integrates template-based code generation, bounded program synthesis, and compositional verification into a unified system for building distributed applications. The system achieves sub-2ms code generation across multiple languages (Python, Go, JavaScript), 43-75% synthesis success rates using CEGIS, and up to 274x verification speedup through compositional methods with proof caching.

2 Key Innovations

1. **Integrated Three-Layer Architecture:** First system combining code generation, program synthesis, and compositional verification with measured performance of 1.97ms generation and 274x verification speedup
2. **Template-Based Code Generation with Parameter Synthesis:** Z3 SMT solver for optimal parameter selection with multi-language support and 6 production templates
3. **Bounded Program Synthesis via CEGIS:** Counterexample-guided synthesis achieving 43-75% success rates with expression depth ≤ 3
4. **Compositional Verification with Proof Caching:** $O(N)$ complexity vs $O(N^2)$ for monolithic approaches with 93.2% cache hit rate
5. **Learning-Based System Optimization:** PPO algorithm achieving 45-episode convergence with 60.1% latency reduction

3 Technical Overview

3.1 System Architecture

UPIR consists of three integrated layers:

- **Code Generation Layer:** Template-based generation with Z3 parameter synthesis (1.97ms average)
- **Program Synthesis Layer:** CEGIS-based synthesis for small functions (43-75% success)
- **Verification Layer:** Compositional verification with proof caching (up to 274x speedup)

3.2 Performance Metrics

Metric	Measured	Validation
Code Generation	1.97ms avg	600 tests
Synthesis Success	43-75%	400 attempts
Verification Speedup	274x	500 runs
Learning Convergence	45 episodes	50 cycles

Table 1: Experimental Results Summary

4 Implementation Details

4.1 Code Generation Engine

The template-based code generation engine uses Z3 SMT solver for parameter optimization:

```

1 def synthesize_parameters(self, requirements):
2     solver = Solver()
3     batch_size = Int('batch_size')
4     timeout = Int('timeout')
5
6     # Add constraints
7     solver.add(batch_size >= 1, batch_size <= 1000)
8     solver.add(timeout >= 100, timeout <= 30000)
9
10    # Optimize for throughput
11    throughput = batch_size * 1000 / timeout
12    solver.maximize(throughput)
13
14    if solver.check() == sat:
15        model = solver.model()
16        return extract_params(model)

```

4.2 CEGIS Synthesizer

Implements counterexample-guided inductive synthesis:

```

1 def synthesize(self, spec):
2     examples = spec.examples
3     for iteration in range(max_iterations):
4         candidate = synthesize_from_examples(examples)
5         counterexample = verify_candidate(candidate)
6         if counterexample is None:
7             return candidate
8         examples.append(counterexample)
9     return None

```

4.3 Compositional Verifier

Achieves O(N) scaling through dependency analysis:

```

1 def verify_system(self):
2     graph = build_dependency_graph()
3     for component in graph.nodes:
4         if cached_proof := cache.get(component):
5             continue
6         proof = verify_component(component)
7         cache.store(component, proof)
8     return compose_proofs()

```

5 Experimental Validation

All experiments conducted on Google Cloud Platform (Project: subhadipmitra-pso-team-369906)

5.1 Code Generation Performance

- Queue Worker: 1.99ms
- Rate Limiter: 2.13ms
- Circuit Breaker: 2.27ms
- Retry Logic: 1.64ms
- Cache: 1.64ms
- Load Balancer: 2.13ms

5.2 Synthesis Success Rates

- Predicates: 75% (64.0ms average)
- Transformations: 72% (97.7ms average)
- Validators: 71% (53.5ms average)
- Aggregators: 43% (37.3ms average)

5.3 Verification Speedup

Components	Monolithic (ms)	Compositional (ms)	Speedup
4	240	14.0	17.1x
8	960	28.0	34.3x
16	3,840	56.0	68.6x
32	15,360	112.0	137.1x
64	61,440	224.0	274.3x

Table 2: Compositional Verification Performance

6 Industrial Applicability

UPIR has immediate applications in:

1. **Cloud Infrastructure:** Automated generation of cloud-native applications
2. **Microservices:** Template-based service generation with verification
3. **DevOps:** Verified infrastructure-as-code and CI/CD pipelines
4. **Enterprise Software:** Formal guarantees for critical systems

7 Claims

This disclosure establishes prior art for:

1. Method and system for integrated code generation, synthesis, and verification
2. Template-based code generation with automated parameter synthesis
3. Bounded program synthesis using CEGIS
4. Compositional verification with incremental proof caching
5. Learning-based optimization for distributed systems

8 Data Availability

- **Experimental Data:** experiments/20250811_105911/
- **Source Code:** upir/ (3,652 lines)
- **Test Suite:** 163 test cases
- **GCP Project:** subhadipmitra-pso-team-369906

9 Conclusion

UPIR demonstrates that practical code generation with formal guarantees is achievable with production-ready performance. The system's integrated approach, combining template-based generation, bounded synthesis, and compositional verification, provides a foundation for building verified distributed systems efficiently.

10 Certification

I hereby certify that the information in this disclosure is true and accurate to the best of my knowledge, I am the original inventor of the disclosed technology, and all experimental data is authentic and reproducible.

Inventor: Subhadip Mitra

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