

# Semiconductor Industry Overview

Now and Future ■■■■■

We are a team of engineers from Taiwan's semiconductor industry with deep expertise in advanced processes and packaging. Our team members have extensive knowledge in AI chips, advanced packaging, CoWoS, SoIC, and silicon photonics (PIC). Additionally, our team is well-versed in semiconductor materials, specialty chemicals, and the semiconductor supply chain.

- We regularly share insightful articles on the semiconductor industry with all friends who are passionate about the field! If you have any questions about the semiconductor industry, feel free to contact us.
- We welcome friends who are interested in the semiconductor industry to get in touch with us.
- We will provide regular updates on the semiconductor industry and welcome feedback and guidance from experts in the field.
- Welcome to join the Substack SEMIVISION subscription and join TSPA community@ Facebook.



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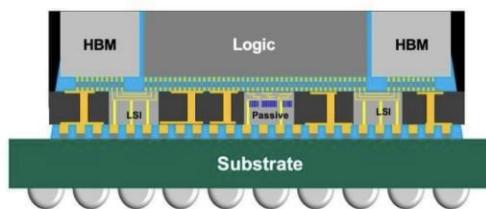
CoWoS-L is TSMC's primary focus for future capacity expansion due to its advanced integration technologies (LSI, eTDC, IVR, etc.). Additionally, it can integrate with optical engines through the COUPE platform, and the size of CoWoS-L offering an interposer area 6x larger than standard solutions. ( based on CoWoS-S 3x interposer with 2700mm<sup>2</sup> )

## CoWoS®

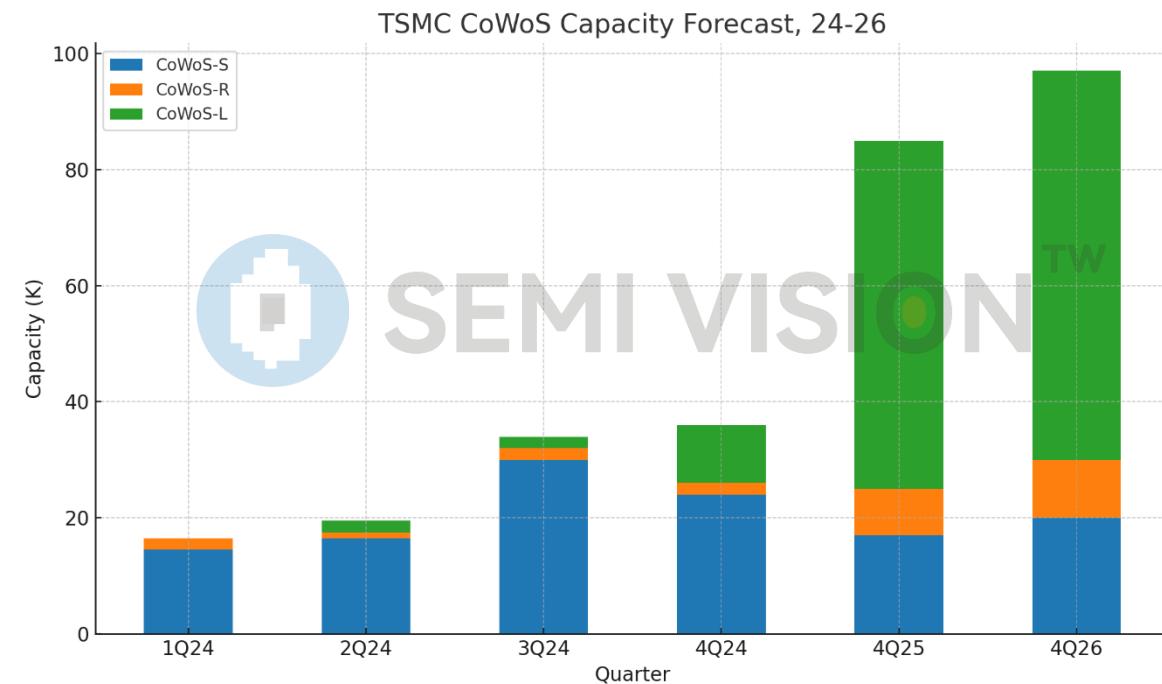
CoWoS®-L is one of the chip-last packages on the CoWoS® (Chip on Wafer on Substrate) platform. It combines the merits of CoWoS®-S and InFO (Integrated Fan-Out) technologies to provide the most flexible integration using an interposer with a Local Silicon Interconnect (LSI) chip for die-to-die interconnect and RDL layers for power and signal delivery.

Key CoWoS®-L features include:

1. LSI chips for a high routing density die-to-die interconnect through multiple layers of sub-micron copper lines. LSI chips can feature a variety of connection architectures, e.g., System on Chip (SoC)-to-SoC, SoC-to-chiplet, SoC-to-High Bandwidth Memory, within each product, and can be used repeatedly in multiple products. The corresponding metal types, layer counts, and pitches align with the offering from CoWoS®-S.
2. A molding-based interposer with a wide pitch of RDL layers on the front-side, back-side and Through InFO Via (TIV) that delivers signal and power provides a low loss of high frequency signals during high-speed transmission.
3. The ability to integrate additional elements, such as stand-alone embedded Deep Trench Capacitors, underneath the SoC die to improve power management.



[https://3dfabric.tsmc.com/chinese/dedicatedFoundry/technology/cowos.htm?fbclid=IwY2xjawGyVXNleHRuA2FlbQlxMAABHeuA1ZL4DtZyzFTu6xKCWsIEJNB2LzykWbiYnsekfAWkRU9X03ht8XzJJg\\_aem\\_a-F6yiXG9WZepvWM6Q3N2Q](https://3dfabric.tsmc.com/chinese/dedicatedFoundry/technology/cowos.htm?fbclid=IwY2xjawGyVXNleHRuA2FlbQlxMAABHeuA1ZL4DtZyzFTu6xKCWsIEJNB2LzykWbiYnsekfAWkRU9X03ht8XzJJg_aem_a-F6yiXG9WZepvWM6Q3N2Q)



CoWoS-R primarily relies on RDL (Redistribution Layer) processes and can achieve the same interposer area as CoWoS-L. However, CoWoS-R faces challenges related to warpage due to material properties of CTE (Coefficient of Thermal Expansion). As a result, the CoWoS-R process is more suited for inference chips, such as AWS chips.

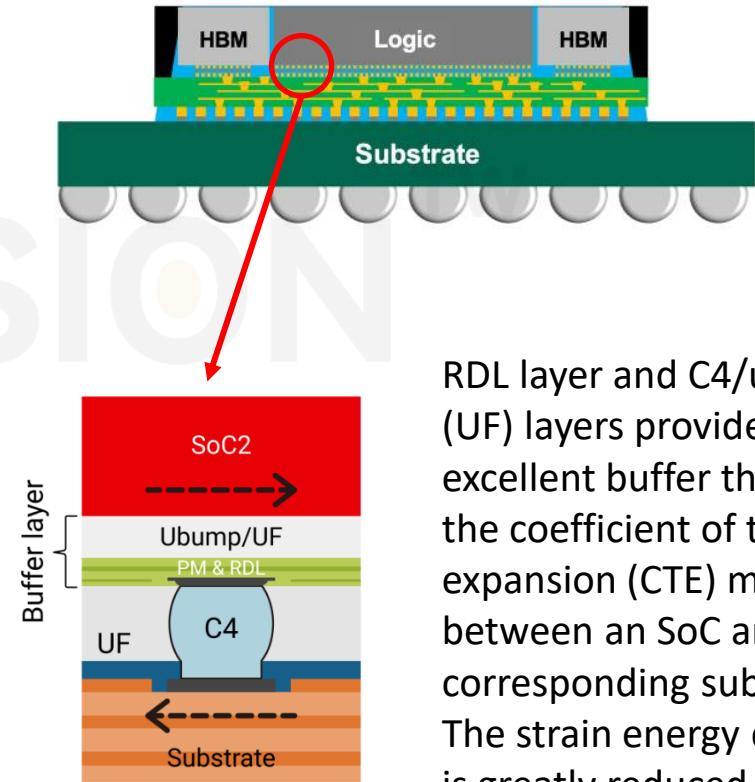
## COWOS-R TECHNOLOGY

### ROADMAP



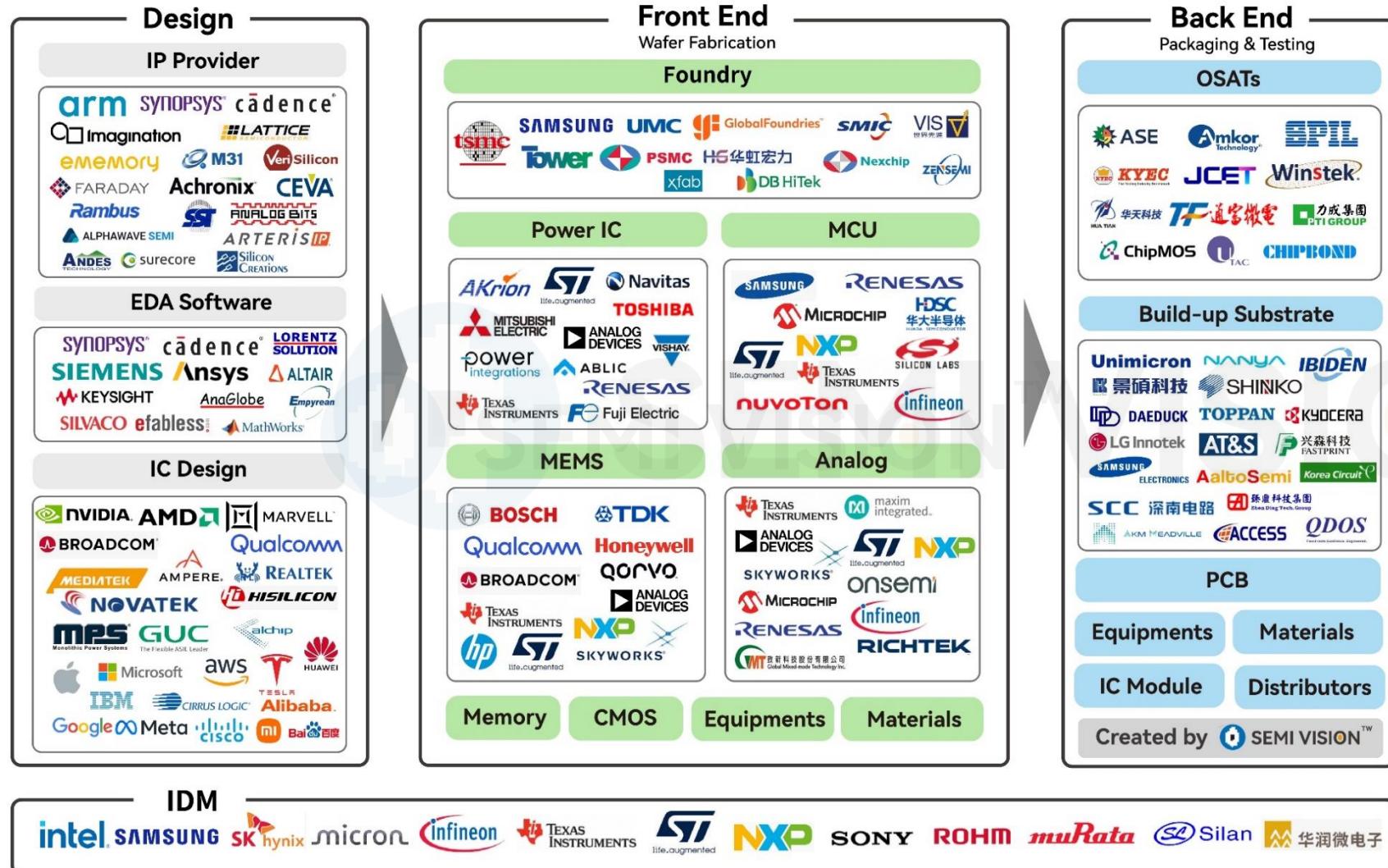
Organic interposer (CoWoS-R) AP technology is one of the most promising heterogeneous integration platforms for HPC and AI applications. Chiplets, HBM, and passives can be integrated into an organic interposer with excellent yield and reliability. CoWoS-R provides low RC interconnect with good signal isolation and design scalability. The new organic interposer CoWoS-R generation integrates both a large amount of high density IPD and fine pitch Si-based connection block for convenient IP migration. The roadmap of CoWoS-R is presented in the table.

	1st Gen	2nd Gen	3rd Gen	4th Gen	5th Gen	6th Gen
Status	In Production	In qualification	LVM	3Q24	1Q25	4Q25
Reticle size	X1.4	X1.7	2x 1.6	X3.3	X4	X5.5
Components	1SoC+2HBM2	1SoC+ 8 IO Die	1SoC + 4 HBM	4 SoC + 8 HBM3	1SoC + 4 Chiplets 12 HBM3(Hi 36 Gb)	4 SoC + 12 HBM3/4
L/S	2/2 μm	2/2 μm	2/2 μm	2/2 μm	2/2 μm	2/2 μm
of Layers	6L	6L	6L	6L	8L	9L
Substrate size	55 mm 55 mm	90 mm 55 mm	100 mm 72 mm 78 mm 96Gb	72 mm 100 mm 100 mm 192Gb	100 mm 98 mm 95 mm 288Gb	98 mm 576Gb



RDL layer and C4/underfill (UF) layers provide an excellent buffer thanks to the coefficient of thermal expansion (CTE) mismatch between an SoC and the corresponding substrate. The strain energy density is greatly reduced in C4 bump area.

# Semiconductor Ecosystem Overview



The semiconductor industry is large and complex, requiring thousands of companies within the supply chain to work together to drive the industry forward.

**Now**

SEMI VISION

## Foundry



OSAT

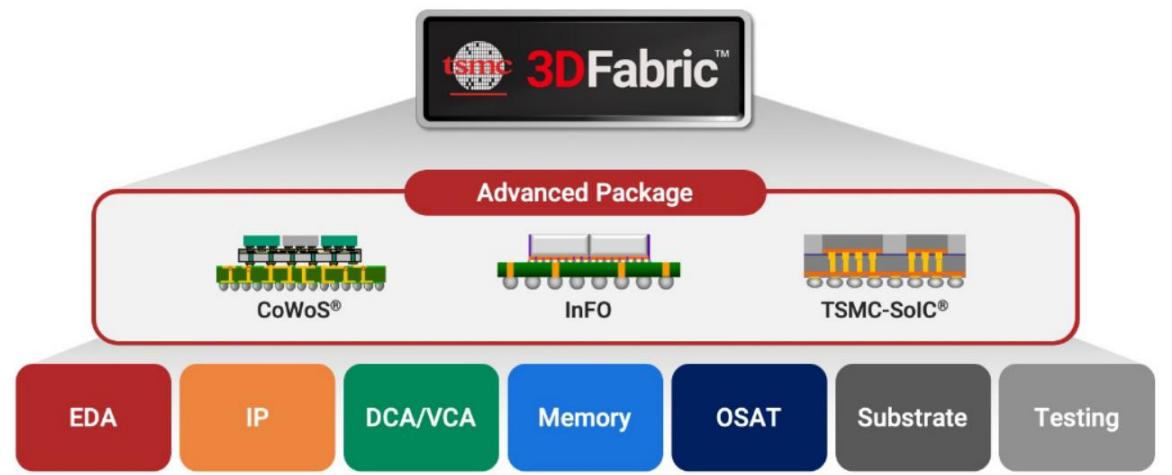
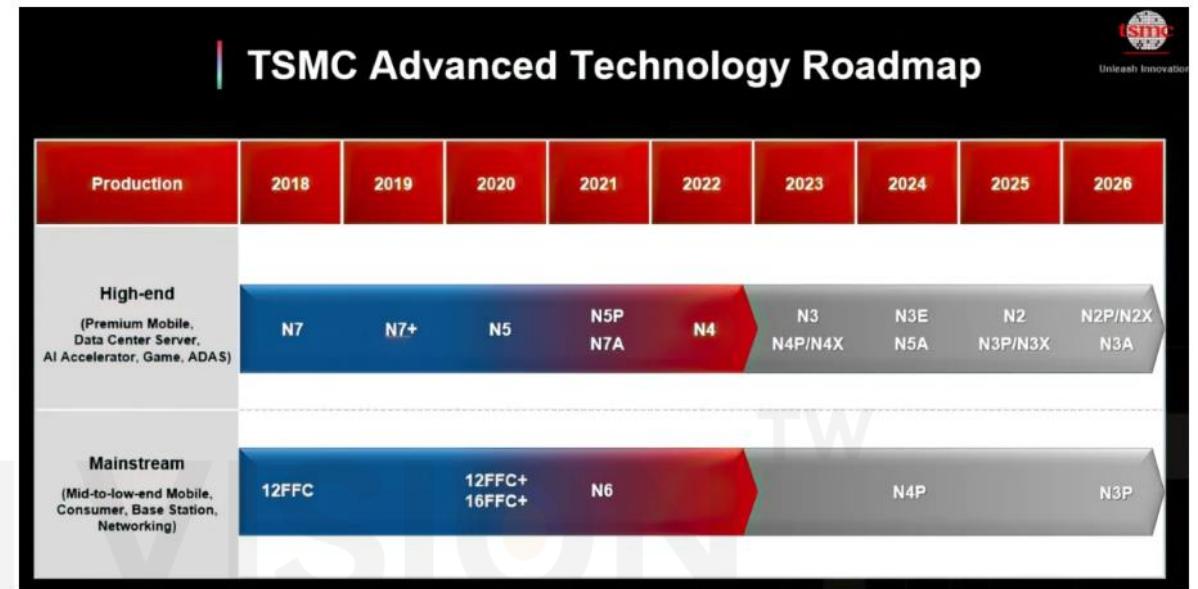
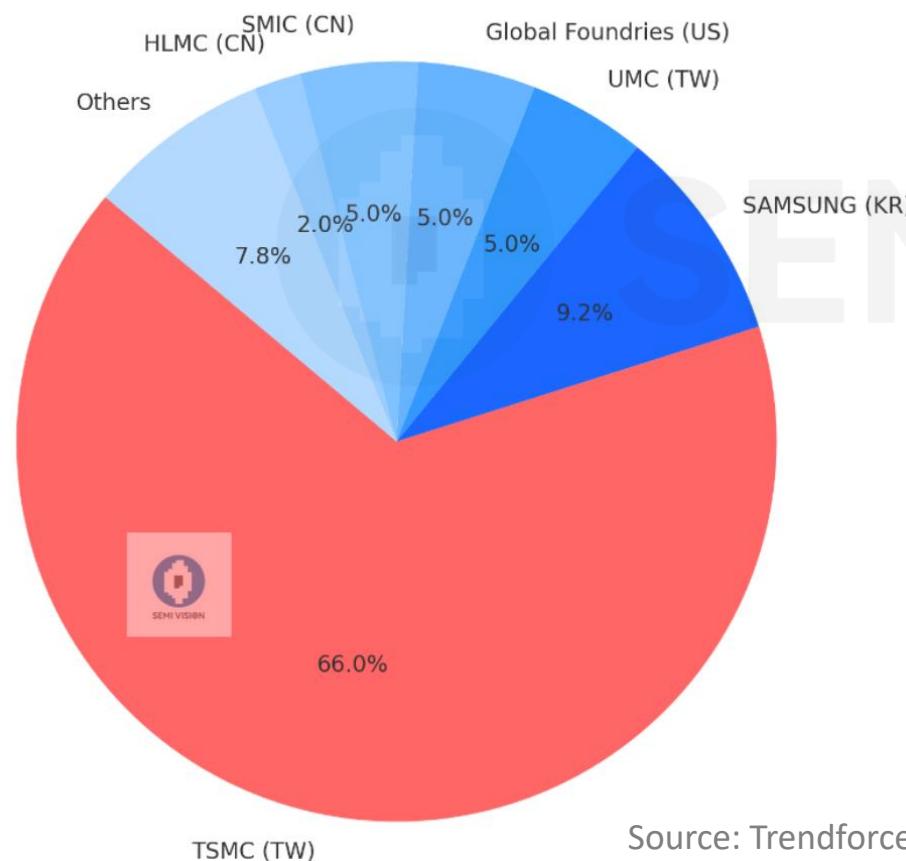


## IC Substrate



- 70% of the foundry market share is in Taiwan.
- TSMC, UMC, VIS, PSMC in Taiwan

## 2025 Major Wafer Foundries Market Share by Companies



Source: tsmc

## 3D Optical Engine (OE) for Next-Gen Communication

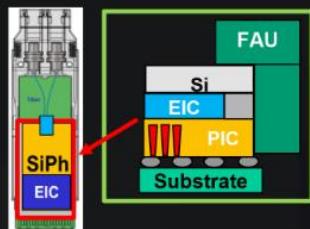


- Optics is crucial for rapid and reliable data transmission and lowering network power consumption for AI
- EIC-on-PIC stacked using the SoIC-X process (COUPE™\*) offers unparalleled interconnect density while maintaining optimal system power
- We will enable COUPE in pluggable in '25, followed by COUPE on substrate in a CoWoS CPO with a 2x reduction in power and a 10x reduction in latency in '26
- COUPE on CoWoS interposer for another 5x reduction in power and 2x reduction in latency is being explored

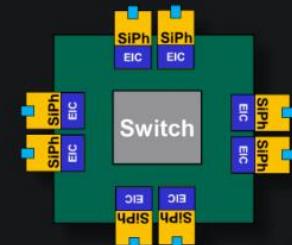
- Pluggable (OSFP\*\*)
- 1.6Tbps OE on Substrate in 2025

- CPO with Switch
- 6.4Tbps OE on Substrate in 2026

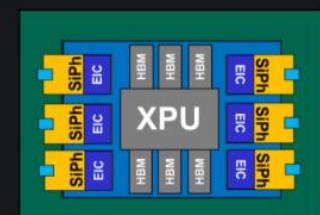
- CPO with XPU
- 12.8Tbps OE on Interposer in Pathfinding



Power: 1X  
Latency: 1X



< 0.5X  
< 0.1X



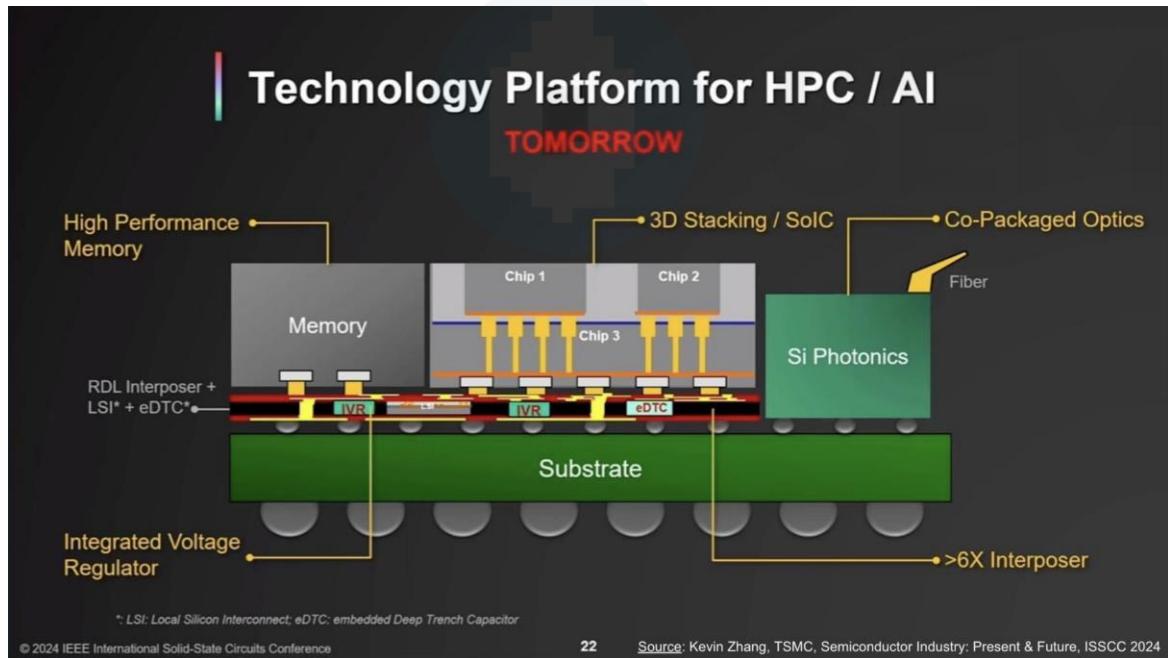
< 0.1X  
< 0.05X

\* COUPE: Compact Universal Photonic Engine

\*\* OSFP: Octal Small Form Factor Pluggable

TSMC's Compact Universal Photonic Engine (COUPE) stacks an electronics integrated circuit on a photonic integrated circuit (EIC-on-PIC) using the company's SoIC-X packaging technology. The foundry says that usage of its SoIC-X enables the lowest impedance at the die-to-die interface and therefore the highest energy efficiency. The PIC itself is produced at a 65nm-class process technology.

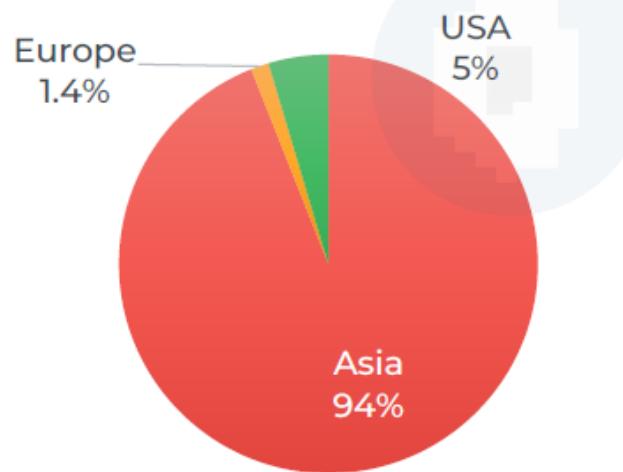
- Optical Engine (PIC bonded to EIC ) integrated to advanced package , such as CoWoS-L
  - PIC Foundry Players: TSMC, UMC, TOWER, Global Foundry, Imec , Intel
  - OSAT Player: ASE , Amkor, TSMC (COUPE Platform)
  - COUPE Platform provide high complexity integration of OE ( Couper , Microlens , Package)
  - Nvidia also focus on OE , HBM and GPU integrated to interposer
  - Lightmatter develop optical chip for OIO (optical I/O) and package completed in ASE and Amkor



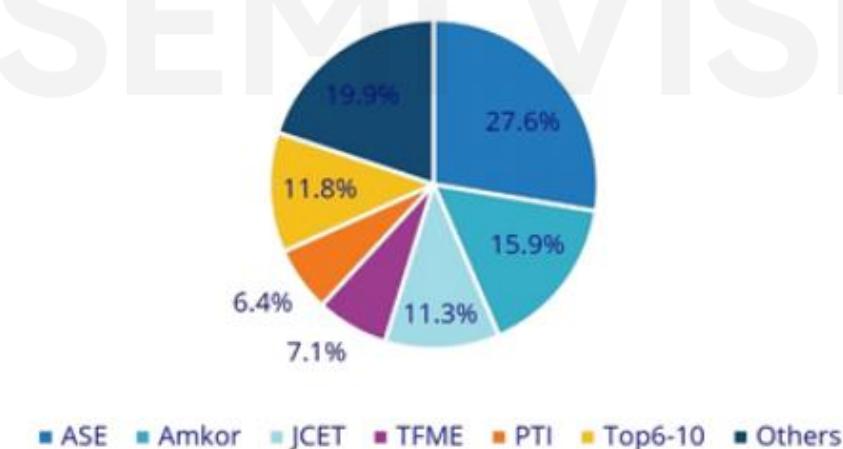
**The silicon photonic chip on Lightmatter's PCIe card receives its light source through optical fibers.**

- Currently, over 90% of the AP revenue is generated in fabs in Asia
- 47% of the OSAT market share is in Taiwan.

Advanced Packaging revenue market share by fab location\* - 2022



Worldwide Top 10 OSAT Companies, 2022 Market Share



## OSATs



Source: Yole, IDC

- ASE provide VIPack platform for advanced package
- ASE focused on CoWoS-S and R development.
- Difficulty of CoW is higher Os, due to ability of lithography and bonding steps.
- CoWoS like flow is very important for OSAT developing.
- ASE is actively advancing 2.5D and 3D packaging technologies, with significant investments in 3D packaging at its K21 and K22 sites.
- Additionally, ASE is expanding production capacity at its SPIL.

## VIPack™: Six Technology Pillars



I	II	III	IV	V	VI
FOPoP	FOCoS	FOCoS – Bridge (Embedded)	FOSiP	2.5D/3D IC	Co-Packaged Optics
Integrated Design Ecosystem					



FOCoS	Fanout	Package	REL Conditions	Results
	23 x 36	62.5x62.5	MSL4 + TCG850x	Qualification Passed
			MSL4 + uHAST264hrs	
			HTST1000hrs	
	24 x 33	57.5x57.5	MSL4 + TCG850x	Qualification Passed
			MSL4 + uHAST264hrs	
			HTST1000hrs	

## ASE Advanced FOCoS Solutions

Technology	FO Chip First		FO Chip Last		FO Bridge	
	Packaging Type	ASE FOCoS-CF	TSMC InFO_R /SoW	ASE FOCoS-CL	TSMC CoWoS_R	ASE FOCoS-B
Structure						
Status	HVM (2016)	HVM (2018)	Qualified	Qualified	HVM (2022)	HVM (2021)

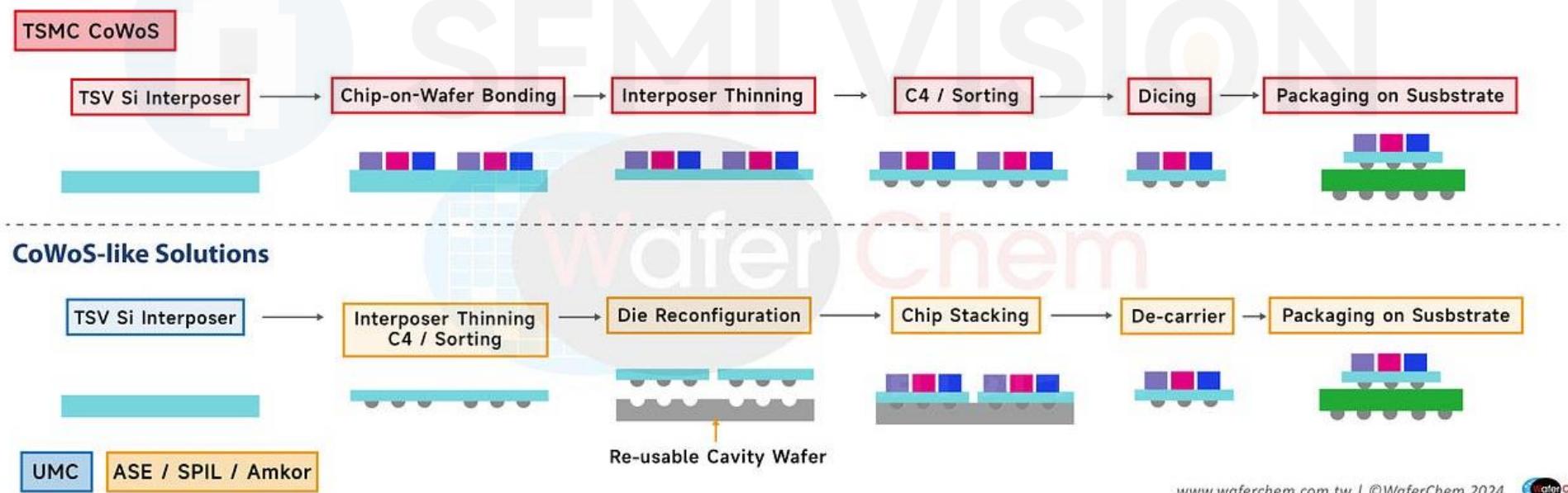
## ASE Advanced 2.5D & 3D Solutions

Technology	2.5D Si TSV		3D			
	Packaging Type	ASE 2.5D Si TSV	TSMC CoWoS_S	ASE 3D - ubump	TSMC SoIC	ASE 3D Hybrid Bonding
Structure						
Status	HVM	HVM	Qualified	Qualified	Development	HVM

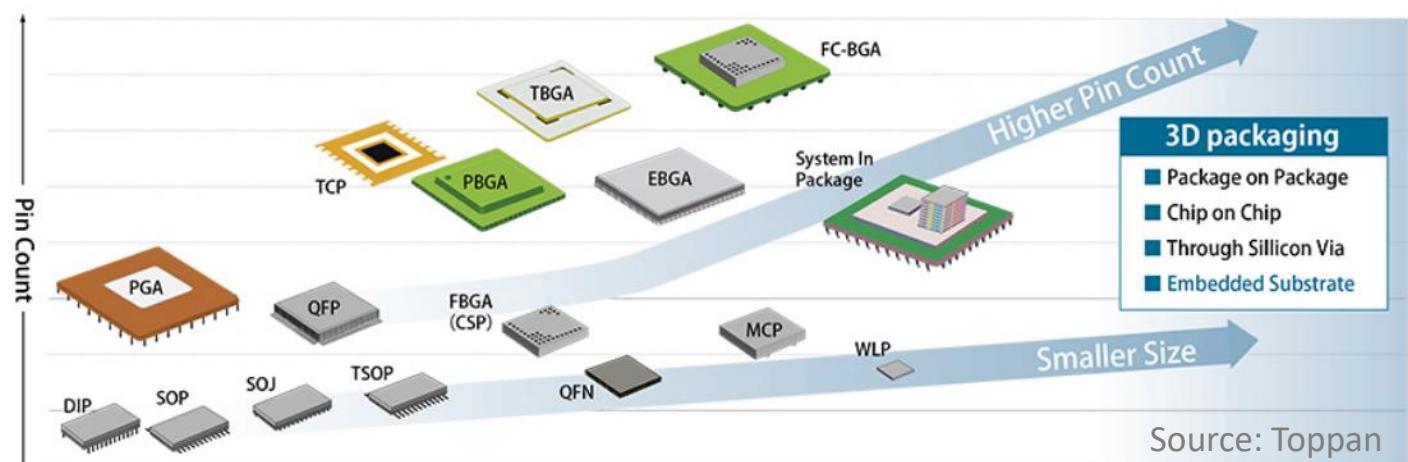
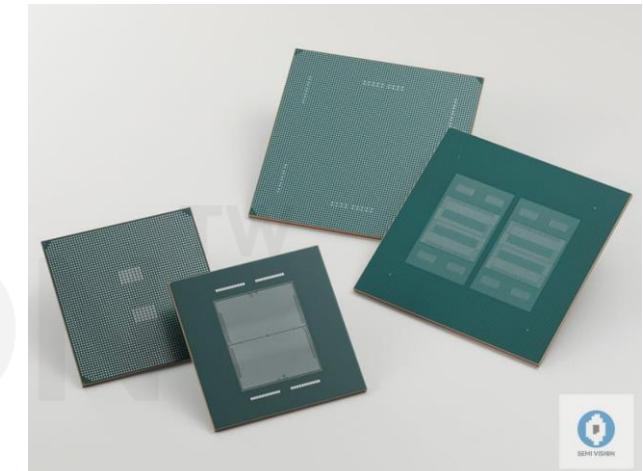
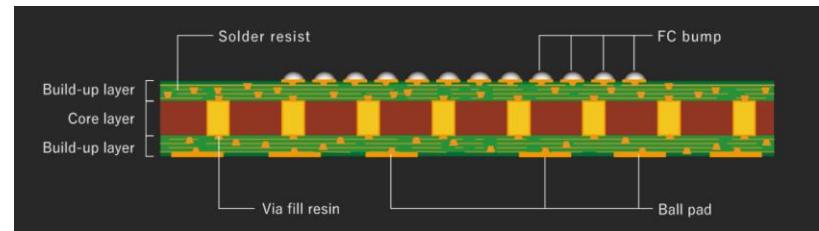
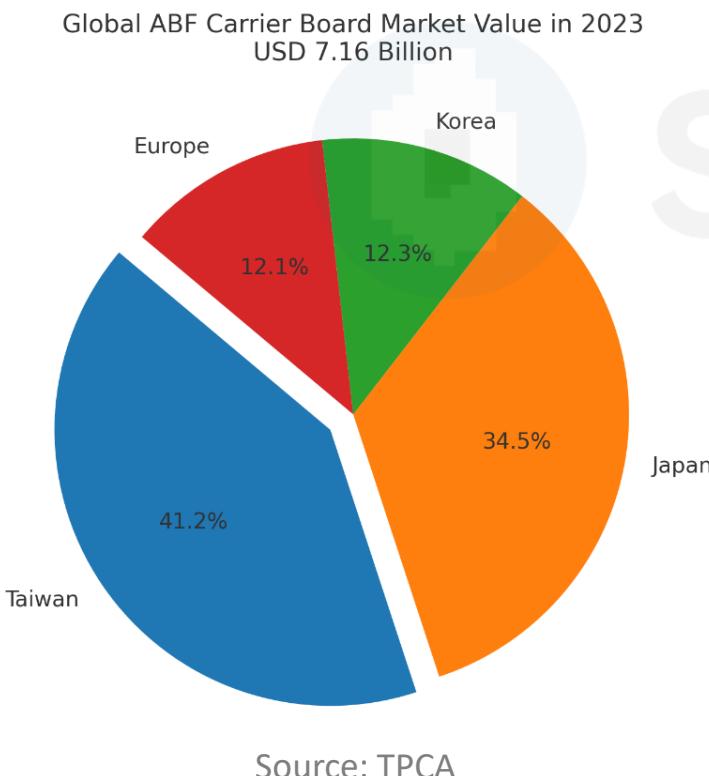
Source: ASE

- Main components in CoWoS Package: RDL layer ( PSPI and PID ) . TSV (Bosch Process) . Bumps (uBump and Cu Pilliar), Bonding (TCB and Hybrid Bonding)
- Any OSAT have many experience in these step, but they face how to control fine pitch and large size of Ai chip due to size of ai chip always larger than tradition chips.
- Material and Semi Equipment are very key to develop CoWoS

## ADVANCED PACKAGING: TSMC CoWoS vs. CoWoS-like Solutions

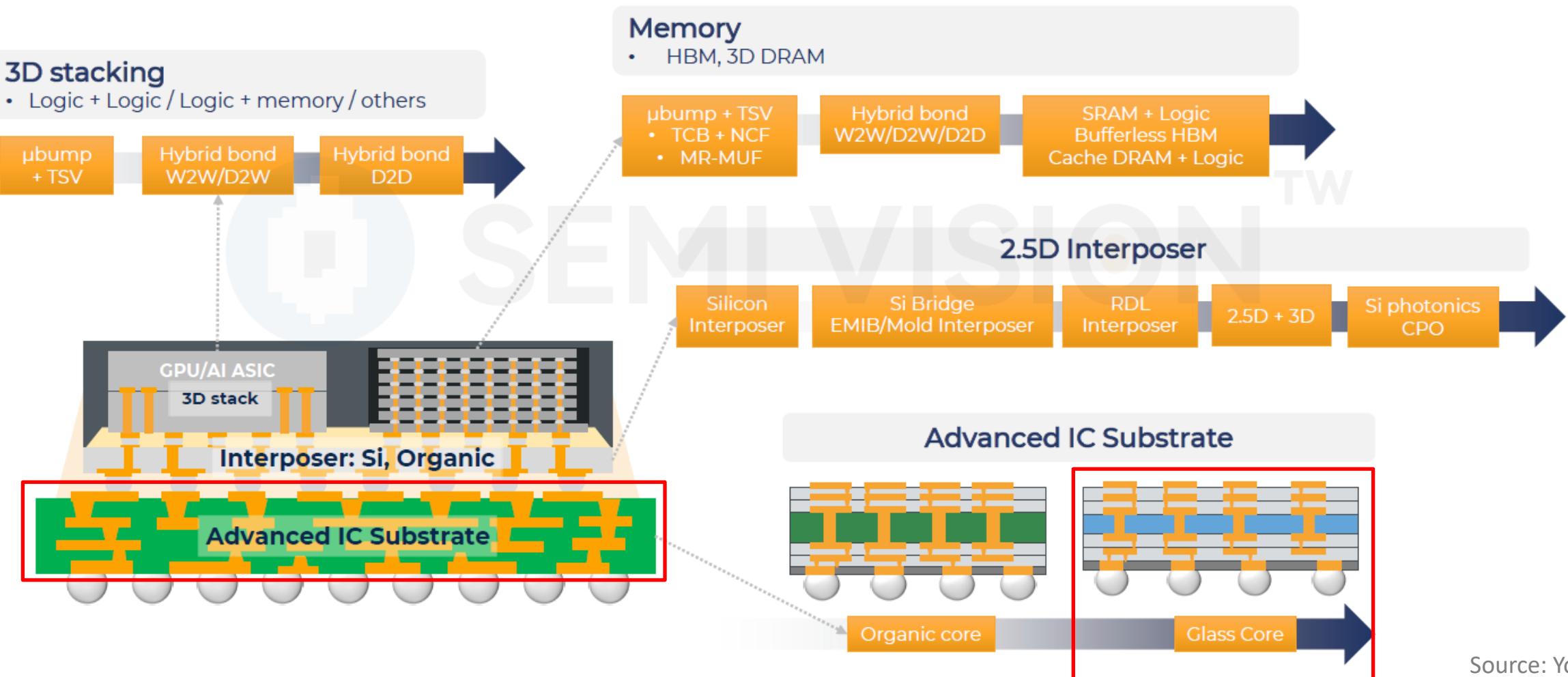


- 41.2% of the IC substrate market share is in Taiwan.
- 34.5% of the IC substrate market share is in Japan.

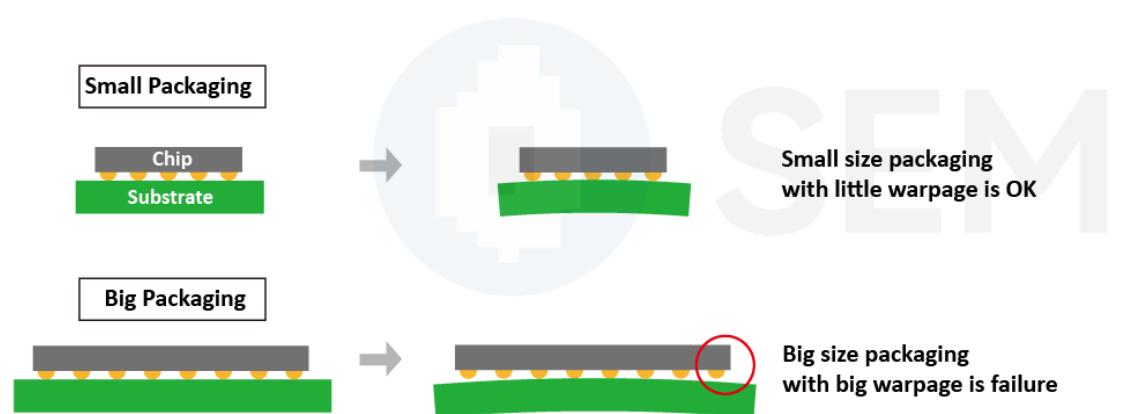


# Why IC Substrate is Important?

- IC substrate is key component in advanced packaging.
- More chips need to be stacked and placed closer together, IC substrate's size is becoming larger.
- New trend of IC substrate: Glass core (less warpage, high density TGV)



- As wafer grinding, the warpage issue is more significant (Small size package verse. Large size package)
- Reduce the stress is very key to improve the CoWoS yield and process window.
- Resonac propose the solution for large size substrate.
- 90% CoWoS's core use Resonac.

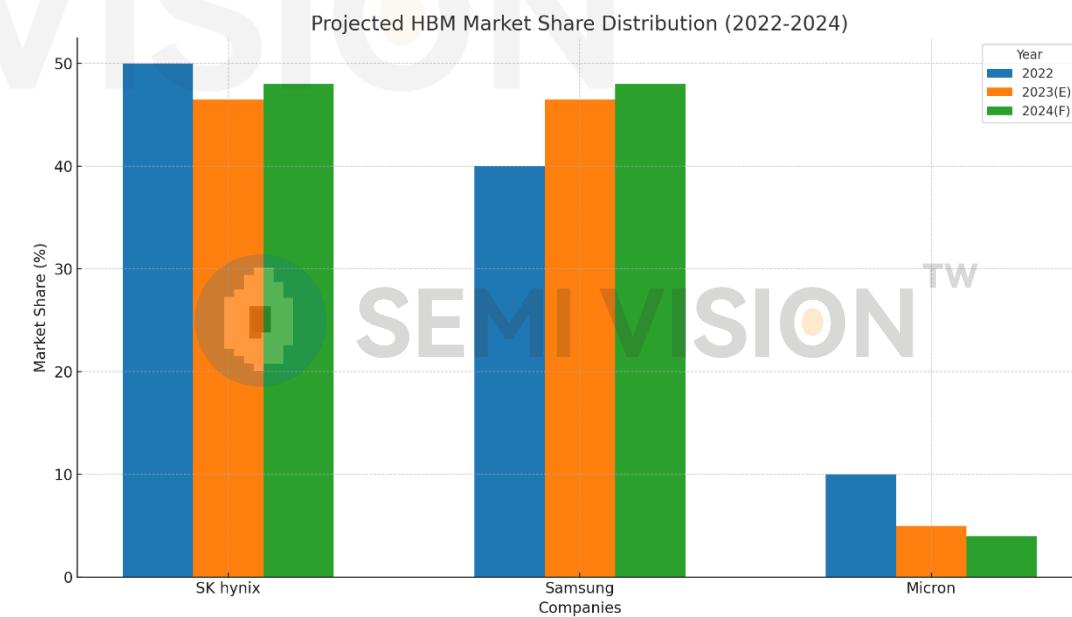
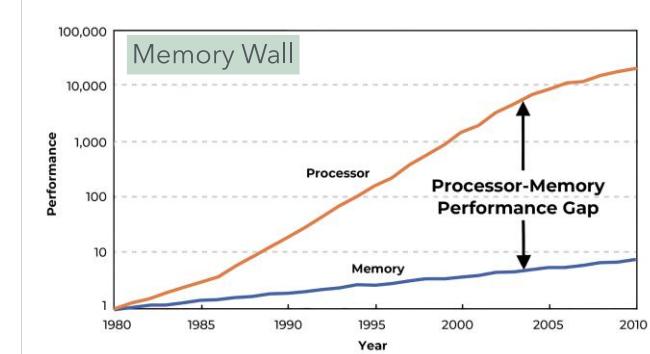


In the CoWoS process, the cores currently used are supplied by Resonac, primarily because Resonac can produce thicker products (1.2mm, 1.4mm, 1.6mm, etc.). A thicker core has greater strength to reduce warpage.

Resonac's proposal for Large Size Substrate			
Challenge in Semiconductors	Requirement To Substrate	Breakthrough During Substrate Process	Proposal / Solution From Material Stand-point
Large body size	Low Warpage High Yield	Warpage Control Shrinkage Control	Low CTE, High Modules Shrinkage Accuracy
High density circuit	Narrow pitch	Fine L/S Fabrication Narrow pitch TH	High Drill-processability
Electrical property	Signal Integration	Pattern, PKG Design	Low Dk/Df
Power delivery	More efficiency Power Delivery	Embedded Multi-layer core (MLC structure)	Super FLAT Core High Resin flow Preprep

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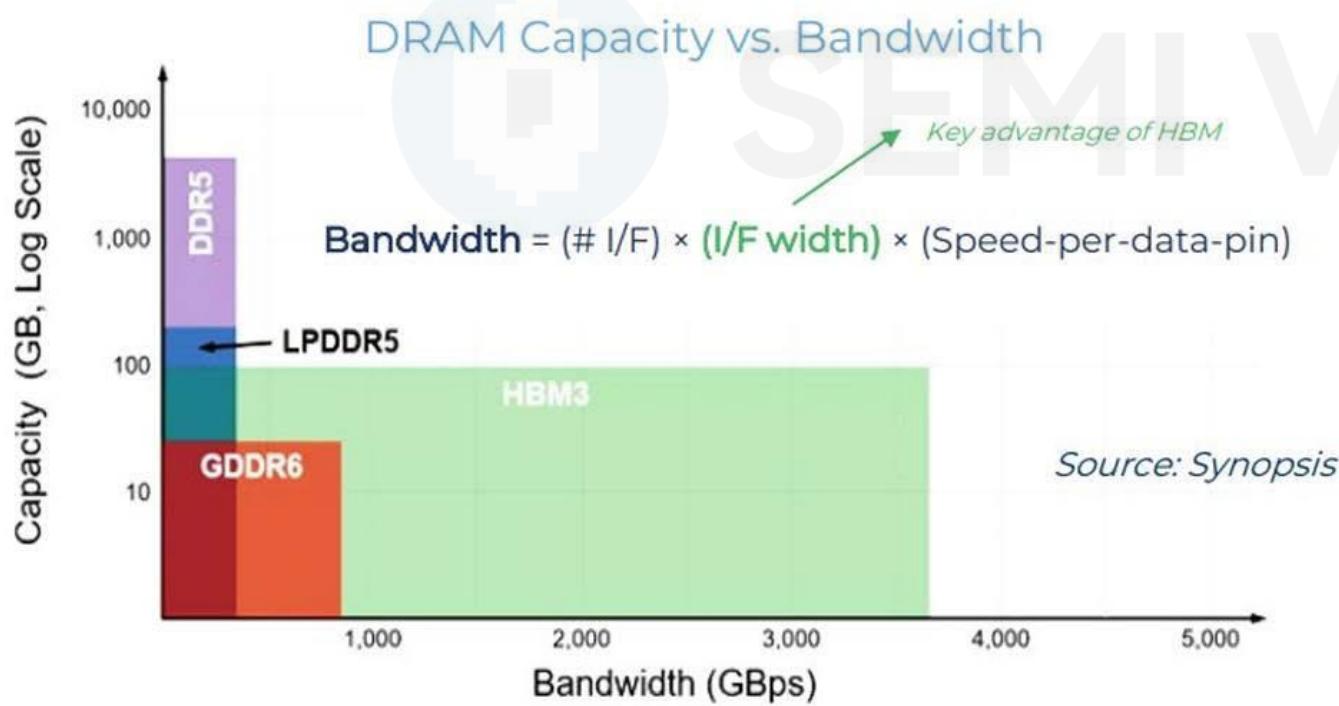
- HBM is a critical development trend for AI chips, as it provides high-bandwidth access speeds, depending on the design of the base die.
- The development of HBM primarily focuses on increasing the stack layers (from 12Hi to 16Hi) and adopting advanced packaging materials, such as MR-MUF (Mass Reflow -Molded Underfill).
- Hybrid Bonding will be adopted at HBM4 and HBM5
- Memory Wall : The Bandwidth gap is very high between processor and memory
- Base die develop depended on TSMC advanced device logic nodes, 12 nm and 5 nm.
- HBM players : SKHynix , Samsung ,Micron



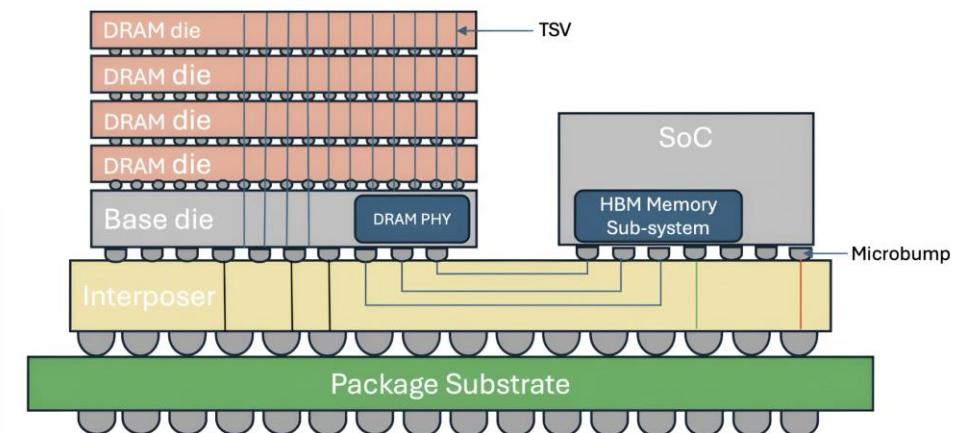
# HBM Bandwidth Calculation

**Bandwidth (GBps):** Total data throughput (in gigabytes per second).

- **# I/F (Interfaces):** Number of interfaces/channels in the memory.
- **I/F width:** Width of each interface (number of data pins per interface).
- **Speed-per-data-pin:** Data rate per pin (in GBps).



	HBM2	HBM2E	HBM3	HBM3E	HBM4
Year	2016	2018	2022	2023	2025
I/Os	1024	1024	1024	1024	2048
Bandwidth (BW)	256 GB/s	460 GB/s	819 GB/s	1+ TB/s	1.5+ TB/s
Interface Width	X64/8 Ch	Backward compatible Additional Features	Not backward compatible with HBM2/2E	Backward compatible to HBM3 Additional Features	Not backward compatible to HBM3

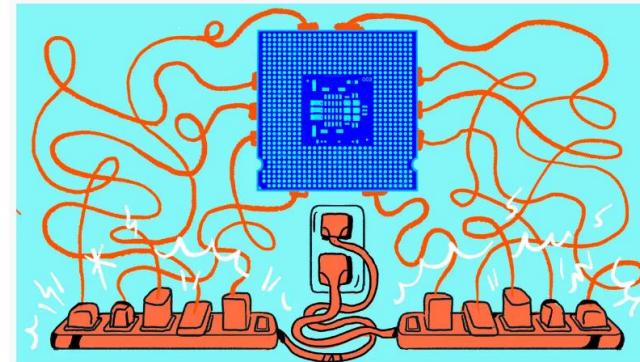


Source: Yole

# Future



## Power issue



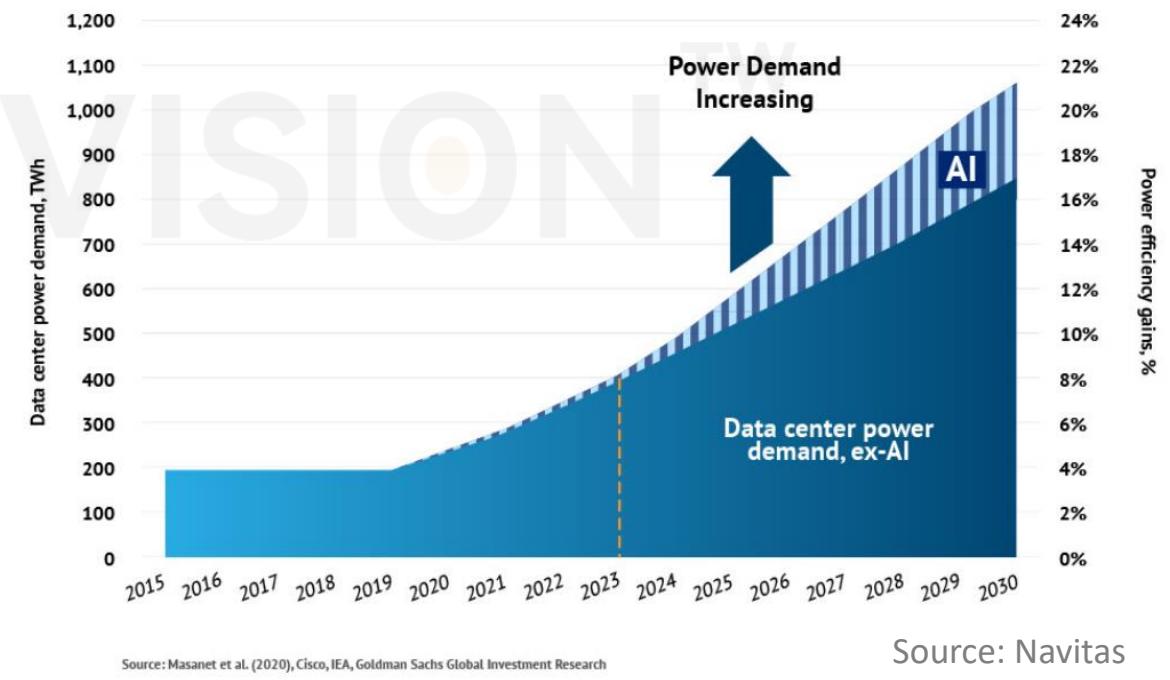
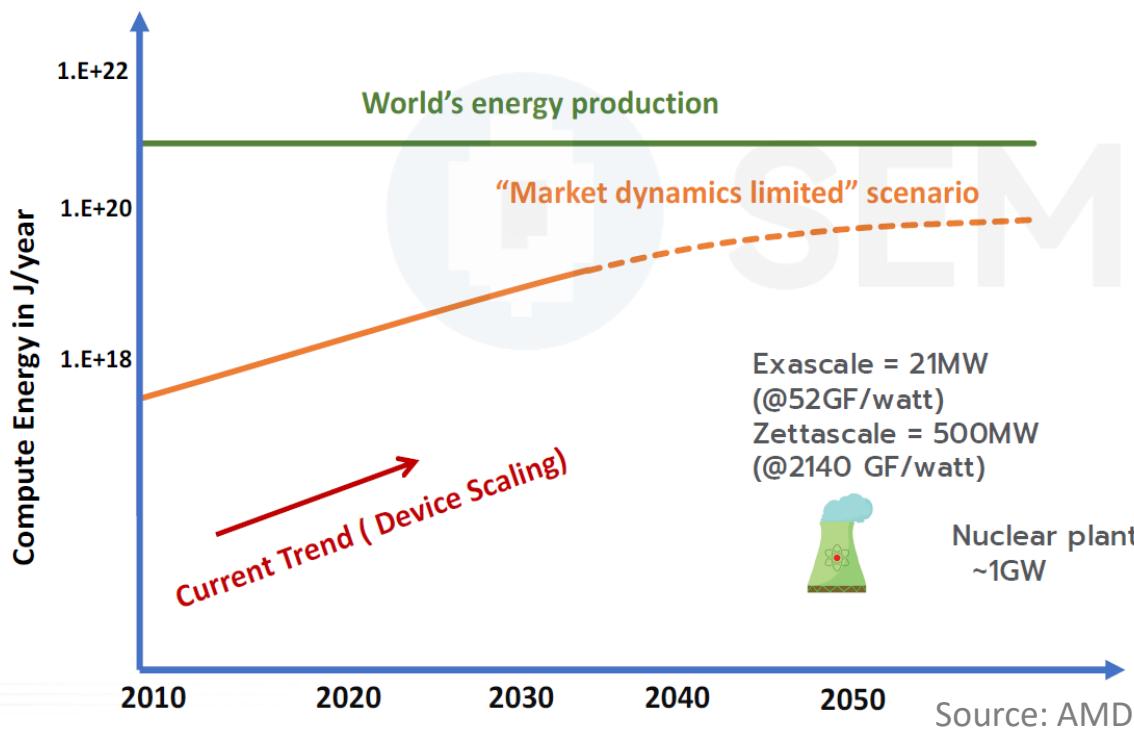
## Geopolitics issue



## CPO issue



- AI drives explosive growth in data processing and computing power.
- The rate of data center growth has accelerated in recent years, with 7,000 facilities built or in construction.
- The state of AI: Global energy consumption from data centers is forecast to break 1 Petawatt-hour by 2026

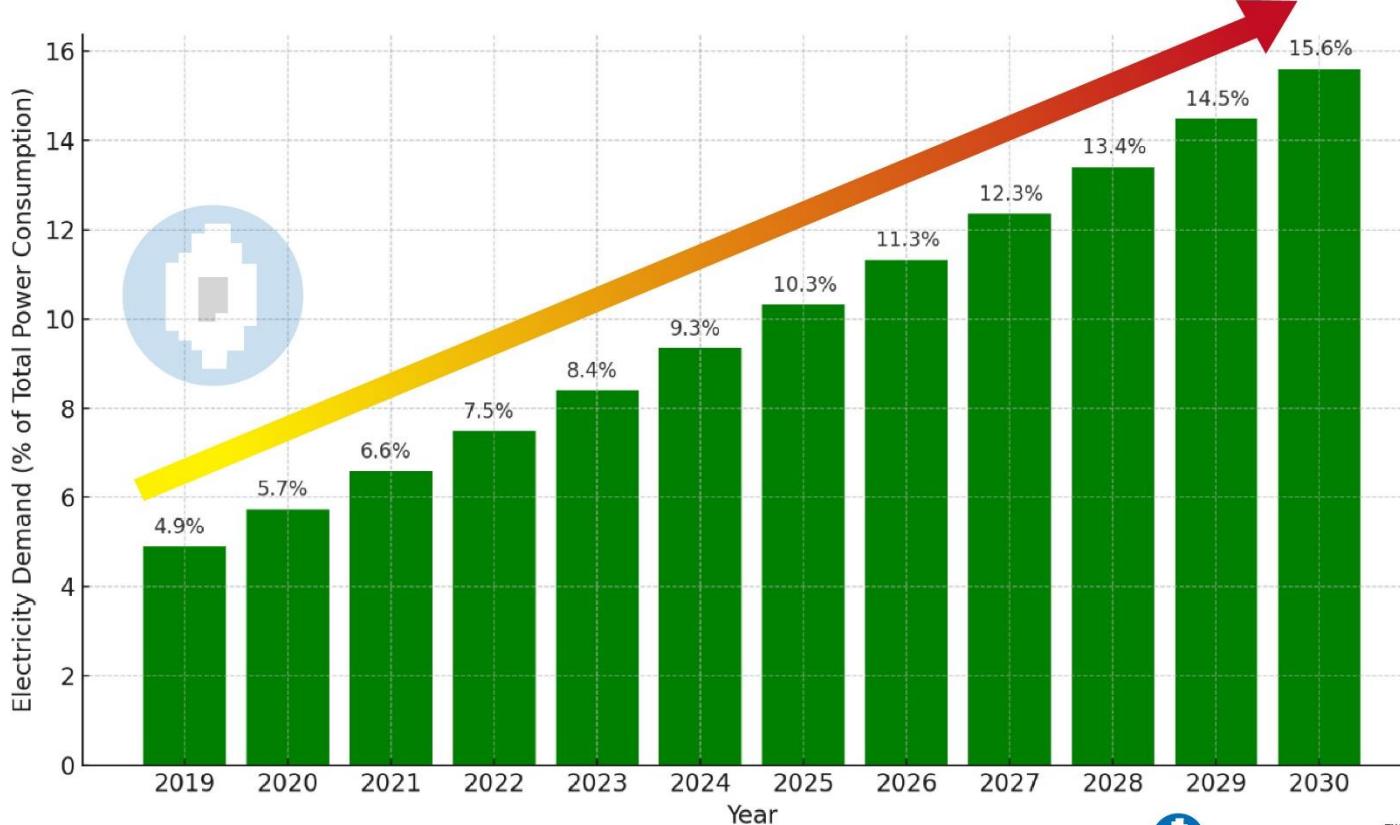


Source: Masanet et al. (2020), Cisco, IEA, Goldman Sachs Global Investment Research

<https://navitassemi.com/the-state-of-ai-global-energy-consumption-from-data-centers-is-forecast-to-break-1-petawatt-hour-by-2026-how-is-the-semiconductor-industry-responding/>

- TSMC used 247,75 GWh electricity in 2023
- 247,750 GWh electricity = 50 million people for household use

## TSMC'S SHARE OF TAIWAN ELECTRICITY CONSUMPTION (2019-2030)

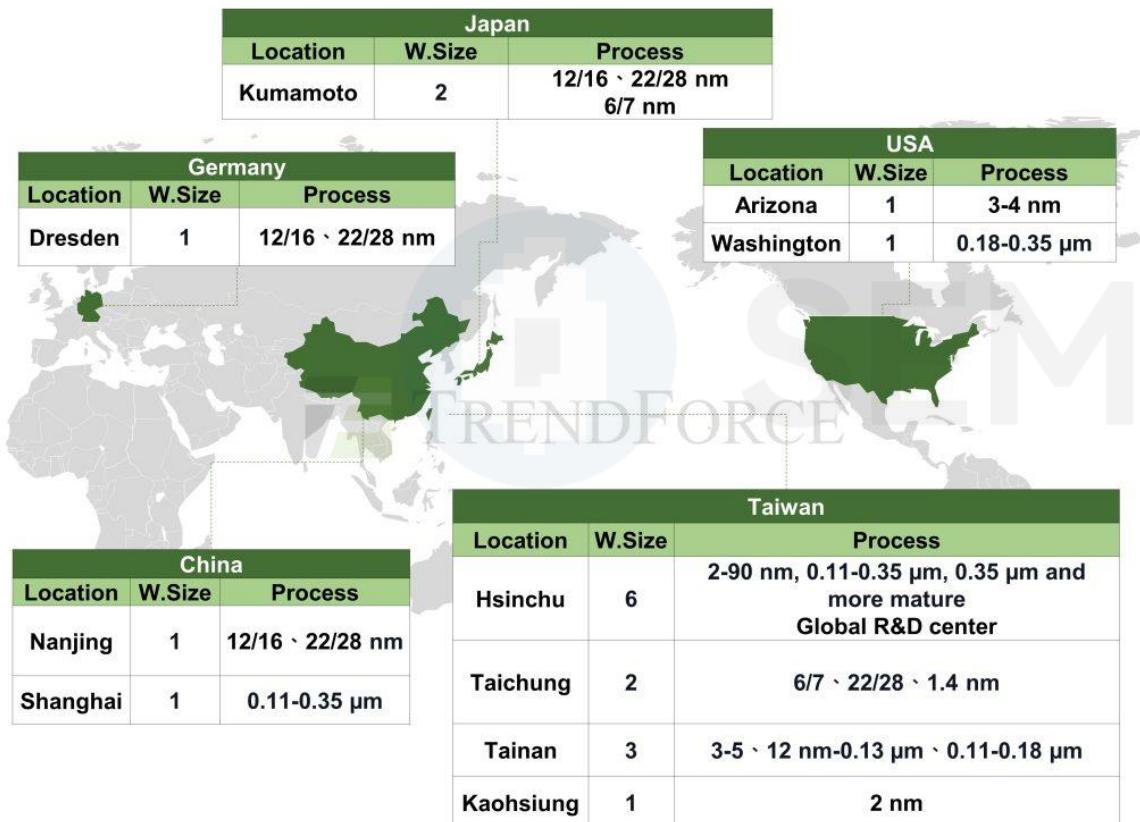


ASML



The production of each advanced chip requires over 4,000 steps, and a single fab contains hundreds of tools. EUV equipment accounts for about 11% of the fab's total electricity consumption, with the remaining power used by other tools, HVAC systems, facility systems, and cooling equipment.

## TSMC's Latest Global Production Capacity Layout



 TRENDFORCE

**Morris Chang said "TSMC "has truly become a highly contested battleground."** 2024 Oct.

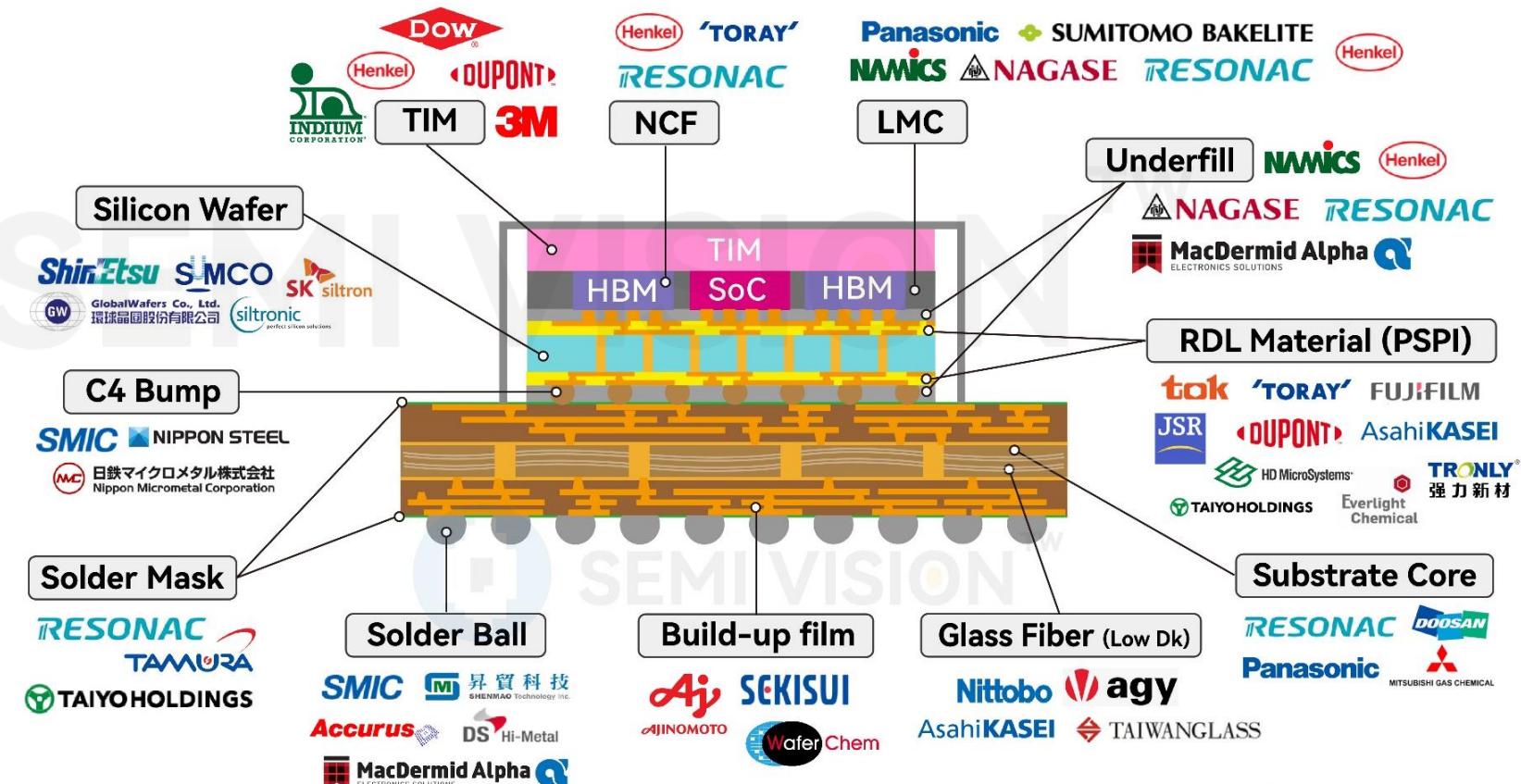
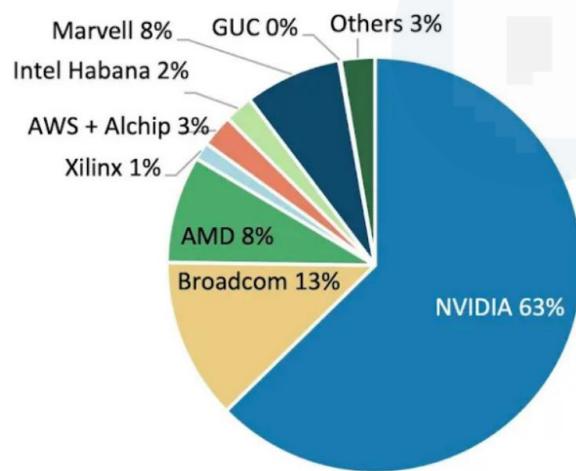
In semiconductors, especially advanced processes, globalization is dead, and so is free trade. In this environment, their challenge is to continue striving for growth.



# CoWoS Supply Chain

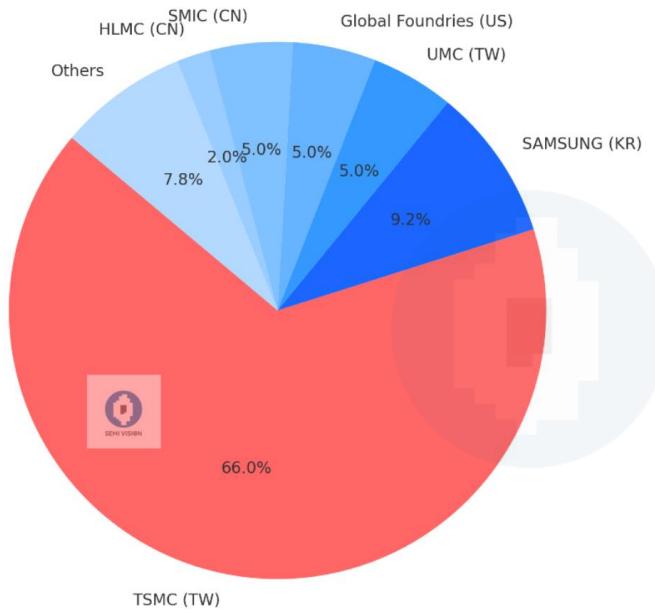
- NVIDIA is projected to dominate 63% CoWoS capacity demand in 2025.
- 90% CoWoS PKG materials from Japan.
- 100% CoWoS PKG in Taiwan but with low material self-sufficiency -> high risk

Global CoWoS capacity demand mix by key customer, 2025e



Created by SEMI VISION™

- According to page 6, 70% of the foundry market share is in Taiwan.
  - 90% Fab equipment from overseas.
  - Low equipment self-sufficiency, high risk



APPLIED MATERIALS

TEL

ASML

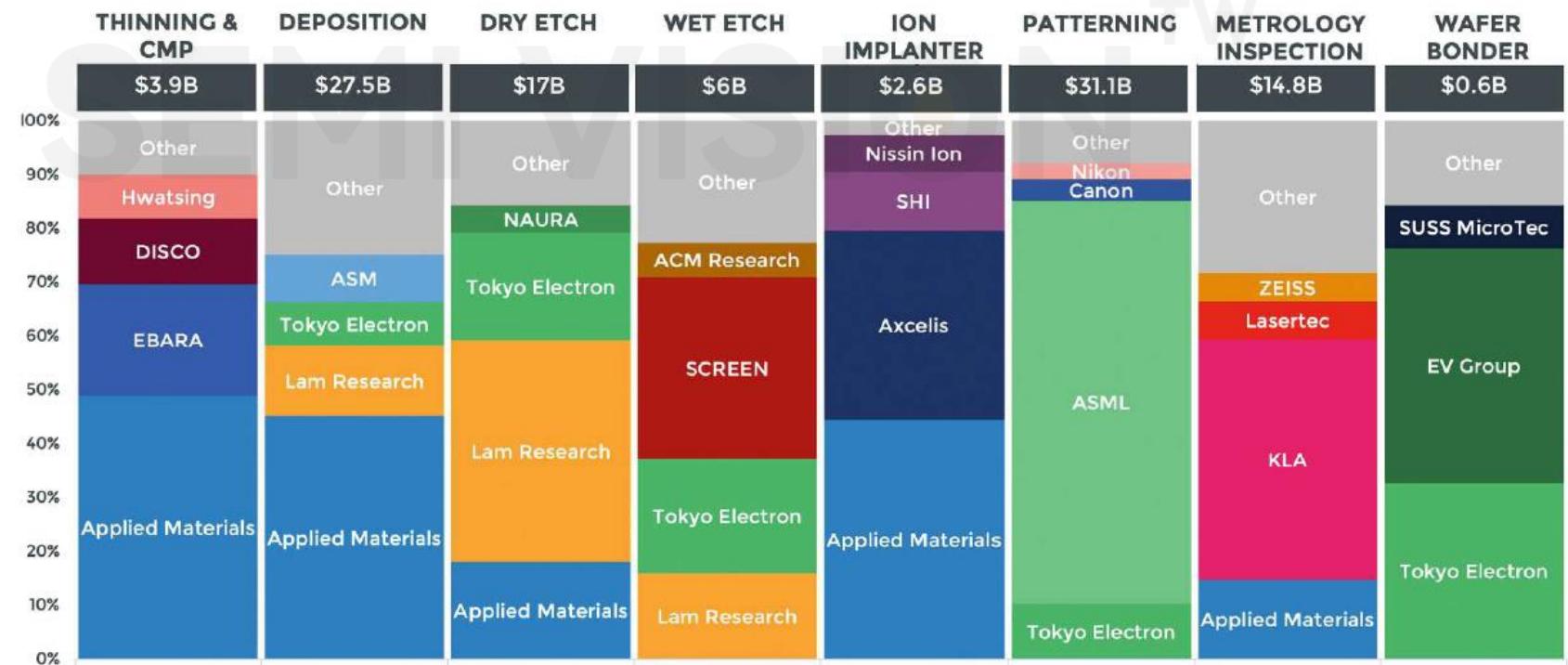


Lam  
RESEARCH

KLA +

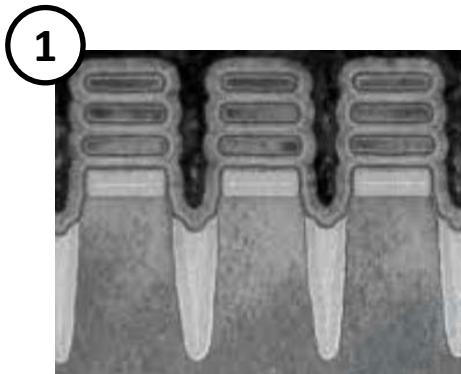
## 2023 WAFER FAB EQUIPMENT VENDOR MARKET SHARE – BY TYPE OF EQUIPMENT

Source: Status of the Wafer Fab Equipment Industry report, Yole Intelligence, 2024



Detailed market shares are available in Yole Group's Status of the Wafer Fab Equipment Industry report.

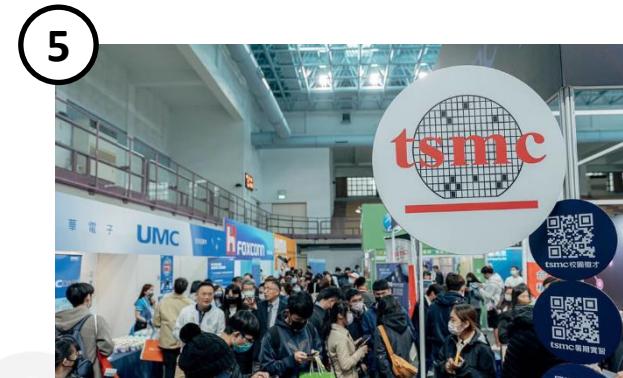
# 5 Semiconductor Industry Challenges in the Future



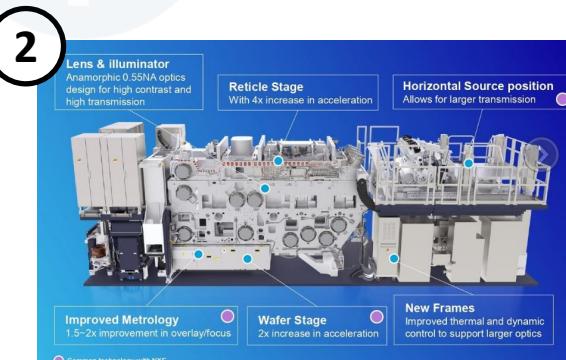
Process Technology Limits



Energy Efficiency



Human Resources Shortages

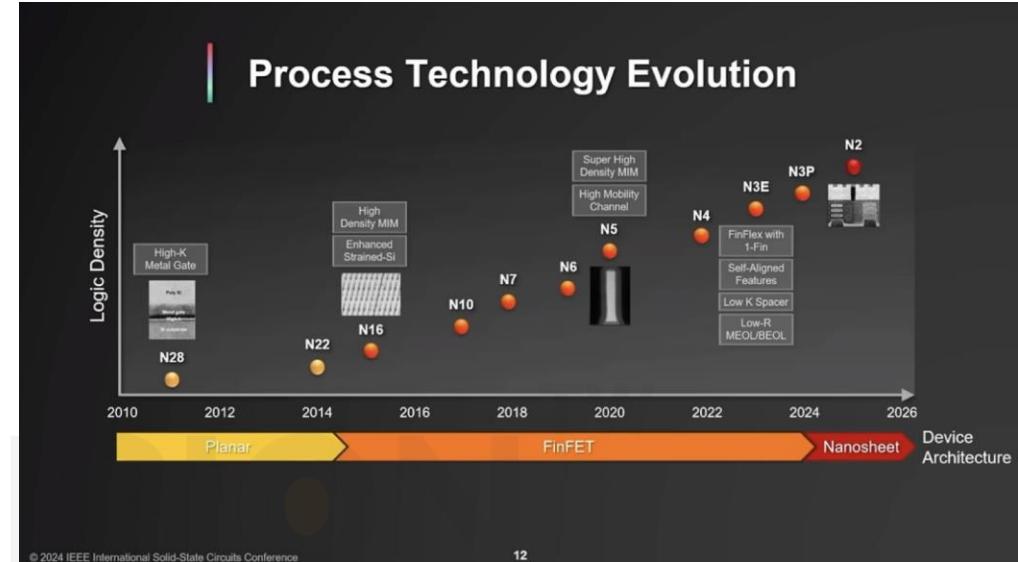
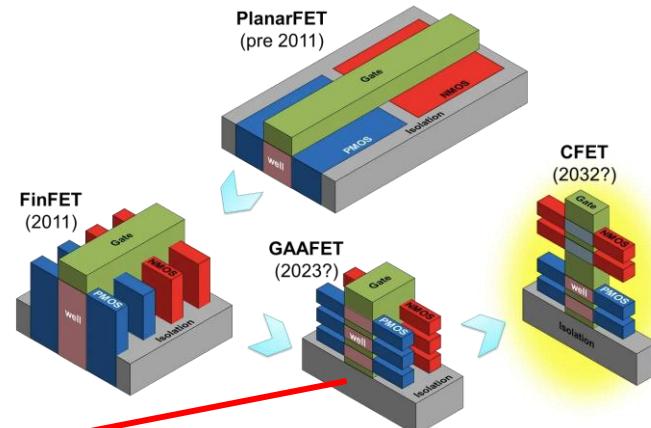
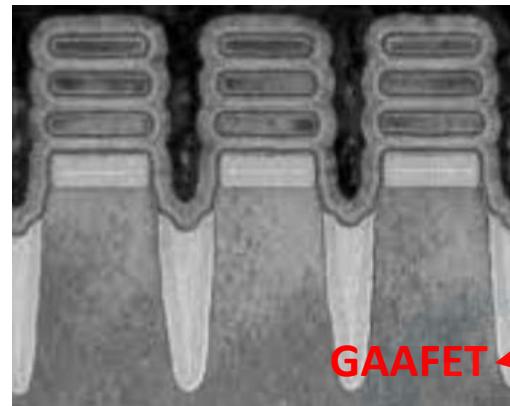


High Costs and Investments



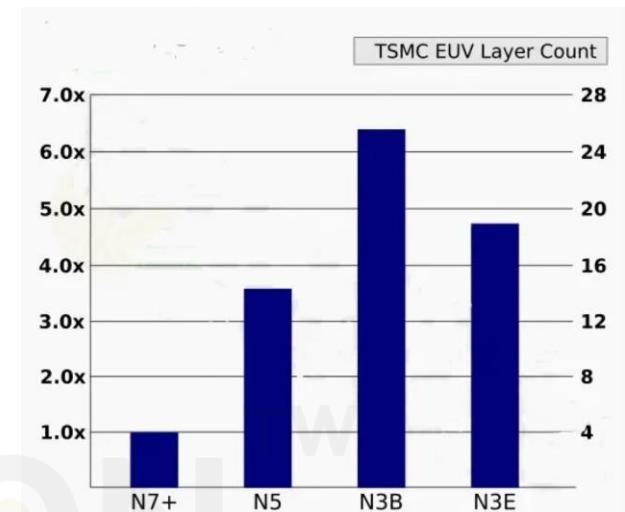
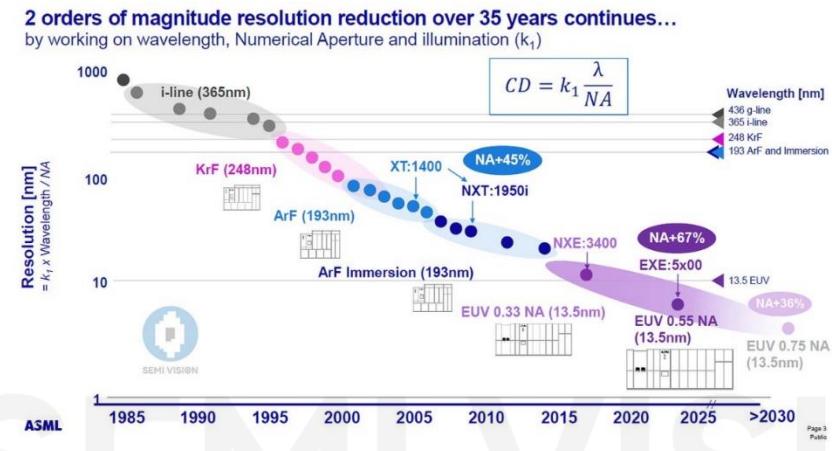
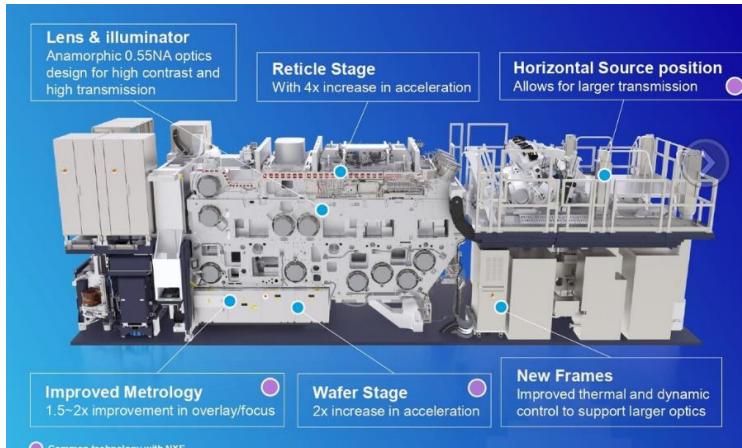
Supply Chain Stability

# Challenge 1: Process Technology Limits



- TSMC proposed N2 device adopt GAA (Gate around all ) FinFET structure.
- CMOS Scaling : Planar CMOS → FinFET → GAA FinFET → CFET ( P and N MOS stacking)
- Higher complexity of CMOS Structure, increase the difficulty of device process development
- Advanced chip design must take STCO (System-Technology Co-Optimization) and DTCO (Design-Technology Co-Optimization) into account, while being integrated with advanced packaging platforms.
- BSPDN (Backside Power Delivery Network)is a good approach to reduce RC delay in advanced logic device and TSMC forecasted MP @ 2026

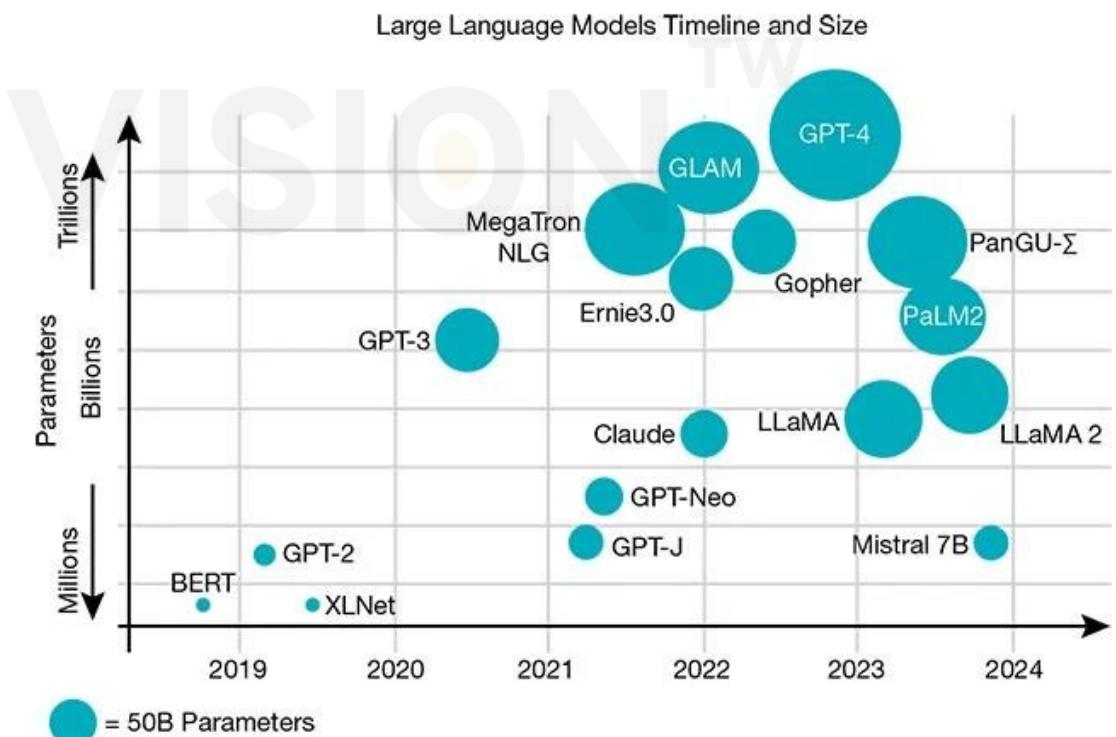
# Challenge 2: High Cost and Investments



- Advanced logic processes primarily utilize EUV lithography and, complemented by DUV immersion and DUV lithography tools.
- The N3 process exhibits variations in EUV masks due to the unique characteristics of its electric devices.
- EUV lithography imposes stringent requirements on photoresists. In EUV processes, both CAR (Chemically-Amplified Resist) and MOR (Metal Oxide Resist) are commonly used.

- Large Language model driven AI grow. (Chat GPT by Open AI)
- Training and inference chips are driving growth in Taiwan's semiconductor industry, particularly through advancements in packaging technologies.
- Major CSP companies are increasingly entering the design of inference chips.

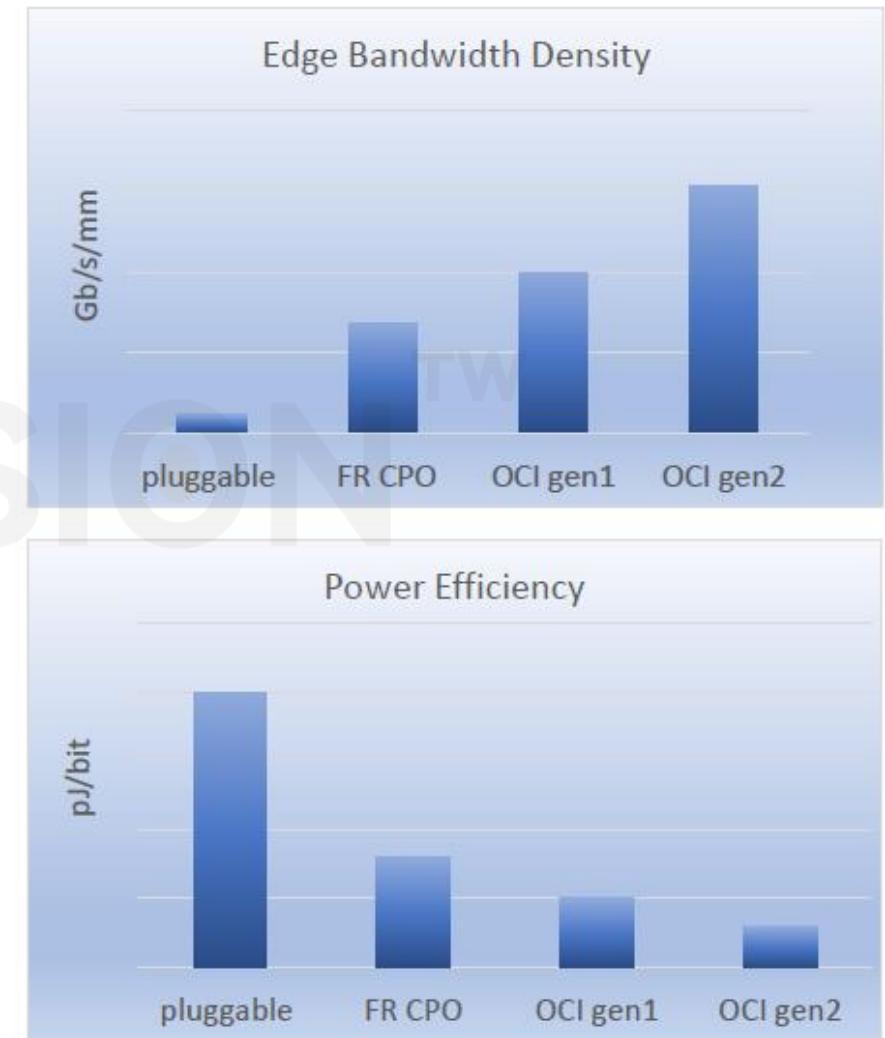
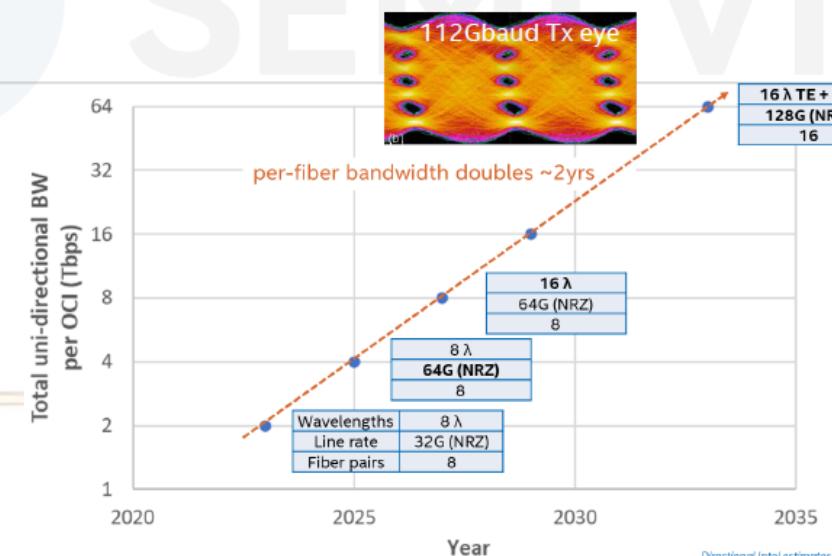
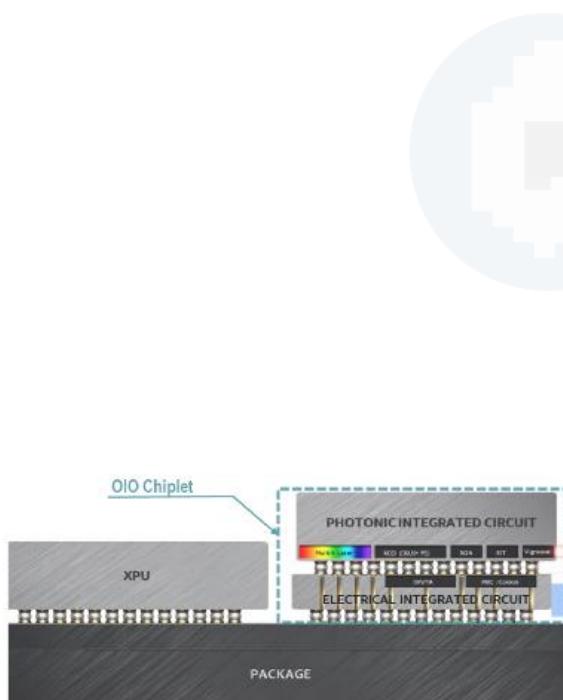
Key Points	Details
AI Model Progress	The new large language models (e.g., GPT-5) failed to launch on schedule, affecting market confidence in AI technology progress.
Computing Power Cost Issues	High computing power demands have made companies more cautious about investing in AI.
Changes in Market's Perception of AI	Last year, the upgrade from GPT-3 to GPT-4 demonstrated significant performance breakthroughs, boosting market confidence in AI's potential. However, in the second half of this year, the delay in GPT-5 has led investors to doubt AI's future development.
Investor Sentiment	Investors are focusing on AI's achievable potential rather than short-term returns. The success of GPT-4 expanded their expectations, encouraging more investment. However, the delay of GPT-5 has limited their imagination of AI's capabilities, impacting funding willingness.



- The scaling law of large language models is not failing but requires new data and application-driven advancements. The media misinterpreted OpenAI's Ilya Sutskever, who was referring to the saturation of gains from pre-training on general internet corpora, not the failure of the scaling law itself. To continue improving large language models, it is necessary to incorporate non-public, private data into the training process, such as user-specific data and user feedback data. Additionally, incorporating multi-modal data for training is another promising direction.
- Nvidia dominates large language model training and inference, but ASICs hold long-term appeal. Nvidia's unique software stack (CUDA, NVLink) and monopoly on HBM memory give it a dominant position in the GPU market, making it difficult for users to switch to AMD GPUs or ASICs. While some companies are exploring AMD GPUs and ASICs as alternatives, challenges in software compatibility and supply chain (e.g., HBM memory) make it unlikely to replace Nvidia in the short term. Enterprises need to consider the total cost of ownership, including hardware costs, energy consumption, maintenance, and other operational expenses when evaluating hardware solutions.
- In conclusion, the scaling law of large language models is not failing but entering a new stage driven by new data and applications. The future focus will be on how to effectively acquire and utilize private data, enhance model capabilities, and drive the development of the AI industry through real-world applications.



- Demonstrated first fully functional OCI link between two CPUs
- SiPh drives power, bandwidth density and cost scaling
- SiPh is key enabler of co-packaged optics
- SiPh is integrated to electrical and optical signal processed.
- DWDM is used to multiple wavelength and equip to EC (Edge Coupler)



- SerDes and PCIe electrical signals are crucial for the development of silicon photonics.
- The substrate material (low loss material) is a significant issue
- SiPh is key enabler of co-packaged optics (CPO).
- Thermal budget for SiPh and Package are need to considered.
- DWDM is used to multiple wavelength and equip to EC (Edge Coupler)

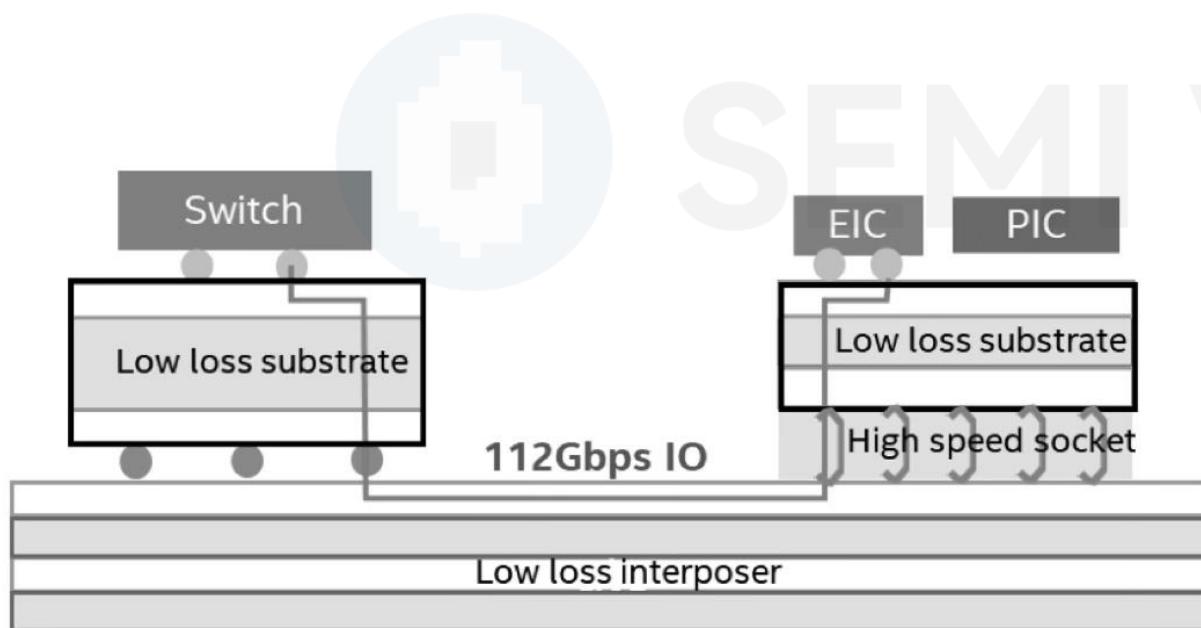
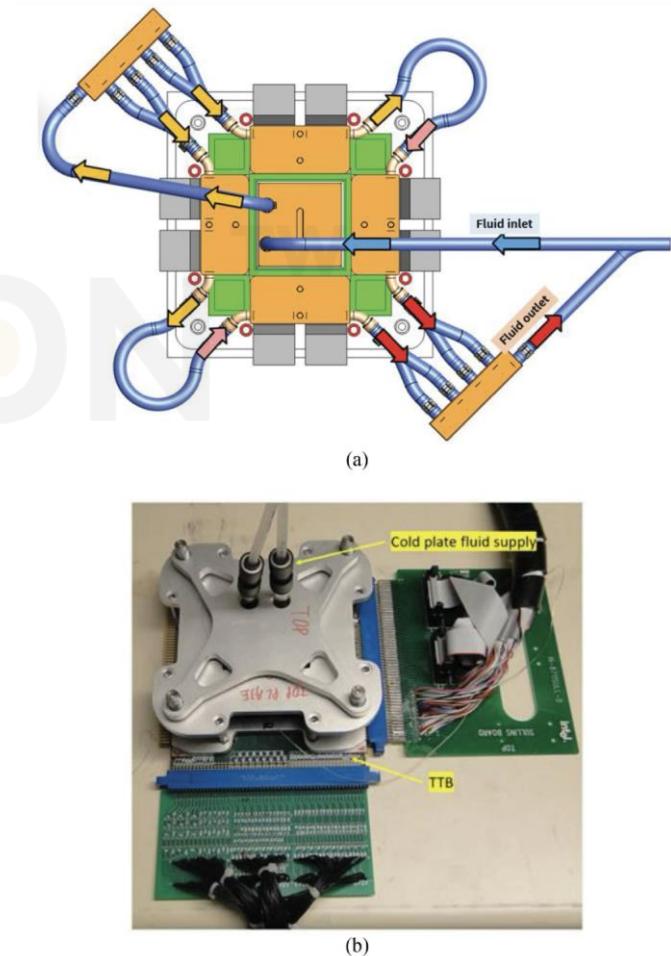


Fig. 17. 112G XSR electrical link topology for a co-packaged optical switch



- Current mainstream PIC design flow is bottom-up: Start from components design, then circuit design, finally verification.
- Components design including layout design and simulation. Layout design including component geometry, process layer, which will be used in real fabrication. Component simulation shows the performance of the component, help designer to predict the component behaviors and optimize the performance.
- Circuit design including circuit layout and simulation. Circuit layout including placement and routing(P&R). Placement is to place components; routing is to connect components through waveguide. Again, circuit layout also design for real fabrication. Circuit simulation is to predict the performance of the photonic circuit.
- Circuit verification: Before designer submit design files to foundry for fabrication, the file needs to be verified to prevent fabrication error. Common circuit verification including design rule checking(DRC), connection checking, post layout simulation.



Yao-Tung Chang  
PDK engineer at  
Luceda Photonics



The current mainstream PIC design flow follows a bottom-up approach: it starts with component design, moves to circuit design, and ends with verification.

➤ **Component Design:**

This stage includes layout design and simulation:

- **Layout Design** involves defining the geometry and process layers of components to ensure they can be fabricated.
- **Simulation** predicts component performance, helping designers understand behavior and optimize functionality.

➤ **Circuit Design:**

This stage also includes layout and simulation:

- **Circuit Layout** involves placement and routing (P&R):
  - **Placement** determines where components are located.
  - **Routing** connects components using waveguides.
  - The layout is prepared for real fabrication.
- **Simulation** predicts the photonic circuit's performance.

➤ **Circuit Verification:**

Before submitting design files to the foundry for fabrication, they must be verified to avoid errors.

Common verification steps include:

- **Connection Checking:** Verifies all components are correctly connected.
- **Post-Layout Simulation:** Predicts circuit performance after layout design.
- **Design Rule Checking (DRC):** Ensures the design follows fabrication rules.

## LUCEDA DESIGN KITS

### Si



### SiN



### InP



### Al<sub>2</sub>O<sub>3</sub>



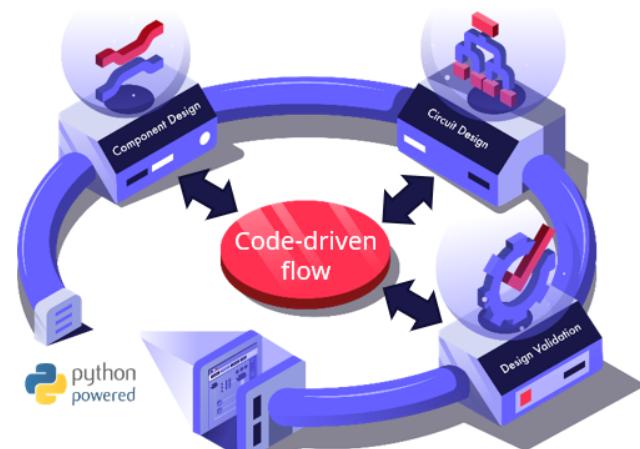
### LNOI



### Assembly & Testing



## Luceda IPKISS



### FEATURES

- Component & circuit layout
- Optical and electrical routing
- EME solver (Camfr)
- Circuit simulation engine (Caphe)
- Schematic capture to IPKISS code (IPKISS Canvas)
- Post-layout validation
- Netlist extraction (optical and electrical)
- Functional verification (IPKISS Canvas)
- GDS export

## FLAGSHIP PRODUCTS



**Luceda IPKISS**



**Luceda AWG Designer**  
Requires IPKISS



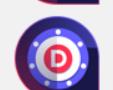
**Luceda IP Manager**  
Requires IPKISS

## PARTNER INTEGRATIONS

### DEVICE SIMULATION



**Link for Ansys Lumerical**  
Requires IPKISS



**Link for 3DS Simulia**  
Requires IPKISS



**Link for Tidy3D**  
Requires IPKISS

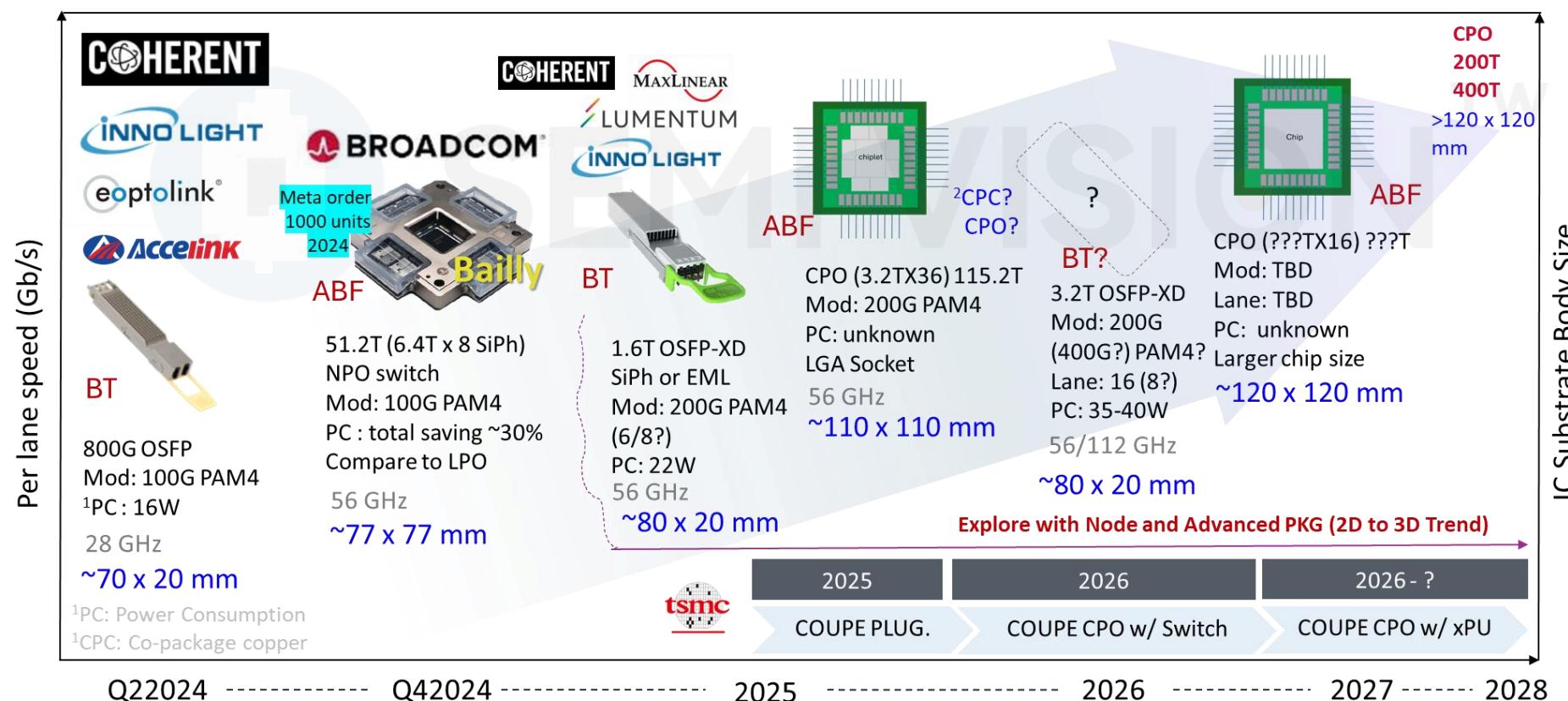


**Link for Siemens EDA**  
Requires IPKISS



**Link for Check Mate DRC**  
Requires IPKISS

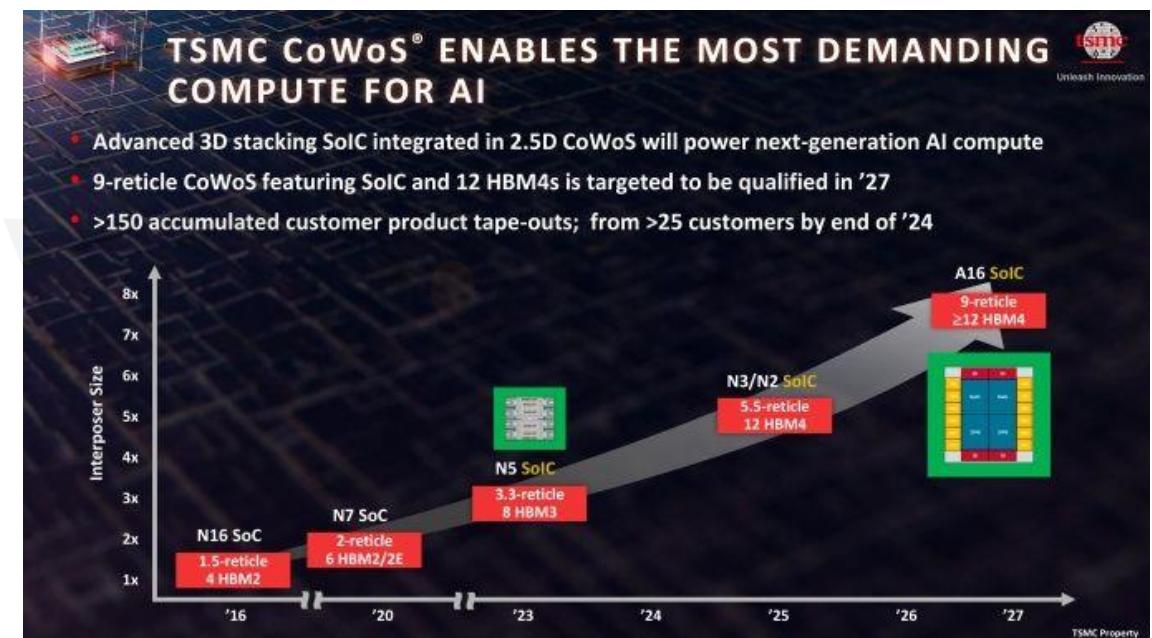
- AI cluster's scale-up and scale-out stages lead to rapidly increased computing
- Pluggable optical TRx suffers from one of the limitations of the form factor; there are more developments toward CPO and/or CPC competition.
- IC substrate side faces a critical challenge owing to high integration between OE/EE and IC to reduce the electrical path, resulting in increasing the substrate layer counts and body size.





**Let's work together to contribute to human technology.**

- Overview of TSMC Technology
- Overview of Advanced Packaging Platforms
- Overview of Foundry SiPh Platforms
- Thermal Budget for AI Chips
- HBM Value Chain
- Testing for Silicon Photonics
- The rising star : CPO and CPC



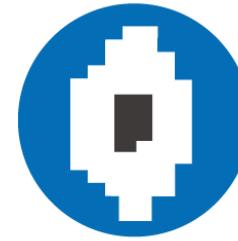
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- Silicon Photonics
- Advanced IP
- Specialty Chemicals
- Specialty Materials
- HBM
- Semiconductor Equipment, and more,

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