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High-bandwidth Chiplet Interconnects for Advanced Packaging Technologies in AI/ML Applications: Challenges and Solutions

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Abstract The demand for chiplet integration using 2.5D and 3D advanced packaging technologies has surged, driven by the exponential growth in computing performance required by Artificial Intelligence and Machine Learning (AI/ML). This paper reviews these advanced packaging technologies and emphasizes critical design considerations for high-bandwidth chiplet interconnects, which are vital for efficient integration. We address challenges related to bandwidth density, energy efficiency, electromigration, power integrity, and signal integrity. To avoid power overhead, the chiplet interconnect architecture is designed to be as simple as possible, employing a parallel data bus with forwarded clocks. However, achieving high-yield manufacturing and robust performance still necessitates significant efforts in design and technology co-optimization. Despite these challenges, the semiconductor industry is poised for continued growth and innovation, driven by the possibilities unlocked by a robust chiplet ecosystem and novel 3D-IC design methodologies.

***Index Terms*— Chiplet Integration, Advanced Packaging, Interconnects, 3D-IC, AI and Compute, Energy Efficiency, UCIe, 3Dblox**

I. Introduction[1]

The demand for artificial intelligence (AI) and machine learning (ML) technologies is growing at an unprecedented pace, far surpassing the pace predicted by Moore's Law. The amount of compute used for AI training has been growing exponentially at 4.1x/year since 2012, outpacing Moore's Law, which predicts a doubling every 24 months [1] [2], as shown in Fig. 1. The increase in the number of parameters in deep learning models enhances their flexibility and potential performance, driving the rapid growth in model complexity. However, this rate of expansion is becoming economically (training cost), technically (size of the computer clusters), and environmentally (carbon footprint) unsustainable [3] [4]. To partially meet the escalating compute demand, it is essential to focus on advancements in algorithm efficiency and semiconductor scaling, aiming to achieve not only higher compute performance but also energy-efficient compute performance [5] [6]. AI workloads require massive parallel matrix multiplication and accumulation operations, which are performed by clusters of parallel computing cores. These workloads demand extensive memory capacity and high interconnect bandwidth. To accommodate this compute need, a typical xPU/accelerator chip nowadays may consists of many compute, memory, and IO chiplets [7] [8] [9], integrated using advanced packaging technologies. Each chiplet is designed within the lithography stepper's photomask limit, or reticle size, of 26 x 33 mm².

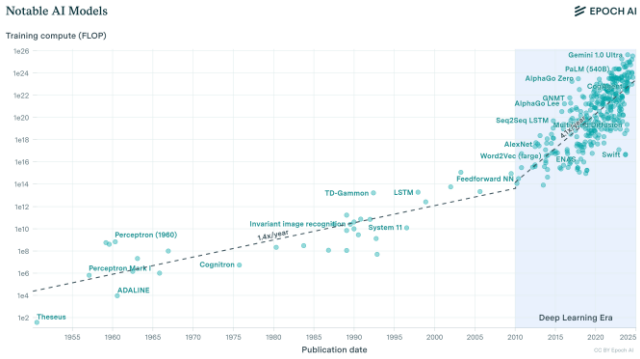

Fig. 1. Trend in the amount of compute used to train the ML models [2]

The use of chiplets offers several significant benefits. By breaking down a large monolithic chip into smaller, yield manageable chiplets, designers can tailor different process technologies to optimize specific functionalities, for example, using the most advanced process node for compute die, and using older generation process nodes for analog centric IO dies and memory dies. This modular approach not only simplifies the manufacturing process but also facilitates rapid system integration, especially when standardized chiplet interfaces are utilized [10] [11]. By leveraging off-the-shelf chiplets, this method is expected to significantly reduce manufacturing costs and design cycle times.

As chiplet-based systems in packages grow in size and complexity, 3D integration [12] and wafer-scale system

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integration [13] [14] [15] will deliver superior power efficiency, exceptional performance, and enhanced cost-effectiveness [16]. However, several critical issues, which are familiar to designers at each generation of products, continue to pose significant challenges in today's larger and more intricate chiplet systems. These challenges include thermal design power (TDP), power delivery network (PDN) loss, mechanical and thermal stress, network topology and routing algorithms, interconnect throughput, energy efficiency, latency, manufacturability, redundancy and repairability, testability, and many more [16] [17] [18] [19] [20] [21] [22]. Addressing these challenges is essential to ensuring the performance and yield of advanced semiconductor solutions.

This article is structured as follows. Section II provides a summary of advanced packaging technologies. Section III discusses die-to-die interconnects for various packaging technologies in large CPU/GPU scale-up systems. Section IV delves into practical issues for chiplet interconnect design, such as serial vs parallel interfaces, chiplet I/F signaling, channel routing and signal integrity, bump map planning, clock schemes, defect repair, ESD roadmap, and power delivery. Section V introduces a comprehensive 3DIC design flow. Finally, Section VI explores future development trends.

II. Advanced Packaging Technologies & New Capabilities

[23] provides an excellent review of advanced packaging technologies, categorizing them into 2D, 2.xD (including 2.1D, 2.3D, and 2.5D), and 3D packaging technologies. According to this classification, if chiplets are placed directly on the package substrate, it is considered 2D packaging. When an intermediate layer such as a thin film, bridge, or passive interposer is used, it falls under the 2.xD category. Specifically, if the interposer is an active die with Through-Silicon Vias (TSVs), it is classified as 3D packaging.

While this categorization is intuitive, it is also somewhat arbitrary. As packaging technologies continue to evolve, the boundaries between these categories may become increasingly blurred. To simplify discussions, most of the intermediate 2.xD technologies are often grouped under the 2.5D category. It is also possible that 2D, 2.5D, and 3D integration techniques will co-exist within advanced packaging solutions, with 3D-IC being used in a broad sense to refer to these solutions. Regardless of these distinctions, the primary focus will remain on leveraging these technologies to achieve superior performance, efficiency, and functionality in semiconductor devices.

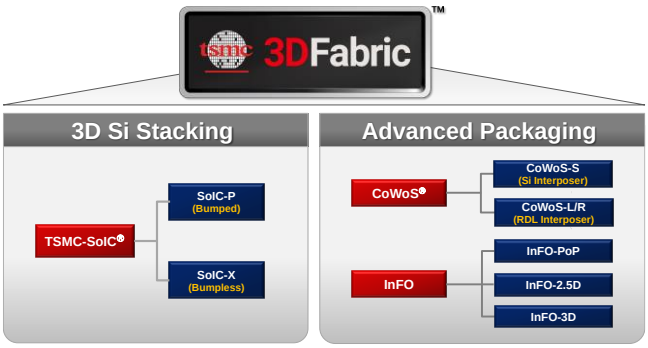


Fig. 2. TSMC 3DFabric Technology portfolio.

Fig. 2 illustrates TSMC's evolving 3DFabric™ technology portfolio. The 3DFabric, as an example of advanced packaging technologies with wide adoption, is a comprehensive set of integration technologies that bring multiple chips together with closer physical proximity and higher interconnect density, all from a single vendor. This integration enables a smaller form factor, better electrical performance, and greatly enhanced data bandwidth. More importantly, these technologies allow system designers to partition a previously monolithic SoC into chiplets and build more powerful systems in a package [5]. The different 3DFabric packaging options maintain consistency. This cohesion is beneficial because the complexity of 3D-IC requires that the design rules pertaining to manufacturability are compatible and consistently verified prior to high-volume manufacturing.

Two distinct packaging platforms emerged from distinctive applications. The first one is the Chip-on-Wafer-On-Substrate (CoWoS™) platform [24] [25], which has been in production since 2012, primarily for high-performance computing. It has 3 sub-families. The CoWoS-S has a silicon interposer which allows very dense metal wires (W/S = 0.4/0.4μm). The CoWoS-R [26] [27] has redistribution layers (RDL) embedded in an organic interposer, with coarser wiring density (W/S = 2/2μm). The CoWoS-L [28] combines the best of the -R and -S: local silicon interconnect (LSI) for high wiring density, and RDL in organic substrate for better electrical performance. The -S or -L option also comes with embedded deep-trench decoupling capacitors (DTC) [29] in the silicon interposer or bridge for enhanced power delivery.

The 2nd one is the Integrated-FanOut (InFO™) platform [30]. InFO has been in mass production since 2016, initially driven by cost effective mobile application. InFO package on package (InFO-PoP) [30] is the first 3D Fan-Out wafer level packaging to integrate SoC with memory packages using fine pitch Copper RDLs. Due to its cost, form factor, and better signal integrity, InFO technology has evolved into many variants, significantly extending to allow integration of more functional chips for HPC applications [15]. The InFO platform also features advanced options such as local silicon bridge for finer pitch metal routing, and embedded decoupling capacitors for superior power delivery. InFO is a chip-first approach, where chips are placed face-down onto a temporary carrier and RDL is built up around them. CoWoS, on the other hand, is a chip-last approach, with chips first fabricated and then placed onto a silicon interposer, which is later attached to a substrate. This distinction in manufacturing steps affect integration density, and thermal

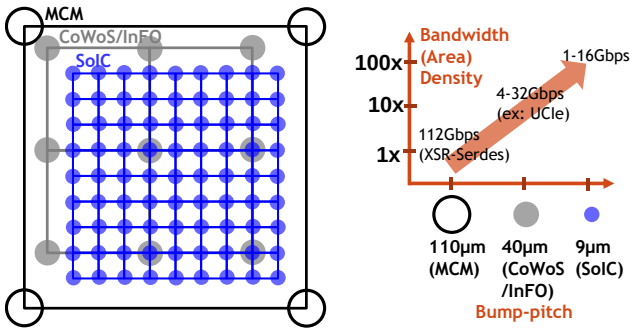


Fig. 3. Bump pitch scaling perspective (XSR: extreme short reach, UCIe: Universal Chiplets Interconnect Express)

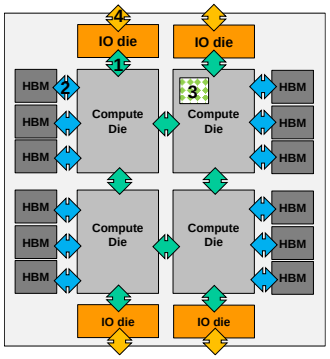


Fig. 4. Die-to-die interconnect applications.

management. Specifically, in a chip-first approach, the silicon will undergo the thermal cycles in subsequent cycles. The cost of late step defects is also significantly higher than a chip-last approach.

3D stacking has been broadly used in memory products, including high-bandwidth memory (HBM) [31] and NAND flash memory [32], and is seeing adoption by chipmakers for increased compute density and data bandwidth [33] [34]. System on Integrated Chips (SoIC™) is for such 3D chip stacking [35]. It includes the SoIC-P with micro-bumps (pitch at 18~25µm) and SoIC-X with advanced bonds (pitch at 3~9µm or below) [36] [37] [38].

SoIC enables seamless integration of multiple chips in a vertically stacked configuration, unlocking new possibilities for system design and performance optimization. Furthermore, SoIC can be combined with CoWoS or InFO to form more powerful and flexible computer systems.

Chip manufacturers and Outsource Semiconductor Assembly and Test (OSAT) providers offer a range of advanced packaging technologies [23] [38] [39], each with unique (dis)advantages and trade-offs in signal integrity, interconnect density, manufacturability, and thermal management. For example, embedded multi-die interconnect bridge (EMIB) [39] by Intel and elevated fan-out bridge (EFB) [40] by AMD, both feature high-density passive bridges without TSVs, complemented by additional RDLs to enhance power integrity. The selection of a particular packaging technology hinges on the specific application requirements and desired performance characteristics, especially in high-performance computing where speed and energy efficiency are crucial. This also imposes constraints and challenges on interconnect design, which will be explored in subsequent sections.

III. Die to Die Interconnect Applications

Fig. 3 shows the chip package evolution from the perspective of bump pitch scaling, starting from the conventional 2D standard package type, or multi-chip modules (MCM) with 110~130µm bump pitch, to 2.5D advanced package type (e.g., CoWoS/InFO) with ~40µm pitch, to 3D chip on wafer or wafer on wafer type (e.g., SoIC) with <9µm pitch [11]. As the bump pitch decreases, the number of die-to-die signals increases quadratically within a given area, thereby increasing bandwidth density. The selection of circuit architecture in the context of pitch scaling depends heavily on factors such as achievable reach, bandwidth, energy efficiency, and latency [41]. For example, high-speed serializers/deserializers (SerDes) operating at ~56/112Gbps [42] are commonly used in MCM packages to maximize data rates per pin. In contrast, 2.5D interposers often employ high-speed parallel data buses due to their superior energy and area efficiency [41]. Meanwhile, advanced 3D stacking technologies benefit most from simpler, lower-speed data buses that utilize minimal CMOS buffers and flip-flops, with no equalizer or calibration circuits, thereby achieving best area bandwidth density and energy efficiency [11].

Fig. 4 depicts an example of multiple chiplets for compute performance scale-up and scaling out for AI applications. The die-to-die interconnects between the chiplets can be categorized to four types: 1) Compute to Compute & Compute to IO: UCIe™ PHY on CoWoS/InFO technology, 2) Compute to Memory: HBM™ PHY on CoWoS technology, 3) Compute to SRAM: 3D-stacking with SoIC technology, and 4) IO chiplet to external IO: XSR-Serdes on standard package technology.

Today's most widely used AI accelerators adopt this type of topology to maximize compute performance and memory access bandwidth [43] [44]. Competing technologies, such as wafer scale systems [13] [14] offer a glimpse into likely candidates of future computing systems. The interconnects and network topologies for these systems will need to evolve accordingly to meet system performance needs.

IV. Chiplet Interconnect Design Considerations

A. Chiplet Interconnect Design Objectives and DTCO

Breaking down a formerly monolithic SoC into multiple chiplets stitched by high bandwidth chiplet interconnects enables a more flexible system partition, with the benefit of improved yield, and fast turnaround time using off-the-shelf chiplets. Standardization of the chiplet interface is an important milestone, as exemplified by Universal Chiplets Interconnect Express (UCIe™) [11].

Before this development, several industry-initiated chiplet

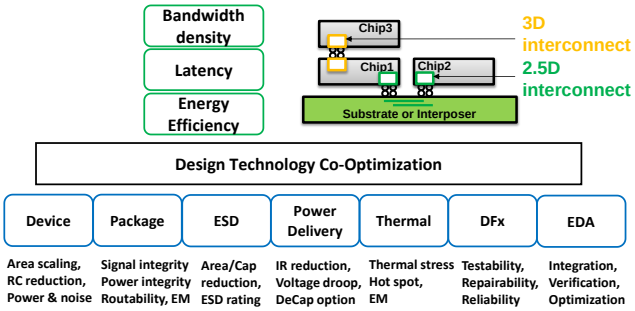


Fig. 5. Chiplet interconnect design considerations.

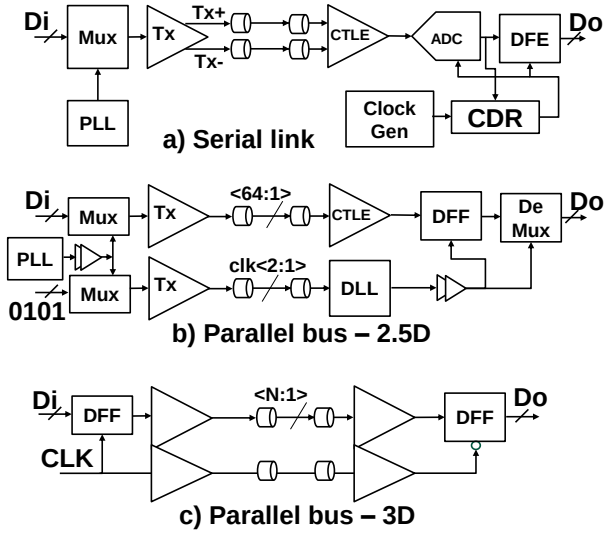


Fig. 6. Die-to-die interconnect applications.

interfaces were adopted to address the requirements of chiplet systems, emphasizing high bandwidth density, low latency, and high energy efficiency. Notable examples include the Advanced Interconnect Bus (AIB) [45], Bunch of Wires (BoW) [46], Open High Bandwidth Interface (OpenHBI) [47], and Lipincon (TSMC proprietary) [48].

Figure 5 provides a comprehensive overview of the multi-faceted design and technology co-optimization (DTCO) efforts aimed at meeting both performance and manufacturing objectives for high-speed interconnects in 2.5D or 3D chiplet-based systems [49]. The scope of DTCO encompasses a wide range of considerations, including but not limited to:

- Device-level optimization: The focus is on pushing transistor bandwidth and noise performance to improve IO energy efficiency.
- Package optimization: Optimizing the package design rules on the interposer by balancing key parameters such as line spacing, layer thickness, and via enclosure, is crucial to power integrity (PI), signal integrity (SI), routability, and manufacturability.
- ESD: New challenges have emerged in ESD protection and ESD modeling for chiplet systems [50]. The ESD rating for advanced packages must be carefully evaluated to ensure that the ESD area and capacitance overhead do not hinder IO energy efficiency.
- Power delivery network (PDN): This entails managing electromigration (EM) and IR drop, voltage droop, and cross-talks originating from power delivery.
- Thermal management: Key challenges include simulating hot spots accurately, and mitigating thermal cycle induced problems, such as timing drift, mechanical stress, and electromigration. It involves implementing solutions, during the design stage [51] or at run-time [52] to keep devices within safe temperature ranges, thereby maintaining performance, reliability, and longevity.
- Designing for testability, repairability, and reliability: Ensuring these aspects contributes to both effective short-term testing and a long-term lifespan, which is crucial for a product's success.
- Design sign-off processes: Efficient, AI-assisted EDA tools and flows are increasingly essential for productivity and optimization [53].

B. *Serial vs Parallel Data Bus*

With standard packages (MCM, or 2D), the pitch of signal bumps and metal wires are coarse. One is forced to maximize per-pin data bandwidth density, using serial link (e.g., PCIe-32/64Gbps, CEI-112/224Gbps) with differential signaling as shown in Fig. 6-a.

Advanced packaging technologies (2.5D) allow one to use a lower data rate per signal pin with a greater number of parallel single-ended signals per unit geometry to maximize beachfront bandwidth density or area bandwidth density (e.g., UCIe x64 at 4-32Gbps) [11]. A parallel interface (Fig. 6-b) stands out in several aspects. First, a parallel interface is accompanied by a forwarded clock for jitter and skew tracking, eliminating the need for a per-lane clock data recovery (CDR) mechanism, resulting in a less complex system and lower latency. Second, the lower data rate operation of the parallel interface means the system suffers less to channel loss, jitter, and cross-talks. Less channel equalization (EQ) is needed, eliminating circuit overheads, and achieving higher bandwidth density and better energy efficiency.

For 3D stacking, with a signal density (pitch P ≤ 9μm), the 3D interconnect circuit area should be smaller than the bump area (P^2) to maximize the interconnect efficiency ($\triangleq$ BandwidthDensity $*$ Energy Efficiency). In this case, the speed of the parallel data bus is constrained to 5Gbps to ease the timing [11]. No calibration and adaptation are needed, effectively reducing power, latency, and area overhead. UCIe-3D^{TM} has this spirit (Fig. 6-c).

C. *Die-to-die Interconnect Signaling*

Advanced packaging technologies enables closer die proximity and reduced interconnect loading, improving signal integrity, data rates and power efficiency. Non-return to zero (NRZ) and 4-level Pulse Amplitude Modulation (PAM4) signaling are likely candidates for different operating speeds. In Fig. 7, an SST (Source-Series Terminated) driver at core supply (e.g., Vdd=0.75V) is commonly used for optimal eye margin and impedance matching. An NFET-NFET driver has been adopted to operate at a low VDDQ (e.g., <0.3 volt) to cut down power consumption [48]. However, this extra power domain may

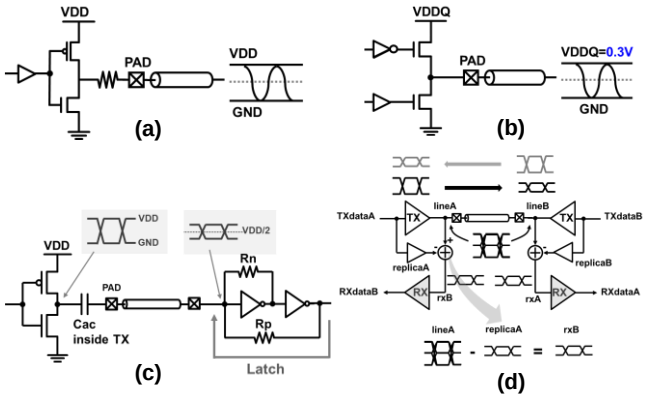


Fig. 7. Die-to-die interconnect signaling: (a) SST driver (b) Low VDDQ NRZ driver (c) AC-coupled [54] (d) Simultaneously bi-directional [56].

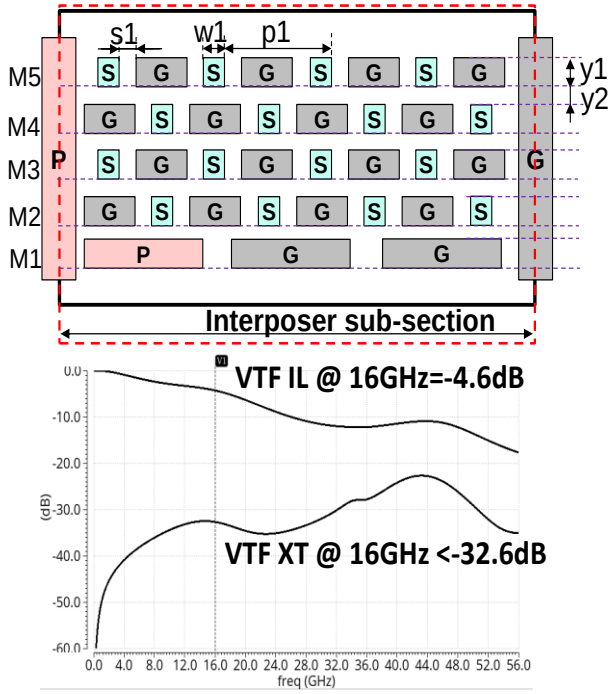


Fig. 8. Channel routability & signal integrity optimization

be undesirable with scarce routing resource. PAM4 is advantageous when there is a significant insertion loss benefit at PAM4 Nyquist frequency than NRZ Nyquist frequency, yet it consumes DC current at the middle levels, making it less suitable for low loss advanced packaging channels. Another alternative low power driver option is AC-coupling [54], which reduces driver strength and signal swing to reduce power. Simultaneous Bi-Directional (SBD) data transmission can also double the data bandwidth for a given beachfront [55] [56].

D. Channel Routability & Integrity Analysis

For high wiring density (e.g., at min spacing of 0.4µm), proper inter-signal shielding is necessary to allow adequate crosstalk isolation and better signal integrity.

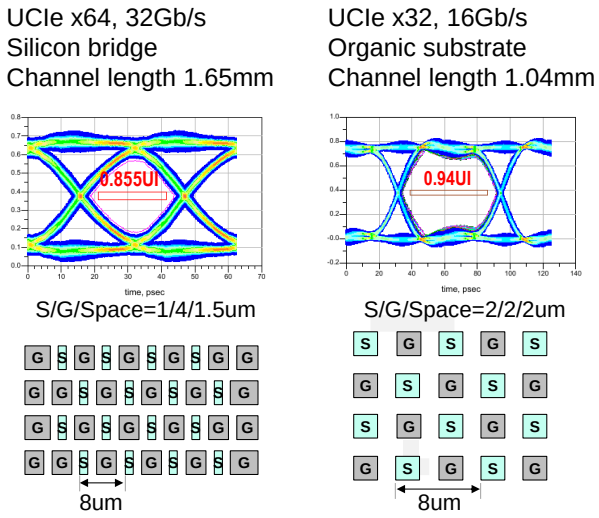


Fig. 9. Channel optimization.

As shown in Fig. 8, channel optimization inside a foundry involves many metrics such as dielectric thickness, metal pitch, metal thickness, available metal layers, via enclosure, stacking rules, etc. Design and technology co-optimization is exercised for the interposers of each advanced technology, which often involves pushing design rules to maintain a good tradeoff between manufacturability, routability and signal integrity (SI, including insertion loss and crosstalk as shown by the plots).

Fig. 9 demonstrates two examples of UCIe D2D routing designs, in two different representative packages and different shielding style. The InFO (silicon bridge) has a local silicon interconnect with 2µm thick metal, and the InFO (organic substrate) has RDL with 2.3µm thick metal. Both has 4 layers of metal for signal routing and additional 1 layer for power mesh. The former has a tighter metal width/spacing granularity. With an 8 µm signal pitch for both cases, the former can afford to have a much wider metal shield, and slightly larger signal to signal spacing. As such, the former is able to operate up to 32Gbps for the x64 UCIe form facor, whereas the latter is only capable of 16Gbps with x32 data lanes due to the more severe crosstalk.

E. 2.5D and 3D Form Factors

A certain form factor of an interconnect module, which encompasses module geometry, signal order, bump pitch, multi-module stacking, etc., is crucial for ensuring integration compatibility among different chiplet vendors. While this standardization introduces rigidness to the chiplet eco-system, it simplifies IP development – only a limited variants of the IP need to be supported. However, it is important to note that a given form factor may not always be optimal in terms of area, power, and cost. Take UCIe as an example: Initially, a x64 (64 Tx + 64 Rx) form factor was released, followed by a x32 (32 Tx + 32 Rx) form factor for low-cost advanced packages with a smaller number of RDL layers. The initial 10-column module was targeting a 45µm bump pitch. To further enhance area efficiency, the consortium later introduced a 16-column module for smaller

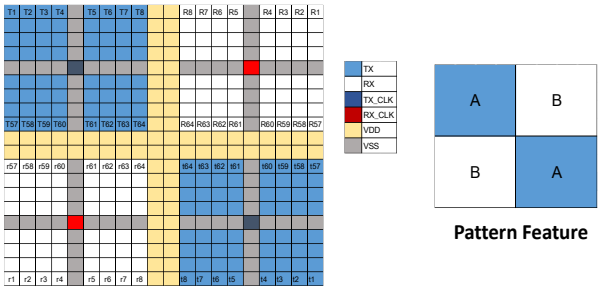


Fig. 10. A universal 3D bump map form factor

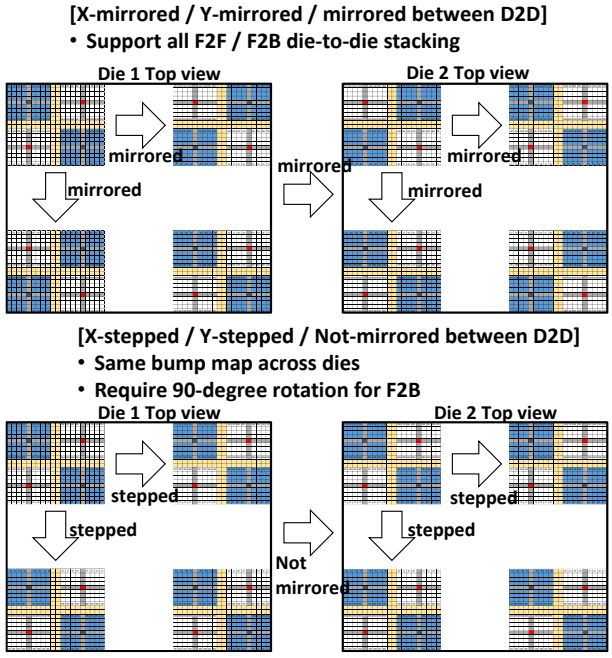


Fig. 11. SoC level Scalability to support arbitrary 3D chiplet stacking (F2F/F2B or rotation).

bump pitches (<38µm) and an 8-column module for larger bump pitches (>50µm) [11]. These successive adaptations balance cost and performance to accommodate varying requirements of different applications.

The current UCIe protocol supports symmetrical bidirectional data transmit and receive, which is typical for data communication between homogeneous xPU chiplets.

In contrast, the High Bandwidth Memory (HBM) interface, a crucial component of the chiplet ecosystem, exhibits asymmetrical memory access (read/write) bandwidth. To extend the interface bandwidth without causing severe signal integrity issues, the forthcoming HBM4 doubles the number of bi-direction data IOs from 1024 to 2048 [31]. Scaling HBM for increased bandwidth is often constrained by routing congestion and signal integrity issues. By transitioning the base die logic to advanced process nodes, we can shorten interconnect routes, enhancing signal integrity and speed. Alternatively, utilizing UCIe-like SerDes IOs for the HBM interface can achieve higher lane rates with fewer signal routes, maintaining the same bandwidth density while improving signal integrity.

One more notable chiplet application is the interface between data converters and logic processors. JESD204D is the latest standard defining high-speed serial interfaces for data converters [57]. It includes the data receive interface for ADCs (Analog-to-Digital Converters) and the data transmit interface for DACs (Digital-to-Analog Converters). The standards are applicable to PCB-level or Multi-Chip Module chiplet integration. However, a chiplet standard for data converters in advanced packages has yet to be established.

While it is conceivable to develop a one-size-fits-all chiplet standard that addresses the three unique types of systems—homogeneous bidirectional core-to-core interfaces, asymmetrical memory access interfaces, and unidirectional data converter interfaces—each system would still require different form factors to achieve optimal performance and efficiency.

3D stacking is a natural choice for achieving greater energy efficiency, primarily because the short inter-die routing significantly reduces the energy required for inter-die data movement. A 3D interconnect cluster is essential for forming a hard IP block with inherent timing robustness, as illustrated in Fig. 6-c. This built-in timing robustness allows for modular timing sign-off, ensuring that the timing validation of each die in a 3D stack can be conducted independently and in a self-contained manner.

In Figure 10, we propose a 3D cluster structure with an AB|BA pattern, where pattern A represents the transmitter (TX) and pattern B represents the receiver (RX), or vice versa. The square-shaped A/B pattern can be configured into various sizes, such as 4x4, 8x8, or 20x20, depending on system requirements. The RX and TX clocks, positioned at the center of their respective regions, achieve optimal balance for each I/O pin and across the dies. Power and ground are symmetrically distributed within the IP cluster. This configuration offers the advantage of designing a single IP block with a specific poly gate orientation that can accommodate any chiplet orientation, assuming that logic-level pin remapping can be readily achieved at the chiplet level.

This structure facilitates easy SoC-level scalability, enabling various chiplet-to-chiplet stacking scenarios through IP instantiation across the SoC. We propose four options for SoC-level scalability in Face-to-Back (F2B) and Face-to-Face (F2F) connectivity: Mirrored or Stepped in the X-direction and Mirrored or Stepped in the Y-direction.

Fig. 11 illustrates two integration examples:

1. Case 1: 'X-mirrored / Y-mirrored / mirrored between D2D' - This configuration supports all F2F and F2B die-to-die stacking scenarios.
2. Case 2: 'X-stepped / Y-stepped / Not-mirrored between D2D' - This setup features the same bump map across dies. It supports F2F stacking but requires a 90-degree rotation for F2B stacking.

These flexible integration methods ensure that the IP cluster can be effectively utilized across a variety of chiplet stacking configurations, promoting scalability and efficiency in SoC design.

F. Lane De-skew and Clock Alignment

On top of the parallel data-bus and forwarded clock topology, there is a need to align the data lanes and clock

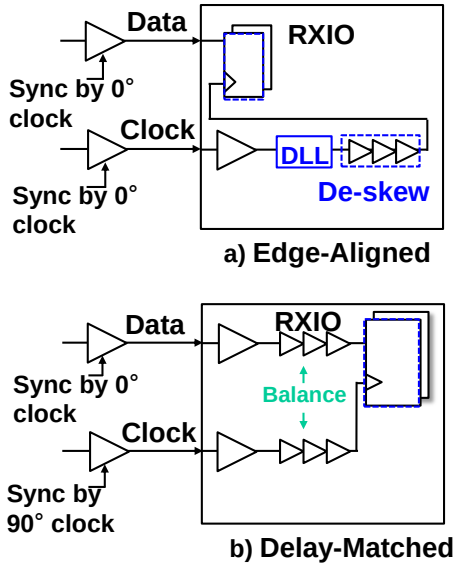


Fig. 12. Edge-aligned vs delay-matched structure.

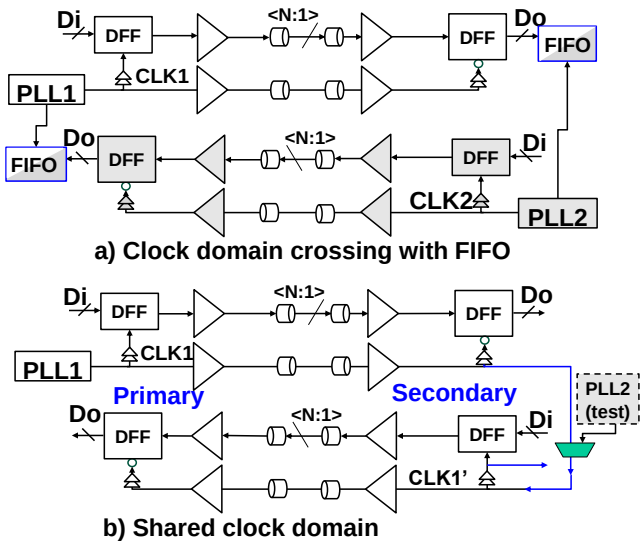


Fig. 13. Data Synchronization with or without FIFO

lanes such that lane to lane skew is minimized. Lane to lane matching is achieved by anti-mirror physical symmetry between the Tx and Rx in the bump map planning. However, the physical symmetry does not hold when one is to interface two different form factors. For example, for an 8-column UCIe to interface with a 10-column UCIe, the channels are intrinsically unmatched. Besides, random circuit mismatch and on-die/on-package wire mismatch add additional skew. One needs to allocate enough skew tuning range on a per-lane basis at the leaf clock tree to achieve per lane skew calibration at the transmitter and/or receiver. Data sampling clock at the receiver is further tuned to the center of the Rx data-eye for best left and right eye margin.

Two clock topologies for the forwarded clock generation are illustrated in Fig. 12. The edge-aligned topology (Fig. 12-a) has data transition and clock transition aligned; a local DLL in the Rx is adopted to generate a 90-degree phase shifted clock to sample the Rx data-eye. The edge-aligned topology aims for less circuitry and better energy efficiency, but it is sensitive to mismatch induced by temperature or voltage drift, making it only suitable for applications with lower data rate (e.g., below 20Gbps). The delay-matched topology (Fig. 12-b) generates I/Q clocks (using DLL or PLL, and phase interpolators) at the Tx side, with the I-clock going to the data path while the Q clock forwarded to the Rx. The clock and data path are structurally matched to maintain good jitter tracking and delay tracking.

In most cases, the transmit die and the receive die are under independent PLLs and clock domains. To enable robust clock domain crossing between two PLL domains, First-In-First-Out (FIFO) data buffers are typically required, which incurs extra power and latency (Fig. 13-a). For interfaces like core-to-memory connections, enforcing a single clock domain between two stacked dies is feasible. In Fig. 13-b, we proposed an alternative scheme to enable a single clock domain between two dies, where the primary clock from PLL1 is forwarded from the primary die to a secondary die and is returned to the primary die. This allows the 3D die to die interface to transmit/receive data without FIFOs. The same timing margin as Fig. 13-a at the boundary of the first capture DFF can be retained. Timing margin for the data recapture after the Rx DFF in the primary die is slightly affected by the delay of the two forwarding clock paths, which is manageable.

G. *Redundancy & Repairability*

Redundancy and repairability are extensively researched topics in the field of microprocessors. [58] identified three distinct redundancy strategies:

- Component-Level Redundancy: This involves having multiple parallel functional units, such as numerous CPU cores. In this arrangement, the failure of one or more cores does not compromise the overall functionality of the system.
- Array Redundancy: This type of redundancy adds spare structures that can replace defective ones. A common application of array redundancy is in cache memory, where spare elements substitute for faulty ones to maintain performance.
- Dynamic Queue Redundancy: This approach entails the ability to mark and disable defective elements dynamically, thereby preventing their use and maintaining the integrity of the system.

By leveraging these redundancy strategies, processors can achieve higher reliability and easier repairability, ensuring robust performance even in the presence of faults.

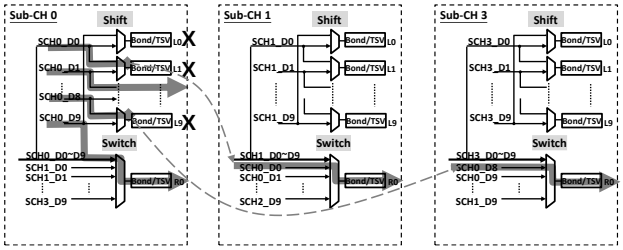


Fig. 14. Redundancy and repair.

Since the die-to-die are connected through dense micro bumps or advanced bonds, defect detection and repair are essential to guarantee chip yield after packaging. All three strategies above can be applicable to chiplet interconnects.

Fig. 14 is an example where a 'Shift and Switch Repair" concept [21] is used to fix three failed lanes with just one-over-ten redundancy in hardware overhead. Probability calculation based on binomial distribution [58] shows that this 30+3 joint repair method can achieve 1000x lower failure rate than 3 separate 10+1 groups.

For mission critical applications, such as automotive, where AI/ML are taking shape, the stake of a processor failure is high, a dynamic reliability management technique where a processor can respond to changing application behavior to maintain its lifetime reliability target is beneficial [59].

Balancing repairability and signal integrity involves making strategic tradeoffs. For instance, separating power and ground bumps is advantageous in preventing permanent short circuit failures [22]. However, this approach may lead to increased area overhead or a compromise in signal integrity.

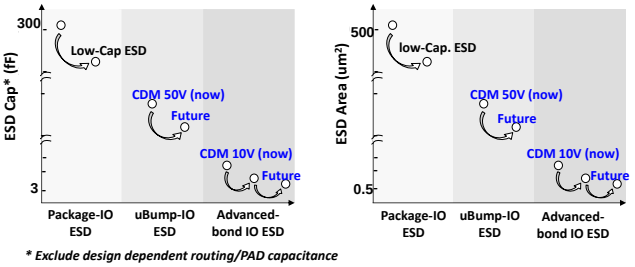


Fig. 15. ESD roadmap

H. *ESD Migration*

As the industry pushes for higher bandwidth, it is crucial for ESD structures to scale accordingly to prevent the large size and high capacitance of ESD diodes from becoming scaling bottlenecks. Failure to address this issue will limit IO energy efficiency. We need to establish an aggressive ESD roadmap for IOs incorporating micro bumps and advanced bonds. Fig. 15 highlights the trend for ESD capacitance and area scaling [6], also showing a reduction in charge device model (CDM) voltage to be supported by the industry.

I. *Power Delivery*

Take the UCIe advanced-package 10-column form-factor as an example: The current density can reach over 4.1A/mm² based on a x64-lanes module size of 388.8μm by approximately 1000μm, under 32Gbps operation and 0.6pJ/bit energy efficiency at 0.75 volts. With such a high current density, we have observed severe electromagnetic (EM) reliability issues on power/ground bumps, which were found to be three times higher than the EM limit allowed by design rules. This issue was mitigated by changing the bump material, but we also had to add more power/ground bumps and update the UCIe bump map to boost reliability and performance.

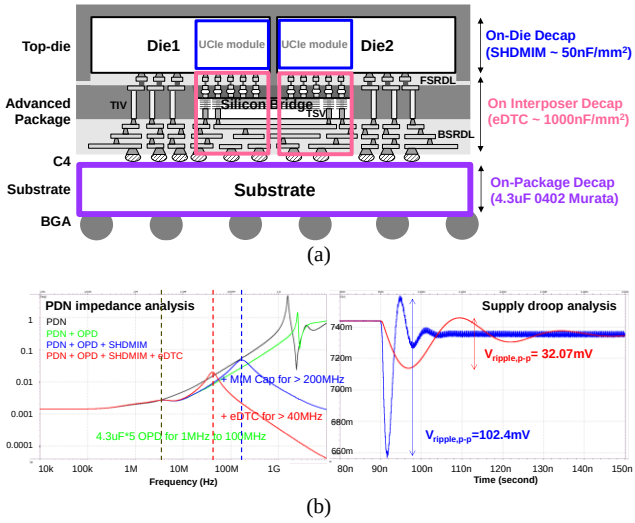


Fig. 16. Decoupling capacitor strategy for power delivery network.

Additionally, the UCIe spec supports clock-gating mode. Going from idle to mission mode introduces a worst-case dynamic current (di/dt), leading to significant voltage droop. This results in higher bit error because of a reduced timing and voltage margin. The most effective di/dt reduction approach is to rely on on-die or on-package decoupling capacitors to suppress the noise ripple. The decoupling cap strategy involves, from top to bottom (See Fig. 16-a), utilizing such as: A) on-package discrete de-coupling capacitors (OPD) typically in the μF range, B) in-package de-coupling capacitors, such as embedded deep trench capacitor (eDTC) on a Si-interposer with greater than 1000nF/mm² capacitance density, and C) On-die decoupling capacitors, which include super high-density MIM capacitors (SHDMIM) with a capacitance density of roughly 50 nF/mm², and device capacitors with a capacitance density of around 10 nF/mm² [29] [49]. Capacitors located on or near the top dies exhibit lower series resistance but also have a lower capacitance density. As the distance from the top die increases, the series resistance also increases. Therefore, when determining the optimal decoupling capacitor strategy, one must consider various factors including technology, cost, area, and noise specifications.

Fig. 16-b shows an example of power impedance optimization and the voltage ripple analysis results [6] [49]. Different capacitors are utilized to suppress the power impedance in respective frequency range. OPD serves to enhance power impedance in the 1MHz~100MHz range. The on-die SHDMIM suppresses the high frequency part beyond 200MHz. And the additional in-package eDTC can further suppress the impedance to even lower frequency range as 40MHz. With eDTC, the voltage ripple was suppressed from 102.4mVpp to 32.07mVpp to be near the targeted 30mVpp specification.

Finally, if a system exceeds its voltage droop tolerance, a comprehensive system-level strategy must be implemented to meet the required low bit error rates. Potential solutions include:

a) Reducing di/dt through lane staggering, which involves transitioning lanes in and out of its idle-state

one at a time. While this method can mitigate voltage droop, it has the drawback of increased link latency.

b) Reducing di/dt by increasing the background current during clock-gating periods. This can be achieved by keeping some or all idle lanes active. Although effective, this approach results in higher power consumption [11].

c) Reducing di/dt by lowering the operational data rate, which, while helpful in managing voltage droop, would lead to a degradation in system performance.

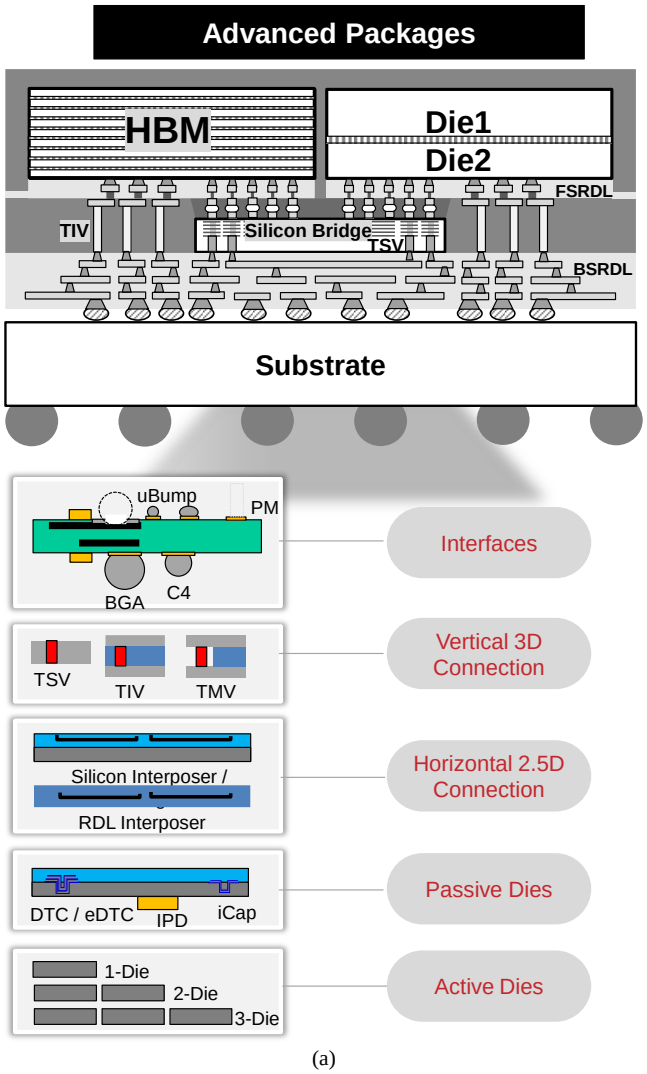
V. Comprehensive 3DIC Design Flow

As illustrated in Fig. 17-a, advanced packaging architecture encompasses a diverse array of package options. These options include varying the number of dies at each level and incorporating various passive devices such as Deep Trench Capacitors (DTC) and Integrated Passive Devices (IPD). The architecture also supports different types of horizontal connections, including silicon interposers and organic interposers, as well as various vertical connections like through silicon vias (TSV), through interposer vias (TIV), and through mold vias (TMV). Additionally, it offers multiple interface types, including advanced bonds, micro bumps, and C4 bumps, along with different stacking orientations such as face-down, face-up, face-to-face, and face-to-back.

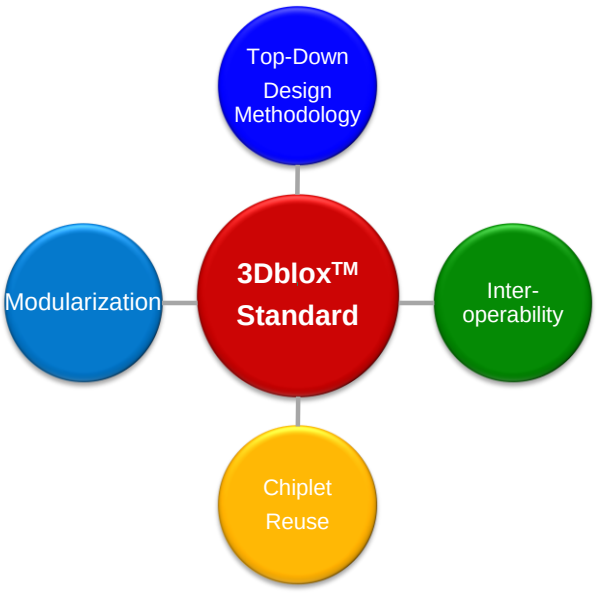
The diverse range of packaging technology offerings within a single or multiple vendors, coupled with the numerous possible combinations, significantly complicates the design process. Additionally, different EDA tools are required for various physical integration and verification tasks, involving multiple IP and tool vendors. Current EDA tools, workflows, and methodologies has been evolving significantly to meet the demands of complex 3D integrations.

To address the challenges in 3D-IC design, the 3Dblox™ open standard [60] has been established and gained wide industry acceptance. As depicted in Fig. 17-a, 3Dblox™ introduces a modular approach, where each physical component within a 3D package is categorized and abstracted into specific modules. Designing a 3D system involves instantiating these modules to create interconnected objects using a high-level programming language, organized hierarchically, similar to traditional SoCs.

See Fig. 17-b for the key features of 3DBlox. To streamline the design process, we integrated assertions directly into the language, enabling a top-down, correct-by-construction design methodology. The hierarchical instantiation feature enhances the reuse of chiplets, promoting design efficiency. With major EDA vendors and semiconductor manufacturers adopting 3Dblox, chiplet integration has become more seamless and significantly more efficient, thanks to improved interoperability. This integration will further accelerate the development and maturity of the 3D-IC ecosystem.



(a)



(b)

Fig. 17. (a) Abundant Choices of 3DIC Architectures (b) 3Dblox unification infrastructure.

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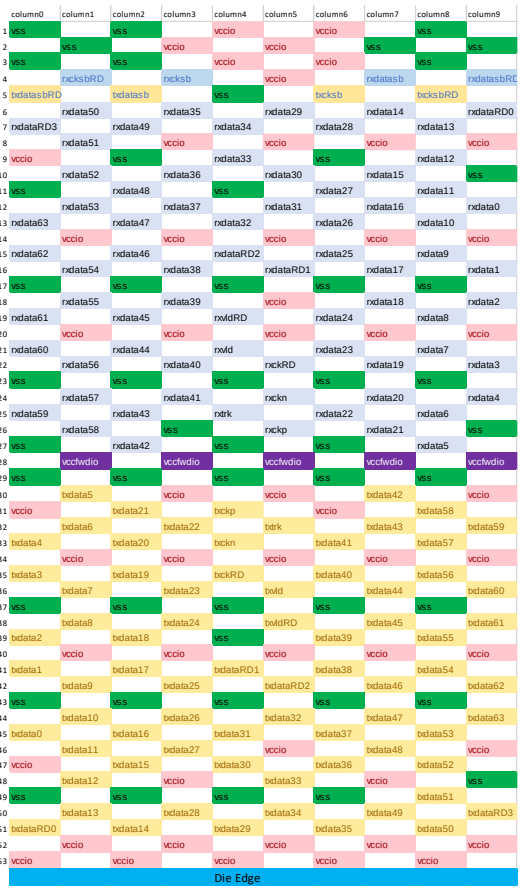
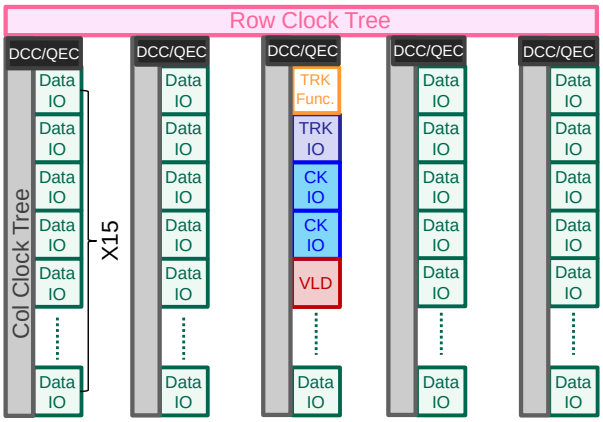
VI. Future Development Trend



(a)



(b)

Fig. 18. (a) UCIe 2.0 bumpmap example (b) Modular design for Chiplet I/F.

A. Design Modularization

Six UCIe form factors [11] have been defined for advanced packages supporting data rates from 4 to 32 Gbps. Fig.18 (a) shows one example of the form-factors. Given the various bump pitches, column numbers, data rates, and technology nodes, the development of intellectual property (IP) becomes a time-consuming and resource-intensive process. To mitigate this challenge, a modularization concept and a compiler-compatible scheme, as illustrated in Fig. 18 (b), have been implemented.

In this approach, the die-to-die interconnect is segmented into repeatable blocks, such as IO lanes, and commonly shared blocks, including DLL, PLL, DCDL, and calibration circuits. Specific floorplan elements, such as clock trees, can be customized and compiled to meet different target specifications.

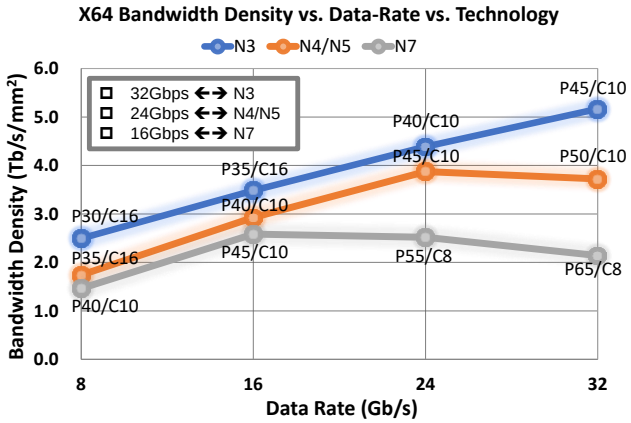


Fig. 19. Technology and bandwidth scaling (Note: P30/C16 refers to 30µm bump pitch, UCIe 16-column form factor)

B. Bandwidth and Energy Efficiency Scaling

Bandwidth density and energy efficiency continue to be the focus for next generation chiplet interconnects.

The package bump pitch and technology nodes significantly impact bandwidth density. Fig. 19 illustrates the area bandwidth density trend based on our first-order estimate using realistic process and package technology scaling factors. To enhance bandwidth density, one can increase the link data rate and/or decrease interconnect bump pitch. However, higher data rates require stronger circuit driving strength and calibration, leading to larger circuit areas. Consequently, bump pitch may need to be adjusted. For instance, with N7 technology, a 45µm bump pitch (P45) supports 16Gbps, while 55µm (P55) and 65µm (P65) are needed for 24Gbps and 32Gbps, respectively, resulting in a decline in area bandwidth density beyond 16Gbps. In contrast, N4/N5 (4nm/5nm) technology supports increased bandwidth density with a data rate up to 24Gbps. N3 allows further bandwidth increase. Design and technology co-optimization will likely modify the trend line slightly, but in general, more advanced technologies like N3 (3nm) offer the benefit of achieving higher area/shoreline bandwidth density and energy efficiency [61].

Taking a different perspective on shoreline bandwidth density, the above study was based on UCIe bump map constraints, resulting in a higher data rate correlating with higher shoreline bandwidth density. This contrasts with the evaluation in [62], which uses pitch scaling in both the x and y directions. As the bump pitch scales down with the data rate while maintaining a bump-limited situation, the shoreline bandwidth density remains constant. In this context,

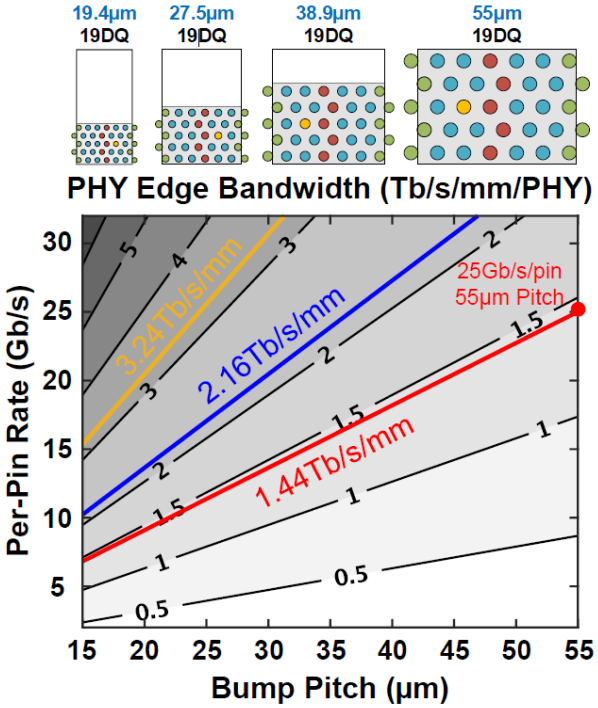


Fig. 20. Scaling for better energy efficiency [62]

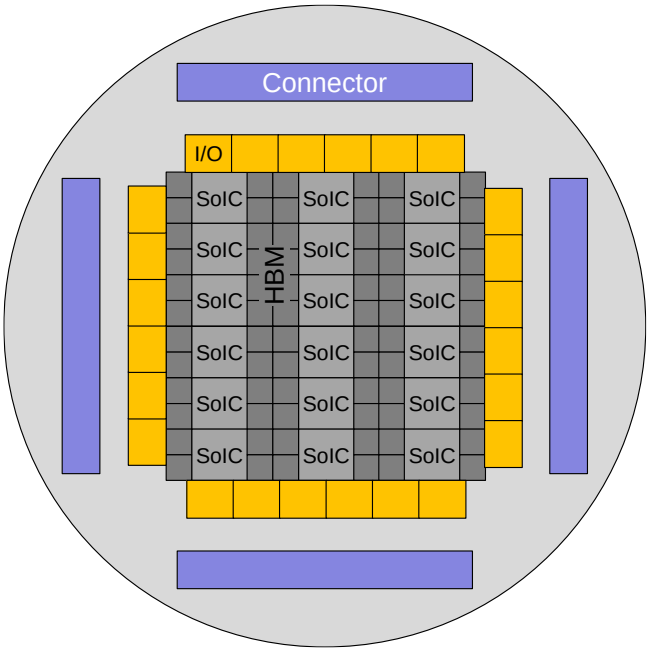


Fig. 21. System-on-wafer scale up (source: TSMC).

lower data rates are expected to enhance energy efficiency due to reduced circuit complexity. Conversely, technology scaling can support more complex designs and increase the data rate for a given bump pitch, leading to enhancements in shoreline bandwidth (e.g., from 1.5 to 2 Tb/s/mm), as illustrated in Fig. 20.

C. *Bigger Systems*

Due to reticle size limitations, the recent trend in AI/ML development is the scaling up at the wafer level (Fig. 21) [13] [14] [15]. By combining the solutions provided by 3DFabric (or equivalent), we can effectively utilize SoIC for integrating SRAM+CPU and HBM+GPU, LSI for integrating CPU+GPU (high density / near reach), LSI for integrating xPU to I/O die, passive LSI for eDTC (for on-package decoupling for supply noise mitigation), and RDL for power delivery and longer reach data transfer at large-scale integration. This wafer-level packaging alleviates the constraints imposed by reticle size limit, while necessitating network-on-wafer [13] [14] and heterogenous (serial and parallel) [18] or hybrid (optical and electrical) links [63] for efficient xPU to xPU inter-connections in the near future. Beyond wafer level packaging, fan-out panel-level packaging (FOPLP) [64] [65] is also on the horizon, promising higher packaging throughput, reduced costs, and potentially larger integrated systems at panel-level, where warpage control remains a significant challenge throughout the entire packaging process [66] [67].

In the meantime, the hunger for higher interconnect data bandwidth density continues, for instance, the UCIe Consortium is working on a 48/64Gbps proposal for inter-die interconnect. For system scaling up and scaling out, on package optical waveguide [68] and co-packaged optical engine [69] remain appealing to the industry.

Bigger systems necessitate vertical power delivery with integrated magnetic components for efficient voltage regulation [70] [71]. The larger-scale integration of CPU, GPU, HBM, SerDes, optical engines, and voltage regulators is a significant undertaking, surpassing some of the existing engineering feats [13] [14] [15]. Achieving this requires a collaborative effort across various industry partners to manage different aspects of technology stacks to achieve high performance while ensuring exceptional power efficiency, signal integrity, thermal management, and structural robustness.

As the chiplet ecosystem becomes more robust and 3D-IC design methodologies advance, new possibilities and greater innovations will emerge.

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