Recent Advances of High-Speed Short-Reach Optical Interconnects for Data Centers

Chongyun Zhang, Graduate Student Member, IEEE, Fuzhan Chen, Graduate Student Member, IEEE, Li Wang, Member, IEEE, Lin Wang, Member, IEEE, and C. Patrick Yue, Fellow, IEEE

(Invited Paper)

Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong

Corresponding Author: C. Patrick Yue (e-mail: eepatrick@ust.hk)

This work was supported in part by the Areas of Excellence Scheme of Hong Kong, under the grant no. AoE/E-601/22-R, in part by the General Research Fund of Hong Kong, under the grant no.16205522 and no.16205023, and in part by the HKUST-Qualcomm Joint Innovation and Research Laboratory.

(Chongyun Zhang, Fuzhan Chen, and Li Wang are co-first authors.)

ABSTRACT The ever-increasing demand for data centers and high-performance computing systems necessitate power-efficient, low-latency, and high-density interconnect design. This article reviews and analyzes recent design challenges and advances of optical transceiver, phase-locked loop (PLL), and clock and data recovery (CDR) for data center applications with a distance of ~100 m. At the transmitter side, non-idealities of the widely used vertical-cavity surface-emitting laser (VCSEL) are described, followed by reviews on existing compensation techniques for those non-idealities. At the receiver side, trade-offs between gain, bandwidth (BW), noise, and linearity in PAM-4 optical receiver design are introduced, and design methods to improve the power efficiency and BW density are particularly discussed. Regarding clock generation which directly affects the performance of the transceiver, compact PLL design techniques focusing on in-band phase noise reduction and low-jitter performance are described. The signal integrity of PAM-4 signal becomes more susceptible to noise and jitter due to reduced signal level spacing. To address the uncorrelated jitter accumulation within the CDR which limits the signal quality and transmission distance, jitter compensation schemes in CDR design are described. And the clock distribution techniques for multi-lane transceiver systems are discussed.

INDEX TERMS Clock and data recovery (CDR), data center interconnect, four-level pulse amplitude modulation (PAM-4), optical receiver, phase-locked loop (PLL), transmitter, vertical-cavity surface-emitting laser (VCSEL).

I. Introduction

The demand on the data centers with higher-speed, lower-cost and more energy-efficient solutions keeps increasing driven by the proliferation of data-intensive applications, such as 5G communications, IoT, cloud services, deep neural networks and machine learning. High-density, low-power interconnects with a distance of lower than 100 m become crucial in high-performance data centers [1]. As the data rate continues to increase, the traditional electrical interconnects within data centers have been pushed to their limits. Electrical I/Os have reached a bottleneck where it is impossible to overcome the bandwidth (BW) limitation without sacrificing other performance metrics like power, reach or cost. Thus, the trend towards optical links has continued to grow due to the benefits provided by the optical channels and the development of electrical-to-optical (E/O) conversion technologies [2]. The modulation format for wireline applications, such as Ethernet [3] and PCIe [4], are migrating towards four-level pulse amplitude modulation (PAM-4) instead of conventional binary-coded non-return-to-zero (NRZ) signaling to double the data rate for a given system BW. However, adapting to PAM-4 comes at the cost of enforced linearity constraints in both

optical and electrical components, and the signal integrity becomes more susceptible to noise and jitter introduced from channel crosstalk and active device noise.

Intensity-modulation and direct detection (IM/DD) optical interconnects are being pushed for 400G Ethernet standards such as IEEE 802.3cm which defines 50-Gb/s per-lane links in four and eight fiber configurations to support traffic up to 400 Gb/s [5]. For short-reach applications (<100m), integrating the transceiver front end like drivers and transimpedance amplifiers (TIAs) in CMOS helps reduce the electrical loss, cost and component counts [6], as shown in Fig. 1, making it a power-efficient solution to extend data rate capacity. Although optical channels have a negligible loss, the opto-electrical components like the vertical-cavity surface-emitting laser (VCSEL) or the photodiode (PD) in the signal path are typically BW-limited and bring extra nonlinearities. The driver and the TIA are designed to compensate for the nonlinearities of optical devices and expand the overall BW. The integration of serializer and sampler with optical interface electronics further scales the BW density and power efficiency, which is preferable for data center applications. Phase-locked loops (PLLs) provide clock generation in high-speed transmitter (TX) design. As the 1- unit interval (UI) period reduces with the increase of data rate, low-jitter clock is needed and becomes crucial to meet the stringent timing requirement. At the receiver (RX) side, the synchronized clock can be obtained from a forwarded clock originating from the TX side in short-reach communication scenarios. For optical and long-reach wireline I/Os, the synchronized clock is commonly extracted from the received data using a clock and data recovery (CDR) loop.

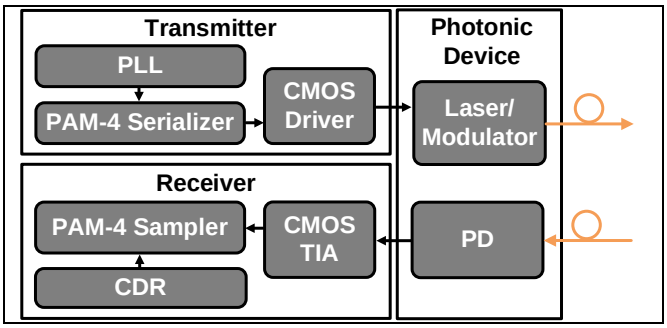

FIGURE 1. Simplified block diagram of a high-speed optical interconnect for data centers.

In this article, based on previous works [7], [8], [9], [10], [11] [12], and [13], we review and analyze the design requirements and challenges of high-speed optical interconnects for data centers. Section II describes the VCSEL non-idealities and PAM-4 optical TX design method to counteract those non-idealities. Section III introduces the design tradeoffs and methods for area and power-efficient PAM-4 optical RX. Section IV introduces the clock generation and distribution, including the low-jitter PLL and the CDR with jitter compensation. Measurement results of TX, RX, PLL and CDR are given in Section V. The conclusion of this article is drawn in Section VI.

II. OPTICAL TRANSMITTER DESIGN

A. VCSEL CHARICTERICTICS

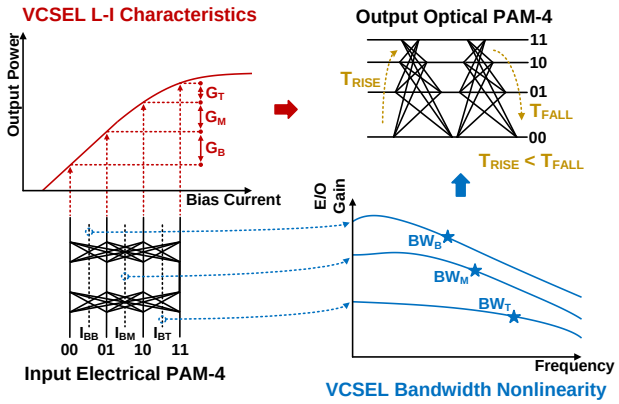

FIGURE 2. Non-idealities of VCSEL.

Taking advantages of low cost and low power consumption, VCSEL has been the mainstream laser in high-speed short-reach optical interconnects inside data centers to perform E/O conversion. However, three non-idealities of VCSEL hinder further improvement of the link speed, as illustrated in Fig. 2. Firstly, the slope of VCSEL's light-current (L-I) characteristics, denoted as η, changes with the bias current [14]. With the increase of the bias current, the slope η decreases. Secondly, VCSEL's BW is also nonlinear with respect to the bias current [2]. With the increase of the bias current, the BW of VCSEL increases. These two non-idealities are negligible when using VCSEL for modulating NRZ signals. However, for optical links using PAM-4 for higher modulation efficiency, the two nonlinearities become issues. When the VCSEL transforms the top, middle, and bottom sub-eyes, the bias currents for the VCSEL can be seemed as I_{BT}, I_{BM}, and I_{BB}, respectively. For the bottom sub-eye, η is the largest, as I_{BB} the smallest compared with I_{BM} and I_{BT}. Inversely, for the top sub-eye, VCSEL has the smallest η. As a result, the amplitude of the top sub-eye is the smallest and that of the bottom sub-eye is the largest. Similarly, owing to the BW nonlinearity, the widths of the three sub-eyes are also different, with the width of the top sub-eye largest and that of the bottom sub-eye smallest. Both non-linearities distort the output optical eye diagram shown in Fig. 2. Furthermore, VCSEL's response to rising transition is faster than falling transition [15]. This asymmetric response issue deteriorates with the decrease of bias current and the increase of the signal data rate. Consequently, the optical eye diagram exhibits an obvious skew. The skew narrows the sampling window of the PAM-4 signal and complicates the implementation of the optical RX.

B. VCSEL TRANSMITTER ARCHITECTURE

Several PAM-4 VCSEL TXs have been proposed recently to overcome the above non-idealities. [16] presents a 64-Gb/s quarter-rate PAM-4 TX in 65-nm CMOS. The simplified architecture of the TX is depicted in Fig. 3(a). A three-tap

analog feedforward equalizer (FFE) is implemented to extend the BW of the E/O system. Moreover, the output driver adopts a push-pull topology, by which the rising and falling transitions of the TX output can be independently adjusted. In this way, the issue of VCSEL's asymmetric response can be resolved. However, as both the PAM-4 top sub-eye and bottom sub-eye are determined by the less significant bit (LSB) data slice, the TX cannot relieve the non-linearities in η and BW versus bias current. [17] implements a 64-Gb/s VCSEL TX in 40-nm CMOS using a similar architecture to [16]. A T-coil is introduced at the output node to boost the BW. And the quality of the optical PAM-4 eye diagram is enhanced compared with that presented in [16]. However, the two non-linearities still have not been properly settled. Some works use the architecture with DAC-based FFE depicted in Fig. 3(b). In [18], a 5-bit DAC is implemented to generate pre-distorted PAM-4 signals with 2.5-tap non-linear FFE. The 5-bit DAC includes a 2-bit symbol DAC and a 3-bit equalization DAC. The codes for the symbol DAC are determined by the current LSB and the most significant bit (MSB) data, while those for the equalization DAC are chosen from a 32x3 lookup table (LUT) depending on the past, current, and future symbols. [19] presents a VCSEL TX using a similar architecture, but the tap number of the non-linear FFE is reduced to 2 including a main-tap and a post-tap. A 7-bit DAC is implemented to generate the equalized PAM-4 signal. The DAC-based FFE could control all 16 transitions of the PAM-4 electrical signal, and thus it can theoretically fully compensate for the VCSEL non-idealities on conditions that the number of the FFE tap and the resolution of the DAC are adequate. However, the DAC-based FFE would increase the latency of the optical link. And with the increase of the tap number, hardware overhead from LUT and digital MUX will increase exponentially.

In [7] and [8], a PAM-4 VCSEL TX with a piecewise compensation scheme is presented. Its conceptual architecture is depicted in Fig. 4. To separately control the three PAM-4 sub-eyes, the input LSB and MSB data are encoded to three unary-weighted data streams. After that, the three data streams determining three sub-eyes are independently processed by three data slices denoted by DS_T, DS_M, and DS_B. The structures of the three data slices are the same. In each slice, serializer is used for serializing the sub-rate unary-weighted data streams to a full-rate unary-data stream. In this way, the BW requirement for the binary-to-unary encoder can be reduced. The equalizer is implemented to control the BW of the data slice. As the BW for the middle sub-eye is smaller than that for the top sub-eye but larger than that for the bottom sub-eye, the equalizer strength in DS_M should be weaker than that in DS_T but stronger than that in DS_B. In this way, the BW nonlinearity can be resolved. The slope η nonlinearity can be settled in a similar way by piecewise tuning the variable-transconductance (Gm) cells of the three data slices. The Gm of DS_M should be smaller than that of DS_T but larger than that of DS_B. Finally, to relieve the asymmetric response issue, the pre-emphasis circuit is included in each slice to speed up the falling transitions. As the discrepancy between the rising and falling transition speeds of the bottom sub-eye is the biggest, the pre-emphasis strength of DS_B should be the strongest, while that of DS_T should be the weakest. In summary, leveraging the binary-to-unary encoder, this TX can independently control the characteristics of the three PAM-4 sub-eyes. Furthermore, by introducing the equalizer, variable-Gm cell and pre-emphasis circuit in the three unary-weighted data slices, slope η nonlinearity, BW nonlinearity and asymmetric response can be well compensated, respectively. Compared with the TX architecture depicted in Fig. 3(a), which cannot fully compensate for the two nonlinearities, the TX in Fig. 4 resolves all three non-idealities in a mixed-signal way. Moreover, compared with the VCSEL TX using DAC-based FFE as depicted in Fig. 3(b), the impact of the compensation methods in this TX on the link latency can be much smaller.

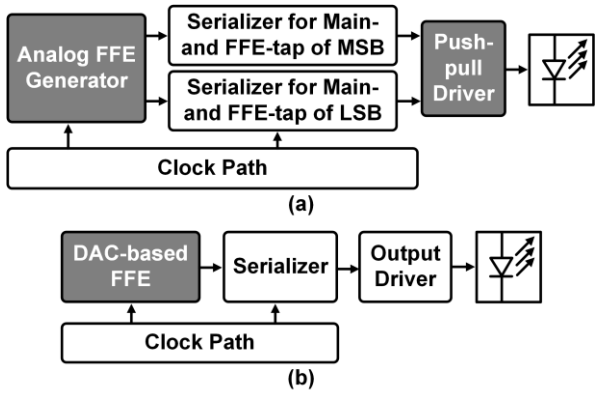

FIGURE 3. (a) VCSEL TX with analog FFE and push-pull output driver, and (b) VCSEL TX with DAC-based FFE.

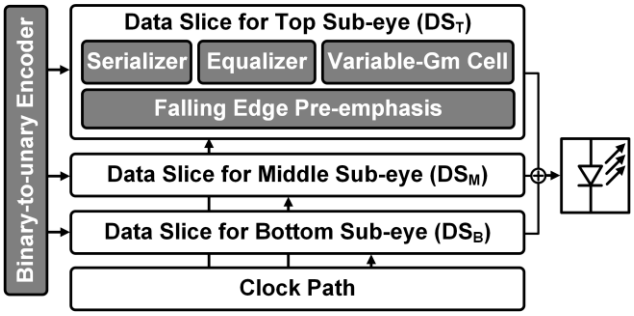

FIGURE 4. Architecture of the VCSEL TX with piecewise compensation scheme.

The key components of the VCSEL TX in Fig. 4 are the variable-Gm cell and falling edge pre-emphasis circuit. Fig. 5 illustrates the schematics of these two components. For the Gm cell, to support the 2-V anode bias voltage required by VCSEL, a cascode structure is adopted to avoid breakdown. Source-degenerated resistor (R1) and capacitor (C1) are inserted to boost the BW of the Gm cell. The output of the pre-emphasis circuit is connected to the source of M4 which is a low-

This article has been accepted for publication in IEEE Open Journal of the Solid-State Circuits Society. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJSSCS.2025.3526132

impedance node to reduce the impact on BW. The pre-emphasis circuit consists of three branches which differ only in transistor sizes. For each branch, the top transistor is gated by the negative input denoted as IN_N, while the bottom transistor is gated by the delayed positive input denoted as $IN_{P,delayed}$. The delay is achieved by a poly resistor in combination with the parasitic capacitance of M5~M7. The middle transistor is gated by a 3-bit control signal SW<0:2> to adjust the strength of pre-emphasizing. During rising transitions of IN_N, the current flowing through VCSEL denoted as I_{VCSEL} decreases. Meanwhile, $IN_{P,delayed}$ falls. As $IN_{P,delayed}$ has a transition speed slower than IN_N, there is a period when both $IN_{P,delayed}$ and IN_N are high, creating a current pulse denoted as I_{pulse}. I_{pulse} accelerates the falling of I_{VCSEL}. In this way, the asymmetrical rising/falling response issue of VCSEL can be relieved. The single-ended output of the Gm cells of the three data slices DS_T, DS_M, and DS_B are combined at the output node of the TX into PAM-4 signal, which is then delivered to the anode of VCSEL via a T-coil and a bond wire. The cathode of VCSEL is wire-bonded back to the TX chip for biasing and supply filtering.

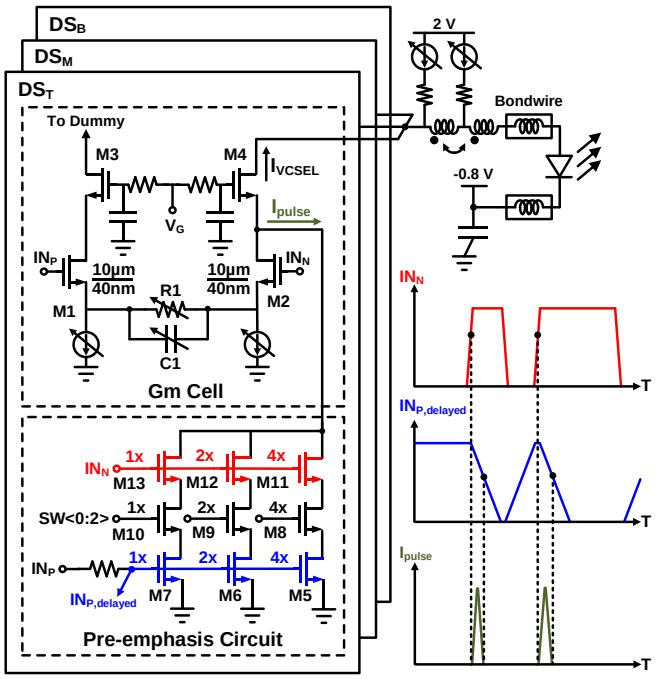

FIGURE 5. Schematics of the VCSEL driver and working principle of the pre-emphasis circuit.

III. OPTICAL RECEIVER DESIGN

A. PAM-4 OPTICAL RECEIVER ARCHITECTURE

The tradeoffs between gain, noise, BW, and linearity make the power-efficient, low-latency, and high-density PAM4 optical RX design very challenging. As illustrated in Fig. 6 (a), to break the tradeoffs, a two-stage front-end design method using CTLE in the TIA to compensate for low-BW transimpedance stage (TIS) is proposed in [20]. At 25-Gb/s, this method produces a significant noise reduction compared to a single-stage TIA. However, the over peaking of CTLE causes extra high-frequency noise and this method becomes power hungry when data rate keeps increasing. [21] uses 2-stage CTLE to boost the TIA BW to 32 GHz in 16nm CMOS, achieving a 0.69-pJ/bit power efficiency. As shown in Fig. 6 (b), inductive multi-peaking scheme is widely used in TIA design, but large area occupied by inductors makes such method unsuitable for high-density design and inductors are in lack of tunability. [22] achieves an impressive BW of 60 GHz in 28-nm CMOS using various inductive peaking techniques, but at the cost of ~0.25 mm^2 area and 0.96-pJ/bit power efficiency. Integrating the equalizer into sampler instead of the TIA provides another option for optical RX design. [23] combines the low-BW TIA with a four-tap decision feedback equalizer (DFE) to overcome the noise-BW tradeoff. A very good sensitivity of –16.8 dBm is achieved in 65-nm CMOS, but the data rate is limited to 12 Gb/s and the 1.9-pJ/bit energy efficiency is still too high. [24] implements a 32-Gb/s PAM-4 optical RX in 40-nm CMOS by combining the TIA with a two-tap DFE. However, three-stage cascaded amplifier-based TIA and three-stage cascaded VGA and CTLE with inductive peaking result in a high power consumption of 4.59-pJ/bit energy efficiency and a rather large area of 0.029 mm^2. [25] achieves the first 100-Gb/s PAM-4 optical RX in 28-nm CMOS by designing a low-BW TIA followed by a PAM-4 sampler including a two-tap FFE and a two-tap DFE. The RX achieves high data rate and good sensitivity, and a distributed current-integrating summer helps close the DFE loop. However, the four-stage pre-amplifier and three-stage post-amplifier with series and shunt peaking in the TIA design and the current-integrating summer are power-hungry and area-inefficient, resulting in a 3.9-pJ/bit power efficiency. In [9], a 48-Gb/s PAM-4 optical RX is achieved in 28-nm CMOS. An energy- and area-efficient TIA front end is realized to preserve the linearity and gain-BW product by removing the CTLE and inductive peaking and employing transadmittance-stage transimpedance-stage (TAS-TIS) topology. Instead of boosting the BW of the TIA, the FFE and DFE at the PAM4 sampler help compensate for the residual inter-symbol interference (ISI) from TIA output and recover the data, thus achieving compact area and low power consumption, as shown in Fig. 6 (c).

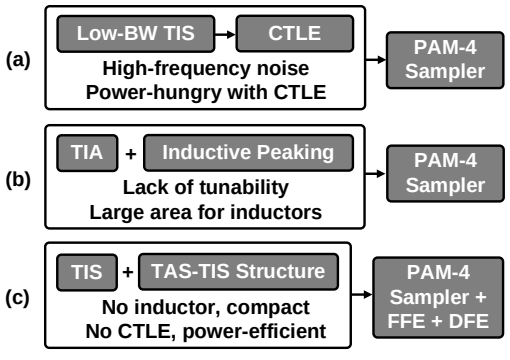

FIGURE 6. (a) A two-stage design method using CTLE to compensate for the low-BW TIS. (b) TIA design using distributed inductive peaking. (c) Post-TIA equalizer integrated at sampler to improve overall BW and sensitivity.

B. PAM-4 OPTICAL RECEIVER DESIGN EXAMPLE

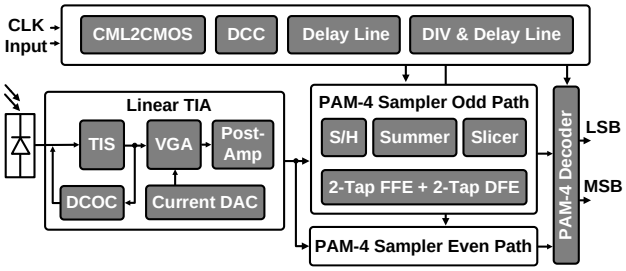

FIGURE 7. Architecture of the PAM-4 optical RX.

Increasing the feedback resistance of TIA helps lower the input-referred noise, with the penalty of a reduced BW and additional ISI. For PAM-4 optical RX design, as demonstrated in [6], by compensating the ISI penalty at the subsequent sampler using FFE and DFE, the overall sensitivity can be improved. Based on this principle, the conceptual architecture of [9] is designed and depicted in Fig. 7. The linear TIA includes a TIS, a variable gain amplifier (VGA), and a post-amplifier (post-amp) to accommodate large input dynamic range with negligible BW variation. After two half-rate sample/hold (S/H) and summers, three slicers in odd/even path and a DAC are employed with a two-tap FFE and a two-tap direct DFE to recover the PAM-4 to three-bit digital thermometer codes. A track-and-regenerate slicer is used to meet the stringent timing constraint of direct DFE at speed higher than 24 GBaud. The recovered thermometer codes are then converted into two-bit binary codes, including a MSB and a LSB output, which are deserialized and sent to off-chip bit error rate (BER) testing. The clock path takes in external half-rate differential clock signals and amplifies them to rail-to-rail.

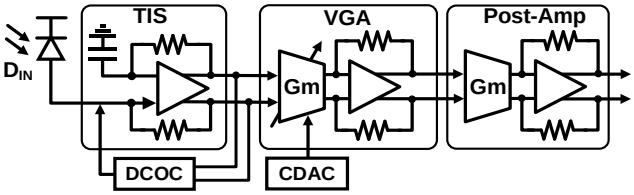

FIGURE 8. Block diagram of CMOS linear TIA.

Fig. 8 shows the block diagram of the CMOS TIA. Passive inductors and CTLE are avoided here, which makes the TIA compact and energy efficient. A pseudo-differential TIS is used as the first stage, and therefore the single-ended to differential circuit is not needed. The VGA provides over 20 dB of dynamic range, and the post-amp provides over 10 dB gain. Both the VGA and the post-amp adopt TAS-TIS topology and use active inductors instead of passive inductors to save area. The common-mode photocurrent and input referred offset voltage are cancelled by the dc offset cancellation (DCOC) loop. At the TIA input, the pseudo-differential push-pull transimpedance stage provides the single-ended to differential conversion, and the TIS employs a current tail for better supply noise rejection [26]. The schematic of VGA is shown in Fig. 9 which adopts TAS-TIS topology but controlling the gain by changing the Gm of the first transadmittance stage, and resistor R_F at second TIS is fixed to maintain a constant BW over gain variations. Therefore, the proposed VGA combines the advantages of both the Gilbert-cell-based VGA and the TAS-TIS structure. With an overall gain of $Gm_{TAS}*R_F$, the input impedance of TIS is reduced to R_F/A_{TIS}, and the low output impedance $1/Gm_{TIS}$ also provides larger capacity for driving the load, where Gm_{TAS} and Gm_{TIS} are the transconductance of TAS and TIS respectively, and A_{TIS} is the gain of feedforward amplifier of TIS. A 5-bit current DAC is used to adjust the VGA gain with a control range up to ~23 dB and the BW variation is less than 0.2 GHz. The full-rate data is then converted into two half-rate data streams at TIA output. The block diagram of half-rate PAM-4 sampler with FFE and DFE is shown in Fig. 10. The FFE is embedded with the S/H circuits by adding the summer to execute the summation of consecutive data sampling. The 3-bit thermometer outputs before and after a SR latch are fed back to the summer to form the first and second tap DFE.

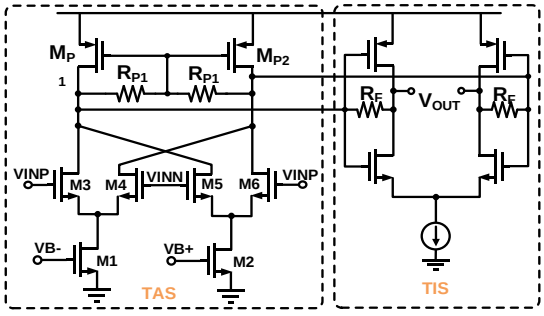

FIGURE 9. Schematic of the proposed Gilbert-TIS VGA.

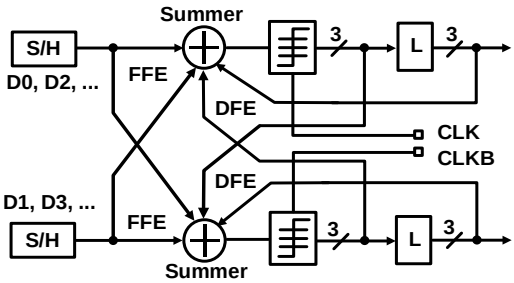

FIGURE 10. Block diagram of half-rate FFE and DFE.

IV. CLOCK GENERATION AND DISTRIBUTION

A. JITTER IN WIRELINE TRANSCEIVER SYSTEM

Jitter in a wireline transceiver system manifest as deviations in the timing of clock or data transitions from their ideal positions. It can be broadly classified into two categories:

random jitter and deterministic jitter. Random jitter is typically caused by various Gaussian noise sources, such as power supply noise, substrate noise, and device noise [27], [28]. In contrast, deterministic jitter arises from specific factors, including cross-coupling, channel loss, and switching power supply effects. Jitter negatively impacts the signal integrity of transceiver systems. On the TX side, it reduces slack time headroom, increases the risk of metastability in the serialization stage, and decreases the horizontal opening of the data eye diagram at the final output stage. On the RX side, uncorrelated jitter between the data and clock signals reduces sampling headroom during the initial sampling stage.

PLL and CDR are essential components for low-jitter clock generation and effective jitter tracking. In designing a PLL, the primary focus is on minimizing the phase noise (PN) of the voltage-controlled oscillator (VCO) while balancing the contributions of in-band PN (mainly from the reference, phase detector, charge pump, and loop filter) and out-of-band PN (primarily from the VCO). For CDR, key design considerations include balancing jitter transfer and jitter tolerance while minimizing jitter generation and peaking. Jitter transfer refers to the ratio of the amplitude of jitter at the output of the CDR to the input jitter. Jitter tolerance indicates the maximum jitter amplitude at a specific frequency that the CDR can handle without introducing errors in the recovered data. In a typical CDR, both jitter transfer and tolerance are dedicated by loop BW. A wider loop BW allows for better tracking of input jitter and ensures reliable data decoding [29], [30]. However, it can also result in greater jitter accumulation in the recovered data and clock, affecting the synchronization of subsequent stages. For VCO-based CDRs, wide BW can lead to increased jitter peaking due to second-order loop dynamics and less regulated PN from the VCO. Therefore, the parameters of the CDR loop components and BW must be carefully designed to effectively track input jitter while avoiding additional jitter generation and peaking [31], [32].

B. *PHASE-LOCKED LOOP ARCHITECTURE*

PLLs play a crucial role in providing low-jitter clock generation for wireline and optical transceiver systems. The increasing demand for 800-Gb/1.6-Tb Ethernet necessitates a 56/112-Gbaud signals with 1-UI periods of 17.8/8.9 ps. Meeting this stringent timing requirement requires the root mean square (RMS) clock jitter to be below 100 fs. The design of an integer-N PLL should minimize the in-band PN contribution and balance the jitter contribution from the reference clock and the VCO. For fractional-N PLLs, the allocation of the PLL loop BW should also consider attenuating the jitter induced by the fractional spurs, which can be pushed to the low-frequency range by using a clock-to-integer frequency ratio.

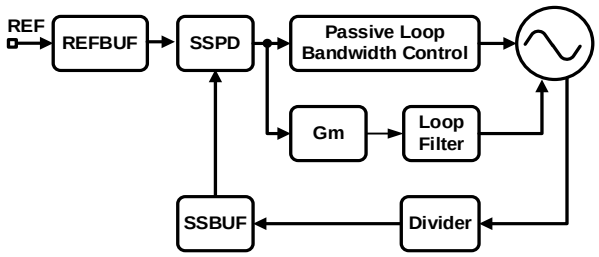

FIGURE 11. Overview of a dual-path PLL architecture.

Over the years, various PLL architectures have been proposed. The most widely used phase-and-frequency detector (PFD) and charge pump (CP) based type-II PLL architecture provides the best robustness and wide lock-in range [33]. However, the PN contribution from the CP [34], integration resistors, and divider can be significant. The sub-sampling PLL (SSPLL) features a much higher phase detector (PD) gain compared to the PFD, and thus can sufficiently attenuate the in-

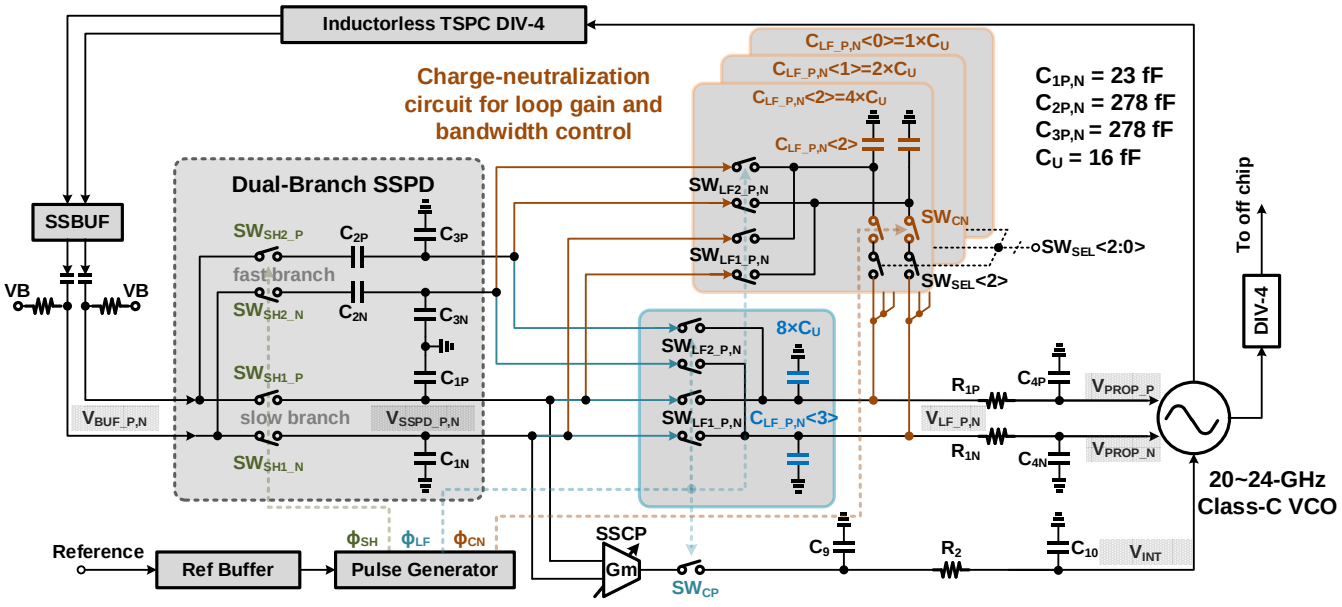

FIGURE 12. System diagram of the DPSSPLL, integrating a P-path with charge neutralization-based gain control scheme, and a narrow-band active I-path.

band PN from the sub-sampling PD (SSPD), the sub-sampling charge pump (SSCP), and the loop filter [35]. Additionally, by directly sampling the feedback signal, the SSPLL can avoid the usage of a divider chain. Recently, the digital PLL (DPLL) has become increasingly popular, featuring outstanding area efficiency by eliminating the loop filter capacitors [36], [37]. The digital implementation also facilitates the nonlinearity calibration, especially for the digital-to-time converter in fractional-N PLLs. In general, analog PLLs, particularly SSPLLs, offer exceptional low jitter performance, while digital PLLs provide better area efficiency, albeit at the expense of relatively higher PN.

C. DUAL-PATH SSPLL DESIGN EXAMPLE

Here, we present an analog SSPLL implementation that achieves optimal jitter performance while attaining a relatively small footprint [10], [11]. As illustrated in Fig. 11, the architecture employs a dual-path (DP) implementation. It features a passive switched-capacitor-based proportional path (P-path) to minimize in-band PN, along with a narrow-band integral path (I-path) that allows for a smaller loop filter capacitance. A charge-domain passive gain control scheme is introduced for the proportional path, enabling a wide gain control range with less than 3 fs of jitter contribution. In the feedback path, a true-single-phase clock (TSPC) divider removes the need for a resonance mode feedback buffer and improves the isolation between the VCO and the SSPD.

Fig. 12 illustrates system diagram of the DPSSPLL. The all-passive differential P-path includes a SSPD with a slow path and a fast feedforward path. The feedforward path incorporates relatively large capacitors (C_3=C_4=278 fF) to introduce a stability zero, enhancing the phase margin. A fixed loop filter capacitor can be designed with an 8-bit capacitor bank (1/2/4/8×Cu) on both the P and N sides of the P-path. Thanks to the differential configuration, the sampled charges on the P- and N-side loop filter capacitors have opposite polarities. The switches SW_{CN} neutralize part of the P/N-side charge in a controllable manner, making the overall P-path gain adjustable. The AC-coupling SSCP in the integral path, similar to the one proposed in [38], ensures minimal offset current. In the I-path, the noises from the SSCP are attenuated by the following loop filter, consisting of 20-pF loop filter capacitance, and thus contributing negligibly to PN. In the feedback path, an inductor-less TSPC divider is utilized as a pre-scaler, offering an area-efficient alternative to the resonance-mode VCO buffer typically used. The fully passive switched-capacitor implementation of the dominant proportional path minimizes in-band jitter contribution. Additionally, the small integration capacitor in the I path, combined with the inductor-less buffer, enables a compact footprint without the need for an off-chip loop filter capacitor.

D. CLOCK AND DATA RECOVERY ARCHITECTURE

CDR topologies include PLLs, delay-locked loops (DLLs), phase interpolators (PIs), and injection-locked (IL) structures. CDR designs based on a PLL topology fall into two categories: reference-based CDR and reference-less CDR. Most existing CDR systems rely on an external reference signal to facilitate low-jitter clock recovery. This external reference, either sourced from off-chip or generated by an on-chip PLL (still with low-frequency external reference), typically possesses significantly lower jitter compared to the input signal. Consequently, reference-based CDR primarily focuses on enhancing jitter tolerance BW while minimizing the generation of additional jitter within the loop. For example, this can be achieved by increasing the gain of the PD while reducing the gain contributions from the subsequent CP and loop filter [29], [30]. In contrast, reference-less CDR, as shown in Fig. 13(a), utilizes an additional frequency tracking loop (FTL) to assist with initial frequency tracking instead of relying on an external reference. During the CDR startup phase, a lock detector (LD) first activates the FTL and then switches to the phase tracking loop (PTL) once the frequency search has stabilized [39]. The dual-loop architecture that incorporates both the FTL and PTL can be further simplified into a single loop, as illustrated in Fig. 13(b). By intentionally creating a mismatch current in the CP, this single loop can search through a wide frequency range, significantly reducing design complexity [40].

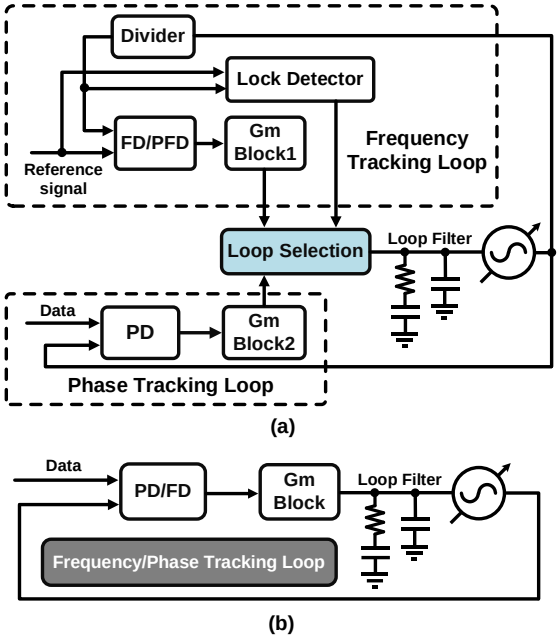

FIGURE 13. Overview of (a) a dual-loop reference-based CDR and (b) a single-loop FD-less reference-less CDR.

One alternative architecture to a CDR-based system is a forwarded-clock system. In a forwarded-clock system, the clock is synchronized from the TX to the RX at the expense of an extra lane. For source-synchronous applications such as chip-to-chip interconnections, DLL-based CDR architecture is widely used, where common PLL-based reference clock generator among multiple channels [41], [42]. Due to the first-order behavior of the DLL, it does not induce jitter peaking or severe jitter generation issues. However, the wide BW of the DLL can potentially introduce additional feedthrough of jitter to the recovered clock and data.

E. CLOCK AND DATA RECOVERY DESIGN EXAMPLE

In typical CDR design, both the jitter tolerance (JTOL) and the jitter transfer (JTRAN) BWs are determined by the CDR loop BW, and such a correlation complicates the clock distribution design. Although wideband CDR improves the JTOL at the initial sampling stage, the captured input jitter and the jitter generated by the CDR will superpose and accumulate at the output of the recovered clock and data. The issue becomes more stringent with the rapid growth of I/O density in high-performance processors and application-specific integration circuits (ASICs) [42], [43]. JTOL and JTRAN decoupling techniques can be used to support wide JTOL BW with suppressed JTRAN to the recovered clock and data of each lane. Various approaches have been proposed for this purpose, including dual-loop configurations [44], [45], and a low-pass loop filter with adjustable loop BW for data and edge samplings [46]. Here, we present a design example that utilizes a jitter-compensation CDR (JCCDR), which provides a wide jitter tolerance BW and reduced jitter transfer.

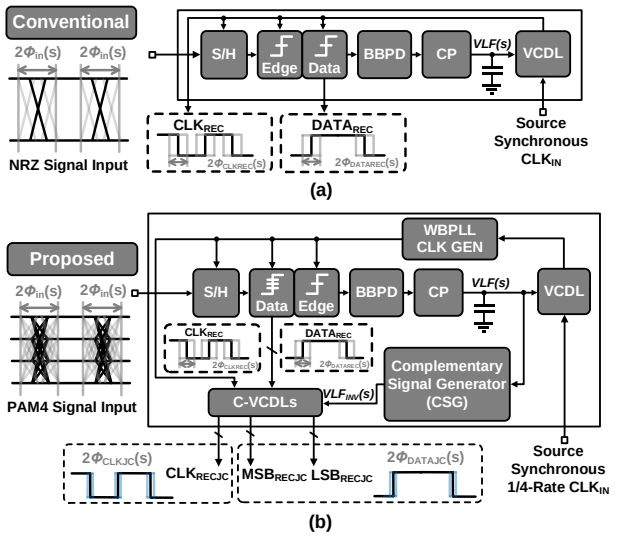

FIGURE 14. (a) System diagram of a conventional DLL-based CDR. (b) System diagram of a PAM-4 JCCDR.

To illustrate the operation of the JCCDR, a conventional DLL-based CDR is shown in Fig. 14(a) as a comparison. Within the DLL BW, the jitter accompanying the input signal is converted proportionally to the loop filter voltage VLF(s) through a bang-bang phase detector (BBPD), a CP, and a loop filter. The jitter information captured by VLF(s) will modulate the VCDL and transfer to the recovered clock, CLK_{REC}. By using the CLK_{REC} to synchronize the S/H and slicers for data recovery, the recovered data $DATA_{REC}$ preserves the same amount of jitter as CLK_{REC}, as illustrated in Fig. 14(a). The JCCDR accommodating PAM-4 input signal is depicted in Fig 14(b) [12], [13]. A DLL tracks the static phase skew and jitter between the input PAM-4 signal and a forwarded clock using a PAM-4 BBPD, a CP, a loop filter, and a VCDL. The DLL yields an output CLK_{DL} which is used as a reference by a wideband PLL (WBPLL) to generate multi-phase clock signals CLK_{REC} for synchronizing the sampling and PAM-4 decoding parts. Clocked by the CLK_{REC}, the PAM-4 decoders recover the most significant bit (MSB_{REC}) and the least significant bit (LSB_{REC}). The recovered CLK_{REC}, MSB_{REC}, and LSB_{REC} are processed by the jitter compensation circuit, which consists of a complementary signal generator (CSG) and VCDL replicas. The CSG detects loop filter voltage VLF(s) and yields an inverted loop filter voltage $VLF_{INV}(s)$, which preserves the same amplitude but inverted phase as VLF(s). The $VLF_{INV}(s)$ controls the VCDL replicas to create the complementary VCDLs (C-VCDLs). The C-VCDLs generate a phase-inverted jitter that counteracts the jitter introduced by the DLL, providing recovered and jitter-attenuated outputs, including CLK_{RECJC}, MSB_{RECJC}, and LSB_{RECJC}.

F. CLOCK DISTRIBUTION

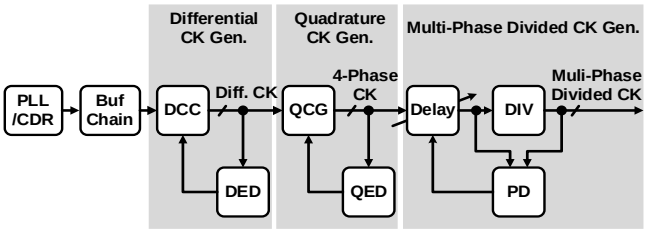

FIGURE 15. Typical clock distribution circuit.

In a multi-lane transceiver system, the clock distribution circuit needs to support various critical functions. First, the high-quality clock generated by the global PLL should be distributed to multiple parallel transceivers without introducing additional jitter. Second, within each local transceiver, the differential error caused by the buffer chain must be corrected before entering the transceiver signal path. Third, in quadrature rate architectures, which are commonly used in high-speed transceivers, it is essential to generate quadrature phases with minimal quadrature error. Any quadrature error can lead to a reduced eye width for the TX or decreased slicing headroom for the RX. Fourth, the clock will be further divided to deserialize data in the RX or serialize data for the TX. The phases of the clocks before and after the divider should be well-aligned to avoid timing conflicts. The architecture of a typical clock distribution circuit is shown in Fig. 15. After the clock is distributed through a buffer chain (Buf Chain) to a local transceiver, a differential clock generator loop is employed to correct errors in both duty cycle and differential signal. This loop consists of a duty cycle correction circuit (DCC) and a differential error detection (DED) circuit. The DED circuit is typically implemented using an XOR-type error detector followed by a low-pass filter and an auto-zero comparator, which convert the duty-cycle error into a 1-bit digital code. The duty cycle error can be corrected by adjusting the slopes of the rising and falling edges using an inverter loaded with a switchable capacitor bank [47].

The subsequent quadrature clock generation circuit includes

a quadrature error correction circuit (QEC), controlled by a quadrature error detection (QED) circuit. To detect quadrature error, a mixer-type detector with a low-pass filter is commonly used to convert the phase error between neighboring quadrature phases into an analog voltage level. Quadrature error correction can be achieved by simply fine-tuning the delays of the four phases. Next, the quadrature clock is divided down to produce multiphase clocks. The phases before and after the divider are compared using a phase detector, which provides feedback to modulate a delay element, ensuring alignment of the clock signals. The phase detector can be implemented using a D flip-flop (DFF), and the delay element can be positioned either before or after the divider. The common approach is to place it before the divider to minimize the number of delay elements required, as one delay element is needed for each phase.

In addition to duty cycle correction, quadrature error correction, and phase alignment, minimizing jitter at the transitions is crucial in designing clock distribution circuits. To reduce random jitter, designers should avoid introducing excessively slow rising and falling edges, which often occur in PIs and delay elements. Conversely, to mitigate noise up conversion during smooth transitions, a larger charging current is typically necessary. To address pattern-dependent jitter, the clock transition time should be significantly shorter than half the clock period. Achieving this requires a backward scaling technique: starting with the finalized data path, calculating the capacitive loading from that path, and then appropriately scaling up the clock buffer to meet the requirements of transition time.

V. MEASUREMENT RESULTS

A. *TRX ELECTRICAL MEASUREMENT*

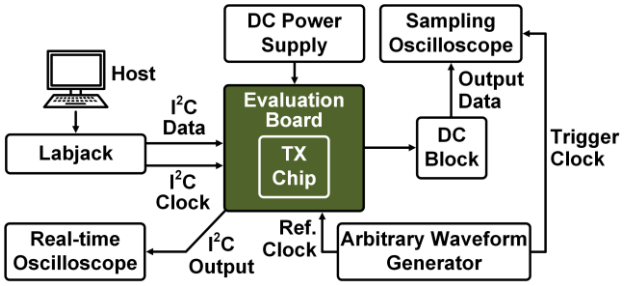

FIGURE 16. Electrical measurement setup for the VCSEL TX.

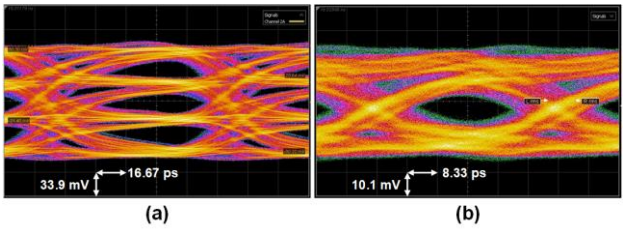

FIGURE 17. Measured (a) 10-Gbaud PAM-4 and (b) 20-Gbaud NRZ electrical eye diagrams.

Although optical TXs are designed for driving optical devices, electrical measurement is necessary before the optical measurement to ensure functionality of the TX chip and facilitate debugging. Fig. 16 shows the electrical measurement setup for the VCSEL TX in [7] and [8]. The TX chip is mounted on a high-frequency evaluation board by bond-wires. I^2C is implemented on-chip to control the operations of the circuits. The serial data and clock for I^2C are provided by a Labjack. And the output of I^2C is delivered to a real-time oscilloscope to ensure that the serial data has been written to the on-chip I^2C correctly. The electrical output of the TX chip is sent via a SMA connector and a DC block to the sampling oscilloscope for eye diagram observation. An arbitrary waveform generator (AWG) generates the reference clock for the on-chip PLL and the trigger clock for the sampling oscilloscope. Fig. 17(a) shows the measured 10-Gbaud PAM-4 eye diagram, demonstrating a single-ended voltage swing of 161 mV. The ratio-of-level mismatch (RLM) of the PAM-4 eye is 94.1%. Fig. 17(b) shows the measured 20-Gbaud NRZ eye diagram with a single-ended swing of 56 mV. It is noted that the output impedance of the TX is designed to be 110 Ω to match the 110-Ω input impedance of VCSEL. And therefore, when the output port of the TX is connected to the 50-Ω input port of the sampling oscilloscope, there will be a severe impedance mismatch between the two ports. This is why the quality of the measured electrical eye diagram is not good, and the measured maximum data rate is not that high. But the measured electrical eye diagrams are still meaningful, as they indicate that the TX works normally.

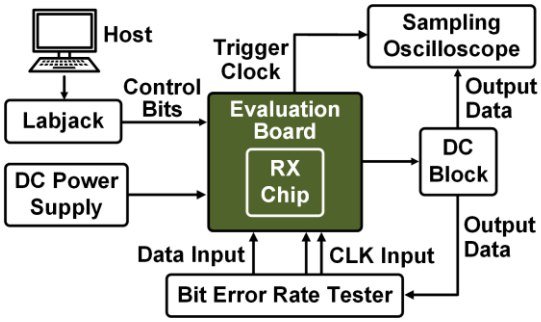

FIGURE 18. Electrical measurement setup for the optical RX.

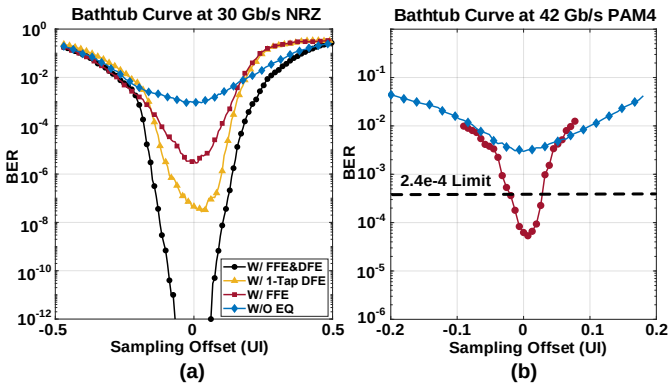

FIGURE. 19. Measured bathtub curves at (a) 30-Gb/s NRZ with 18-mV amplitude and (b) 42-Gb/s PAM-4 with 40-mV amplitude.

Fig. 18 shows the electrical measurement setup for the PAM-4 RX in [9]. Before wire-bonding the RX chip to the PD, time-domain electrical measurements are performed using a BER tester (BERT) as the data source with a 20-dB 67-GHz attenuator. The BERT also generates half-rate differential clock signals for the RX chip, and the chip sends out a divided clock to the sampling oscilloscope as a trigger clock. The electrical output of the RX chip is sent via a SMA connector and a DC block to the sampling oscilloscope for eye diagram observation and to the BERT for BER testing. The measured bathtub curves of 30-Gb/s NRZ with 18-mV amplitude and 42-Gb/s PAM-4 with 40-mV amplitude are shown in Fig. 19. At 30 Gb/s, only 1e-4 BER is achieved when RX FFE is enabled and DFE is disabled, while an error-free eye opening of 0.13 UI is achieved when both FFE and DFE are enabled. At 42 Gb/s, the BER is still higher than 2.4e-4 pre-FEC BER limit when RX FFE is enabled. After enabling both FFE and DFE, the BER can be improved to < 1e-4. It should be noted that electrical measurement is used to verify the function of the RX design before the optical measurement, and the characteristic of the single-ended electrical input signal through the 50Ω PCB trace is different from the signal from the PD output.

B. TRX OPTICAL MEASUREMENT

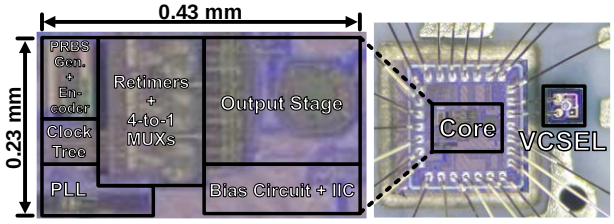

FIGURE 20. Die photo of the VCSEL TX.

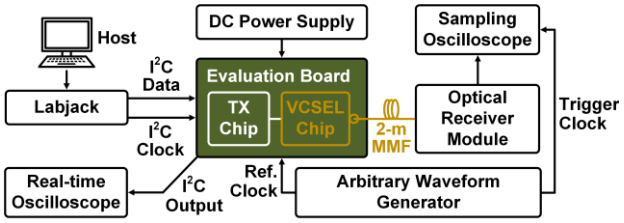

FIGURE 21. Optical measurement setup for the VCSEL TX.

Fig. 20 shows the micrograph of the TX in [7] and [8], in which a commercial VCSEL is wire-bonded with the chip for optical testing. Fig. 21 presents the optical measurement setup for the VCSEL TX. The control part and the DC power supply are the same as the electrical measurement setup described in part A of this section. For the high-speed part, an AWG generates reference clock for the on-chip PLL inside the TX. With the clock, the TX outputs the high-speed electrical signal to the VCSEL, and the VCSEL performs E/O conversion. A multi-mode fiber (MMF) with a length of 2 m is used to couple the light from the VCSEL to an optical RX equipment, and the output of the optical RX is connected to a sampling oscilloscope for eye diagram observation. The measured 56-Gb/s optical eye diagrams with different settings of equalization, pre-emphasis and gain for three data slices are shown in Fig. 22. When the equalization and pre-emphasis are turned off and the gains of the three data slices are set to the same, as shown in Fig. 22(a), the eye diagram indicates a severe horizontal skew of about 4.76 ps. Only the top sub-eye can be clearly opened as it has higher bandwidth, while the middle and bottom sub-eyes are closed since they are biased at low currents which bring inadequate bandwidths. The average sub-eye height and width are 12.12 μW and 2.39 ps, respectively. After the equalization and pre-emphasis circuits are enabled and the characteristics of equalizations, pre-emphasis and gains of the three data slices are piecewise set, the optical eye diagram is clearly opened, as shown in Fig. 22(b). The average sub-eye height and width are enhanced to 45.46 μW and 7.99 ps, respectively. The eye skew is significantly reduced to 1.77ps. And the RLM of the eye diagram is 90%. The quality improvement of the optical eye diagram verifies the effectiveness of the proposed compensation techniques for the VCSEL non-idealities. Thanks to the compact analog implementation, the die area of the proposed TX is much smaller than those of [18] and [19] which use digital signal processing (DSP) to compensate for VCSEL non-idealities. Compared with [16], [17], and [48] which also adopt analog methods, the proposed TX fully compensates for the VCSEL's non-idealities.

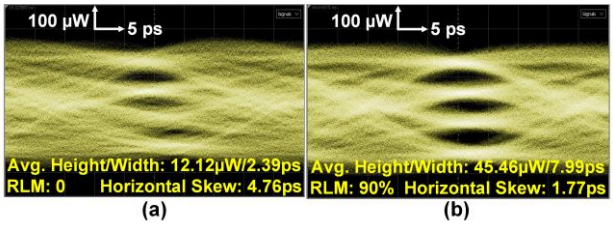

FIGURE 22. Measured 56-Gb/s PAM-4 optical eye diagrams with (a) equalizations and pre-emphasis turned off, and the gains of three slices set to the same, and (b) equalizations and pre-emphasis turned on, and the gains, equalizations and pre-emphasis of three slices piecewise set.

Fig. 23 shows the micrograph of the optical RX in [9], in which a commercial PD is wire-bonded with the chip for optical testing. Fig. 24 presents the optical measurement setup for the optical RX. The light source is coupled to the PD through a 1-m optical fiber. The input signal is generated from an optical reference TX driven by a pattern generator, and the optical power level is adjusted by an internal optical attenuator. The output of the RX is connected to the BERT for BER testing. Bathtub curves are measured for 28-Gb/s NRZ with -8.0-dBm input OMA and 48-Gb/s PAM4 with -4.6-dBm input OMA, shown in Fig. 25 (a) and (b) respectively. At 28 Gb/s, only 1e-4 BER is achieved when RX FFE is enabled and DFE is disabled, while an error-free eye opening of 0.13 UI is achieved when both FFE and DFE are enabled. At 48 Gb/s, after enabling

both FFE and DFE, the BER can be improved to < 1e-5. The 1e-12 BER at 30-Gb/s NRZ indicates the direct DFE works and verifies slicers and DFE operation. The RX consumes 61.4 mW at 48-Gb/s PAM4 with an active area of only 0.06 mm^2 while the TIA contributes 13.1 mW, resulting in 1.28-pJ/bit (0.27 pJ/bit for TIA only) efficiency. In this design, the data rate is mainly limited by the noise performance of the front end. The resistors used to form active inductors in the post-amp bring extra noise, whose value should be carefully chosen considering the noise-BW tradeoff. Compared with [23], [49], [50], [51], this work achieves integration of CMOS linear TIA and PAM-4 sampler with higher data rate and better linearity. Compared with [24] which achieved 36 Gb/s PAM-4 with 4.0 pJ/bit power consumption and -4.8 dBm sensitivity, this work shows higher data rate and better sensitivity with much lower power consumption. Though the data rate of this design is only ~0.5x of [25], the area is 7x smaller and the power consumption of the RX data path and TIA is more than 3x and 4x smaller.

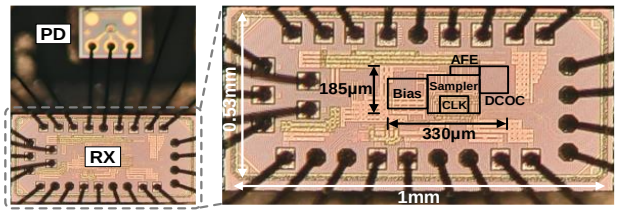

FIGURE 23. Die photo of the optical RX.

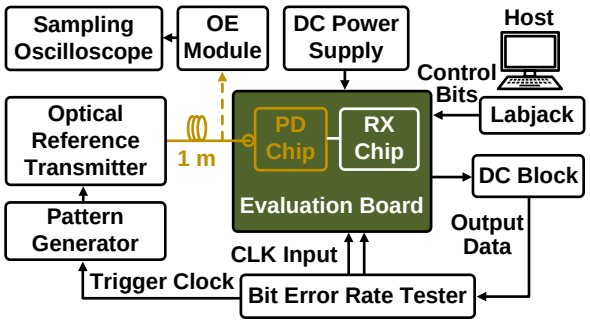

FIGURE 24. Optical measurement setup for the optical receiver.

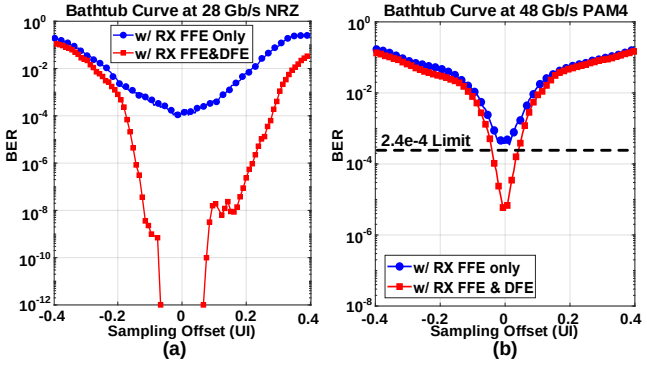

FIGURE 25. Measured bathtub curves at (a) 28-Gb/s NRZ with –8.0-dBm input OMA and (b) 48-Gb/s PAM-4 with – 4.6-dBm input OMA.

C. PLL MEASUREMENT

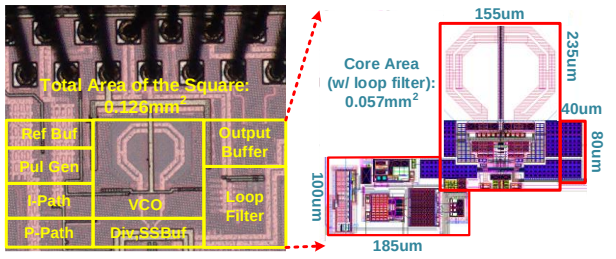

FIGURE 26. Die photo of the DPSSPLL.

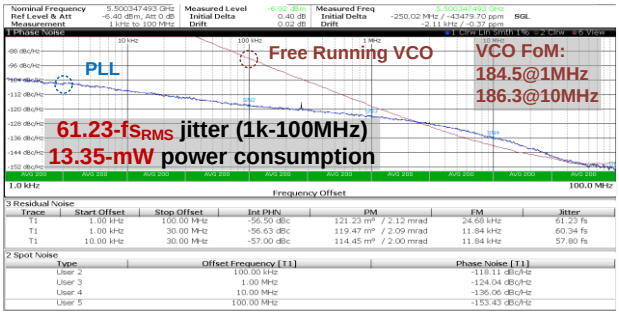

FIGURE 27. Measured phase noise and RMS jitter.

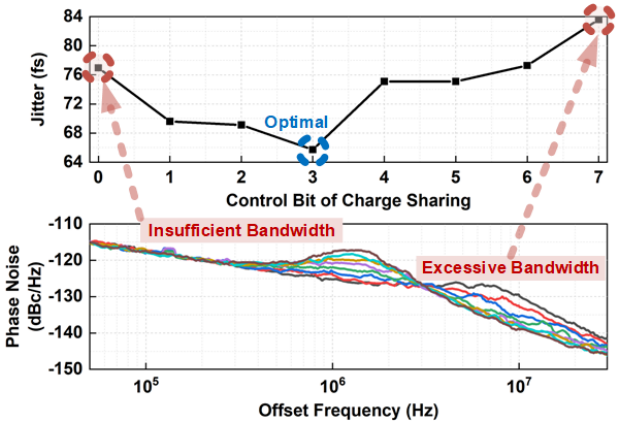

FIGURE 28. Measured RMS jitters and phase noises over different charge neutralization control codes.

The DPSSPLL in [10] is prototyped using a 40-nm CMOS process and the chip micrograph is shown in Fig. 26. It operates at a center frequency of 22 GHz with a total power consumption of 13.35 mW under a dual voltage supply of 0.9 V (for other blocks) and 0.8 V (specifically for the VCO). The PN performance of the free-running class-C VCO and the PLL are illustrated in Fig. 27. The free-running VCO exhibits PN levels of -106.2 dBc/Hz at 1 MHz and -127.9 dBc/Hz at 10 MHz with a power consumption of 7.4 mW. When integrating the PN from 1 kHz to 100 MHz, the DPSSPLL achieves an RMS jitter of 61.23 fs using a 250-MHz input reference signal. Accounting for both jitter performance and power consumption, the figure-

of-merit (FoM_{jitter}) of the PLL is calculated to be -253.0 dB. To demonstrate the effectiveness of the proposed charge neutralization scheme, Fig. 28 illustrates the evolution of RMS jitters and PN profiles under various charge neutralization control codes. As the charge neutralization capacitance increases, the PN is initially dominated by reference PN due to excessive BW, and eventually dominated by VCO PN due to insufficient BW. Optimal RMS jitter is achieved by balancing the contributions of reference and VCO PNs. Across the widest integration range, the proposed DPSSPLL exhibits competitive performance with a rms jitter of 61.23 fs and low power consumption of 13.35 mW. To quantify the PLL's performance, we calculate the jitter-power FoM using the formula $FoM_{PLL} = 20\ \log10(\sigma_{rms}) - 10\ \log10(P_{PLL})$. The resulting FoM_{PLL} of −253.0 dB is among the state-of-the-art results [52], [53], [54], [55], [56]. In addition, within a narrower integration range of 10 kHz to 30 MHz, the FoM_{PLL} is −253.5 dB at 22 GHz and −253.9 dB at 20 GHz. The proposed PLL benefits from its DP architecture, low-Gm SSCP, and inductorless TSPC divider, resulting in a compact core area of only 0.057 mm^2, including the loop filter capacitor. This core area is among the smallest in the similar frequency range for analog and digital PLLs.

D. CDR MEASUREMENT

The chip micrograph in [12] and [13] is shown in Fig. 29, and the measurement setup for the CDR is shown in Fig. 30. A low-frequency power and control PCB is used for setting the VDD bias point and control bits. Another high-frequency PCB is employed for chip mounting and transmission line routing. The PAM-4 data and 1/4-rate clock signals from the pattern generator are transmitted through a pair of high-frequency coaxial cables and a 3-cm PCB transmission line into the chip. The Labjack feeds the control bits to the on-chip I2C module. The recovered and jitter-compensated 1/4-rate data and clock signals are sent to the BERT and the sampling oscilloscope for BER testing and eye diagram observation. The measurement is divided into three parts: basic CDR measurement, JTOL measurement, JTRAN measurement, and jitter compensation measurement. Fig. 31 (a) shows the eye diagrams of the recovered CLK_{RECJC}, MSB_{RECJC} and LSB_{RECJC} with 60-Gb/s PAM4 input. For inputs with an additional 50-ps_{PP} jitter at 10 kHz and 40 MHz, the comparison of LSB_{REC} and LSB_{RECJC} eye diagrams demonstrates a significant jitter compensation percentage of 64% and 48%, respectively, as shown in Fig. 31 (b). The JTOL measurement in Fig. 31 (c) shows a bandwidth of 40 MHz with a minimum amplitude of 0.2 UI_{PP}, which is supported by the wide CDR loop bandwidth. In the JTRAN measurement, when the jitter compensation function is disabled, the JTRAN BW is close to the JTOL bandwidth. However, when the jitter compensation function is enabled, the JTRAN amplitude can be significantly reduced. For instance, at a low offset frequency of 10 kHz, the JTRAN is attenuated to below -8 dB compared to cases without jitter compensation. The proposed CSG supports wideband jitter attenuation by generating a complementary jitter that effectively negates the input jitter across a broad bandwidth. In [57] and [58], PI-based CDR was employed for tracking the uncorrelated jitter between data and clock. In [46] and [59], splitting data and clock paths in the CDR were adopted to support a wide JTOL BW with suppressed JTRAN. Thanks to the proposed jitter compensation scheme, this work achieves the highest JTRAN suppression with the widest JTOL BW for PAM-4 RX over the 50-Gb/s data rate reported to date. The JTRAN can be kept below −8 dB, covering the low-frequency jitter range down to dc.

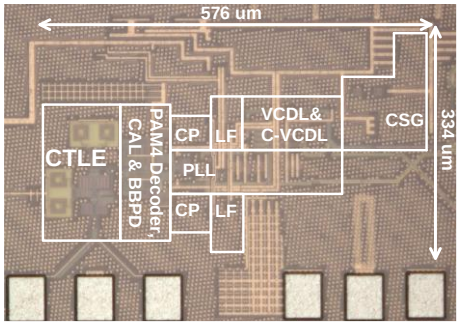

FIGURE 29. Die photo of the JCCDR.

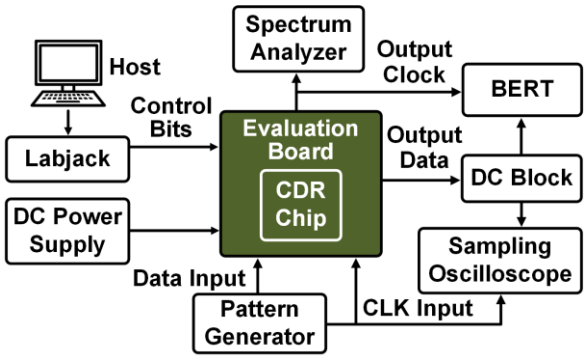

FIGURE 30. Measurement setup for the JCCDR.

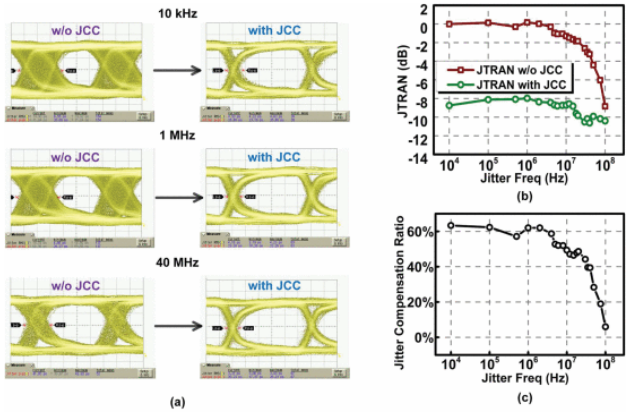

FIGURE 31. (a) Comparison of eye diagrams with and without enabling the JCC function. (b) Measured JTRAN versus jitter frequency with and without JCC function. (c) Calculated jitter compensation ratio versus jitter frequency.

VI. CONCLUSION

Low-power, low-cost, and high-speed interconnects are needed in data centers with a maximum distance of 100 m. IMDD optical links are used to meet the BW requirements in an energy-efficient manner. The BW limitation and degradation

of nonlinearity and sensitivity due to the E/O and O/E conversion bring extra challenges for optical transceiver design. At the TX side, three non-idealities of the VCSEL including the BW nonlinearity, slope of L-I curve η nonlinearity, and asymmetric responses to rising/falling edges limits the speed of the PAM-4 optical link. Several techniques such as DSP-based FFE and piecewise compensation scheme can compensate for those idealities effectively. In the future, close-loop compensation techniques for the non-idealities and temperature sensitivity of the VCSEL are to be explored. At the RX side, trade-offs between gain, BW, noise, and linearity make PAM-4 optical RX design even more challenging, and the design considerations of improving power efficiency and BW density are ever more important. Flip-chip co-packaged TIA and PD is becoming a promising solution to reduce the parasitics and support high I/O density compared to traditional wire-bonding solutions. TIA co-design with on-chip LDO also shows the potential to further improve input sensitivity, and the requirement of large input dynamic range poses another challenge for TIA design. Clock generation directly affects the performance of the transceiver, and compact PLL design focusing on in-band PN reduction and low-jitter performance is described. Trade-offs between JTOL and JTRAN complicate the clock distribution design and limit the signal quality and transmission distance due to the accumulated jitter. Jitter compensation schemes in CDR design are described to address the accumulation of uncorrelated jitter.

REFERENCES

[1] M. Raj, Y. Frans, P. Chiang, *et al*, "Design of a 50-gb/s hybrid integrated si-photonic optical link in 16-nm FinFET," *IEEE J. Solid-State Circuits*, vol.55, no. 4, pp.1086–1095, Apr. 2020.

[2] M. Raj, M. Monge and A. Emami, "A modelling and nonlinear equalization technique for a 20 Gb/s 0.77 pJ/b VCSEL transmitter in 32 nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol.51, no. 8, pp.1734–1743, Aug. 2016.

[3] K. Gopalakrishnan, A. Ren, A. Tan, *et al*, "A 40/50/100Gb/s PAM-4 ethernet transceiver in 28nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Jan. 2016, pp.62–63.

[4] D. D. Sharma, "PCI express® 6.0 specification at 64.0 GT/s with PAM-4 signaling: A low latency, high bandwidth, high reliability and cost-effective interconnect," in *Proc. IEEE Symp. High-Perform. Interconnects (HOTI)*, Aug. 2020, pp.1–8.

[5] J. Lavrencik, S. Varughese, N. Ledentsov, L. Chorchos, N. N. Ledentsov and S. E. Ralph, "168Gbps PAM-4 multimode fiber transmission through 50m using 28GHz 850nm multimode VCSELs," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, Mar. 2020, pp.1–3.

[6] H. Li, C. Hsu, J. Sharma, J. Jaussi and G. Balamurugan, "A 100-Gb/s PAM-4 optical receiver with 2-tap FFE and 2-tap direct-feedback DFE in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol.57, no. 1, pp.44–53, Jan. 2022.

[7] F. Chen, C. Zhang, L. Wang, Q. Pan and C. P. Yue, "A 2.05-pJ/b 56-Gb/s PAM-4 VCSEL transmitter with piecewise nonlinearity compensation and asymmetric equalization in 40-nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 11, 2023, pp.373–376.

[8] F. Chen, C. Zhang, L. Wang, Q. Pan and C. P. Yue, "A 56-Gb/s PAM-4 VCSEL transmitter with piecewise compensation scheme in 40-nm CMOS," submitted to *IEEE J. Solid-State Circuits.*

[9] C. Zhang, L. Wang, Z. Liu, *et al*, "A 48-Gb/s half-rate PAM4 optical receiver with 0.27-pJ/bit TIA efficiency, 1.28-pJ/bit RX efficiency, and 0.06-mm^2 area in 28-nm CMOS," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 16, 2024, pp.1–2.

[10] L. Wang, Z. Liu, R. Ma and C. P. Yue, "A 20-24-GHz DPSSPLL with charge-domain bandwidth optimization scheme achieving 61.3-fs RMS jitter and -253-dB FoM jitter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 21, 2024, pp.1–2.

[11] L. Wang, Z. Liu, R. Ma and C. P. Yue, "A compact 20-24-GHz sub-sampling PLL with charge-domain bandwidth control scheme," *IEEE J. Solid-State Circuits*, pp.1–17, Nov. 2024.

[12] L. Wang, Z. Zhang and C. P. Yue, "A 60-Gb/s 1.2-pJ/bit 1/4-rate PAM4 receiver with a -8-dB JTRAN 40-MHz 0.2-UIPP JTOL clock and data recovery," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 13, 2021, pp.1–2.

[13] L. Wang, Z. Zhang, C. Wang, R. Azmat, W. Shi and C. P. Yue, "A 60-Gb/s 1.2-pJ/bit 1/4-rate PAM-4 receiver with a jitter compensation CDR," *IEEE J. Solid-State Circuits*, vol.59, no. 2, pp.1–15, Feb. 2024.

[14] G. Belfiore, R. Henker and F. Ellinger, "40 Gbit/s 4-PAM VCSEL driver circuit with power roll-off compensation," in *Proc. IEEE Int. Midwest Symp. Circuits SysT. (MWSCAS)*, Aug. 2018, pp.747–750.

[15] D. Kucharski, Y. Kwark, D. Kuchta, *et al*, "A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 /spl mu/m CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2005, pp.222–594 Vol. 1.

[16] J. Hwang, H. Choi, H. Do, *et al*, "A 64Gb/s 2.29pJ/b PAM-4 VCSEL transmitter with 3-tap asymmetric FFE in 65nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2019, pp.C268–C269.

[17] H. Do, J. Sull, S. Lee, K. Lee and D. Jeong, "A 64 Gb/s 2.09 pJ/b PAM-4 VCSEL transmitter with bandwidth extension techniques in 40 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 7, 2021, pp.1–3.

[18] A. Tyagi, T. Iwai, K. Yu, *et al*, "A 50 Gb/s PAM-4 VCSEL transmitter with 2.5-tap nonlinear equalization in 65-nm CMOS," *IEEE Photon. Technol. Lett.*, vol.30, no. 13, pp.1246–1249, Jul. 1. 2018.

[19] P. Peng, P. Lee, H. Huang, *et al*, "A 56-Gb/s PAM-4 transmitter/receiver chipset with nonlinear FFE for VCSEL-based optical links in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol.57, no. 10, pp.3025–3035, Oct. 1. 2022.

[20] D. Li, G. Minoia, M. Repossi, *et al*, "A low-noise design technique for high-speed CMOS optical receivers," *IEEE J. Solid-State Circuits*, vol.49, no. 6, pp.1437–1447, Jun. 1. 2014.

[21] D. Patel, A. Sharif-Bakhtiar and T. C. Carusone, "A 112-Gb/s - 8.2-dBm sensitivity 4-PAM linear TIA in 16-nm CMOS with co-packaged photodiodes," *IEEE J. Solid-State Circuits*, vol.58, no. 3, pp.1–14, Mar. 1. 2023.

[22] H. Li, G. Balamurugan, J. Jaussi and B. Casper, "A 112 Gb/s PAM4 linear TIA with 0.96 pJ/bit energy efficiency in 28 nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp.238–241.

[23] M. G. Ahmed, M. Talegaonkar, A. Elkholy, *et al*, "A 12-Gb/s -16.8-dBm OMA sensitivity 23-mW optical receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol.53, no. 2, pp.445–457, Feb. 1. 2018.

[24] W. Ho, Y. Hsieh, B. Murmann and W. Chen, "A 32 Gb/s PAM-4 optical transceiver with active back termination in 40 nm CMOS technology," *IEEE Open J. Circuits Syst.*, vol.2, pp.56–64, 2021.

[25] H. Li, C. Hsu, J. Sharma, J. Jaussi and G. Balamurugan, "A 100-Gb/s PAM-4 optical receiver with 2-tap FFE and 2-tap direct-feedback DFE in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol.57, no. 1, pp.44–53, Jan. 2022.

[26] T. Huang, T. Chung, C. Chern, M. Huang, C. Lin and F. Hsueh, "A 28Gb/s 1pJ/b shared-inductor optical receiver with 56% chip-area reduction in 28nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2014, pp.144–145.

[27] N. D. Dalt and A. Sheikholeslami, *Understanding Jitter and Phase Noise.* New York: Cambridge University Press, 2018.

[28] K. S. Oh and X. Yuan, *High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting.* Prentice Hall, 2011.

[29] G. Hou, B. Razavi and S. Clerc, "A 56-Gb/s 8-mW PAM4 CDR/DMUX with high jitter tolerance," *IEEE J. Solid-State Circuits*, vol.57, no. 9, pp.2856–2867, Sep. 2022.

[30] Z. Zhang, Z. Zhang, Y. Chen, *et al*, "A 64-Gb/s reference-less PAM4 CDR with asymmetrical linear phase detector soring 231.5-fsrms clock jitter and 0.21-pJ/bit energy efficiency in 40-nm CMOS," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2023, pp.1–2.

[31] G. Shu, S. Saxena, W. Choi, *et al*, "A reference-less clock and data recovery circuit using phase-rotating phase-locked loop," *IEEE J. Solid-State Circuits*, vol.49, no. 4, pp.1036–1047, Apr. 2014.

[32] W. Yin, R. Inti, A. Elshazly, M. Talegaonkar, B. Young and P. K. Hanumolu, "A TDC-less 7 mW 2.5 Gb/s digital CDR with linear loop dynamics and offset-free data recovery," *IEEE J. Solid-State Circuits*, vol.46, no. 12, pp.3163–3173, Dec. 2011.

[33] D. Turker, A. Bekele, P. Upadhyaya, *et al*, "A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2018, pp.378–380.

[34] B. Razavi, "Jitter-power trade-offs in PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.68, no. 4, pp.1381–1387, Apr. 2021.

[35] X. Gao, E. A. M. Klumperink, M. Bohsali and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N," *IEEE J. Solid-State Circuits*, vol.44, no. 12, pp.3253–3263, Dec. 2009.

[36] W. Wu, C. Yao, C. Guo, *et al*, "A 14-nm ultra-low jitter fractional-N PLL using a DTC range reduction technique and a reconfigurable dual-core VCO," *IEEE J. Solid-State Circuits*, vol.56, no. 12, pp.3756–3767, Dec. 2021.

[37] M. Mercandelli, A. Santiccioli, S. M. Dartizio, *et al*, "A 12.9-to-15.1GHz digital PLL based on a bang-bang phase detector with adaptively optimized noise shaping achieving 107.6fs integrated jitter," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2021, pp.445–447.

[38] L. Wang, Z. Liu and C. P. Yue, "A 24-30 GHz cascaded QPLL achieving 56.8-fs RMS jitter and −248.6-dB FoM jitter," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 11, 2023, pp.1–2.

[39] H. S. Muthali, T. P. Thomas and I. A. Young, "A CMOS 10-Gb/s SONET transceiver," *IEEE J. Solid-State Circuits*, vol.39, no. 7, pp.1026–1033, Jul. 1. 2004.

[40] L. Wang, Y. Chen, C. Yang, *et al*, "A 10.8-to-37.4 Gb/s reference-less FD-less single-loop quarter-rate bang-bang clock and data recovery employing deliberate-current- mismatch wide-frequency-acquisition technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.70, no. 7, pp.2637–2650, Jul. 2023.

[41] A. Ragab, Y. Liu, K. Hu, P. Chiang and S. Palermo, "Receiver jitter tracking characteristics in high-speed source synchronous links," *J. Elect. Comput. Eng.*, vol.2011, no. 2011, pp.352–366, Jan. 2011.

[42] S. Ma, H. Yu, Q. J. Gu and J. Ren, "A 5-10-Gb/s 12.5-mW source synchronous I/O interface with 3-D flip chip package," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.66, no. 2, pp.555–568, Feb. 2019.

[43] V. Taraate, *ASIC Design and Synthesis: RTL Design using Verilog.* Cham, Switzerland: Springer, 2021.

[44] D. Dalton, K. Chai, E. Evans, *et al*, "A 12.5 Mb/s to 2.7 Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2005, pp.230–595 Vol. 1.

[45] G. Shu, W. Choi, S. Saxena, T. Anand, A. Elshazly and P. K. Hanumolu, "A 4-to-10.5Gb/s 2.2mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2014, pp.150–151.

[46] X. Zheng, C. Zhang, F. Lv, *et al*, "A 40-Gb/s quarter-rate SerDes transmitter and receiver chipset in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol.52, no. 11, pp.2963–2978, Nov. 2017.

[47] P. Peng, Y. Chen, S. Lai and H. Huang, "A 112-Gb/s PAM-4 voltage-mode transmitter with four-tap two-step FFE and automatic phase alignment techniques in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol.56, no. 7, pp.2123–2131, Dec. 2020.

[48] M. H. Kashani, H. Shakiba and A. Sheikholeslami, "A low-power high-BW PAM4 VCSEL driver with three-tap FFE in 12-nm CMOS FinFET process," *IEEE J. Solid-State Circuits*, vol.59, no. 7, pp.1995–2004, Jul. 2024.

[49] H. Kang, I. Kim, R. Liu, *et al*, "A 42.7Gb/s optical receiver with digital CDR in 28nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 11, 2023, pp.9–12.

[50] A. Sharif-Bakhtiar and A. C. Carusone, "A 20 Gb/s CMOS optical receiver with limited-bandwidth front end and local feedback IIR-DFE," *IEEE J. Solid-State Circuits*, vol.51, no. 11, pp.2679–2689, Nov. 2016.

[51] M. G. Ahmed, D. Kim, R. K. Nandwana, A. Elkholy, K. R. Lakshmikumar and P. K. Hanumolu, "A 16-Gb/s -11.6-dBm OMA sensitivity 0.7-pJ/bit optical receiver in 65-nm CMOS enabled by duobinary sampling," *IEEE J. Solid-State Circuits*, vol.56, no. 9, pp.2795–2803, Sep. 2021.

[52] Y. Hu, X. Chen, T. Siriburanon, *et al*, "A 21.7-to-26.5GHz charge-sharing locking quadrature PLL with implicit digital frequency-tracking loop achieving 75fs jitter and −250dB FoM," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2020, pp.276–278.

[53] J. Lee, Y. Jo, W. Yu, *et al*, "A 16GHz 33fs rms integrated jitter FLL-less gear shifting reference sampling PLL," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp.1–2.

[54] W. Tao, W. Zhao, R. B. Staszewski, F. Lin and Y. Hu, "An 18.8-to-23.3 GHz ADPLL based on charge-steering-sampling technique achieving 75.9 fs RMS jitter and -252 dB FoM," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2023, pp.1–2.

[55] S. Kalia, S. Finocchiaro, T. Dinc, *et al*, "A sub-100 fs RMSjitter 20 GHz fractional-N analog PLL with a BAW resonator based on-chip 2.5 GHz reference," *IEEE J. Solid-State Circuits*, vol.57, no. 5, pp.1372–1384, May. 2022.

[56] E. Thaller, R. Levinger, E. Shumaker, *et al*, "A K-band 12.1-to-16.6GHz subsampling ADPLL with 47.3fsrms jitter based on a stochastic flash TDC and coupled dual-core DCO in 16nm FinFET CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2021, pp.451–453.

[57] Y. Fan, A. Kumar, T. Iwai, *et al*, "A 32-Gb/s simultaneous bidirectional source-synchronous transceiver with adaptive echo cancellation techniques," *IEEE J. Solid-State Circuits*, vol.55, no. 2, pp.439–451, Feb. 2020.

[58] Y. Lee, W. Ho and W. Chen, "A 25-Gb/s, 2.1-pJ/bit, fully integrated optical receiver with a baud-rate clock and data recovery," *IEEE J. Solid-State Circuits*, vol.54, no. 8, pp.2243–2254, Aug. 2019.

[59] M. Hossain, E-Hung Chen, R. Navid, *et al*, "A 4×40 gb/s quad-lane CDR with shared frequency tracking and data dependent jitter filtering," in *Proc. IEEE Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2014, pp.1–2.

Chongyun Zhang (Graduate Student Member, IEEE) received the bachelor's degree in electronic science and technology from Xi'an Jiaotong University, Xi'an, China, in 2020. He is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology.

His current research interests include high-speed low-power integrated circuit design for optical communication interconnects.

Li Wang (Member, IEEE) received the bachelor's degree in microelectronics from the Huazhong University of Science and Technology, Wuhan, China, in 2016, and the Ph.D. degree from The Hong Kong University of Science and Technology, Hong Kong, in 2021.

He is currently a Postdoctoral Fellow with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology. His current research interests include the integrated circuit design for high-speed wireline transceiver, mmWave transceiver, and frequency synthesizer.

Fuzhan Chen (Graduate Student Member, IEEE) received the B.S. degree from Hefei University of Technology, Anhui, China, in 2017, and then recommended to University of Chinese Academy of Sciences, Beijing, China, where he obtained the M.S. degree in 2020. He is currently pursuing the PhD degree in the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong SAR, China.

His research focuses on transceiver integrated circuit design for high-speed optical and wireline communications.

Lin Wang (Member, IEEE) received the B.Sc. degree in applied physics from the Hefei University of Technology (HFUT), Hefei, China, in 2015, and the M.Eng. degree in integrated circuit engineering from the University of Chinese Academy of Sciences, Beijing, China, in 2019. She received the Ph.D. degree from The University of Macau (UM) in 2024.

She is currently a Post-Doctoral Fellow at the IC Design Center, The Hong Kong University of Science and Technology. Her research interests are focused on the high-speed clock and data recovery circuit and high-speed wireline receiver design.

C. Patrick Yue (Fellow, IEEE) received the B.S. degree (Hons.) in electronic and computer engineering from The University of Texas at Austin, Austin, TX, USA, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1994 and 1998, respectively. Based on his Ph.D. thesis work, he co-founded Atheros Communications, San Jose, CA, USA, in 1998 and contributed to the development and deployment of the world's first IEEE802.11a CMOS Wi-Fi transceiver system-on-chip (SoC). In 2002, he joined Aeluros, Mountain View, CA, USA, to work on CMOS high speed PHY/SerDes IC design and signal integrity issues in chip packaging. From 2001 to 2003, while working at the startups, he was a Consulting Assistant Professor at the Department of Electrical Engineering, Stanford University, focusing on research in the area of high-frequency CMOS IC design and RF device modeling. In 2003, he joined the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, USA, as an Assistant Professor. In 2006, he moved to the University of California at Santa Barbara, Santa Barbara, CA, USA, where he was promoted to a Full Professor in 2010. Since 2011, he has been a Professor at the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong. From 2014 to 2015, he was the first Associate Provost for Knowledge Transfer at HKUST. In 2016, he took a sabbatical leave from HKUST to Tsinghua University, Beijing, China, as a Visiting Chair Professor at the Institute of Microelectronics. In 2017, he established LiPHY Communications, Tsim Sha Tsui, Hong Kong, and in 2024, he founded High5 Semiconductor (Hong Kong) Ltd., Science Park, Sha Tin, Hong Kong. Currently, he is the Director of the Integrated Circuit Design Center (ICDC), the Optical Wireless Lab (OWL), and the Qualcomm Joint Innovation and Research Laboratory, HKUST. He has contributed to over 270 peer-reviewed articles, which have amassed more than 10 000 citations. He holds 24 granted patents, with over ten pending, and has authored two book chapters. His research interests include optical wireless physical layer circuits and systems, high-speed wireline communication SoC, millimeter wave communication and sensing circuits, indoor positioning and image processing technologies for robotic applications, edge computing accelerator design for the Internet of Things (IoT) applications, and artificial intelligence (AI)-powered smart power networks.

Prof. Yue is a fellow of OSA. Since 2021, he has been a member of the Editorial Board of IEEE ACCESS. He was honored with the Eleventh Guanghua Engineering Science and Technology Youth Award by Chinese Academy of Engineering (CAE) in 2016. He and his students received the IEEE International Solid-State Circuits Conference (ISSCC) Best Student Paper Award in 2003, the IEEE International Wireless Symposium (IWS) Best Student Paper Award in 2016, and the IEEE Circuits and Systems Society Outstanding Young Author Award in 2017. In 2024, he received the IEEE Symposium on VLSI Technology and Circuits Test of Time Award. He has been actively involved in several technical program committees, including the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE Symposium on VLSI Circuits (VLSI-Circuits), the IEEE RFIC Symposium (RFIC), the IEEE European Solid-State Circuits Conference (ESSCIRC), the IEEE IWS, and the IEEE Asian Solid-State Circuits Conference (A-SSCC). He held the position of Vice-President of Membership of the IEEE SSCS from 2016 to 2021. He has served as an Editor for IEEE ELECTRON DEVICE LETTERS and IEEE Solid-State Circuits Magazine and a Guest Editor for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. Since 2018, he has been an Editor of PROCEEDINGS OF THE IEEE. He was an Elected AdCom Member of the IEEE Solid-State Circuit Society (SSCS) from 2015 to 2017 and served as an SSCS Distinguished Lecturer from 2017 to 2018.