

The Gallium Nitride (GaN) Transistor Patent War: Year 2

Deep dive into the world-wide patent war involving EPC, Innoscience and Infineon



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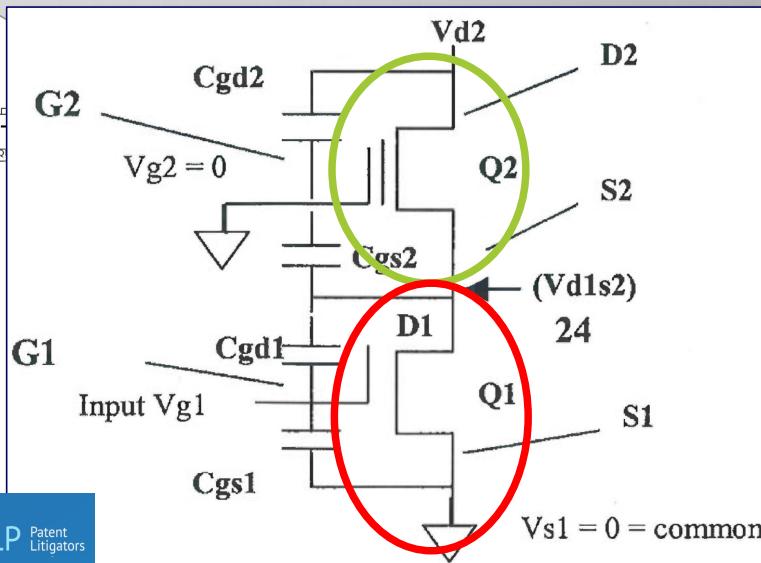
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Patent
Litigators



U.S. 8,264,003: Merged Cascode Transistor Circuit

<p>(12) United States Patent Herman</p> <hr/> <p>(54) MERGED CASCODE TRANSISTOR</p> <p>(75) Inventor: Thomas Herman, Manhattan Beach, CA (US)</p> <p>(73) Assignee: International Rectifier Corporation, El Segundo, CA (US)</p>	<p>(10) Patent No.: US 8,264,003 B2</p> <p>(45) Date of Patent: Sep. 11, 2012</p> <hr/> <p>FOREIGN PATENT DOCUMENTS</p> <table border="0"> <tr> <td>JP</td> <td>2001-210657</td> <td>8/2001</td> </tr> <tr> <td>JP</td> <td>2002-076020</td> <td>3/2002</td> </tr> <tr> <td>JP</td> <td>2008-522436</td> <td>6/2008</td> </tr> <tr> <td>WO</td> <td>WO 2005/079370</td> <td>9/2005</td> </tr> </table> <p>OTHER PUBLICATIONS</p>	JP	2001-210657	8/2001	JP	2002-076020	3/2002	JP	2008-522436	6/2008	WO	WO 2005/079370	9/2005
JP	2001-210657	8/2001											
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JP	2008-522436	6/2008											
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OTHER PUBLICATIONS

ABSTRACT

A merged gate transistor in accordance with an embodiment of the present invention includes a semiconductor element, a supply electrode electrically connected to a top surface of the semiconductor element, drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode, a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also capacitively coupled to the semiconductor element. The first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

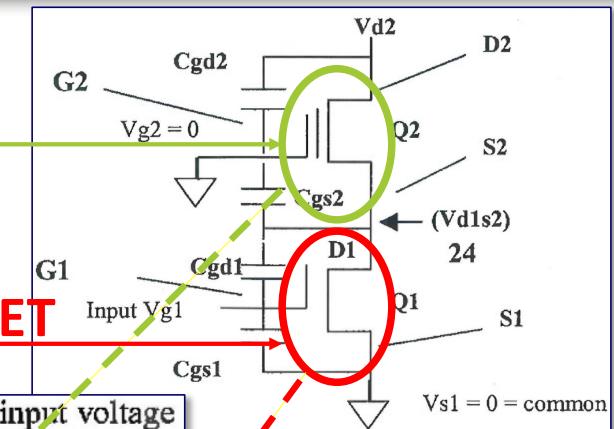
'003: Requires a Pair of e-mode and d-mode FETs

1. A merged cascode transistor circuit comprising:
an input voltage signal source having an input voltage signal;
a constant voltage source having a predetermined constant voltage;
a merged cascode transistor comprising:
a semiconductor element;
a source electrode electrically connected to a top surface of the semiconductor element;
a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;

Depletion mode FET

Enhancement mode FET

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Accused Device Uses a Pair of e-mode FETs

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
[1PRE] A merged cascode transistor circuit comprising:	To the extent the preamble is limiting, the preamble is met. Innoscience's ISG3201 is a co-packaged product that integrates two 100V enhancement mode GaN devices with a half-bridge gate driver.

3. General description

The ISG3201 is a 100V Copak product in Innoscience's SolidGaN family. It integrates two 100V enhancement mode GaN devices with a 100V half-bridge gate driver. ISG3201 employs bootstrap technique for high-side driver voltage and can operate up to 100V. The

See Ex. 31 at 1 (ISG3201 Datasheet, annotations added)

Accused Device Uses a Pair of e-mode FETs

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.	<p>The low side INN100W032A transistor in ISG3201 meets this limitation.</p> <p>As shown in the cross-sectional view TEM image of INN100W032A, a drain region (denoted by "D1") of the enhancement mode transistor Q1 is merged with a source region (denoted by "S2") of the depletion mode transistor Q2 at the node in the semiconductor element.</p> <p>(Cross-sectional view TEM image of INN100W032A, annotations added)</p>

Accused Device Uses a Pair of e-mode FETs

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	<p>As discussed above in connection with limitation [1C5], the second gate G2 is coupled to the semiconductor element through an insulating layer, which is an insulated gate. Therefore, the second portion of the transistor (Q2) is an insulated gate transistor using an insulated gate G2, which according to the textbook "GaN Transistors for Efficient Power Conversion" is a common way to produce a depletion-mode transistor.</p> <p>There are two common ways to produce a d-mode HEMT device. The initial transistors introduced in 2004 had a Schottky gate electrode that was created by depositing a metal layer directly on top of the AlGaN. The Schottky barrier was formed using metals such as Ni-Au or Pt [9–11]. Depletion-mode devices have also been made using an insulating layer and metal gate similar to a MOSFET [12]. Both types are shown in Figure 1.6.</p> <p style="text-align: center;">GaN Technology Overview</p> <p style="text-align: right;">7</p> <p>Figure 1.6 Cross section of a basic depletion-mode GaN HEMT with (a) Schottky gate, or (b) insulating gate</p> <p>See Ex. 28 at 24-25 (GaN Transistors for Efficient Power Conversion, 2nd edition, annotations added)</p> <p>Furthermore, Innoscience's own website explains that without a Schottky contact on a p-GaN layer (such as the case with the insulated gate G2 on Q2), "the natural form of GaN HEMTs" is a depletion mode transistor.</p>