1.6 Tbps FOWLP-Based Silicon Photonic Engine for Co-Packaged Optics

Xin Li, Sajay Bhuvanendran Nair Gourikutty, Jiaqi Wu, Teck Guan Lim, Pengfei Guo, Jaye Charles Davies, Edward Sing Chee Koh, Boon Long Lau, Ming Chinq Jong, Ser Choong Chong, San Sandra, Chao Li, Guo-Qiang Lo, Surya Bhattacharya, and Jason Tsung-Yang Liow

***Abstract*— Co-packaged optics (CPO) has emerged as a promising solution to address the limitations of traditional pluggable optical transceivers, offering enhanced bandwidth, improved energy efficiency, and reduced signal loss. This paper presents a low-cost, volume-manufacturable Fan-Out Wafer Level Packaging (FOWLP) silicon photonic engine with an aggregate data transmission capacity of 1.79 Tbps (8 x 224 Gbps). The FOWLP platform enables the seamless integration of Electronic ICs (EICs) and Photonic ICs (PICs) without wire bonds, preserving signal integrity and minimizing losses. By demonstrating 112 Gbaud NRZ (112 Gbps/λ) and PAM4 (224 Gbps/λ) transmission with minimal digital signal processing, this work highlights the potential of silicon photonics for 200 Gbps/λ Co-Packaged Optics (CPO) and Linear Pluggable Optics (LPO) applications. The findings underscore the enhanced signal integrity, power efficiency, and reduced latency achieved with FOWLP, addressing critical bottlenecks in hyperscale data centers and AI/ML clusters.**

***Index Terms*—advanced packaging, Co-Packaged Optics, Fan-Out Wafer Level Packaging, silicon photonics**

I. INTRODUCTION

In recent years, the demand for higher data rates, lower latency, and reduced power consumption in data centers and high-performance computing (HPC) systems has driven significant advancements in optical communication technologies. Co-packaged optics (CPO) has emerged as a promising solution to address the limitations of traditional pluggable optical transceivers, offering key advantages including enhanced bandwidth, improved energy efficiency, and reduced signal loss [1][2]. The adoption of co-packaged optics is facilitated by several technological advancements. Innovations in silicon photonics have played a crucial role. Silicon photonics leverages the mature CMOS fabrication infrastructure, allowing for the mass production of photonic components and circuits at a lower cost and with high precision [3]. Furthermore, it is also able to tap on developments in advanced packaging technologies, such as wafer-level packaging and 3D integration, to enable the dense and efficient packaging of optical and electronic dies or chiplets within a compact footprint [4] [5] [6] [7].

Several advanced packaging technologies have emerged, including through-silicon vias (TSV)-based, glass-based, and fan-out wafer level packaging (FOWLP) based approaches, with each having advantages and disadvantages. TSV-based CPO involves fabricating TSVs on the PIC wafer, enabling dense integration and minimizing signal propagation distances [5] [7]. This approach offers high bandwidth density and shorter signal path lengths. However, TSV manufacturing can be complex and costly especially at low volumes [8]. Hence, it may not be an ideal approach for high mix, low volume silicon photonics transceiver applications. Glass-based CPO utilizes glass substrates to integrate both electronic and optical components [9] [10]. While glass-based CPO is promising in terms of performance, manufacturing costs are high and integration density is comparatively limited as there is no option to embed EIC or PIC dies within the glass interposer itself. FOWLP is a mature low-cost advanced packaging technology with widespread and high-volume use in electronic chip applications [11] [12]. FOWLP offers excellent scalability, enabling the integration of multiple optical and electronic dies within a compact package. Like TSV, EICs or PICs can be embedded within the FOWLP interposer itself, enabling dense integration and ultra-short signal paths where required. This approach also allows for efficient thermal dissipation and is compatible with existing semiconductor manufacturing processes.

We demonstrated a silicon photonic engine fabricated using an FOWLP-based advanced electronic-photonic packaging approach [13] [14] [15]. The FOWLP-based platform supports the seamless integration of EICs and PICs without wire bonds, thereby minimizing signal losses and enhancing signal integrity. The PIC is embedded within the FOWLP interposer. The optical ports on both the PIC surface

This work was supported in part by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore under grant number I2001E0071.

Xin Li, Jaye Charles Davies, Edward Sing Chee Koh and Jason Tsung-Yang Liow are with Rain Tree Photonics Pte Ltd, 82 Playfair Road, #03-01, D'Lithium, 368001, Singapore (e-mail: xinli@raintreephotonics.com, jayedavies@raintreephotonics.com, edwardkoh@raintreephotonics.com, jasonliow@raintreephotonics.com)

Sajay Bhuvanendran Nair Gourikutty, Jiaqi Wu, Teck Guan Lim, Boon Long Lau, Ming Chinq Jong, Ser Choong Chong, San Sandra and Surya Bhattacharya are with Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 2 Fusionopolis Way, #08-02, Innovis, 138634, Singapore (e-mail: nairs@ime.a-star.edu.sg, wu_jiaqi@ime.a-star.edu.sg, limtg@ime.a-star.edu.sg, laubl@ime.a-star.edu.sg, mcjong@ime.a-star.edu.sg, chongsc@ime.a-star.edu.sg, sandra_san@ime.a-star.edu.sg, bhattass@ime.a-star.edu.sg).

Pengfei Guo, Chao Li and Guo-Qiang Lo are with Advanced Micro Foundry, 11 Science Park Road, 117685, Singapore (e-mail: guop@advmf.com, lic@advmf.com, logq@advmf.com).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org

and edges are maintained in pristine condition for optimal optical coupling. In this work, we demonstrated 112 Gbaud NRZ (112 Gb/s) and 112 Gbaud PAM4 (224 Gb/s) transmission for both direct probing of the photonic engine and probing through the organic substrate on which the photonic engine is packaged. 112Gbaud NRZ and PAM4 reception was also demonstrated through direct probing of the photonic engine. An aggregate data rate capability of 1.792 Tbps was achieved using 8 transmit and receive channels.

II. FOWLP-Based Silicon Photonic Engine

Fig. 1 shows the schematic of the FOWLP-based photonic engine. The PIC is embedded in mold and EIC is assembled on the package surface. A 2-layer front-side redistribution layer (FRDL) and a single layer backside redistribution layer (BRDL) were fabricated for interconnections, supporting DC power supply, low and high speed signaling for the photonic engine. High speed transmission lines were designed to support 200Gbps/lane signals on the FRDL. Through Mold Via (TMV) were developed for interconnecting between the bottom of the OE package and the top. TMVs were also designed to support 200Gbps/lane applications. RDL metal with 15μm line/space and TMVs enable fine pitch interconnects with low parasitics and good impedance control.

EICs can be flip-chip attached on top of the package using micro-bumps with Under Bump Metallization (UBM) on the FOWLP FRDL. This configuration allows the EICs to be attached directly above the PIC's RF I/O pads, providing the shortest path to minimize RF loss and parasitics. This is advantageous for high-speed driver and transimpedance amplifier (TIA) interconnections. At the bottom of the package, Controlled Collapse Chip Connection (C4) bumps were fabricated, enabling the photonic engine to be packaged onto a substrate.

The Spot Size Converters (SSC) on the PIC were preserved during the fan-out process, facilitating optical edge coupling for the PIC. Open windows in the RDL dielectric expose the vertical couplers on the PIC, allowing the photonics engine to also support vertical optical coupling in and out of the package.

Figure 2 shows a photo of the fabricated 1.6Tbps photonic engine, which has a footprint of 9.5mm x 13mm. The PIC used in the photonic engine contains 8 high-speed 200Gbps/lane silicon modulators, 8 waveguide germanium photodetectors, thermo-optic components and other passive photonic circuits, supporting an aggregate transmit and receive capability of 1.6Tbps. By scaling up the channel count on the PIC or increasing the number of PIC chiplets in the FOWLP, the photonic engine's aggregate data rate can be further increased.

The PIC is designed with SSCs at one edge, facilitating edge coupling to external optical I/O during module packaging. Test structures using vertical grating couplers were also utilized for wafer-level testing and characterization.

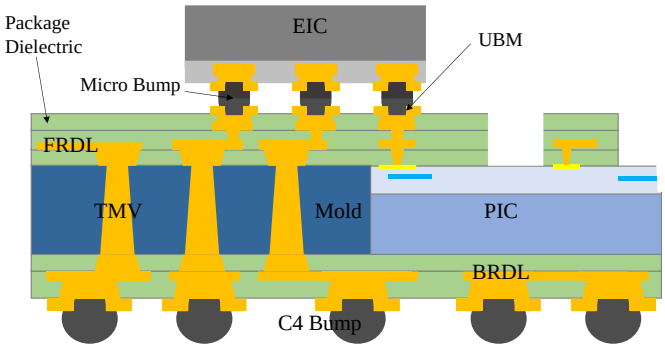

Fig. 1. Schematic of the FOWLP-based photonic engine.

The packaging is executed on a 300mm Fan-Out Wafer-Level Packaging (FOWLP) line equipped to handle the entire assembly and fabrication process. Known Good Dies (KGDs) from the silicon PIC wafer were selected for the FOWLP process after PIC wafer-level testing. The completed optoelectronic (OE) packages were then singulated and assembled onto organic substrates using C4 bumps. Figure 3 shows an image of the photonic engine packaged with organic substrates. Transmission lines were designed on the organic substrate to deliver electrical modulation signals to the photonic package.

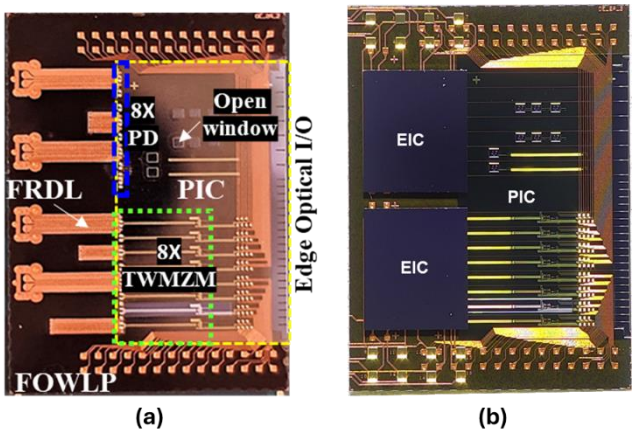

Fig. 2. Photo of a 1.6 Tbps Photonic Engine (a) without and (b) with flip-chip attached EICs.

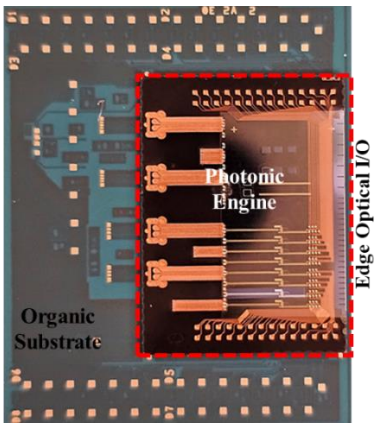

Fig. 3. Photo of a photonic engine packaged onto an organic substrate.

III. Fabrication

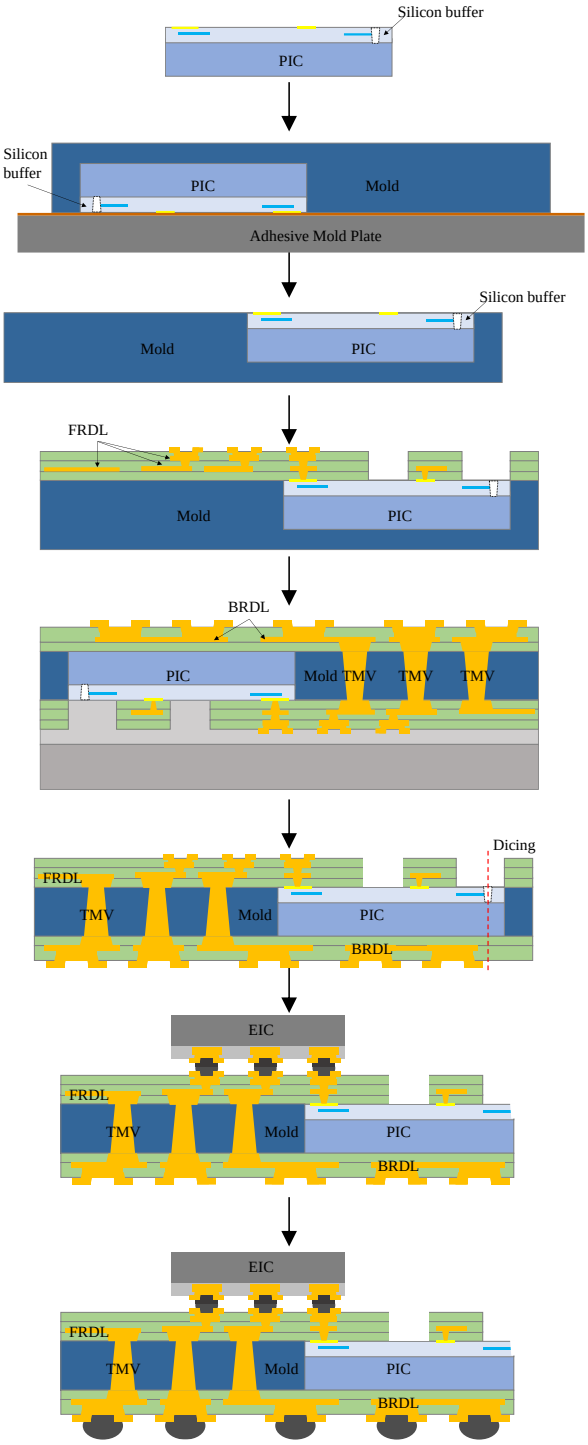

Fig. 4. FOWLP fabrication process flow.

The fabrication process, illustrated in Figure 4, begins with the selection of KGD of the PIC, which are placed face-down on an adhesive mold plate. This assembly undergoes compression molding to form a reconstituted molded wafer. After separating the reconstituted wafer from the mold plate, it undergoes FRDL metal and dielectric processing. The FRDL comprises two metal layers for routing and an UBM layer with exposed bond pads where the EICs are bonded.

After front-side processing, the wafer is thinned from the backside to 300μm or less, exposing the PIC. Infrared signals help align lithography with front-side marks to build the TMV structure on the backside. TMVs with 150μm diameters were laser-drilled on the mold compound, tapering to around 60μm at the bottom, landing on the front RDL copper layer. The TMV sidewalls were metallized with PVD deposition of titanium and copper seed layer followed by copper electroplating to connect the front and back RDLs.The TMVs have a diameter, height, and pitch of 150μm, 300μm and 300μm, respectively. The BRDL consists of one metal layer and UBM.

A key challenge in the FOWLP process is encapsulating the PIC without affecting its optical coupling ports. The SSC is vulnerable to contamination and damage if it comes into contact with the epoxy mold compound (EMC). Such contamination and damage would significantly reduce the coupling efficiency, making it essential to preserve the integrity of the PIC's optical edge couplers to meet output power standards. A specially designed silicon buffer structure is employed to protect the optical coupling structures of the PIC during the FOWLP molding process. This dam-like structure prevents the EMC from coming into direct contact with the SSCs, thereby protecting them.

Completed FOWLP wafers were then singulated using dicing, which simultaneously exposes the SSCs for optical edge coupling. EICs were also assembled on top of the package using flip-chip. The photonic engine can subsequently be packaged onto the substrate using C4 bumps, which have a diameter of 120μm and a pitch of 250μm.

IV. FOWLP-Based Silicon Photonic Engine Characterization

A. FOWLP RF characterization

The RF performance of the FOWLP was evaluated using a 3D electromagnetic simulator (Ansys HFSS). Fig. 5 shows the simulated S-parameters of the FOWLP packaged on an organic substrate. The total RF loss, which includes the 2 mm substrate transmission line, TMV and RDL is 1.1 dB at 56 GHz, with a return loss of less than -18 dB. Specifically, the simulated RF loss for the TMV is under 0.3 dB at 56 GHz, and the return loss is below -25 dB. Additionally, S-parameters of the TMV were measured using a probe station with probes on both the front and back sides. The measured return loss is less than -15 dB, and the insertion loss is under 0.5 dB for frequencies up to 50 GHz (Fig. 6(b)). The experimental measurements align well with the simulated RF performance of the TMV. Both simulated TMV and measured TMV test structures have differential insertion loss better than 0.5 dB up to 50 GHz. The simulation has better performance than measurement. The possible reasons of discrepancies are process deviations, the double-sided measurement setup and errors caused by the double-sided RF probes' calibration. Therefore, the FOWLP demonstrates the capability to integrate PIC, EIC, and packaging with minimal loss and excellent signal integrity, thus supporting 200G/lane signal transmission.

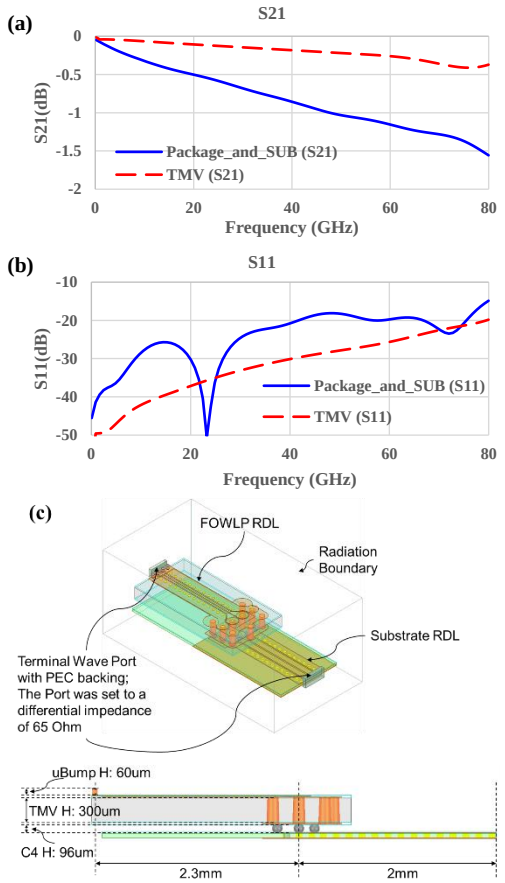

Fig. 5. Simulated (a) S21 and (b) S11 of FOWLP packaged on organic substrate. (c) Schematic of simulated interconnect.

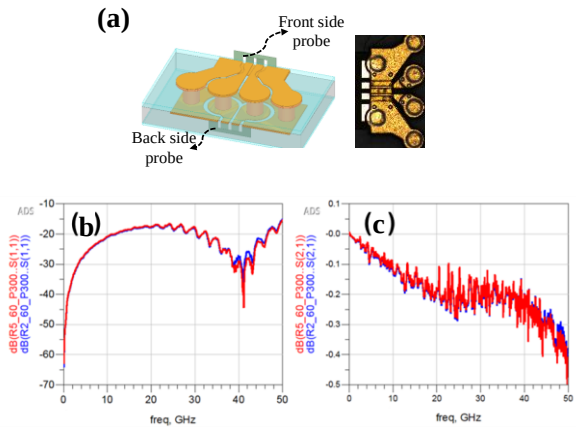

Fig. 6. (a) TMV test structure; (b) measured S11 and (c) S21 of the TMV test structure.

B. Optical coupling evaluation

For optical coupling evaluation, we designed a U-shaped SSC loopback structure with a 250µm pitch to assess the optical coupling efficiency post fan-out packaging. The SSC edge couplers are optically aligned with an external fiber array, also with a 250µm pitch. As shown in Fig. 7, the coupling loss is less than 2dB per facet after packaging even without using index-matching epoxy. This measured package coupling loss is comparable to the PIC's bare die test results, indicating that the FOWLP packaging process does not degrade the edge coupler performance.

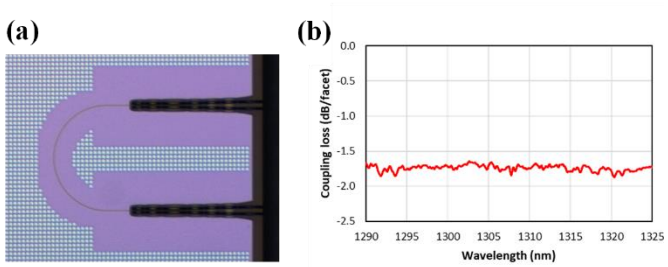

Fig. 7. (a) U-shaped SSC (similar to those in OE) loopback test structure and (b) coupling loss of the FOWLP (The coupling loss was extracted from the total insertion loss divided by two. The waveguide loss is negligible due to its short length.).

C. Wafer level electrical testing

To verify the integration process with respect to electrical continuity, daisy chain structures of metal interconnects (Fig. 8(a)) are designed. These daisy chains consist of copper interconnects in the RDL and TMVs. To facilitate automated testing of all daisy chains at the wafer level, special probing structures were created in the fanout area, as shown in Fig 8(a). A Multi-channel System-on-Chip (SoC) automated test equipment system (Advantest V93K) was employed along with an automated wafer prober to check the continuity within the daisy chains. The tester results show that all daisy chains are continuous without any open defects. Fig. 8(b) shows an example of the wafer level connectivity test structure and the measured resistance.

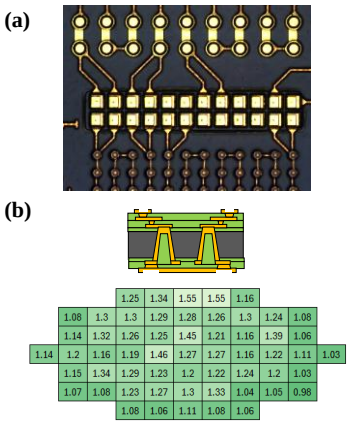

Fig. 8. (a) Daisy chain structures of metal interconnects and (b) daisy chain test structure schematic and wafer level measured resistance.

D. Wafer level optical testing

The FOWLP process preserves the PIC's vertical coupling capability by opening windows in the RDL dielectric, exposing the vertical grating couplers on the PIC. This allows the fabricated photonic engine to be tested at the wafer level using vertical couplers. Fig. 9(a) illustrates the wafer-level measurement using an in-house opto-electrical wafer-level tester. Fig 9(b) shows the wafer-level optical test data for four types of photonic sub-circuits on each PIC in the package. Due to a

limited number of PIC dies, each FOWLP wafer was populated with only 9 PIC dies, which span across the wafer vertically and horizontally to cover both centre and edge regions. For this test, we tested 4 different optical sub-circuits on each of these 9 packages on the wafer, which gives a total of 36 tested sub-circuits. These photonic sub-circuits are designed to be sensitive to changes in the physical properties of the PIC. With the exception of one sub-circuit, which was affected by a particle on the vertical coupler, the remaining 35 sub-circuits maintained consistent performance after FOWLP processing. This demonstrates that the packaging process does not degrade the optical characteristics of the PIC chiplets. It also shows that the fabricated FOWLP wafer can be automatically tested at wafer level with high throughput, similar to a silicon wafer.

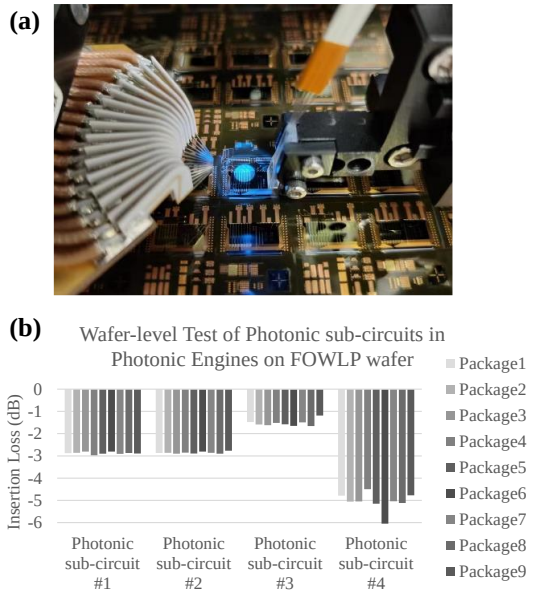

Fig. 9. (a) Wafer-level measurement using an in-house opto-electrical wafer-level tester and (b) wafer-level optical test results.

V. Transmitter Characterization

The 1.6T transmission was demonstrated under two test conditions. First, the transmitter was tested by probing a 900µm FRDL RF transmission line connected to the Traveling Wave Mach-Zehnder Modulator (TWMZM) on the PIC (Fig. 10(a)). This setup emulates the scenario where an MZM driver is co-packaged on the FOWLP, providing electrical RF modulation signals from the driver. The photonic engine was also tested after being packaged on an organic substrate (Fig. 10(b)). Here, the RF signal is fed into the TWMZM on the photonic engine through a 2mm substrate RDL, TMV, and 3.2mm FRDL, emulating a direct-drive configuration where the Switch ASIC directly drives the modulator.

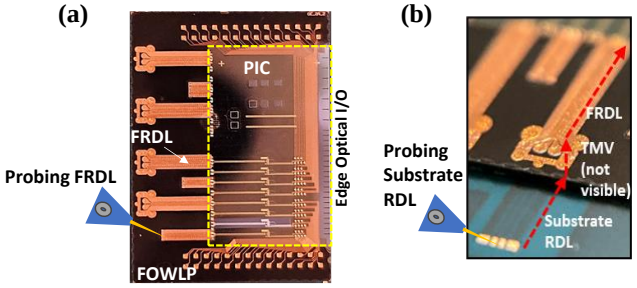

Fig. 10. Illustration of (a) FRDL probing configuration and (b) substrate RDL probing configuration (emulates Direct-Drive configuration).

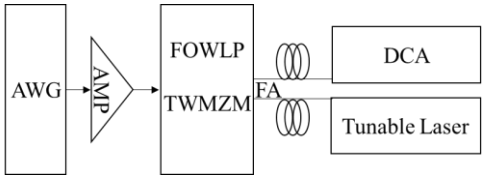

Fig. 11. Transmitter measurement experimental setup.

Fig. 11 shows the transmitter measurement experimental setup. An RF modulation signal was generated using a Keysight Arbitrary Waveform Generator (AWG) and amplified by an external driver before being applied to the transmitter. Excess RF losses from the setup, including RF cable and connector losses, were de-embedded. Continuous wave light source and modulated optical signals were coupled into and out of the package using a fiber array. The generated optical signal was captured using a Keysight Digital Communication Analyzer (DCA).

A. FOWLP FRDL-probed Configuration

First, a 112 GBaud NRZ transmission was evaluated. Fig. 12 shows the NRZ eye diagrams (FRDL probing configuration). Only a 5-tap FFE, which is commonly available in 100G SERDES, was used on the transmitter side. The 112Gb/s NRZ eyes are wide open without any receive-side equalization, demonstrating a transmission capability of 112Gb/s per lane and an aggregate data rate of 896 Gb/s. The 112 GBaud NRZ transmission required no complex digital signal processing, significantly reducing power consumption and link latency compared to current 112Gb/s PAM4 links, which necessitates PAM4 encoding and decoding and receive-side FFE. This approach enables enhanced power efficiency and reduced latency, which can help to address the challenges in hyperscale data centers and AI/ML clusters.

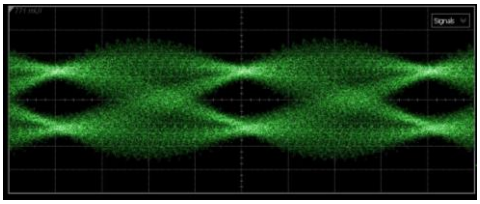

Fig. 12. 112 Gbaud NRZ eye diagram without post-equalization using FRDL probing configuration.

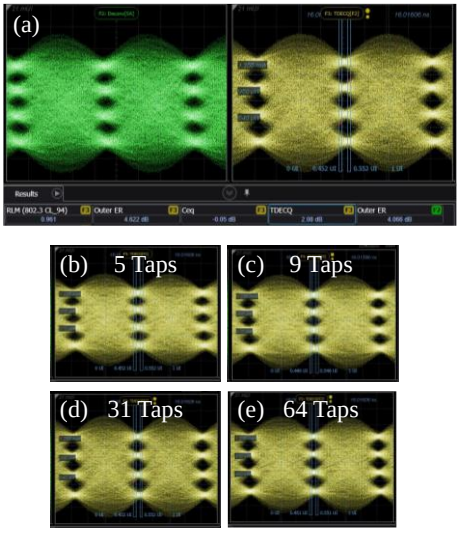

Fig. 13. Photonic Engine 112 GBaud PAM4 transmitter eye diagrams: (a) 224Gbps PAM4 and equalized eye diagram using 31 FFE taps (ER=4.066 dB, TDECQ=2.08 dB) (b)-(e) equalized eye diagram using 5, 9, 31 and 64 FFE Taps.

Next, 112 GBaud PAM4 (224 GBps/λ) transmission performance was evaluated. Fig. 13(a) shows the optical 224 Gb/s PAM4 eye diagram and the equalized PAM4 eye diagram using a 31-tap FFE equalizer. A Transmitter and Dispersion Eye Closure Quaternary (TDECQ) of 2.08 dB and an Extinction Ratio (ER) of 4.066 dB were achieved. Fig. 13 (b) to (e) show the equalized PAM4 eye diagrams using 5, 9, 31, and 64 FFE taps, achieving TDECQ of 3.46 dB, 2.44 dB, 2.08 dB, and 1.47 dB, respectively. A TDECQ of 2.44 dB was achieved with just 9 taps, making it compliant with the IEEE 802.3dj 200G/lane standard. The FOWLP demonstrated excellent signal integrity for 112 GBaud PAM4 transmission, supporting an aggregate 1.792 Tb/s transmission using the 8-channel photonics engine. Performance can be further improved by optimizing the impedance matching between the TWMZM and RDL RF transmission line.

B. Direct-Drive Configuration

112 GBaud NRZ transmission was also evaluated when the photonic engine was packaged onto an organic substrate. For comparison, a TWMZM was measured by directly probing its probe pads. Fig 14 (a) and (b) shows the eye diagrams without and with 5-tap FFE receive-side equalization, respectively. Both eyes are wide open using only 5-tap FFE transmit-side pre-emphasis. TDEC was evaluated using different numbers of receive-side FFE for both directly-probed TWMZM and direct-drive configurations (through package RF interconnect). The directly-probed TWMZM exhibited slightly better performance and required fewer FFE taps for optimal TDEC performance. Due to the excellent signal integrity, the direct-drive configuration also exhibited good TDEC even without receive-side equalization. This is advantageous for AI/ML interconnect applications where low power dissipation and low latency are critical.

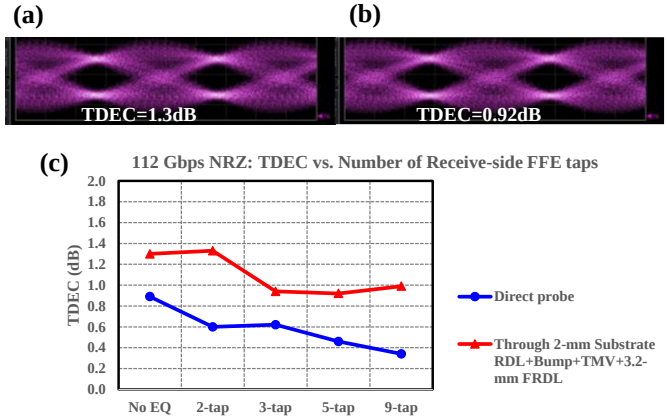

Fig. 14. Direct-drive configuration: (a) Transmitter 112 Gbaud NRZ eye diagrams without 5-tap post equalization, (b) transmitter 112 Gbaud NRZ eye diagram with 5-tap post equalization and (c) TDEC using different numbers of receive-side FFE for both FRDL-probed TWMZM and direct-drive configurations.

Fig. 15 shows the PAM4 eye diagrams of the direct-drive configuration after 5-tap (a) and 21-tap (b) receive-side FFE. The 21-tap FFE removed more signal impairment, resulting in more open eyes. Fig. 15 (c) compares the TDECQ performance for direct-drive configuration and the directly-probed TWMZM. Due to channel impairments presented in the packaged photonic engine (RF loss, impedance discontinuities at various interfaces), the direct-drive configuration requires approximately twice as many FFE taps to achieve the same TDECQ performance. Unlike wire bonding, the impedances of the various interconnects within the FOWLP package are all adjustable by design. The impedance discontinuities can hence be reduced in the next iteration of design optimization. Fig. 16 shows the eye diagram after transmit-side FFE taps optimization, achieving an outer ER of 4.28 dB and a TDECQ of 2.32 dB using 21-tap receive-side FFE. Successful 224 Gbps PAM4 transmission was demonstrated with the FOWLP packaged on the organic substrate, showing that the 1.6T photonic engine can be directly driven by an ASIC through the substrate and fan-out package.

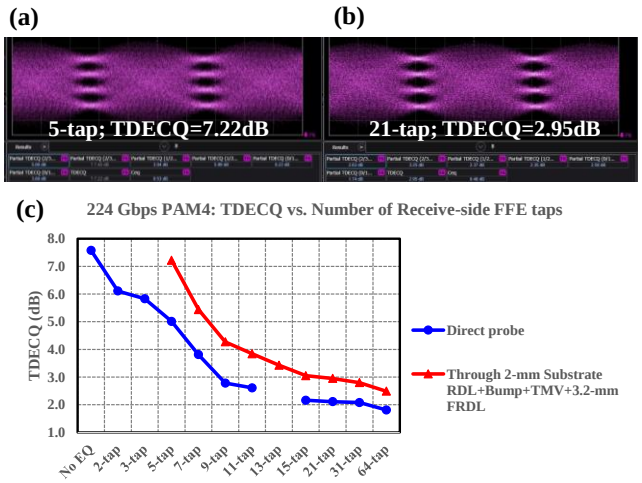

Fig. 15. Direct-drive configuration: (a) Transmitter 112 Gbaud PAM4 eye diagrams using 5-tap post equalization, (b) transmitter 112 Gbaud NRZ eye diagram using 21-tap post equalization and (c) TDECQ using different numbers of receive-side FFE for both directly-probed TWMZM and direct-drive configurations.

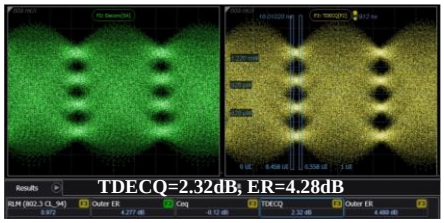

Fig. 16. 112 GBaud PAM4 transmitter eye diagrams using direct drive configuration (ER=4.28 dB, TDECQ=2.32 dB).

VI. Receiver Characterization

The receiver was also tested by directly probing the FRDL transmission line connected to the high-speed photodiode on the PIC. This setup emulates the scenario where a transimpedance amplifier (TIA) is flip-chip attached on top of the FOWLP photonic engine in close proximity to the photodiode. Fig. 17 shows the experimental setup used for receiver evaluation. An in-house silicon photonic TWMZM transmitter board was used to generate the reference transmitter optical signal. Electrical modulation signals were generated using a Keysight AWG and amplified to drive the TWMZM transmitter board. The modulated optical signal was then coupled into the photonic engine package using a fiber array. On the FOWLP photonic engine, the germanium photodetector was connected to the probe pads via a 1 mm-long FRDL RF transmission line. The received electrical signal was captured using a Keysight DCA. Excess losses introduced in the experimental setup, such as RF cables and connector losses, were de-embedded.

Fig. 18 (a) and (b) shows the generated reference transmitter 112 Gbps NRZ eye diagram and the received electrical NRZ eye diagram, respectively. A 5-tap pre-emphasis was applied using the AWG to compensate for link impairment. The received electrical eyes are wide open without further post-equalization. This demonstration showcases a 112 GBaud NRZ link using only transmitter-side 5-tap FFE, highlighting the excellent signal integrity provided by the FOWLP. This approach is well-suited for 100G links where low system complexity, low power consumption, and low link latency are essential.

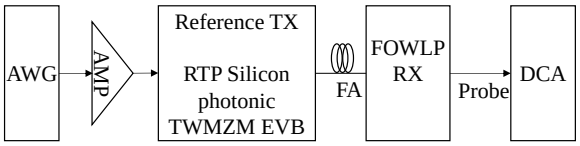

Fig. 17. Photonic engine receiver measurement experimental setup. On the FOWLP photonic engine, the germanium photodetector was connected to the probe pads via a 1 mm-long FRDL RF transmission line.

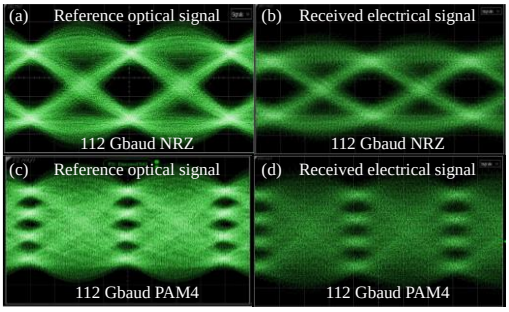

Fig. 18. (a) Reference transmitter 112 Gbps NRZ eye diagram; (b) received electrical NRZ eye diagram; (c) reference transmitter 224 Gbps PAM4 eye diagram and (d) received electrical PAM4 eye diagram.

The 224Gb/s PAM4 reference transmitter optical and received electrical eye diagrams are shown in Fig. 18(c) and (d), respectively. The received eyes are also wide open with clearly distinguishable levels. Due to the excellent signal integrity provided by the FOWLP, we demonstrated that the photonic engine can also receive 8 channels of 224Gb/s PAM4 signals.

VII. Conclusion

In this work, we have demonstrated a low-cost, volume-manufacturable FOWLP-based silicon photonic engine package with an aggregate 1.79 Tbps (8 x 224 Gbps) transmit and receive capacity. We achieved both 112 GBaud NRZ (112 Gbps/λ) and PAM4 (224 Gbps/λ) transmission with minimal digital signal processing, demonstrating the viability of employing silicon photonics for 200 Gbps/λ CPO and LPO applications. Hence, by leveraging the enhanced signal integrity offered by FOWLP to reduce digital signal processing, such photonic engines will enable improved power efficiency and reduced latency for future optical interconnects for hyperscale data centers and AI/ML clusters. By scaling up the channel count on the PIC or by increasing the number of PIC chiplets in the FOWLP, the aggregate transmission capability can be further improved.

REFERENCES

[1] J. Williamson, “Co-packaged Optics: Putting the Pieces Together,” Optical Connection Magazine, pp. 34–39, Sep. 2022.

[2] M, Tan et al., “Co-packaged optics (CPO): status, challenges, and solutions,” Front. Optoelectron. 16, 1 (2023). doi.org/10.1007/s12200-022-00055-y

[3] Y. Shi et al., "Silicon photonics for high-capacity data communications," Photon. Res. 10, A106-A134 (2022)

[4] H. Hsia et al., "Heterogeneous Integration of a Compact Universal Photonic Engine for Silicon Photonics Applications in HPC," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 263-268, doi: 10.1109/ECTC32696.2021.00052.

[5] R. Nagarajan et al., "2.5D Heterogeneous Integration for Silicon Photonics Engines in Optical Transceivers," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 29, no. 3: Photon. Elec. Co-Inte. and Adv. Trans. Print., pp. 1-10, May-June 2023, Art no. 8200209, doi: 10.1109/JSTQE.2022.3214418.

[6] N. C. Abrams et al., "Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers," in Journal of Lightwave Technology, vol. 38, no. 13, pp. 3346-3357, 1 July1, 2020, doi: 10.1109/JLT.2020.2967235

[7] S. Razdan, P. De Dobbelaere, J. Xue, A. Prasad and V. Patel, "Advanced 2.5D and 3D packaging technologies for next generation Silicon Photonics in high performance networking applications," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 428-435, doi: 10.1109/ECTC51906.2022.00075.

[8] S. Shekhar, W. Bogaerts, L. Chrostowski et al. “Roadmapping the next generation of silicon photonics,” Nat Commun 15, 751 (2024). https://doi.org/10.1038/s41467-024-44750-0

[9] L. Yeary et al., "Co-packaged Optics on Glass Substrates for 102.4 Tb/s Data Center Switches," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 224-227

[10] L. Brusberg et al., "Glass Interposer for High-Density Photonic Packaging," 2022 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, 2022, pp. 1-3.

[11] J. H. Lau et al., "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 10, pp. 1729-1738, Oct. 2017, doi: 10.1109/TCPMT.2017.2715185

[12] V. S. Rao et al., "Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multi-layer Fine Pitch RDL for Mobile Applications," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2016, pp. 1522-1529, doi: 10.1109/ECTC.2016.203.

[13] X. Li et al., "1.6 Tbps (224 Gbps/λ) Silicon Photonic Engine Fabricated with Advanced Electronic-Photonic FOWLP for Co-Packaged Optics and Linear Drive Applications," 2024 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, 2024, pp. 1-3.

[14] S. B. N. Gourikutty et al., "Towards Heterogeneous Integrated Electronic-Photonic Packages for Hyperscale Data Centers," 2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC), Singapore, 2021, pp. 37-41

[15] S. B. N. Gourikutty et al., "A Novel Packaging Platform for High-Performance Optical Engines in Hyperscale Data Center Applications," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 422-427