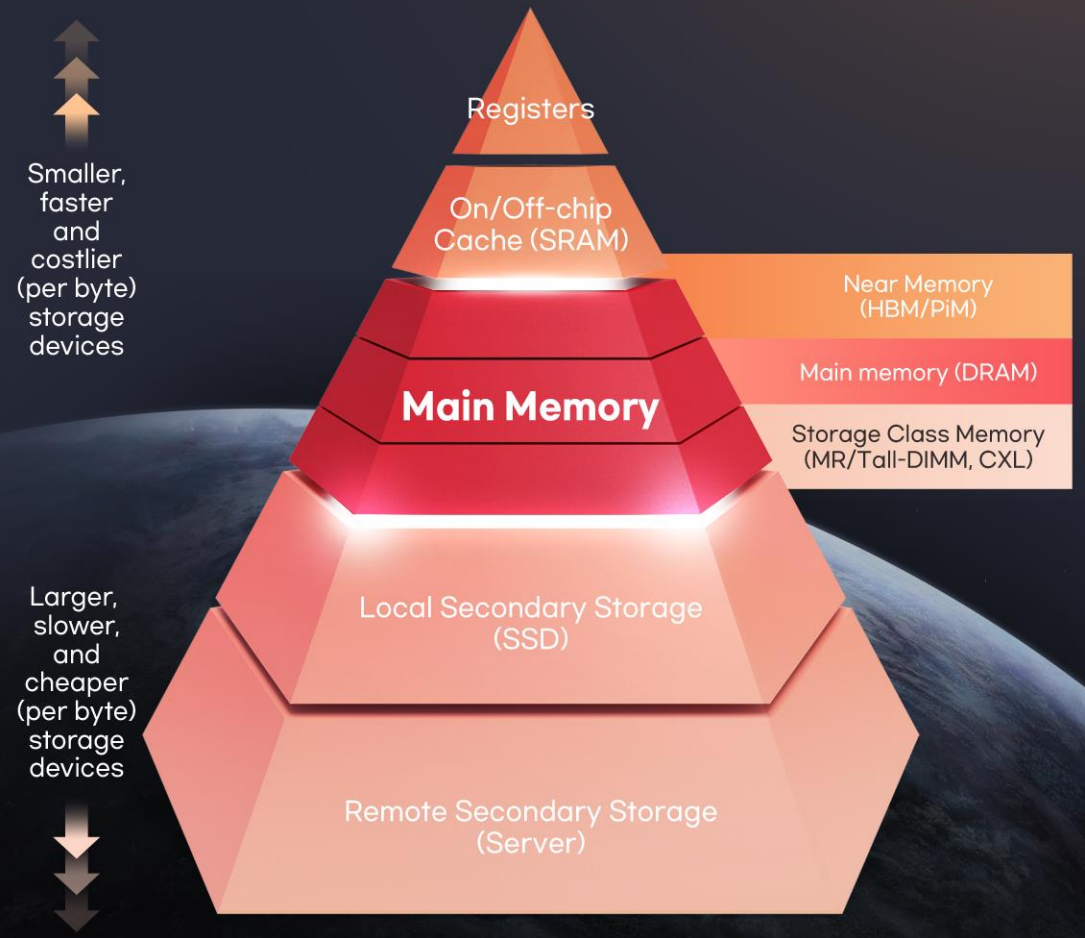
2023 Tech Seminar

Competitive Edge of SKH's HBM

Gyu Jei Lee I SK hynix PKG Development

Transforming Memory Performance Needs

Increasing importance of "Latency, Bandwidth*, Capacity" for optimal data transfer within the system



Multi → Many Core

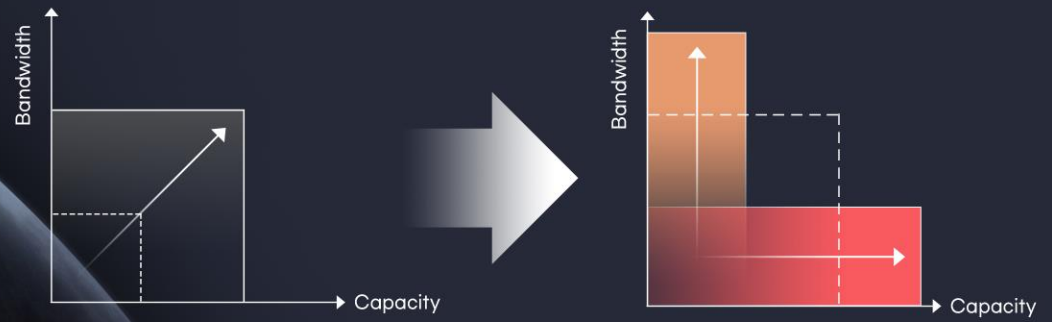
Heterogeneous Computing

- DRAM with on-chip cache

Homogeneous Memory

Heterogeneous Memory

- HBM (Bandwidth), ULM (Power)
- PIM (Offloaded Memory Operation), CXL (Emerging Interface)



*Bandwidth = Amount of data that can be transmitted within a given period of time
= Transfer Speed x # of Data paths(I/O)

*Source : S.H.Lee (SK hynix), IRPS Keynote Speech (2021)

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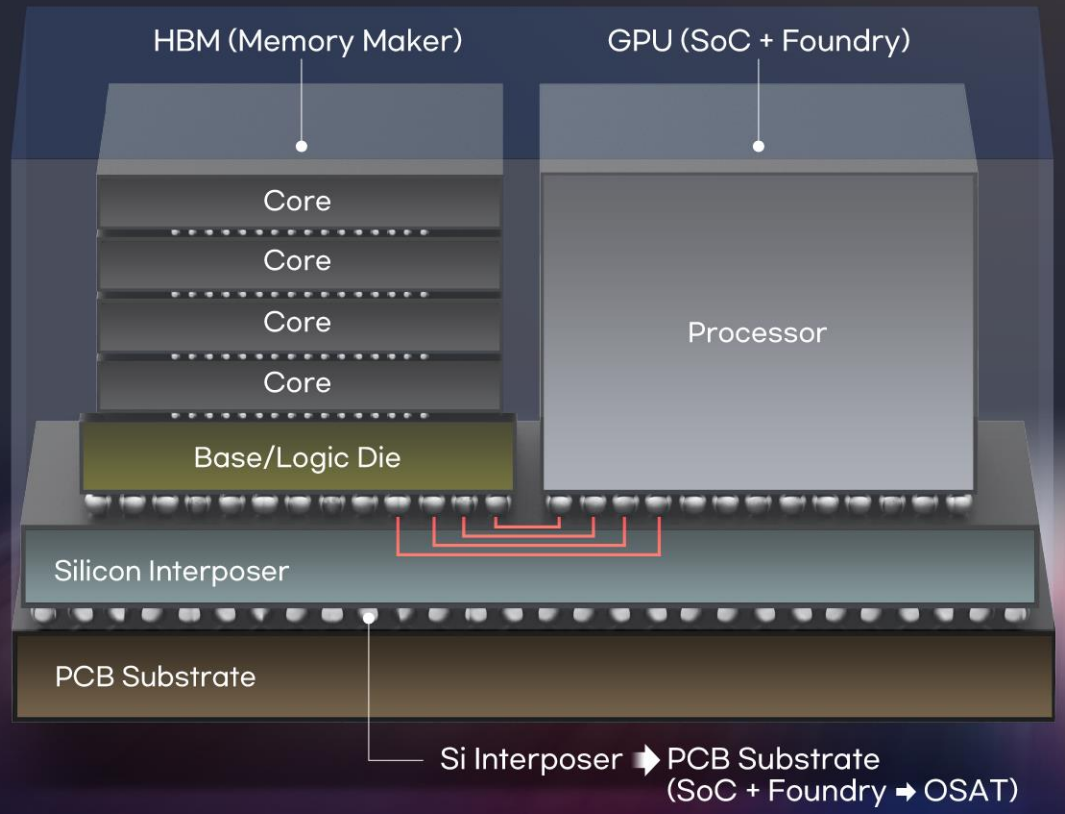
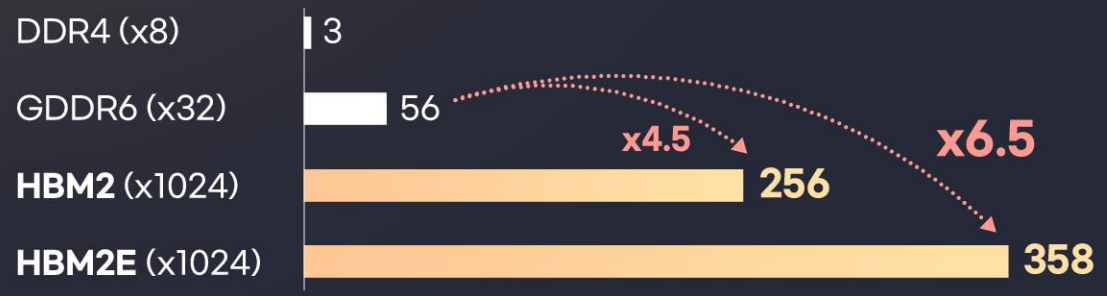
What is High Bandwidth Memory?

Memory that enables fast transfer of vast data with 1,024 Wide I/Os and 200GB~400GB high bandwidth

| 2.5D SIP(CoWoS) |



High Bandwidth [GB/s]



High Power Efficiency

*SiP (System in Package)

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Main Applications of HBM

Enables high bandwidth & space efficiency in applications such as HPC, Server, Network

Server & HPC

(Bandwidth, Capacity)

NVIDIA A100, DGX, H100

*Source: NVIDIA, CISCO, AMD, APPLE website

Network & Graphics

(Bandwidth)

CISCO 8000 Series

Desktop & Notebook

(Bandwidth, Cost)

AMD Radeon Pro 5600M
(Apple MacBook Pro)

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Leader of AI Memory, SK hynix

Enhancing company value based on tech readiness, wide product portfolio, preemptive & efficient investments

Outstanding HBM3E performance & quality based on numerous SiP field data

'15
HBM
(2Gb/1.0Gbps)

'18
HBM2
(8Gb/2.4Gbps)

'20
HBM2E
(16Gb/3.2Gbps)

- **World's fastest development**
- **x2** capacity per die
- **x1.5** Bandwidth
- Improve 36% thermal resistance

'22
HBM3
(16Gb/5.6Gbps)

- **World's first & only mass production**
- **x1.5** capacity with 12Hi line-up
- **x1.8** Bandwidth
- On-Die ECC
- Advanced Power management (Refresh rate expansion by Temp.)

'24
HBM3E
(24Gb/8.0Gbps)

- **x1.5** capacity per Core-die
- **x1.4** Bandwidth
- Improve 10% thermal resistance
- 0.9x Power efficiency (pJ/bit)

'26
HBM4

- 2K IO for B/W
- On going discussion in JEDEC
- Hybrid bonding
- Logic Foundry

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HBM Process Flow

HBM process comprises of Fab process, Bumping/Stacking process, and produced in KGSD* form

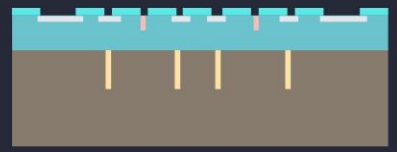
FAB | **Wafer Test** | **Bumping/ Stacking** | **KGSD* Test**

1 Silicon Etch

2 TSV Cu Fill

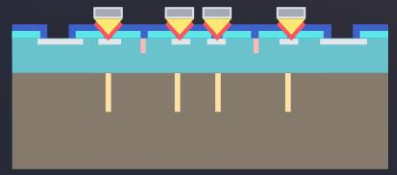
3 TSV Cu CMP

4 BEOL Metallization

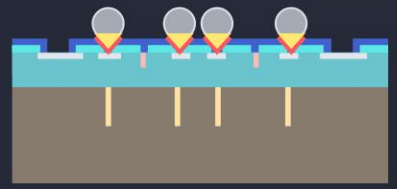


*KGSD (Known Good Stacked Die)

5 Front Side Bump Formation

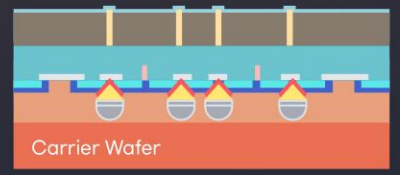


6 Wafer Solder Reflow

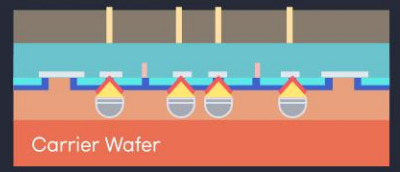


7 Temporary Carrier Bonding

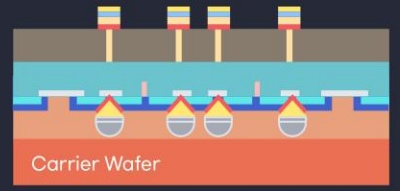
8 TSV Exposure & Back Side Passivation



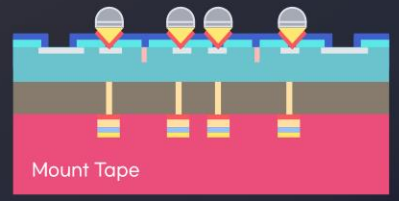
9 Passivation CMP & TSV Cu Exposure



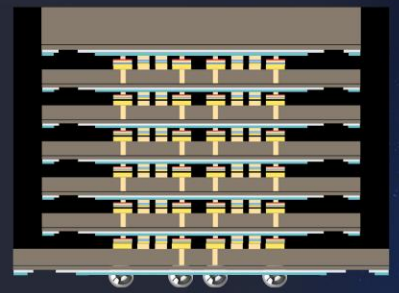
10 Back Side Bump Formation



11 Carrier Wafer Debonding & Thin Wafer Mounting On Tape



12 Chip Stacking & PKG Assembly With Overmold



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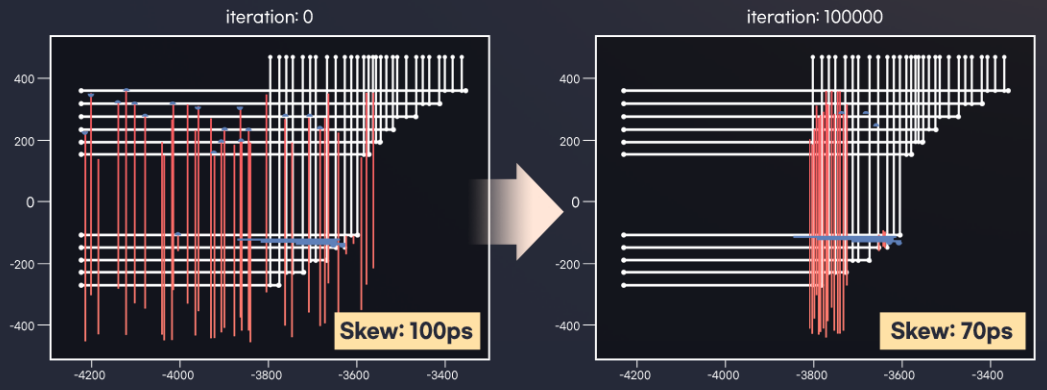
SK hynix HBM Strengths

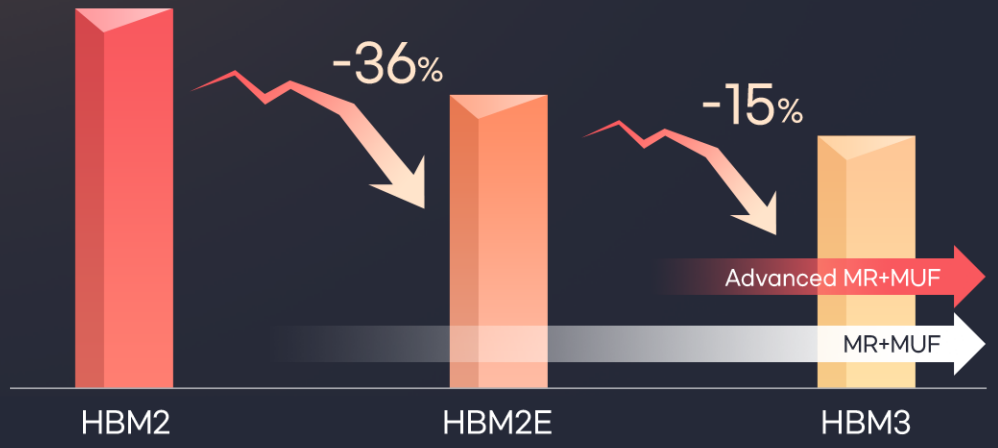
Speed & thermal advantages enabled by architecture optimization and proprietary tech

Speed

Signal line optimization based on machine learning



Heat dissipation



Time to Market

- Simultaneous evaluation of internal baseline & customer sampling
- Ensure internal baseline consistency from customer feedback (build virtuous cycle)

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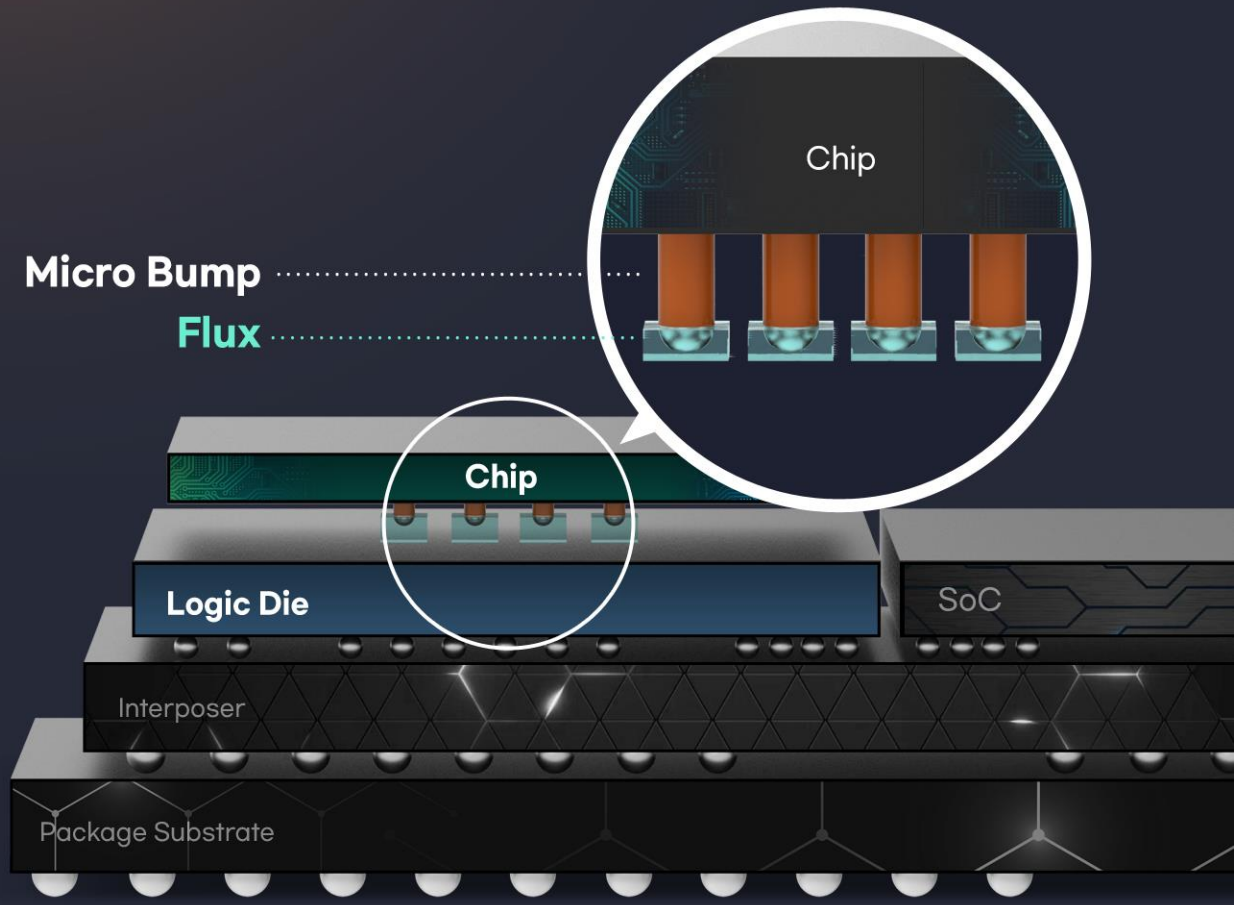
MR-MUF* Process

Reflow & Molding done simultaneously at room temperature, achieves 3~4x thermal bumps for heat dissipation
(Low Stress 10N/Room-Temp → Reflow)

MR-MUF Mass Reflow

1. **Stacking of micro bump-attached chip by applying metal molding material**
2. Melt all micro bumps at once, connecting chip and circuit
3. Gapfill between chips or between substrate, insulation and molding done simultaneously



*MR-MUF (Mass Reflow Molded Underfill)

MR-MUF* Process

Reflow & Molding done simultaneously at room temperature, achieves 3~4x thermal bumps for heat dissipation
(Low Stress 10N/Room-Temp → Reflow)

MR-MUF Mass Reflow

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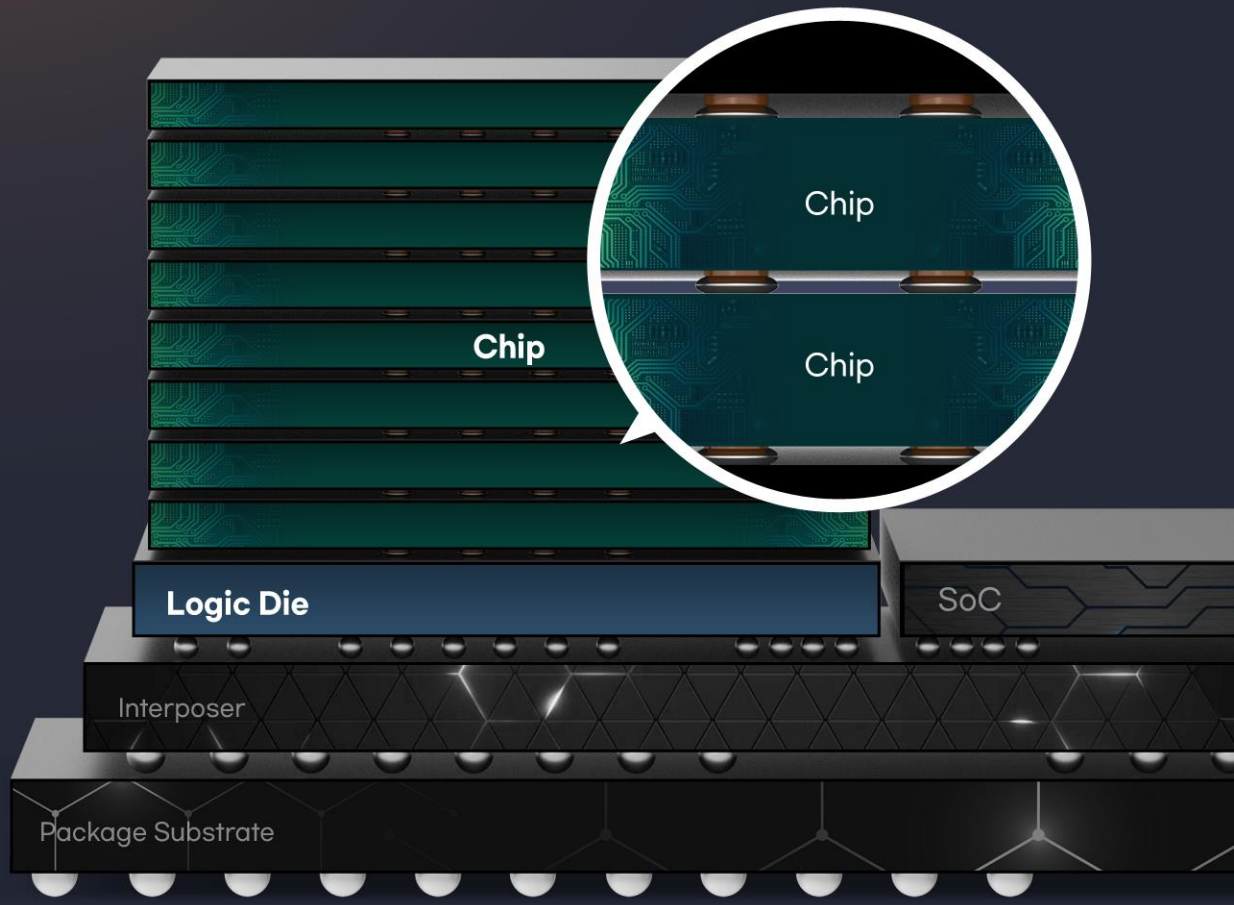

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MR-**MUF** Molded UnderFill

1. Stacking of micro bump-attached chip by applying metal molding material
2. Melt all micro bumps at once, connecting chip and circuit
3. **Gapfill between chips or between substrate, insulation and molding done simultaneously**

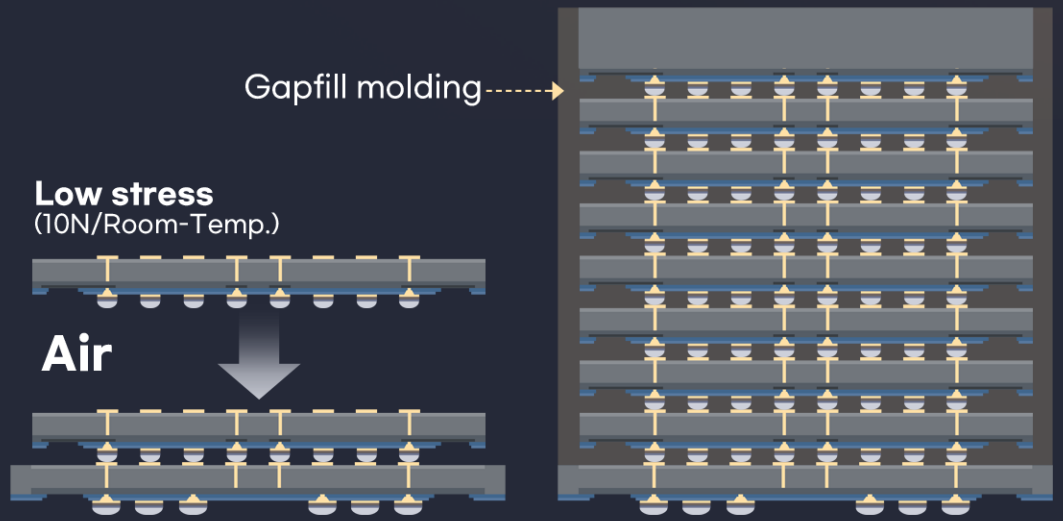
*MR-MUF (Mass Reflow Molded Underfill)

Comparison of Staking Method

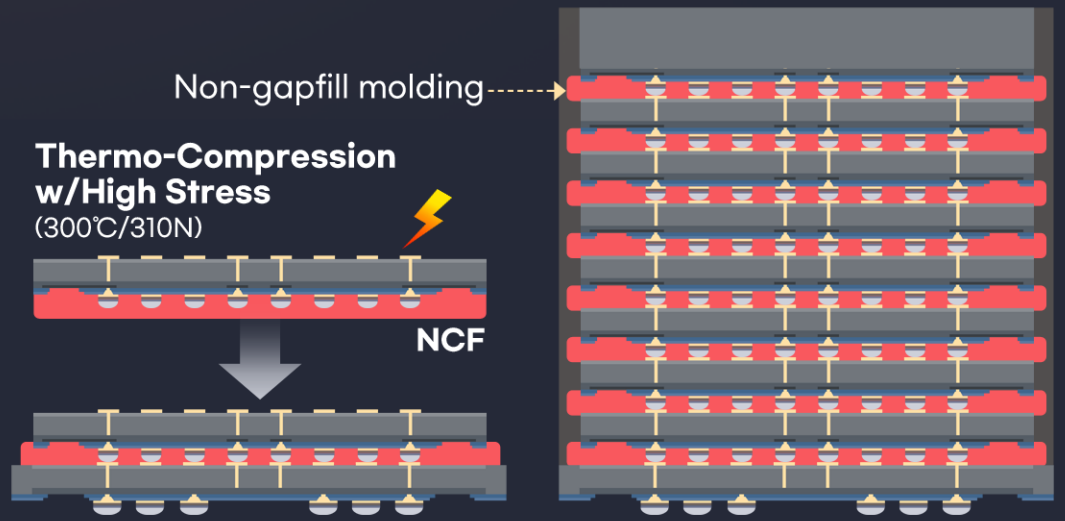
- Unlike TC-NCF*, penetrating bump through Gapfill molding (NCF) with high temp. & force is unnecessary
- Bonding done at idle stage, so key tech is ① **Chip warpage control**, ② **Gapfill-MUF material**
- ① Warpage control relates to **Nonwet yield (mass failure)**, ② MUF relates to **Void quality/reliability between chips**

※ Max. # of bumps from TC-NCF is 60k each

MR-MUF



TC-NCF



*TC-NCF: Thermo-Compression Non Conductive Film

Competitive Edge of SK hynix MR-MUF

Built technological entry barriers through years of proprietary control tech and exclusive rights to MUF materials

- Exclusive rights to MUF materials & molding equipment
- Advanced capabilities of chip-to-wafer warpage control tech
- Possession of proprietary control tech, such as high pressure molding tech

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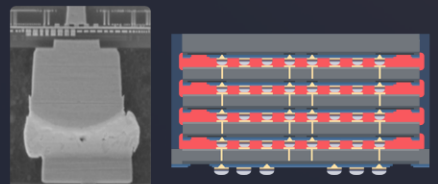
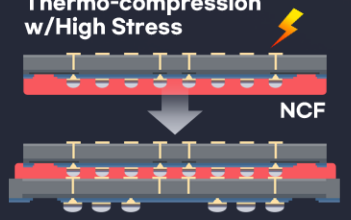
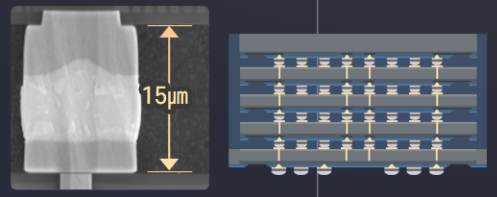
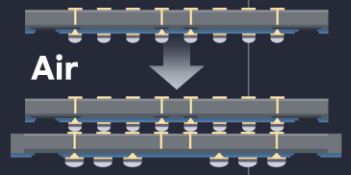
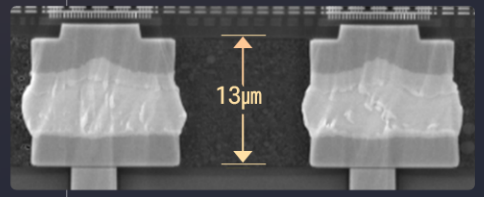
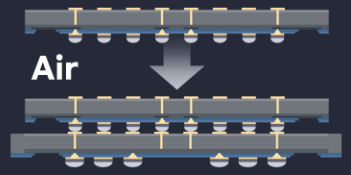
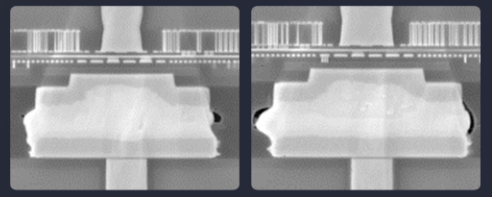
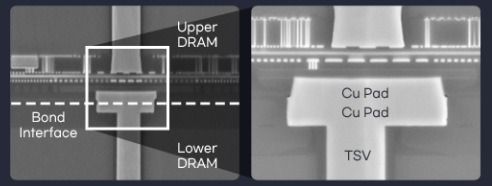
Strategies to Maintain HBM Competitiveness

Solidify HBM leadership through innovation of Advanced PKG tech

(1) Thermal bump maximization, (2) Gap height control, (3) Thermal enhanced filler

	HBM2	HBM2E	HBM3	HBM3 (12Hi) / HBM3E	HBM4
Stacking Tech.	TC-NCF	MR-MUF		Advanced MR-MUF	TBD
Remark	 Thermo-compression w/High Stress  NCF ✓World 1st TSV chip stack	 15μm Low Stress Air  ✓Low bond force & Robust joints: Higher Bump portion (thermal dissipation↑)		 13μm Low Force & thermal Air  ✓More Enhanced thermal dissipation : Lower gap height & thermal resistance↓	 Advanced MR-MUF  Hybrid Bonding
Achievable Stack Height	4Hi / 8Hi	4Hi / 8Hi		8Hi / 12Hi	12Hi / 16Hi
Thermal R (Relative)	○ (1.0)	○ (0.65)	○ (0.55)	◎ (0.5)	◎ (0.4 ~ 0.5)

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Making a better world with all members of society
by leading the tech-based IT ecosystem

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AI Market Outlook

Myoung Soo Park I SK hynix DRAM Marketing


AI and Memory:
Transforming Tomorrow's Technology Landscape
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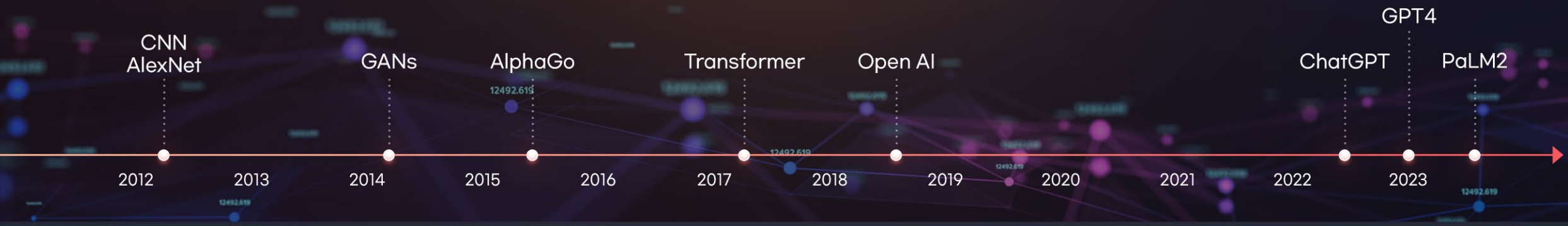
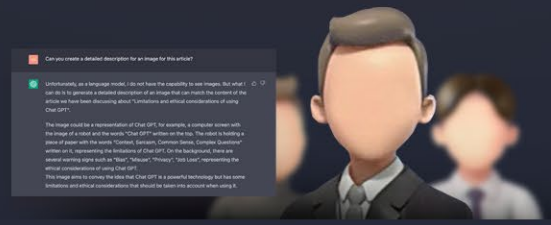
Beginning of AI Era

Generative AI: A decade of cumulative knowledge from theory to application





$1T+

Generative AI Revenue by 2032

(Source: Bloomberg, IDC)

560mn

ChatGPT MAU

(Source: SEMrush, Piper Sandler Research)

400+

ChatGPT Plugin Apps

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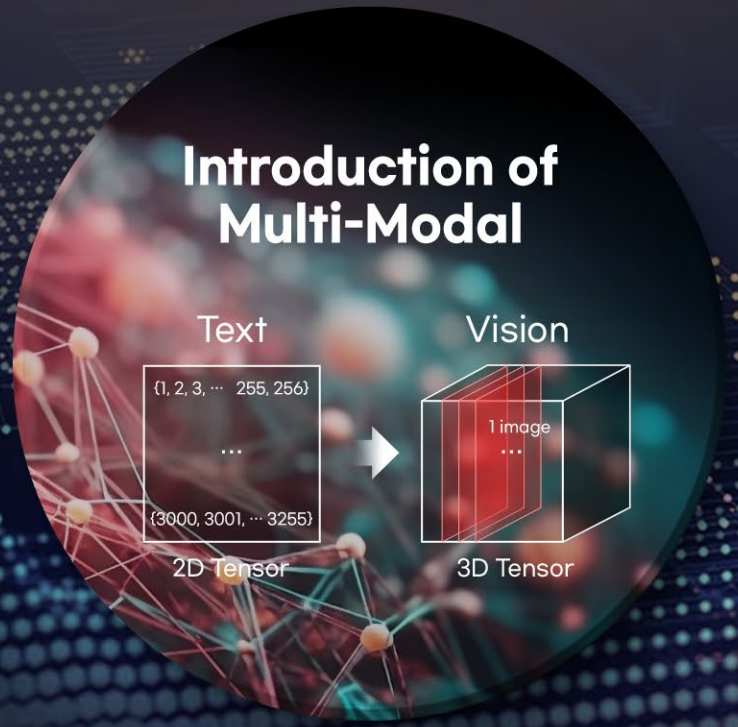
Vast H/W Needs and Ever-Increasing IT Infra Demand

Unprecedented levels of IT infra growth required to support exponentially increasing data processing needs in AI



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Competition in AI, the Driver Behind Memory Demand Growth

Evolution of AI to drive quantitative/qualitative growth of memory demand

General Server

HBM -

DDR5 **500GB**

AI Server

HBM **500GB+**

DDR5 **2~4x**

PiM
Process In Memory

CXL Memory
Compute eXpress Link

Computational Storage

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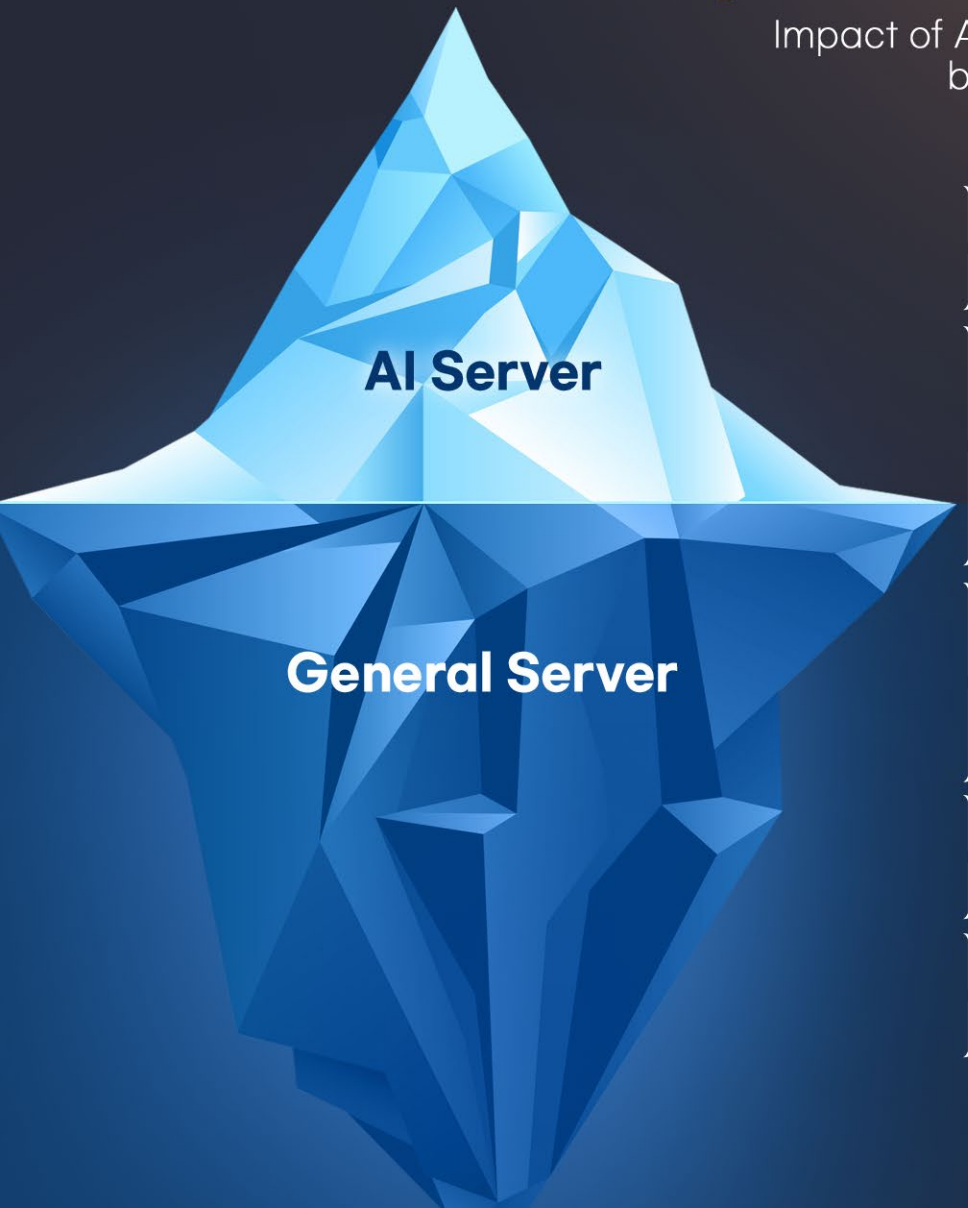
A Paradigm Shift: The Next Big Cycle of Growth

Impact of AI's explosive growth not limited to AI Servers,
but across broader IT Infra demand



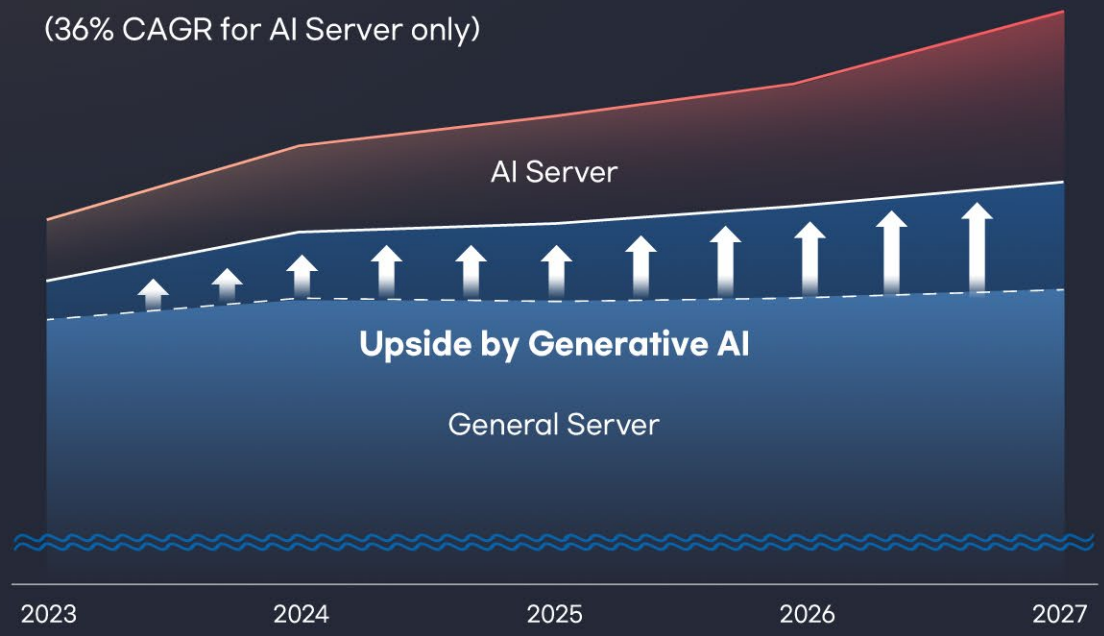
- Training
- Inference
- API & Management Platform
- Parameter Tuning
- IT Infrastructure

Server Set growing at

HSD% CAGR

fueled by Generative AI

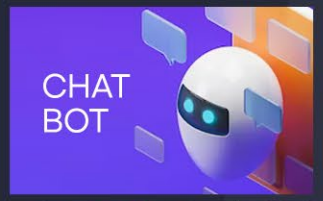
(36% CAGR for AI Server only)

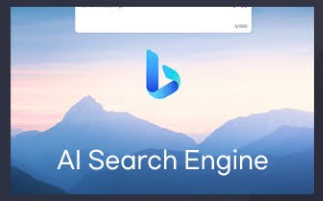


AI Memory Demand

Exponential memory demand growth mid-to-long term, even in conservative scenarios

Demand Service Type





Supply Accumulated Workload

DRAM Demand Upside from AI Servers

Solid demand growth mid-to-long term with explosive growth in AI market

Current Year

17%

In 5 Years

~38%

| AI Server Portion Out of Total Server Memory |

※ HBM / DDR4&5 included

| DRAM Demand Upside Driven by AI |

+40B Gb

For 5 years

AI Server
General Server

3~5X

Following years

+ On-device / Extended Application
+ New Memory Solution

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SK hynix's Market Position

Unparalleled leadership and No.1 position in HBM3/DDR5 market

World No.1 HBM3

HBM3 Market Share, 2023

Yr '24
Biz size more than 2X

World No.1 DDR5

DDR5 128GB Market Share, 2023

Yr '24
Biz size more than 2X

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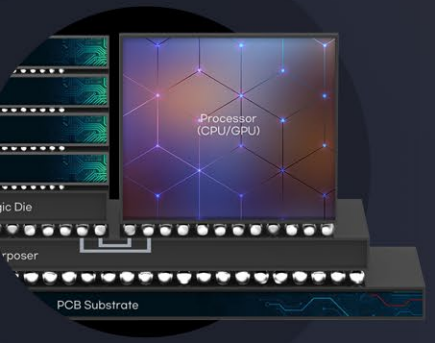
HBM/DDR5 Biz. Dynamics & SK hynix's Strengths

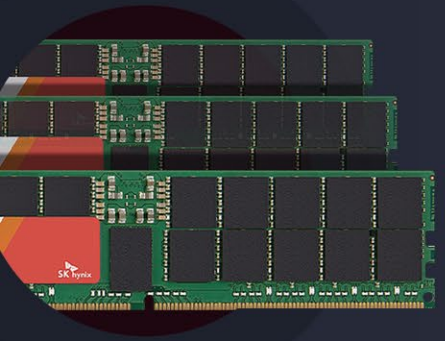
Best Memory Partner vouched by customers



HBM Biz Dynamics

- Complex biz. ecosystem
- Make-to-Order biz. Model
- Preemptive investments (for special process) based on demand estimates

→ High entry barrier for later entrants



DDR5 Biz Dynamics

- TSV essential for high-density modules (TSV required for 256GB+ modules even with 32Gb mono die)
- Increased # of product types & quality risk with new component additions on module

→ Leadership determined by product competitiveness

Right Partner, due to…

- Pre-validation & strengthened quality obtained by close collaboration with customers/SoC partners
- Unparalleled competitiveness in performance/quality/ supply capability/tech support
- Collaboration experience with major players and deep understanding of AI Ecosystem

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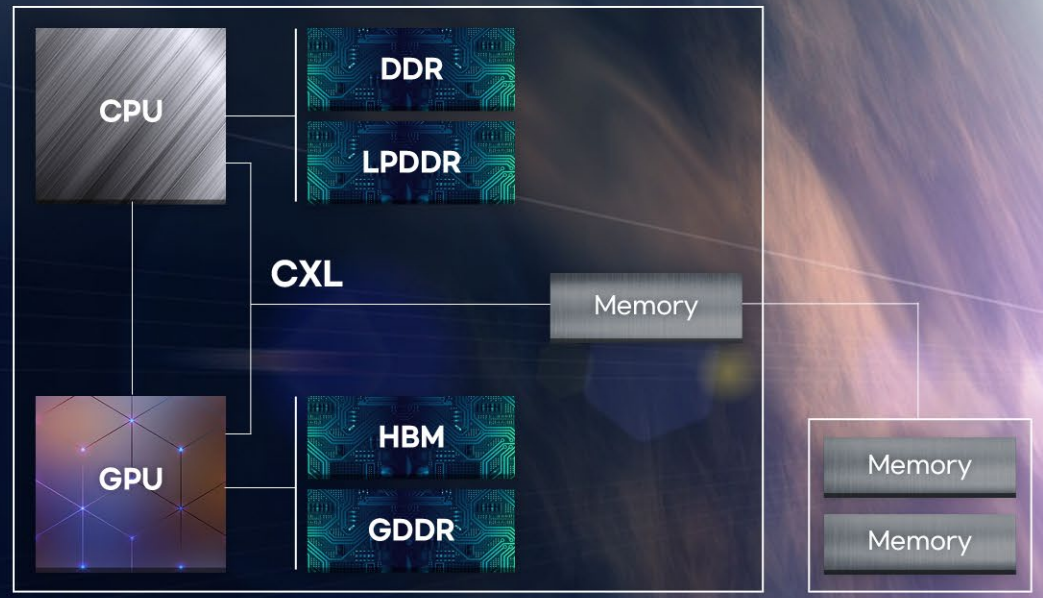
Heterogeneous Concept



Memory **Diversification** | Memory **Expansion** | Memory **Sharing/Pooling**

Always No.1

with Technology Leadership

PiM
Process In Memory

CXL Memory
Compute eXpress Link

Computational Storage

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