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ABSTRACT

Epitaxially grown Si/$Si_{1-x}Ge_x$ multi-stacks with ≥100 bilayers (≥200 sublayers) are being considered for three dimensionally vertically stacked dynamic random access memory devices. Because of the lattice mismatch between $Si_{1-x}Ge_x$ and Si, the high total layer thickness, and the need for sharp interfaces, it is challenging to develop a low cost epitaxial growth process. This work describes the material characteristics of multi-stacks containing up to 120 pairs (241 sub-layers) of {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} epitaxially grown on 300 mm Si wafers, with fully strained layer stacks at the inner part of the wafers. This Ge concentration allows a high etching selectivity during selective lateral $Si_{0.8}Ge_{0.2}$ removal later in the device fabrication. However, misfit dislocations are formed near the rim of the wafer, as the wafer edge lowers the energy barrier to form misfit locations. The drive for layer relaxation is reduced by reducing the lattice mismatch between Si and $Si_{1-x}Ge_x$. This can be done either by adding carbon into the $Si_{1-x}Ge_x$ or by reducing the Ge concentration in the $Si_{1-x}Ge_x$ layers. It will also be discussed how deposition on the reactor quartz tube might affect the temperature of the growing surface, leading to drifts in both layer-to-layer and within-wafer uniformities, and how these issues can be mitigated.

I. INTRODUCTION

Future scaling schemes of dynamic random access memory (DRAM) devices are expected to switch from vertical channel structures to three dimensionally (3D) stacked horizontal channel structures, schematically illustrated in Fig. 1 and similar to the gate all around (GAA) concept of metal–oxide semiconductor (MOS) devices.[1–5] Device fabrication will start with the epitaxial growth of an epitaxial Si/$Si_{1-x}Ge_x$ multi-stack, where ≥100 bilayers are targeted (≥200 sublayers). The Ge concentration in the $Si_{1-x}Ge_x$ should be sufficiently high, to enable, after fin patterning, a lateral $Si_{1-x}Ge_x$ removal with high etch selectivity to the adjacent Si layers.[6–8] On the other hand, the lattice mismatch between $Si_{1-x}Ge_x$ and Si sets a risk for layer relaxation, which can occur either via the formation of misfit dislocations or, at higher growth temperatures, via the so-called 3D island growth.[9–12] Layer relaxation via the formation of misfit dislocations has indeed been reported for multi-stacks consisting of 15 pairs of {20 nm Si/40 nm $Si_{0.7}Ge_{0.3}$},[13] 19 pairs of {32 nm Si/24 nm $Si_{0.8}Ge_{0.2}$},[14] and >6 pairs of {30 nm Si/53–63 nm $Si_{0.795}Ge_{0.205}$}.[15] In case of Si/$Si_{1-x}Ge_x$ multi-stacks for 3D DRAM applications, the risk for strain relaxation is reduced by considering thick Si/thin $Si_{1-x}Ge_x$ layers.[1,3,4] The lateral $Si_{1-x}Ge_x$ recess is then followed by a vertical Si thinning to obtain the required thickness for the Si channels. For epitaxial Si/$Si_{1-x}Ge_x$ multi-stacks with ≥100 bilayers and $Si_{1-x}Ge_x$ thicknesses of 10–15 nm, the total $Si_{1-x}Ge_x$ thickness still exceeds the theoretical critical thickness for layer relaxation.[9–11] Avoiding layer relaxation of the metastable epi-stack remains challenging, especially at the edge of the wafer[12,16,17] and if growth imperfections are locally present.[18] The latter is affected by the choice of the epitaxial growth conditions, e.g., in view of maximizing processing throughput.[19] Other challenges are the up to a factor 1000 difference in individual and total layer thickness, the

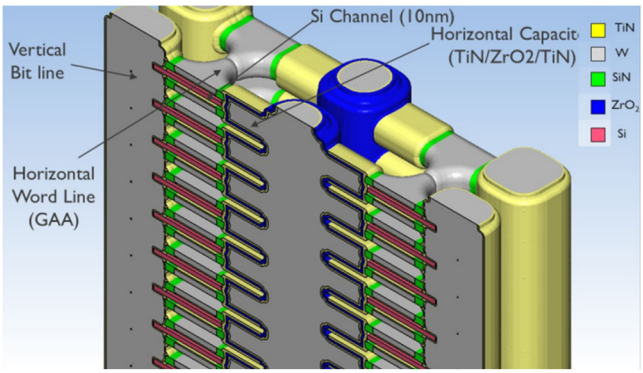

FIG. 1. Schematic of the 3D DRAM architecture.

requirement to maintain steep interfaces between individual layers, and the required uniformity control in thickness and composition not only laterally over the wafer but also through the stack from top-to-bottom and for each individual layer. Indeed, changes in the substrate surface temperature have been reported during the epitaxial growth of $Si/Si_{1-x}Ge_x$ multi-layers both on bulk Si[13] and on Si-on-oxide (SOI) wafers.[20] In the case of $Si/Si_{1-x}Ge_x$ growth on bulk Si, the changes in substrate surface temperature are affected by the deposition on the reactor quartz tube as discussed later in this paper. Finally, the wafer bow needs to be kept under control to enable accurate lithography steps after the layer growth.

The current paper describes the material properties of {20–65 nm Si/10–15 nm $Si_{1-x}Ge_x$} multi-layers epitaxially grown on 300 mm Si wafers. After a motivation of the choice of the used process conditions, the material characteristics of a multi-stack containing 120 pairs (241 sub-layers) of {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} will be presented, showing a fully strained layer stack at the inner part of the wafer. At the edge of the wafer, misfit dislocations are nevertheless present. Next, it will be discussed how the lateral thickness uniformity over the wafer might vary during growth. This effect is reduced by improving the control of the reactor quartz temperature. In this section, the vertical layer-to-layer uniformity will also be reported. For 30 bilayer stacks, it will finally be shown, how the density of misfits at the wafer edge varies as a function of the lattice mismatch.

II. GROWTH AND CHARACTERIZATION PROCEDURES

The epitaxial layers on top of 300 mm Si(001) wafers were grown in production compatible ASM Intrepid® RP-CVD cluster tools.[21] In addition, a few $Si_{1-x-y}Ge_xC_y$ growth studies on 200 mm Si(001) wafers have been performed, using an ASM Epsilon®2000 epi-reactor.[22,23] These systems are equipped with horizontal, cold wall, single wafer, load locked reactors each with a lamp-heated graphite susceptor in a quartz tube. The process temperature is monitored and controlled by thermocouples placed in the susceptor. The two available ASM Intrepid® RP-CVD cluster tools are different hardware generations. An important difference is the cooling of the reactor tube. The newer tool allows to control the reactor tube temperature.

Before layer deposition, the Si(001) wafer surface received a conventional wet-chemical clean. The native oxide has been removed *in situ* by a thermal treatment at a sufficiently high temperature (>1000 °C). Careful optimization of the temperature profile within the epi-reactor allows to avoid the formation of slip lines during the pre-epi bake.[12] Epitaxial growth was carried out at a reduced pressure using H_2 as carrier gas and conventional precursor gases {SiH_4, SiH_2Cl_2, GeH_4 [5% (Intrepid®) or 1% (Epsilon®) diluted in H_2], and B_2H_6 (50 ppm diluted in H_2)}. The $Si_{1-x}Ge_x$ layers were always nominally undoped. The Si layers were either undoped or contained a nominal boron concentration of 1×10^{18} cm^{-3}. This doping concentration is too low to expect any measurable impact on the growth behavior. The ASM Epsilon®2000 also contains a connection to a precursor gas for carbon doping (SiH_3CH_3, 1% diluted in H_2). During layer growth, the wafer rotates with a speed of 35 rotations per minute. The layer thickness over the wafer has been fine-tuned by growing single $Si_{1-x}Ge_x$ layers and Si-cap/$Si_{1-x}Ge_x$ double layers and measuring the thickness profiles over the wafers for different temperature settings during the growth. Optimizing the H_2 carrier gas flow and the temperature profile during layer growth has been enabled relative standard deviations in layer thickness <1.3%.[12]

The layer stack as targeted for 3D DRAM applications consists of a multi-stack with repeating $Si/Si_{1-x}Ge_x$ bilayers where the individual layer thicknesses are defined by the device integration scheme.[1–5] In the current work, the number of repeating bilayers has been varied between 3 and 120, and the nominal Si and $Si_{1-x}Ge_x$ thicknesses have been set to 20, 30, 60, or 65 nm for Si and to 10 or 15 nm for $Si_{1-x}Ge_x$, respectively. In some cases, an additional boron doped Si buffer layer has been grown in between the Si substrate and the $Si/Si_{1-x}Ge_x$ multi-stack. After the epitaxial growth of the multi-stack, the substrate can suffer from a severe wafer deformation, which varies as a function of the number of bilayers, the composition of the $Si_{1-x}Ge_x$ layers, and the strain state of the layer stack.[16] This wafer deformation has been measured using a Patterned Wafer Geometry tool (PWG5™) from KLA.[24] Wafer bows exceeding 100 μm have been compensated by depositing a compressive silicon nitride stressor layer on the wafer backside.[25] Before depositing the nitride stressor, the front side of the wafer was covered by a protective 1 μm thick deposited silicon oxide layer, which was afterwards removed by a buffered HF solution. Still, backside deposition of the silicon nitride stressor might create some damage/add some particles on the front side of the wafer. These types of particles/damages are not related to the epi processing.

A broad range of material characterization techniques have been used to study the epitaxial material properties. Light scattering is generally accepted to determine wafer quality and cleanliness. The technique is also suitable to study the crystalline quality after hetero epitaxy.[12,26–29] Non-uniformities on the wafer surface will cause increased light scattering. Besides the signal from large size imperfections such as particles, there is a background signal that contains information about surface roughness and surface defects. The low frequency component of the background signal (haze) of such a light scattering tool can be related to a slowly varying surface roughness. Imperfections and haze data are collected from a wafer surface by illumination with a laser beam, collecting the scattered light through an optics system, and amplifying the scattered light with a photomultiplier tube. In this work, the approach reported in Ref. 29 has been followed using the KLA Surfscan® SP5, which executes both the inspection and the in-line data analysis. After

the signal is collected, the resulting data are analyzed to determine the presence of Light Point Defects (LPDs) aligned either horizontally or vertically. It is well-known that $Si_{1-x}Ge_x$ strain relaxation goes together with the formation of misfit dislocation causing a typical crosshatch pattern on the wafer surface.[10–12] The crosshatch pattern is vertically (i.e., perpendicular to the tangent at the wafer notch) or horizontally aligned (perpendicular to the previous ones) and as such, it is possible to use this characteristic for their classification.[29] Surface haze maps and scattered light intensity plots have been taken with edge exclusions of 3 mm. The surface morphology was further studied by in-line atomic force microscopy (AFM) using an automated Park NX-3DM from Park Systems, by in-line scanning electron microscopy (SEM) inspections using automated defect inspection systems which probe several regions over the wafer such as the KLA Electron-Beam Wafer Defect Review (EDR™) System, and the automated optical inspection system.[30] The observed surface morphologies after epitaxial growth did not show clear differences compared to those of the incoming wafers. The presence/absence of misfit dislocations was also studied by room temperature photoluminescence (PL) measurements, which have been performed using a production compatible En-Vision-3000 system from Semilab.[31,32] This inspection system allows for automatic 200/300 mm wafer tests and targets quick, non-contact and non-destructive detection of nm scale PL active buried defects. The Micro-PL measurement, for characterizing optical properties of materials on a micrometer scale, is based on a high intensity illumination at 532 nm. The detection is carried out at either band-to-band PL, with a peak intensity at 1100 nm (1.127 eV), or using a 1400 nm long pass filter for 1400–1600 nm (0.89–0.78 eV).

The Ge concentration in $Si_{1-x}Ge_x$ layers, the Si and $Si_{1-x}Ge_x$ layer thicknesses, and the possible presence of layer relaxation were extracted from high resolution x-ray diffraction (HRXRD) $\omega - 2\theta$ scans and reciprocal space maps (RSMs) using Bruker JVX7300M x-ray metrology tools. Also, the individual thicknesses of $Si/Si_{1-x}Ge_x$ bilayers have been measured by HRXRD collecting data points at six different positions over the wafer (line scan from wafer center to 20 mm from the edge). In case of multi-stacks, data fitting was done assuming a repetition of $Si/Si_{1-x}Ge_x$ bilayers with identical layer thicknesses and composition. For single $Si_{1-x}Ge_x$ layers and for $Si/Si_{1-x}Ge_x$ double layers, the within-wafer uniformity of individual layer thicknesses was measured by means of spectroscopic ellipsometry (KLA Spectra CD™100) following the measurement routines described in Refs. 33 and 34 (49 point line scan over the full diameter with 5 mm edge exclusion). Multi-stacks with 3–120 $\{Si/Si_{1-x}Ge_x\}$ bilayers were also studied by cross-sectional transmission electron microscopy (TEM) to confirm two-dimensional layer by layer growth, to confirm the absence or presence of misfit and threading dislocations, and to study possible variations in individual layer thicknesses through the layer stack. Energy-dispersive x-ray spectroscopy (EDX) was used to study possible top-down variations in composition. The interface abruptness between two sublayers of the epi-stack has been characterized by high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM).[35] The TEM specimens were prepared by focused ion beam (FIB) with a target lamella thickness of ~80 nm. The effect of the lamella thickness on the extracted interface thickness is supposed to be negligible. Si and Ge depth profiles have been obtained by secondary ion mass spectrometry (SIMS) using an ultra-low energy capable SIMS instrument (SC-Ultra) with an O_2^+ sputtering beam of 150–500 eV.[36] A Cs^+ beam has been used to verify the absence of background contamination of oxygen and carbon as this provides a lower detection limit ($\sim 2 \times 10^{17}$ cm^{-3} for both elements).

III. CHOICE OF GROWTH CONDITIONS

Using $Si/Si_{1-x}Ge_x$ multi-stacks, with ≥100 bilayers for 3D DRAM applications, sets a need to develop low cost deposition schemes. This requires high throughput processing, which is typically achieved at higher growth temperatures.[19,37,38] On the other hand, a maximum in growth temperature is set by the requirements to enable 2D layer growth, steep gradients in concentrations at the $Si/Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x/Si$ interfaces, and aiming a defect free and fully strained layer stack without the presence of misfit dislocations.[9–12,16] At low growth temperatures, the abruptness of the compositional change at $Si/Si_{1-x}Ge_x$ interfaces is limited by Ge segregation occurring during Si layer growth on top of the $Si_{1-x}Ge_x$ surface. The most abrupt interfaces have been obtained when using a chlorinated chemistry.[39,40] This sets a preference for using dichlorosilane (DCS, $SiCl_2H_2$) as Si precursor gas. However, in the given temperature range, it provides significantly lower deposition rates compared to SiH_4, especially for the Si-growth.[37,38] The use of DCS sets, therefore, a need to use a higher growth temperature, which increases the risk for Si/Ge interdiffusion in the first layers while growth proceeds. The effect of process temperature on Si/Ge intermixing during epitaxial growth is illustrated in Fig. 2. A series of epitaxial layers have been grown with the stack shown in Fig. 2(a) and using identical growth conditions for all layers. The epitaxial growth was immediately followed by an *in situ* post epi anneal at different temperatures and for a total duration, which is similar to the deposition time as needed for the epitaxial growth of ~100 $\{Si/Si_{1-x}Ge_x\}$ bilayers when using DCS as Si precursor gas. This allows to study the possible presence of Si/Ge interdiffusion without suffering from degradations in depth resolution during the SIMS measurement, which would be a limitation in case of real multi stacks with a total of 100 bilayers. Figures 2(b) and 2(c) show the Si/Ge intermixing for the different post-epi annealing temperatures. The increment of the width of the Ge profile indicates that a measurable Si/Ge intermixing is seen for all post-growth annealing conditions used in this experiment (≥755 °C). At these growth temperatures, Si/Ge intermixing will cause a degradation of the interface sharpness during the deposition of tall multi-stacks. The use of SiH_4 as Si precursor gas during Si-growth allows to reduce the growth temperature while still obtaining acceptable growth rates. In this case, the Si/Ge intermixing is significantly lower as confirmed by the SIMS data shown in Fig. 3. An epi-stack of 10 nm $Si_{0.8}Ge_{0.2}$-cap/6× {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} has been grown. In case of the second wafer, the growth has been interrupted after the deposition of the last Si-layer while keeping the reactor temperature at the growth temperature (675 °C) and this for a duration which is equivalent to the deposition of 60 additional bilayers. The SIMS spectra of both samples are exactly overlapping, which shows that the Si/Ge intermixing is below the detection limit of the measurement technique. Unfortunately, it is not possible to compare the interface

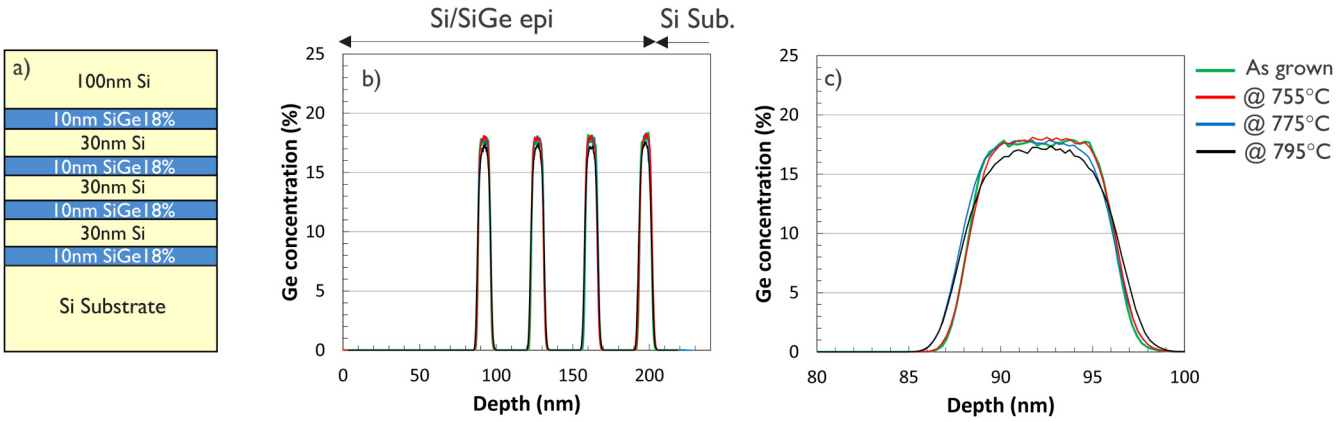

FIG. 2. (a) $Si/Si_{0.82}Ge_{0.18}$ multi-stack processed to study the impact of high temperature growth on Si/Ge intermixing. The epitaxial growth was followed by *in situ* post-epi anneals at different temperatures and a duration of 172 min. (b) and (c) Ge profiles as measured by SIMS and for different post-epi anneals. (b) Full layer stacks and (c) area around the topmost $Si_{0.82}Ge_{0.18}$ layers. The x-axis of the profiles has been slightly re-aligned to correct for small differences in sputter rates during the SIMS measurements.

sharpness for the spectra shown in Fig. 2 vs those shown in Fig. 3, as the SIMS measurement conditions were not identical. The spectra reported in Fig. 3 have been extracted with a higher sputter energy of the O^{2+} beam, which degrades depth resolution. If not mentioned differently, the epitaxial layers discussed in the remaining sections have been grown with this set of growth conditions. $Si_{1-x}Ge_x$ layers have been grown using SiH_2Cl_2 and GeH_4 and Si-layers with SiH_4, both at a growth temperature of 675 °C.

IV. CHARACTERISTICS OF $Si/Si_{1-x}Ge_x$ MULTI-LAYERS AND PROCESS IMPROVEMENTS

A. 120× {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$}

Cross-sectional TEM images confirm the excellent material quality with two-dimensional layer growth and smooth $Si/Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x/Si$ interfaces as shown in Fig. 4(a) for a multi-stack consisting of 120 pairs of {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} layers. No misfit or threading dislocations are detected. EDX measurements confirm a constant $Si_{0.8}Ge_{0.2}$ layer-to-layer composition from top to bottom. The high material quality and the absence of strain relaxation have been confirmed by RSM [Fig. 4(b)]. The red arrow shows the position of the peak assigned to the Si substrate. The multiple higher-order satellite peaks are assigned to the multi-stack and are vertically aligned with respect to the Si substrate peak. This indicates that no strain relaxation can be measured for the 120 bilayer stack. The thickness fringes are well resolved and the peak sharpness [in Q(x) direction] is given by the resolution limit of the measurement setup. The absence of layer relaxation for a total nominal $Si_{0.8}Ge_{0.2}$ thickness of 1.2 μm is remarkable as it is far above the theoretical critical thickness for layer relaxation

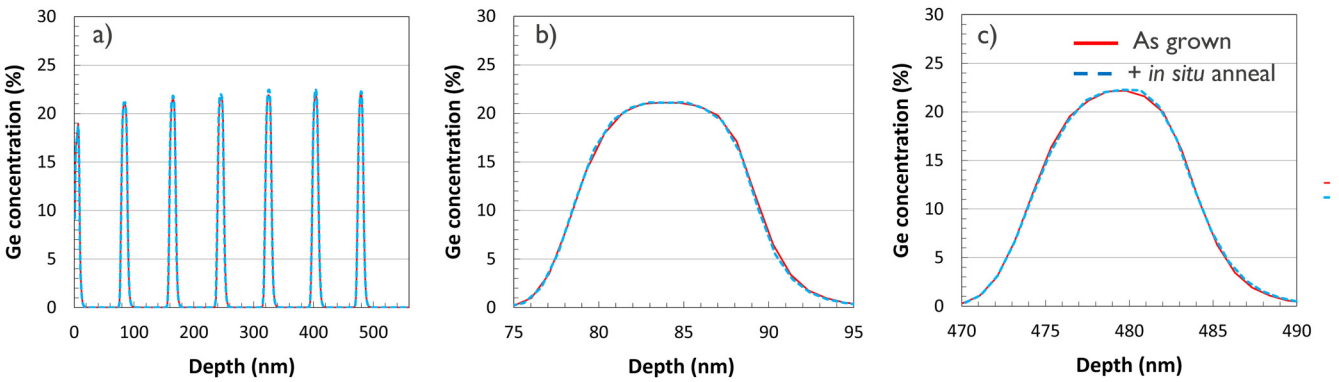

FIG. 3. Ge profiles as measured by SIMS for two multi-stacks consisting of 10 nm $Si_{0.8}Ge_{0.2}$-cap/6×{65 nm Si/10 nm $Si_{0.82}Ge_{0.18}$}//Si substrate. The layer for which the Ge profile is plotted in blue, received an additional *in situ* anneal at 675 °C for 152 min in between the last Si-layer and the $Si_{0.8}Ge_{0.2}$-cap. (a) Ge profiles over the full depth of the epi-layer, (b) Ge profiles around the sixth $Si_{0.8}Ge_{0.2}$-layer, and (c) Ge profiles around the first (deepest) $Si_{0.8}Ge_{0.2}$. The x-axis of the profiles has been slightly re-aligned to correct for small differences in sputter rates during the SIMS measurements.

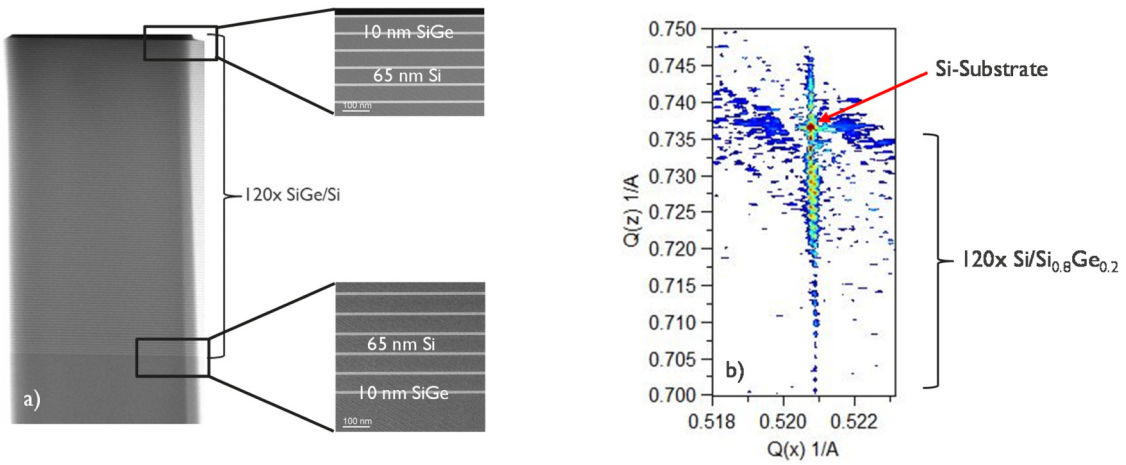

FIG. 4. (a) Cross-sectional TEM image and (b) RSM around 224 reciprocal lattice points as measured for an epitaxial multi-stack consisting of 10 nm $Si_{0.8}Ge_{0.2}$-cap/120×(65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$)//Si substrate and obtained at the center of the wafer.

(15 nm for a single $Si_{0.8}Ge_{0.2}$ layer[10]) and also above the experimental critical thickness reported for a single $Si_{0.8}Ge_{0.2}$ layer (<300 nm[11]), although it is known that higher metastable critical thicknesses can be reached for $Si/Si_{1-x}Ge_x$ multi-layers.[16] Still, the capability to deposit a total $Si_{0.8}Ge_{0.2}$ thickness of 1.2 μm without measurable layer relaxation is only possible by growing the epitaxial layer at a sufficiently low temperature and by minimizing contamination such as particles and oxide incorporation in the epitaxial layer.[12,18,41] The oxide and carbon levels in the epitaxial layers are indeed below the SIMS detection limit ($\sim 2 \times 10^{17}$ cm^{-3} for both elements). This is obtained by applying a thermal removal of the native oxide before the epitaxial growth and the use of the purest process gases which are commercially available. The number of particles on the incoming 300 mm wafers can be kept below 5 for a particle size of ≥100 nm, and the choice of process gases, especially the use of DCS during $Si_{1-x}Ge_x$ growth, allows to avoid growth imperfections. All of this increases the energy barrier that needs to be overcome to break chemical bonds at the substrate/$Si_{1-x}Ge_x$ interface, therefore preventing the formation of misfit dislocations, except for the area near the wafer bevel as discussed in Sec. IV C.

The interface abruptness has been extracted from horizontally integrated HAADF-STEM contrast images. Figure 5(a) shows, as an example, a cross-sectional HAADF-STEM taken at the bottom part of the 120×bilayer stack discussed before. The HAADF-STEM contrast is approximately proportional to the square of the atomic number, which allows to extract the Ge depth profiles [Fig. 5(b)]. The integrated contrast has been fitted with the Sigmoid function, which is expressed as

$$f(x) = \frac{C}{1 + e^{\frac{\pm (z_0 - x)}{\tau}}} + b, \quad (1)$$

where C and b are constants and z_o denotes the position of the interface. The value of 4τ is used as the interface thickness.[42] Note that the integrated contrast profile shown in Fig. 5(b) has been obtained by integrating over a large area of the TEM specimen [in the given example, the integration was done over the area which is in Fig. 5(a) marked by the yellow square]. The extracted 4τ values include contributions from interfacial roughness and are therefore larger than the values obtained when extracting the contrast profile from a vertical line scan. The interfaces from Si (bottom side) toward $Si_{0.8}Ge_{0.2}$ (top side) are, as expected, slightly sharper than the interfaces from $Si_{0.8}Ge_{0.2}$ (bottom side) toward Si (top side) [Fig. 5(b)]. For the latter one, the abruptness of the compositional change is affected by Ge segregation, occurring during Si layer growth on top of the underlying $Si_{0.8}Ge_{0.2}$ surface. Still, the values of the interface thicknesses as extracted for the bottom layers of the multi-stack are relatively high and larger compared to those obtained for the upper part of the layer stack (Table I). This indicates that there is still some Si/Ge interdiffusion during the deposition of the epi-stack, which has, depending on the number of bilayers, a thickness of up to 9 μm.

These material properties are obtained at the inner part of the wafer (radius of at least 10 cm from the wafer center) showing the potential of these epi-layers for 3D DRAM applications. Still, the epi-layers are not yet perfect, and some material parameters need to be improved. Examples are the vertical layer-to-layer uniformity in thickness, a degradation in within-wafer uniformity in layer thickness during the growth, and the presence of layer relaxation at the edge of the wafer. These items are discussed in Secs. IV B and IV C.

B. Lateral and vertical control of layer thickness and composition

A critical look at the cross-sectional TEM images of Fig. 4(a) shows that the layer stack with 120 $Si/Si_{0.8}Ge_{0.2}$ bilayers suffers from vertical layer-to-layer variations in layer thickness. This becomes more clear when placing the images taken at the top and bottom of the stack next to each other (Fig. 6). In the top part of the stack, the repeating bilayers are thinner compared to those at the bottom of the

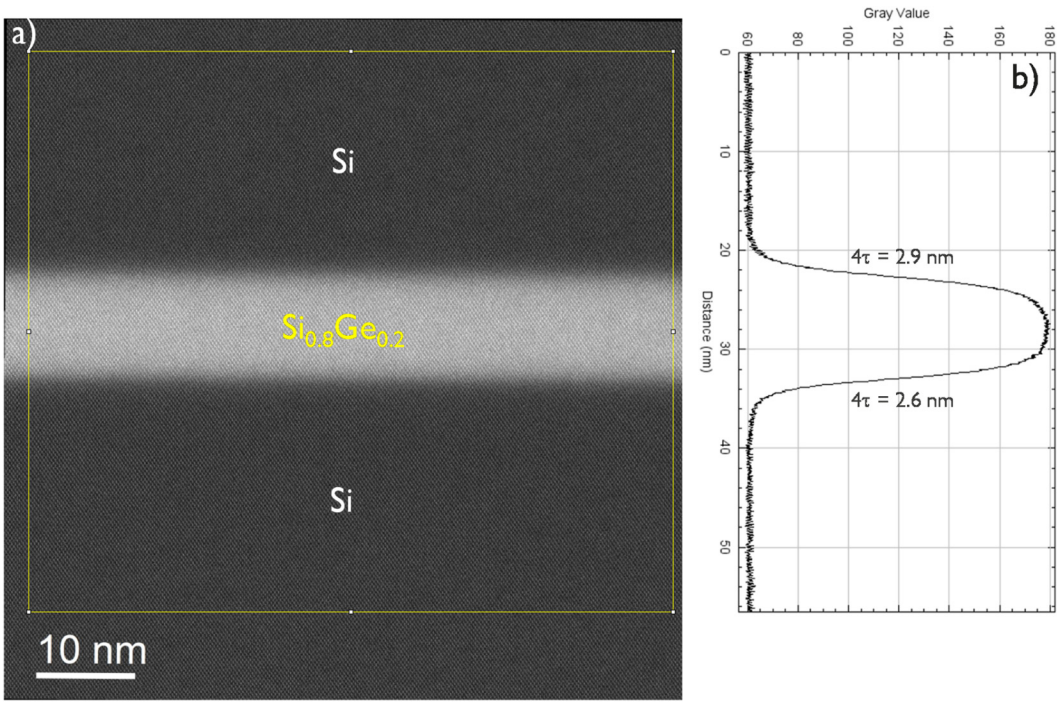

FIG. 5. (a) Cross-sectional HAADF-STEM taken at the bottom part of the 120× bilayer stack reported in Figs. 4(a) and (b) corresponding to horizontally integrated contrast profile. The numbers mentioned at the Si/$Si_{0.8}Ge_{0.2}$ and $Si_{0.8}Ge_{0.2}$/Si interfaces are the interface thicknesses obtained after fitting the contrast profiles with the Sigmoid function. The yellow square in (a) marks the area of the TEM specimen over which the contrast image integration was done.

stack, although exactly the same process settings have been used, including the same deposition times. This variation in layer thickness is also reflected in the XRD ($\omega - 2\Theta$) spectra. In Figs. 7(a) and 7(b), the measured XRD spectrum as obtained for a multi-stack consisting of 60 bilayers is compared with the spectrum as predicted by the fitting software. The peak at 0 arcsec appears from the Si substrate and the multiple higher-order satellite peaks (mainly at negative angles) are due to the superlattice periodicity. The peaks with the higher intensities are assigned to the $Si_{0.8}Ge_{0.2}$ layers, and their positions are close to those predicted by the model. This confirms that both the composition and the layer thicknesses are close to the specified values (20% Ge and 10 nm, respectively). However, at angles below −1000 arcsec, the peaks are broader and eventually split into double peaks. As a result, the predicted peaks with a lower intensity and assigned to interference fringes linked with the Si sublayers are (nearly) invisible in the measured XRD spectrum shown in Fig. 7(a). An automatic fitting of the XRD spectrum could still be done, assuming equal thicknesses and compositions for all Si and $Si_{1-x}Ge_x$ layers, except for the Si_{1-x}-Ge_x-cap layer. The fitting calculated a thickness of 11.7 nm and a Ge concentration of 22.9% for the $Si_{1-x}Ge_x$-cap layer and a multi-stack consisting of 60×{64.2 nm Si/10.7 nm $Si_{0.805}Ge_{0.195}$}. These thicknesses and compositions are close to the nominal values. Still, the peak broadening suggests a non-uniformity in the layer stack as confirmed by cross-sectional TEM inspections and also reported by other researchers.[13]

TABLE I. Si-top/$Si_{0.8}Ge_{0.2}$ and $Si_{0.8}Ge_{0.2}$-top/Si interface thicknesses expressed in nm as extracted in the upper and lower parts of epitaxially grown Si/$Si_{0.8}Ge_{0.2}$ multi-stacks with different numbers of bilayers.

		First		Second		Third		Bottom	
Wafer label	No. of bi-layers	Si/SiGe	SiGe/Si	Si/SiGe	SiGe/Si	Si/SiGe	SiGe/Si	Si/SiGe	SiGe/Si
AL401908/D07	4	1.60	0.96	1.64	1.05	1.64	0.94	1.71	0.94
AE350987/D21	4	1.51	0.65						
AE310920/D15	60	1.83	1.30					2.79	2.42
AE314029/D02	120							2.86	2.59

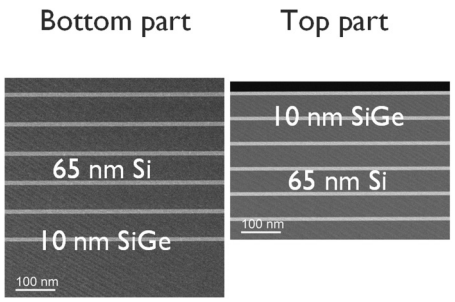

FIG. 6. Vertical layer-to-layer variation in layer thickness illustrated by placing the cross-sectional TEM images taken at the top and bottom of the stack with 120× bilayers [Fig. 4(a)] next to each other.

The vertical variation in layer thicknesses is not seen for layers with a significantly lower total thickness. Indeed, the XRD spectra are better resolved for epi-stacks with a lower number of bilayers where we also reduced the thickness of the individual Si layers [Fig. 7(c)]. In this case, the high intensity peaks are sharper and the fringes assigned to the Si layers are clearly observed.

The vertical variation in layer thicknesses, as seen for rather thick layer stacks, goes together with a change of the within-wafer uniformity of the individual layer thicknesses. Si-cap/19 nm $Si_{0.75}Ge_{0.25}$//Si substrate double layers with different Si thicknesses have been grown to visualize the variation in within-wafer uniformity as a function of the total epitaxial layer thickness (Fig. 8). For a nominal Si-cap thickness of 250 nm, the thickness is uniform from the center (radius = 0 mm) to the last measurement point, which has been taken at 20 mm from the wafer edge. In the given case, both the relative standard deviation in thickness (1.25%) and the relative thickness range (3.6%), defined as 100 * (maximum–minimum)/average, are similar to the data obtained after process optimization, which is typically done by growing single $Si_{1-x}Ge_x$ layers or Si-cap/$Si_{1-x}Ge_x$ bilayers with thicknesses in the range of 50–80 nm. The different Si-cap/19 nm $Si_{0.75}Ge_{0.25}$ double layers reported in Fig. 8 have been grown using the same process setting, except for the Si deposition time. With increasing Si-thickness, the thickness uniformity slightly degrades, especially near the edge of the wafer,

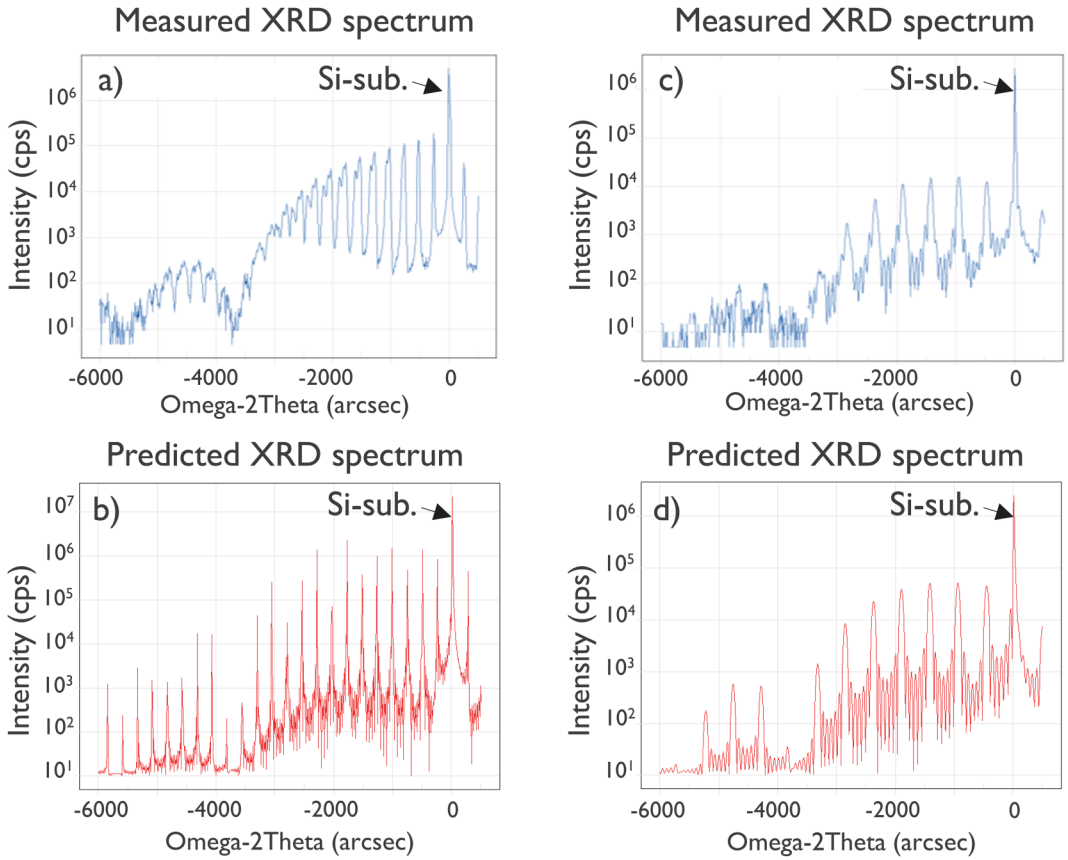

FIG. 7. (a) and (c) Measured and (b) and (d) predicted XRD (ω-2Θ) scans as obtained for epitaxial multi-stacks consisting of (a) and (b) 10 nm $Si_{0.8}Ge_{0.2}$-cap/60×(65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$)//Si substrate and (c) and (d) 10 nm $Si_{0.8}Ge_{0.2}$-cap/6×(30 nm Si/10 nm $Si_{0.8}Ge_{0.2}$)//Si substrate. The measured spectra have been taken at the center of the wafer surface.

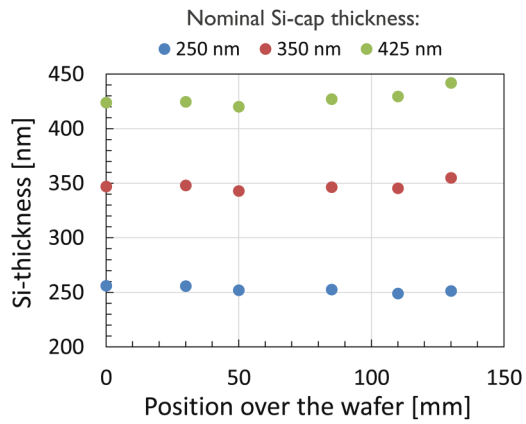

FIG. 8. Variation in within-wafer uniformity with layer thickness as extracted from XRD spectra for Si-cap/19 nm $Si_{0.75}Ge_{0.25}$//Si-substrate layers with different Si thicknesses. The position over the wafer reflects the distance from the wafer center.

resulting in a relative standard deviation in layer thickness of 1.8% and a relative thickness range of 5.1% as measured for the layer with a measured average Si thickness of 428 nm (nominal Si thickness of 425 nm).

Kong *et al.* suggested that the layer-to-layer variations are related to changes in the substrate surface temperature.[13] Alternatively, the stability of the epitaxial growth process can also be affected by a changing temperature of the reactor quartz tube. During epitaxial growth, deposition occurs on the wafer surface, the surrounding susceptor and, to a certain degree, also on the cooled reactor quartz tube. The coating on the quartz tube affects its (unwanted) light adsorption from the heating lamps. This effect increases the temperature of the reactor tube and, as a result, also the temperature distribution of the process gases inside the reactor. This, in turn, results in (small) variations in growth rate which are expected to vary over the wafer surface. The uncontrolled deposition on the quartz might, therefore, be responsible for the drift in thickness uniformity over the wafer as experimentally observed for thicker layers. The results discussed so far have been obtained in the epi-system, which does not allow to monitor and control the quartz temperature. An improved control of the reactor quartz temperature does lead to a reduced variation in growth rate as well as a reduced degradation of the within-wafer non-uniformity in layer thickness. For the newer epi-system, which enables a better control of the reactor tube temperature,[21] the variation in within-wafer uniformity and the vertical layer-to-layer uniformity are indeed less severe.

Figure 9 compares a selection of XRD spectra as obtained from epitaxial multi-stacks grown on both epi-systems. In this example, the epitaxial growth started with the deposition of a 200 or 225 nm thick Si-buffer, followed by the repeating deposition of three bilayers consisting of {15 nm $Si_{0.8}Ge_{0.2}$/60 or 65 nm Si}, and finished by a final 15 nm $Si_{0.8}Ge_{0.2}$-layer and a 20 or 25 nm thick Si-cap. During the execution of the growth studies, the individual layer thicknesses have been slightly adapted, motivated by optimizations in the device integration flow. These (small) modifications in the layer stack do not affect the conclusions of the reported experiment. At the center of the wafer, the XRD spectra are well defined, independent of the chosen epi-system. For the layers grown in the "older" epi-system, the XRD spectra taken further away from the center are less well defined. The background is higher and the individual peaks are less well resolved. The latter is most likely explained by variations in the individual thicknesses of the $Si_{0.8}Ge_{0.2}$ and/or Si layers, as confirmed by cross-sectional TEM. These layer-to-layer variations in thickness are also expected from the previous discussion as the nominal total epi thickness of 460 nm is higher than the minimal thickness above which changes in growth rate have been observed (Fig. 8). The XRD spectra as measured for

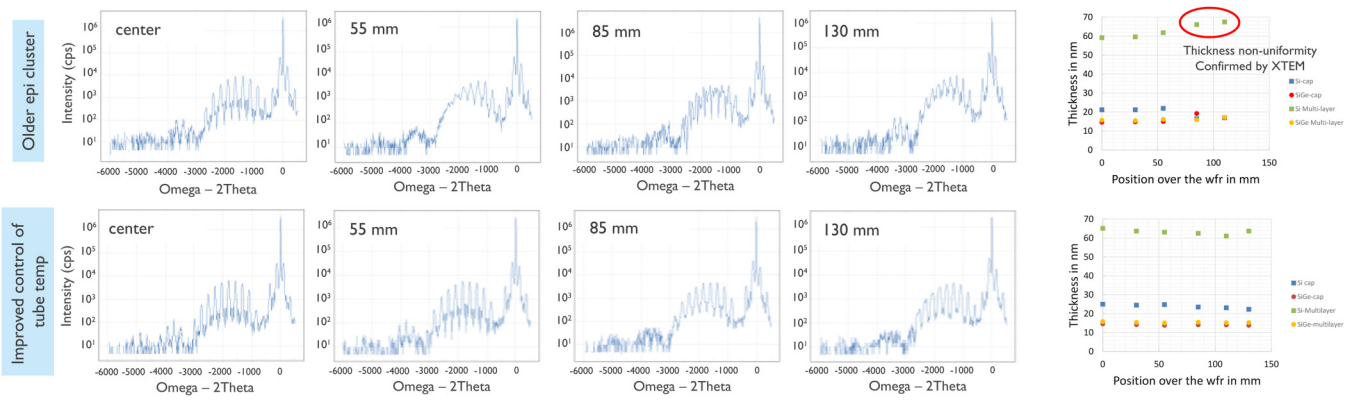

FIG. 9. XRD spectra as obtained for epitaxial multi-stacks consisting of 20 or 25 nm Si-cap/15 nm $Si_{0.8}Ge_{0.2}$-cap/3×(60 or 65 nm Si/15 nm $Si_{0.8}Ge_{0.2}$)/200 or 225 nm Si-buffer//Si substrate and for different positions over the wafer and the extracted layer thicknesses obtained from the different XRD spectra. The results on the top (bottom) line have been obtained from an epi-layer grown in the "older" ("newer") epi-system, where the "newer" systems allow a better control of the temperature of the cooled quartz reactor. For the results shown in the top line, it was not possible to get a reliable fit for the XRD data obtained at a radius of 130 mm from the wafer center. The layer reported in the bottom line has slightly higher nominal Si thicknesses.

the epi-layer grown in the "newer" epi-system, which allows a better control of the quartz temperature, show less variation as a function of the position over the wafer (Fig. 9, bottom line). The widening of the individual peaks is clearly less pronounced. This illustrates improvements in (vertical) layer-to-layer thickness uniformities for the $Si_{0.8}Ge_{0.2}$ and the Si layers, as again confirmed by TEM inspections. The individual layer thicknesses of the multi-stack have been extracted using a fitting model, which assumes that all repeating $Si_{0.8}Ge_{0.2}$ layers have the same thickness and composition. The same assumption was made for the three Si layers in the repeating part of the stack. The thicknesses, extracted from the XRD spectra reported in the top line of Fig. 9, show again a layer thickening toward the edge of the wafer. This layer thickening is larger compared to the non-uniformity achieved during process tuning, but it is in line with cross-sectional TEM results. Here, it needs to be noted that for the spectrum measured at a radius of 130 mm from the center, a reliable data fitting was not possible. A better lateral uniformity in layer thickness has been obtained for the multi-stack grown in the newer epi-system. The within-wafer uniformity in layer thickness is, for all individual layers, very close to those obtained for tuning experiments where single $Si_{0.8}Ge_{0.2}$-layers and Si-cap/$Si_{0.8}Ge_{0.2}$-bilayers were grown. Similar improvements in the vertical and lateral layer uniformities have been obtained for multi-stacks consisting of 30×{65 nm Si/15 nm $Si_{0.8}Ge_{0.2}$} bilayers.

C. 30×bilayers without misfit dislocations at the wafer edge

In Sec. IV A, we reported the ability to deposit multi-stacks containing 120×{65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} bilayers which are, at the inner part of the wafer, fully strained. However, near the edge of the wafer, misfit dislocations are formed as the wafer edge lowers the energy barrier to form misfit dislocations.[12,16,17] The density and the length of these misfit dislocations vary with the number of Si/$Si_{1-x}Ge_x$ bilayers (Fig. 10) and also as a function of the lattice mismatch between the $Si_{1-x}Ge_x$ layers and the Si substrate (Figs. 11 and 12). AFM measurements across the wafer were acquired on a wafer that contains 30 bilayers, confirming smooth surfaces without crosshatch (except for the wafer edge), and quadratic mean (Rq) values falling in the range of 96–110 pm. The presence of misfit dislocations near the wafer edge can also be visualized by x-ray topography (XRT) and room temperature photoluminescence measurements.[43,44] For the latter, no misfit dislocations are seen at the inner part of the wafers as shown in Figs. 13(a) and 13(c) for multi-stacks consisting of 30 and 60 bilayers, respectively. In the case of the stack that consists of 30 pairs of {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} layers, the areas near [110] and equivalent oriented wafer edges are also free of misfit dislocations [Fig. 13(b), 0°, 90°, and 180°]. These are the parts of the wafer edge, parallel or perpendicular to the tangent at the wafer notch. In these directions, the crystal structure, consisting of two interpenetrating face centered cubic cells, contains a row of zigzag bonds. Misfit dislocations are, however, visible in the remaining area near the wafer edge, having interrupted zigzag bonds [Fig. 13(b), 45° and 135°, and Fig. 10]. In the case of 60 bilayers, misfit dislocations are present at the rim of the wafer at every angle [Fig. 13(c)], although the density of misfits might be somewhat lower when the wafer edge is parallel to the [110] or equivalent directions [Figs. 10 and 13(d)].

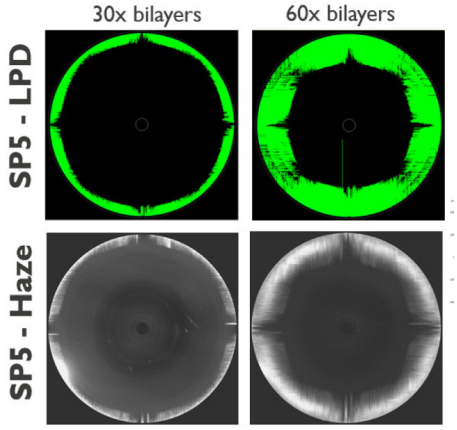

FIG. 10. Presence of misfit dislocations near the edge of the wafer as seen for multi-stacks containing 30×or 60× {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} bilayers and visualized by KLA Surfscan® SP5 LPD maps and haze maps.

The drive for layer relaxation can be reduced by reducing the lattice mismatch between the $Si_{1-x}Ge_x$ layers and the Si substrate. This can be obtained by either reducing the Ge content in the $Si_{1-x}Ge_x$ layers[10,11] or by adding C into the $Si_{1-x}Ge_x$ lattice.[45] The Ge concentration in the $Si_{1-x}Ge_x$ is typically controlled by adjusting the gas flows of the Si- and Ge-precursors. When growing the Si/$Si_{1-x}Ge_x$ multi-stacks on 300 mm wafers, the highest possible growth rates were targeted. For the $Si_{1-x}Ge_x$ growth, the highest possible DCS gas flow was used and the Ge concentration has been controlled by varying the GeH_4 gas flow. In this way, the Ge concentration can, in a controllable way, be reduced down to a certain value, which depends on the size of the mass flow controller (typically, it is advised not to use gas flows lower than 5% of the maximal flow range). The two ASM Intrepid® cluster tools used in this work have slightly different hardware configurations. As a result, the lowest controllable Ge concentration, obtained by changing the GeH_4 gas flow, slightly differs for both systems. The Ge concentration in the $Si_{1-x}Ge_x$ layers can be further reduced by adding SiH_4 to the DCS/GeH_4 gas mixture. Figure 11 shows some typical examples of LPD maps as obtained for multi-stacks containing 30×{65 nm Si/15 nm $Si_{1-x}Ge_x$} bilayers where the Ge concentration in the $Si_{1-x}Ge_x$ has been varied and different combinations of process gases have been used. A reduction of the Ge concentration in the $Si_{1-x}Ge_x$ layers reduces the driving force to form misfit dislocations, as mentioned before. In addition, adding SiH_4 to the DCS/GeH_4 gas mixture leads to a small reduction of the thermal budget during epitaxial growth, as the addition of SiH_4 to the gas mixture results in an increased $Si_{1-x}Ge_x$ growth rate and the deposition times have been reduced accordingly. Near the edge of the wafers, both the density and the length of the misfit dislocations are reduced with reducing Ge concentration in the $Si_{1-x}Ge_x$. However, the addition of SiH_4 to the DCS/GeH_4 gas mixture increases the risk to incorporate crystal imperfections during the

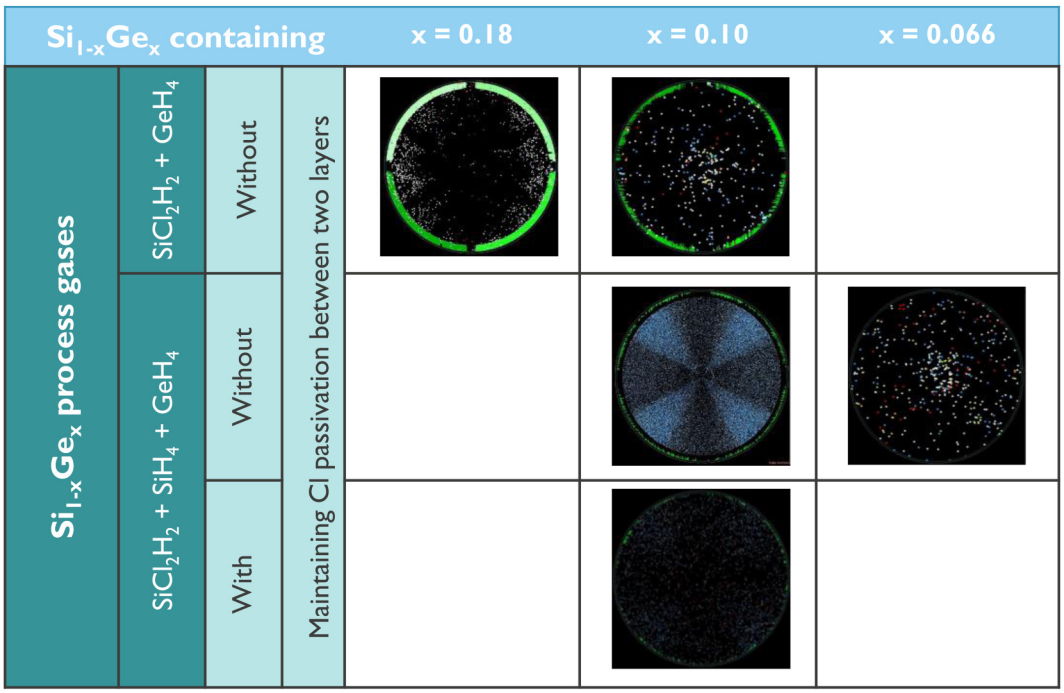

FIG. 11. KLA Surfscan® SP5 LPD maps taken with an edge exclusion of 3 mm, showing how the number of misfit dislocations near the edge of the wafer decreases with decreasing Ge content as observed for multi-stacks containing 30×{65 nm Si/15 nm $Si_{1-x}Ge_x$} bilayers. The green lines at the edge of the wafer reflect the presence of misfit dislocations. The smaller dots that are (eventually) present all over the wafer reflect the presence of particles and growth imperfections with a diameter of ≥55 nm. A part of these LPDs is being added during the deposition of the backside silicon nitride stressor layer. The "Maltese cross" that is visible in the center figure is a well-known measurement artifact and ignored in the discussion.

growth (Fig. 11, middle line, and x = 0,10).[19] This wafer shows indeed a uniform increase of small LPDs all over the wafer, which cannot be assigned to front-side damage during the deposition of the silicon nitride stressor layer on the wafer backside. These growth imperfections are expected to be polycrystalline[19] or amorphous.[46] In early work, they have been predicted to appear if the ratio of the incoming atom flux on the growing surface and the self-diffusion coefficient of silicon needed to arrange the arriving atoms on proper lattice sites are out of balance.[47] Other groups explained the amorphous defects by the formation of clusters of hydrogen and/or contaminant atoms severely poising available lattice sites on the wafer surface[48] and more recently by chemical reactions in the gas phase leading to clustering and adsorption on the growing surface.[49] Lattice defects can act as nucleation sources for misfit dislocations, also at the inner part of the wafer.[18] The formation of these growth imperfections can be largely suppressed by maintaining a Cl-passivated growth surface during the transition between two growth steps (Fig. 11, bottom line, and x = 0,10). While Si growth and etch is being kept in balance on defect free areas, the presence of Cl either enables a successful removal of previously formed amorphous growth imperfections or the Cl passivation suppresses the formation of amorphous Si on the wafer surface. The latter should occur at the initial stage of defect formation. The improvement in material quality goes together with a partial reduction of the number of misfit dislocations at the edge of the wafer. The complete avoidance of the formation of misfit dislocations has, for the given set of growth conditions, been obtained for a Ge concentration of 6.6%. The 30×{65 nm Si/15 nm $Si_{0.934}Ge_{0.066}$} bilayers were epitaxially grown on a 300 mm Si wafer and the total $Si_{0.934}Ge_{0.066}$ thickness (450 nm) exceeds the critical thickness for layer relaxation (200 nm, taking into account a doubling of the critical thickness for $Si/Si_{1-x}Ge_x$ hetero-layers). The suppression of misfit formation near the wafer edge is also reflected in the surface haze values. The presence of misfit dislocations near the edge of the wafer is reflected by a higher surface haze. For wafers without misfit dislocations, the surface haze is more uniform and also near the

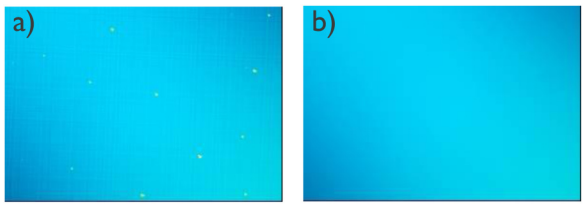

FIG. 12. Misfit dislocations as observed by Nomarski microscopy for (a) 50×{20 nm Si/10 nm $Si_{0.789}Ge_{0.211}$} and (b) 50×{20 nm Si/10 nm $Si_{0.785}Ge_{0.210}C_{0.0046}$} epitaxially grown on 200 mm Si substrates.

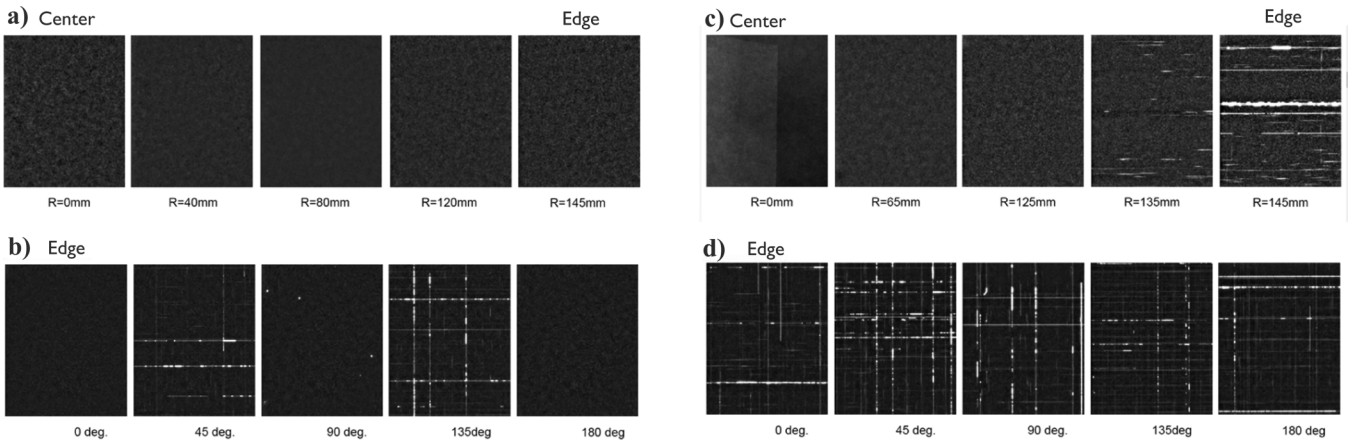

FIG. 13. 1400 nm long pass filter PL measured on epitaxial {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} bilayers. The field of view is 140×175 μm^2, and R is the radial distance from the wafer center. (a) and (b) 30× bilayers. (c) and (d) 60× bilayers. (a) and (c) From center to edge over the wafer. (b) and (d) At different positions near the edge of the wafer (R = 147 mm), where 0° is at the east side of the wafer and the rotation is done counterclockwise.

edge closer to the (lower) values obtained at the inner part of the wafer. The "Maltese cross," which is visible in the center figure, is a well-known measurement artifact and ignored in the discussion. The Maltese cross is due to the fact that the overall analysis is directional, i.e., not axis symmetric.[28]

A reduction in the Ge concentration in the $Si_{1-x}Ge_x$ layers immediately affects the $Si_{1-x}Ge_x$ etching characteristics,[50,51] which are applied at a later stage in the 3D DRAM device flow. With reducing Ge concentration, it might be more difficult to maintain a high etching selectivity between $Si_{1-x}Ge_x$ and Si. Therefore, the alternative option, to reduce the lattice mismatch by C co-alloying, is also being considered.[52] In addition, it has been reported that the presence of C at the Si-top/$Si_{1-x}Ge_x$ interface helps to maintain steep gradients in composition.[53] On the other hand, the (metastable) solubility of C in $Si_{1-x}Ge_x$ is limited. A high $Si_{1-x-y}Ge_xC_y$ material quality can only be maintained up to a critical carbon concentration, which depends on the growth conditions.[19,54] The 300 mm ASM-Intrepid® clusters used in this work are not equipped with a C-precursor gas, while methylsilane (SiH_3CH_3) is available on one of our 200 mm ASM-Epsilon®2000 epi-reactors. Some limited growth tests were done to illustrate the impact of C on layer relaxation. In this case, SiH_4 (instead of DCS) and GeH_4 were used as process gases for the deposition of the $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers, while SiH_4 was also used for Si deposition. The nominal deposition temperature was 600 °C for all layers. Figure 12 shows the surface morphology as observed at the inner part of the wafer for multi-stacks consisting of 50 pairs of {20 nm Si/10 nm $Si_{0.789}Ge_{0.211}$} and 50 pairs of {20 nm Si/10 nm $Si_{0.785}Ge_{0.210}C_{0.0046}$}, respectively. The addition of SiH_3–CH_3 to the gas mixture has a small impact on the deposition rate and the deposition times have been adjusted accordingly. The higher growth rate at relatively low growth temperatures, as obtained when using SiH_4 (instead of DCS) as Si precursor gas during $Si_{0.789}Ge_{0.211}$ and Si-growth, goes together with an enhanced risk for the incorporation of crystal imperfections during the growth.[19] In Fig. 12(a), these growth imperfections are visible as "white dots." Growth imperfections can act as nucleation sources for misfit dislocations, as mentioned earlier.[18] As a result, the multi-stack consisting of 50×{20 nm Si/10 nm $Si_{0.789}Ge_{0.211}$} bilayers is partially relaxed and misfit dislocations are seen all over the wafer [Fig. 12(a)]. The addition of a nominal C concentration of 0.46% into the $Si_{0.789}Ge_{0.211}$ reduces the lattice mismatch equivalent to an effective Ge concentration of ~15.9% as extracted from XRD measurements. This reduction in lattice mismatch is reflected in the surface morphology of the multi-stack where $Si_{0.789}Ge_{0.211}$ has been replaced by $Si_{0.785}Ge_{0.210}C_{0.0046}$. For this epi-stack, the density of misfit dislocations at the inner part of the wafer is significantly reduced [Fig. 12(b)].

V. SUMMARY

Strained layer stacks containing up to 120 pairs (241 sub-layers) of {65 nm Si/10 nm $Si_{0.8}Ge_{0.2}$} and epitaxially grown on 300 mm Si(001) wafers are reported. Such layers are of interest for 3D DRAM device concepts. While the inner part of the wafer is fully strained and free of misfit dislocations, misfit dislocations are formed near the rim of the wafer, as the wafer edge lowers the energy barrier to form misfit locations. The drive for layer relaxation is reduced by reducing the lattice mismatch between Si and $Si_{1-x}Ge_x$. This can be achieved either by adding carbon into the $Si_{1-x}Ge_x$ or by reducing the Ge concentration in the $Si_{1-x}Ge_x$ layers. Epitaxial layers containing 30×{65 nm Si/15 nm $Si_{0.934}Ge_{0.066}$} bilayers which are, over the full 300 mm wafer, free of misfit dislocations have been processed. However, this modification in composition has a direct impact on the etching characteristics during the lateral $Si_{1-x}Ge_x$ recess later in the device flow. Maintaining a high etching selectivity of $Si_{1-x}Ge_x$ with respect to the adjacent Si layers becomes significantly more challenging with decreasing Ge concentration. The effect of co-alloying $Si_{1-x}Ge_x$ with C on the etching characteristics still needs to be investigated. The variation in etching characteristics might be different for wet-chemical vs dry etching routines. First in-house

studies using a wet-chemical etching routine showed a limited impact on etching selectivity. The growth conditions have been chosen to provide 2D layer growth and keeping a balance between acceptable throughput and the sharpest possible interfaces although Si/Ge interdiffusion during the epitaxial growth of the up to 9 μm thick layers was not completely suppressed. The Si/$Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/Si interface thicknesses indeed increase from the top to the bottom of the layer stack. A variation in interface characteristics might also affect the etching characteristics during lateral $Si_{1-x}Ge_x$ recess. Its impact on the thickness and thickness uniformity of the final Si channels is not *a priori* clear as the lateral $Si_{1-x}Ge_x$ recess is followed by a vertical thinning of the Si layers. The impact of the top-to-bottom variation in interface thickness on the characteristics of the Si channels needs to be investigated. The formation of growth imperfections, acting as nucleation centers for misfit dislocations, is a severe risk when using SiH_4 as process gas. It has been largely suppressed by maintaining a Cl-passivated growth surface during the transition between two growth steps. Deposition on the reactor quartz tube might affect the temperature distribution of the process gases inside the reactor, leading to variations in both layer-to-layer and within-wafer uniformities during the epitaxial growth. Improvements in temperature control of the reactor tube allow (partial) circumvention of these issues.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

R. Loo: Investigation (lead); Methodology (lead); Writing – original draft (lead); Writing – review & editing (lead). **M. Beggiato:** Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **Y. Shimura:** Formal analysis (supporting); Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **N. Rassoul:** Conceptualization (equal); Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **W. Vanherle:** Investigation (supporting); Writing – review & editing (supporting). **F. Seidel:** Methodology (supporting); Writing – review & editing (supporting). **K. Paulussen:** Methodology (supporting); Writing – review & editing (supporting). **A. Merkulov:** Methodology (supporting); Writing – review & editing (supporting). **M. Ayyad:** Methodology (supporting); Writing – review & editing (supporting). **I. Lee:** Supervision (supporting); Writing – review & editing (supporting). **A. Belmonte:** Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Supervision (equal); Writing – review & editing (supporting). **R. Langer:** Supervision (equal); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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