The demand for processing power in HPC (High Performance Computing), AI (Artificial Intelligence) and ML (Machine Learning) is increasing at an unprecedented rate and although Moore’s law isn’t happening anymore, by its strictest definition, it is still delivering steady improvements in processor performance, albeit at a slower pace.However, the same improvements are not being seen for the chip-to-chip and chipto-memory interconnect technology, where there is an ever-widening gap between the needs and the reality, writes Dr Jess Brown, Business Development, Avicena.

The growth in Large Language Models (LLMs) has completely outpaced the increase in memory bandwidth for in-package high-bandwidth memory (HBM) stacks, as shown in Figure 1. In fact, over the last 5 years LLM parameter count has grown by several orders of magnitude, whereas HBM memory bandwidth has only grown by one order of magnitude.Electrical interconnects have fundamental limits in terms of reach, size and power efficiency, especially at higher data rates, which is causing this disparity. Therefore, there is a need for low power, compact, short-reach, fast link technologies at a reasonable price point. This article delves into the revolutionary realm of optical links based on GaN µLEDs, offering a transformative approach to chip-to-chip interconnects that promise unparalleled levels of ultralow power consumption, exceptional bandwidth density, and minimal latency, which is in stark contrast to existing SerDes-based solutions.

INTERCONNECTS: THE OPTIONS

There are two types of interconnect base technologies available: electrical and optical. The diagram below (Figure 2) shows a Figure-of-Merit (FoM)for these two types of technology indifferent configurations. The FoM plotsthe product of bandwidth density andenergy efficiency against link reach,from 0.1mm to 1,000m. For short reachcommunications (<10cm) electrical links still currently offer the best performance, whereas for long distance communications (>10m), conventional optical technologies offer the best performance, but for the middle range of 1cm to 10m neither offers optimum performance. Existing multi-mode Vertical-Cavity Surface-Emitting Laser (VCSEL) based links, although well suited for distances up to 100m, are not ideal for shorter optical interconnects, primarily because high-density processors run at elevated temperatures and VCSELs have a limited tolerance for high temperature operation. Silicon Photonics (SiPh) represent another optical link technology under development and evaluation. However, these were originally developed for medium to long-haul applications, which translates to SiPh interconnects having poor efficiency performance (>5pJ/bit) for short reach interconnects. Moreover, both VCSEL and SiPh based links typically use Serialisers/De-serialisers (SerDes), discussed in the next section, to achieve the high link bandwidth of > 100Gbps per lane, which adds a significant overhead in terms of power. Therefore, there is currently a gap between electrical and existing optical solutions, since these technologies cannot provide an optimum solution for on-board data transfer, typically in the 1cm to 10m distance, which is the range for most chip-to-chip interconnects. Avicena’s technology can fill this void and provide advantages with an optical µLED based interconnect chiplet, offering ultra-fast, low-power interconnects that bridge the gap between internal processing performance and chip-to-chip communications, for interconnects that reach up to 10m.

TO SERDES OR NOT TO SERDES

Distributed data processing needs high speed data transfer between ICs, whether that is between the processors, between the processors and memory, or both.Parallel and serial communications are the two options to transfer data between these chips. Parallel data transfer requires multiple connections between ICs, whereas serial data transfer only needs one pair of connections. On-chip communications is typically completed in a parallel format, so to enable serial interconnects a Serialiser-Deserialiser (SerDes) function block providing parallel to serial and serial-to-parallel conversion is required to enable serial communication between the two blocks. The transmitter section is a parallel to serial converter and the receiver section is a serial to parallel converter and most devices offer full-duplex operation, i.e. data in both directions at the same time. The reason for SerDes is to reduce the number of data paths needed to transmit data (and the associated number of connecting pins or wires) while achieving high link bandwidth. It additionally addresses other issues that come with transmitting parallel data electrically, such as susceptibility to electromagnetic interference and the likelihood of clock timing skew. A SerDes chip might also include an encoder, clock multiplier unit, physical coding sub-block, clock and data recovery unit, input and output staging areas, Forward Error Correction (FEC) blocks and other components. For long distance optical links there are clear advantages for using SerDes based interconnects because they minimise the number of costly, laserbased transmitters. However, when connecting ICs over distances of up to a few meters, there are clear advantages of using parallel links because ICs feature wide and relatively slow buses with clock speeds of a few Gbps internally. Avicena have developed an optical solution, using µLEDs, that overcome the disadvantages of SerDes, but still employ optical technology to gain all the associated benefits. Removing the need for SerDes, Avicena’s LightBundleTM consists of an array of GaN µLEDs and Si PDs bonded to a transceiver ASIC. The µLEDs are connected via a fibre bundle to the matching array of PDs on the corresponding receiver transceiver ASIC and vice versa. A typical LightBundle link has a few hundred channels each operating at a few Gbps, providing aggregate throughputs of > 1Tbps per link. The modest per-channel speeds are wellmatched to typical IC clock speeds and obviate the need for SerDes and enable the most efficient optical links at <1pJ/bit. GaN µLEDs are already used in free-space Visible Light Communications (VLC), but at limited data rates. Avicena have managed to develop µLEDs that can operate at data rates of over 10Gbps. With this patented technology it has been demonstrated that not only can these µLEDs be modulated at high data rates, but they can also achieve bandwidth densities of > 2Tbps/mm with a power efficiency of < 1pJ/bit. The LightBundle transceiver chiplet can be either co-packaged with the processor using a silicon interposer or an organic substrate or it can be placed on the board and connected to the processor IC package via PCB traces. The only thing that changes in the different applications is the electrical interface between the LightBundle IC and the processor IC. Fundamentally, any electrical interface can be supported by the LightBundle interconnect. The LightBundle transceiver ASIC will convert the electrical data format to match the optical µLED transmission format. Parallel electrical interfaces are best suited to work in combination with the parallel optical µLED array interface of the LightBundle chiplet since no power hungry SerDes will be needed. The IC will either match the electrical lane rate to the data rate of each individual µLED link or provide a simple muxing/demuxing function to keep latency and energy

consumption to a minimum. A prime candidate for the electrical interface is the Universal Chiplet Interface Express (UCIe) which is gaining broad industry support, but other protocols like BoW or the emerging UALink are possible as well. Table 1 compares the advantages and disadvantages of parallel versus SerDes as well as the option of Avicena's µLED optical solution and it can be seen here that Avicena's LightBundle solution offers the best solution for chip-to-chip communications and interconnects.

CONCLUSION

Due to the limitations of traditional SerDes based optical interconnects the HPC, AI and IC industry is constantly evaluating innovative solutions to enable high bandwidth density, high energy efficiency and low latency interconnects for short to intermediate reach of up to a few meters. µLED technology, renowned for its application in high-resolution displays and lighting systems, has demonstrated the potential to redefine the landscape of data communication at the chip level. By combining the intrinsic advantages of light as a medium for data transmission with the 2D layout of LED arrays, µLED based optical links present a ground-breaking avenue for achieving previously unattainable levels of performance in interconnect architectures.