Semiconductor Science and Technology

PAPER • **OPEN ACCESS**

Design and simulation of a III-Nitride light emitting transistor

To cite this article: Mohammad Awwad *et al* 2024 *Semicond. Sci. Technol.* **39** 115014

OPEN ACCESS
IOP Publishing
Semiconductor Science and Technology
Semicond. Sci. Technol. **39** (2024) 115014 (8pp)
https://doi.org/10.1088/1361-6641/ad7754

Design and simulation of a III-Nitride light emitting transistor

Mohammad Awwad[1,*], Sheikh Ifatur Rahman[1], Chandan Joishi[1], Joe McGlone[1], Betty Lise Anderson[1] and Siddharth Rajan[1,2]

[1] Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210, United States of America
[2] Department of Materials Science and Engineering, The Ohio State University, Columbus, OH 43210, United States of America

E-mail: awwad.9@osu.edu

Received 26 April 2024, revised 26 June 2024
Accepted for publication 4 September 2024
Published 1 October 2024

Abstract

This paper describes the design and characteristics of monolithically integrated three-terminal gated III-Nitride light emitting diodes (LEDs) devices. The impact of channel doping and thickness on the voltage penalty of the transistor-LED hybrid device is analyzed, and it is shown that with appropriate design, low voltage drop can be realized across integrated gated LED structures. The impact of device design on the switching charge is investigated, and it is shown that the adoption of an integrated LED/transistor structure can reduce the switching charge necessary for operation of a switched LED display device by an order of magnitude when compared with stand-alone light-emitting diodes.

Keywords: monolithic integration, microLED, MESFET, GaN.

1. Introduction

The III-nitride material system has been the key technology enabling solid-state lighting technologies, with widespread applications ranging from the field of general illumination to micro- light-emitting diode (LED) display systems and communications [1–5]. Emissive display technologies based on GaN/(In,Ga),N heterostructure light-emitting diodes with high pixel density, luminance, efficiency and large color gamut are of great interest for applications such as wearable technologies, mobile devices and virtual displays [6–8]. While high pixel density requirements for these display applications are fulfilled using scaled ($<15\mu$m) light-emitting diodes, scaling of the mesa dimensions lead to additional challenges for integration of LEDs and electronic drivers. Besides, it is desirable to have color and luminance variation created using a combination of three colors- red, green, and blue in micro-LED display technologies.

Given the performance variation in GaN/(In,Ga)N heterostructure-based LEDs at different emission wavelengths, it is necessary to use them at their optimum conditions to achieve maximum power savings. Extensive research on the integration of micro-LEDs for display applications in mobile devices, wearables and AR-VR technologies have shown great possibilities using both heterogeneous and monolithic integration [9–11]. The most widely used method to fabricate an active-matrix micro-LED display is to transfer the micro-LED chips onto a circuit board with a backplane [12, 13]. This method involves epitaxial growth of the LED wafer, patterning, etching, lift-off, and physical bonding of the micro-LED chips formed on different wafers that act as the sources of the red, green, and blue colors [14, 15]. This method performs well with large area displays with lower resolution but has performance and yield limitations when utilized in

* Author to whom any correspondence should be addressed.

the fabrication of micro-LED displays for high-resolution and high-speed operation. Such challenges include difficulties in the alignment and bonding of the electrical interconnects of the micro-LED chips with the backplane circuitry, and a low production yield due to separate implementation of the three-color chips [16]. To solve these issues and introduce the next generation of display technology, power electronics combined with LEDs based on GaN are being pursued. Monolithic integration of GaN switching devices with the micro-LEDs sharing the same material platform offers certain advantages over heterogeneous integration. GaN transistors monolithically integrated on the LED for voltage driving would benefit from growth performed in a single epitaxial step and fewer fabrication processes, and the excellent performance offered by GaN transistors. The key advantage of a three-terminal gated LED is that it can greatly reduce the requirements on the switching devices driving LEDs since such a device enables *capacitive* rather than *current* control of the LED optical output. In case of the conventional two-terminal PN junction LEDs, the charge accumulated on the diode capacitance is relatively large since it is associated with charging and discharging the depletion region across the entire emitting active region. The circuits designed for switching these must supply this charge and the LED current. However, in the gated LED case, the device is switched by only modulating the gate charge (Q_G). Therefore, if the modulated gate charge is designed to be lower than the depletion region capacitance charge of the LED, the charge needed for switching the gated LED device is lower than an LED. Thus, the adoption of integrated 3-terminal gated LEDs can make control circuits simpler and more efficient.

Integration of GaN-based transistors and LEDs on the same epi-wafer can enable high power and high efficiency voltage-controlled modulated visible light emission while eliminating interconnects and reducing the spacing between each pixel. GaN based LEDs offer higher efficiencies of up to 80%, improved long-term reliability, and the ability to be manufactured at the microscale (less than 5 μm). Previous demonstrations of monolithic integration of GaN LEDs with GaN transistor technologies used regrown transistor structures on the side and interconnects between the LED and the transistors. Such integration methods possess challenges to device performance from the regrowth impurities and device spacing alongside a complicated process flow. Recently Hartensveld *et al* demonstrated a voltage-controlled LED using a nanowire structure and a GaN FET for monolithic integration [17]. Memon *et al* reported a three-terminal LED via monolithical integration of metal/Al_2O_3 dielectric layer directly on the p-layer [18, 19]. Bhardwaj *et al* also showed light-emitting field-effect transistor (LEFET) using the benefits of bottom tunnel junction (TJ)-based LEDs [20]. In the report, they vertically integrated nanowires/Fin n-FETs with planar LEDs to control the LED emission profile. In this work, we discuss the design and characteristics of *monolithic planar* gated LED structures that are well-suited for existing LED process flows. The proposed design has a much lower switching charge compared to the stand-alone LED and removes the requirement for the driver circuit to provide LED drive current and stored charge. Therefore, using this design, we aim to reduce the current requirements and complexity of the controlling circuits, and to enable future intelligent multifunctional displays.

2. Theory and design

The schematics of the device designs investigated here is shown in figure 1. The total device length is 8 μm. All the device parameters (current/capacitance) are normalized to a default width of 1 μm in the simulation. The device structure consists of a metal-semiconductor field-effect transistor (MESFET) with GaN/(In, Ga)N based heterostructure LEDs. For the p-down structure, the light emitting transistor (LET) is designed using a bottom tunnel junction-based structure as shown in figure 1(a), which enables a conductive n-type region on the top surface, which can then be used to create a conductive channel for an n-channel transistor. P-down LEDs (using bottom tunnel junctions) have been reported with low voltage operation [21] and low injection barrier for carriers into the active region [22]. We note that the analysis here is also relevant for both p-up devices with a top tunnel junction as shown in figure 1(b), with some differences that will be discussed in this manuscript. Recently, experimental demonstration of such an LET was achieved, and is reported separately [23].

The simulated device consists of a p-down $In_{0.25}Ga_{0.75}N$ QW LED on the top of a GaN homojunction TJ and a lateral depletion-mode MESFET transistor integrated at the top. The fully transparent homojunction TJ design has already been demonstrated to show low voltage drop for LED operation [24, 25] with a reduced voltage penalty. A green emitting (520 nm) LED above the homojunction TJ was implemented through a 3 nm $In_{0.25}Ga_{0.75}N$ single quantum well (SQW) sandwiched between two undoped GaN barrier layers. No additional AlGaN blocking layer was required in this design for the LED due to a built-in barrier in the InGaN QW that arises from the polarization charges [25].

A GaN MESFET was added above the LED on an n-doped channel layer, formed at the top of the heavily doped n-type current spreading layer. Vertical electron blocking from the source of the transistor was realized in the design with a semi-insulating (SI) blocking layer. Such a blocking layer profile below the source and gate could be achieved by introducing acceptor-like traps via ion implantation, typically done using nitrogen or helium ions [26], with a density larger than the background donor concentration. This would create a vertical electron-blocking path from the source to the drain but permit electron flow through a narrow lateral channel. The thickness and trap density were chosen to ensure that no vertical current flows between source and drain. The values chosen here are based on experimentally achievable values from implantation, are similar to those used in an experimentally demonstrated version of this device [23]. It is very important for the implanted insulating region to have overlap with source and gate to ensure that all current can only flow laterally through the channel, and then vertically into the aperture un-implanted LED regions. Optimal values of doping density and thickness

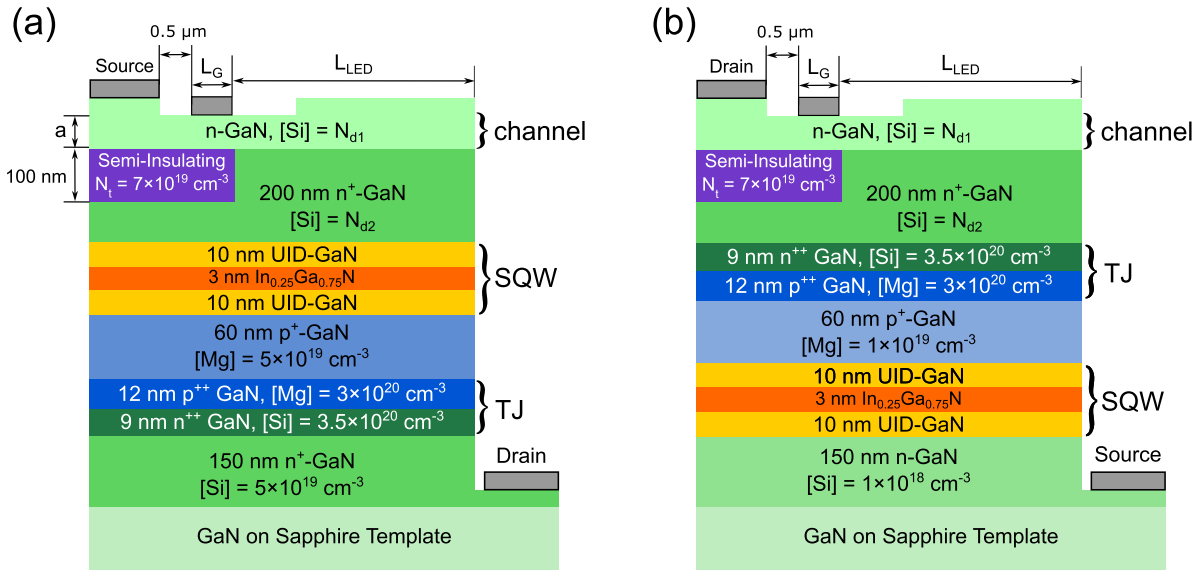

Figure 1. Two-dimensional schematics of the light emitting transistors (LETs): (a) P-down configuration. (b) P-up configuration.

of n^+−GaN layer below the channel were considered during the simulation to ensure efficient current spreading in the device. Source and drain contacts were assumed to be perfectly ohmic in this simulation, while the gate Schottky contact with a metal work function of 5.15 eV was considered [27], which results in a barrier height ~1 eV. A recessed gate design enabled high channel-length-to-thickness (L_G/a) aspect ratio without compromising the source resistance. The design parameters for the simulation including gate length (L_G), channel thickness (a), channel doping level (N_{d1}), and LED length (L_{LED}) were optimized for high on-off LED current ratio, strong gate control, and reduced gate charge (Q_G) to promote fast switching.

Our target is to achieve a high on-off current ratio while still maintaining low channel resistance. We consider device designs that enable LED current ratings of up to 1 kA cm^{-2} in the on-state, while simultaneously having strong gate control to suppress current <0.01 A cm^{-2} in the off-state. To determine the channel parameters for the LED current requirements, we used the gradual channel approximation (GCA) mathematical model for a MESFET [28, 29]:

$$I_D = I_{max}\left[\frac{V_{ch}-V_{GS}}{\phi_{00}} - \frac{2}{3}\left(\frac{\phi_{bi}-V_{GS}+V_{ch}}{\phi_{00}}\right)^{\frac{3}{2}} + \frac{2}{3}\left(\frac{\phi_{bi}-V_{GS}}{\phi_{00}}\right)^{\frac{3}{2}}\right] \quad (1)$$

such that:

$$I_{max} = \frac{qaWN_{d1}\mu_n\phi_{00}}{L_G}, \quad W = \frac{I_D}{J_{LED}L_{LED}} \quad (2)$$

where q is the elementary charge, μ_n is the doping dependent electron mobility in the channel estimated by the Albrecht model [30], ϕ_{00} is the full depletion potential, V_{ch} is the voltage across the channel (V_{ds} in a conventional transistor), W is the device width, and J_{LED} is the current density passing through the LED in A cm^{-2} whose length is L_{LED}. A 3-dimensional schematic of the MESFET part with labelled parameters is shown in figure 2(a). From (1) and (2), we can get an estimate of the voltage penalty V_{ch} added by the transistor at a normally-on condition ($V_{GS} = 0$) gate bias as shown in figure 2(b). The maximum channel thickness a_{max} is limited by the breakdown field F_{BR} of GaN at full depletion such that: $a_{max} = F_{BR}\epsilon/qN_{d1}$. The practical channel thicknesses considered here are still below a_{max} for a wide range of doping levels owing to the relatively high breakdown field of GaN (3.3 MV cm^{-1}) [31]. From the plot, we observe that decreasing the channel doping below 10^{18} cm^{-3} will significantly increase the voltage penalty at high injection regime for channel thickness, $a = 50$ nm. However, increasing the channel doping beyond 3×10^{18} cm^{-3} would increase the electric field near the metal-semiconductor Schottky junction at pinch-off as shown by the marked breakdown points in figure 2(b). Therefore, a channel doping concentration of 10^{18} cm^{-3} and thickness of 50 nm was adopted to achieve low channel resistance and strong gate control for small area micro-LEDs ($L_{LED} < 5$ μm).

Micro-LEDs with larger area (5 μm $< L_{LED} <$ 20 μm) require higher transistor current ratings (I_D) to maintain J_{LED}. Increasing I_D with the same channel resistance results in increasing the channel voltage (V_{ch}). Figures 2(c) and (d) show a plot of the calculated V_{ch} versus L_{LED} for various gate lengths (L_G) and channel thicknesses (a), respectively. From the two plots, we observe an increase in the device voltage penalty as the micro-LED area increases. Therefore, reducing the channel resistance via shorter L_G and/or higher channel thickness is necessary for larger area micro-LEDs.

For linear current spreading/distribution along the LED length, the voltage drop associated to inject the current in the x-direction should not exceed the thermal voltage kT. This can

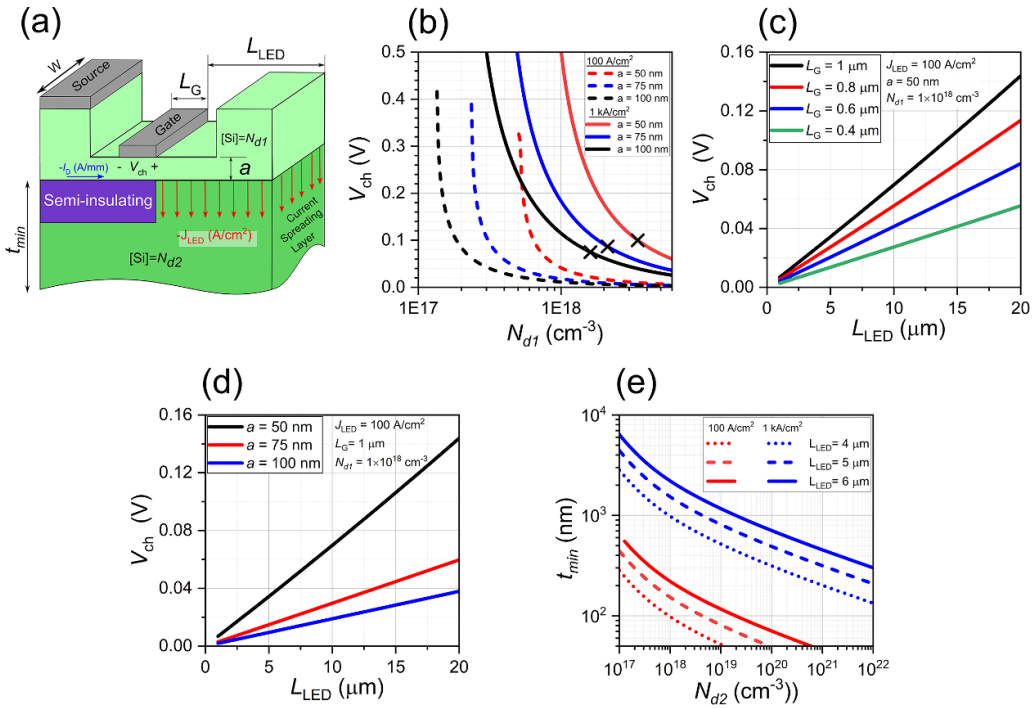

Figure 2. (a) 3-dimensional schematic of the MESFET with labelled parameters. (b) Channel voltage versus doping concentration at various channel thicknesses and currents, × markers indicate doping levels above which channel breaks down at full depletion. (c) Channel voltage versus L_{LED} at various gate lengths. (d) Channel voltage versus L_{LED} at various channel thicknesses. (e) Estimated minimum thickness of the current spreading layer versus its doping concentration.

be expressed by the following inequality:

$$\int_0^{L_{LED}} \frac{J_{LED}L_{LED}}{qn_{sheet}\mu_n}\left(1-\frac{x}{L_{LED}}\right)dx < kT \tag{3}$$

Solving the integral, we get:

$$n_{sheet} = t_{min}N_{d2}^{+} = \frac{J_{LED}L_{LED}^2}{2q\mu_n kT} \tag{4}$$

where t_{min} is the minimum layer thickness required to linearly spread a current of density J_{LED} along an L_{LED} length with a voltage drop less than kT, N_{d2}^{+} is the ionized doping concentration assuming incomplete ionization.

A plot of the calculated t_{min} versus doping concentration at 100 A cm^{-2} and 1 kA cm^{-2} is shown in figure 2(e). It is observed that it gets harder to spread the current over larger distances and/or for higher current density. Therefore, we chose $L_{LED} = 4\,\mu$m, $t = 200$ nm and $N_{d2}^{+} = 5\times10^{19}$ cm^{-3} as design parameters for this layer. This will allow a good current spreading for 100 A cm^{-2} current range. However, for 1 kA cm^{-2} current, we expect some voltage penalty that exceeds kT.

3. Simulation and results

To validate the feasibility of the proposed design, the DC characteristics, optical power spectrum, transient, and AC characteristics were simulated using the Silvaco simulation tool. Physics models (listed in table 1) were selected to match the processes taking place in each region. We used a SQW instead of a MQW region in the design and simulation to reduce the complexity and reach convergence faster, since the design is considered as an integrated multi-device design. Spontaneous and piezoelectric polarization interface charge were calculated using previous models [32–34] and included in the simulation.

Figure 3(a) shows the I_D–V_{DS} characteristics of p-down LET for $V_{GS} = 0$ to –5 V for a device with $L_G = 1\,\mu$m, and $L_{LED} = 4\,\mu$m. Other I–V simulation results for $L_{LED} = 10\,\mu$m and $L_{LED} = 20\,\mu$m (not shown here) coincides with that shown in figure 3(a). As shown in the plot, the device turns on at ~2.5 V, which is similar to the turn-on voltage of the TJ LED device without the transistor. High on-off current ratios of $\sim8\times10^5$ at $V_{DS} = 2.9$ V ($J_{LED} = 100$ A cm^{-2}) and $\sim7\times10^6$ at $V_{DS} = 3.95$ V ($J_{LED} = 1$ kA cm^{-2}) are observed. The equivalent I_D–V_{DS} characteristics of p-up LET are shown in 3(b). A turn-on voltage of ~2.7 V can be observed which is higher than that of p-down LET due to the higher injection barrier as mentioned earlier. The simulated I_D–V_{DS} characteristics of the p-up LET agree with the measured preliminary I_D–V_{DS} characteristics shown in figure 3(c) of our recently implemented p-up LET. The turn-on voltage of the practically implemented device is observed to be higher than that in simulation since a MQW was grown in the practical device while a SQW was used in the simulation. To study the voltage penalty introduced by the controlling MESFET, a reference TJ LED is simulated with exactly the same design parameters as the proposed device except that both the implant-insulated region and

Table 1. Physics models used in the simulation.

Model	Description	Parameters
Fermi–Dirac	Statistics of carrier concentration in doped regions	
Incomplete ionization	A model that accounts for dopant freeze-out. Typically, it is used at low temperatures.	$E_A = 140$ meV [35], $E_D = 28$ meV [36]
Albrecht	Low field mobility model.	$a = 2.61 \times 10^{-4}$ V s cm^{-2}, $b = 2.9 \times 10^{-4}$ V s cm^{-2} [30]
k.p	Kronnig–Penney model effective masses and band edge energies for drift-diffusion simulation.	
Thermionic emission	A model for the transport of energetic carriers across a semiconductor-semiconductor interface	$\phi_m = 5.1$ eV [37]
Non-local band-to-band tunneling	Allows modeling of tunneling current between heavily doped pn regions	$m_e = 0.2m_0$, $m_h = 0.8m_0$ [38]
Concentration-dependent lifetime	Shockley-Read-Hall recombination using concentration dependent lifetimes	$\tau_{no} = \tau_{p0} = 5 \times 10^{-7}$ s [39]
Spontaneous recombination	computes total radiative recombination rate and include it into drift-diffusion equations	
Optical generation/Radiative recombination	Quantitative model for electron–hole pair optical generation/radiative recombination process.	$C^{opt} = 4.3 \times 10^{-11}$ cm^{3}s^{-1}

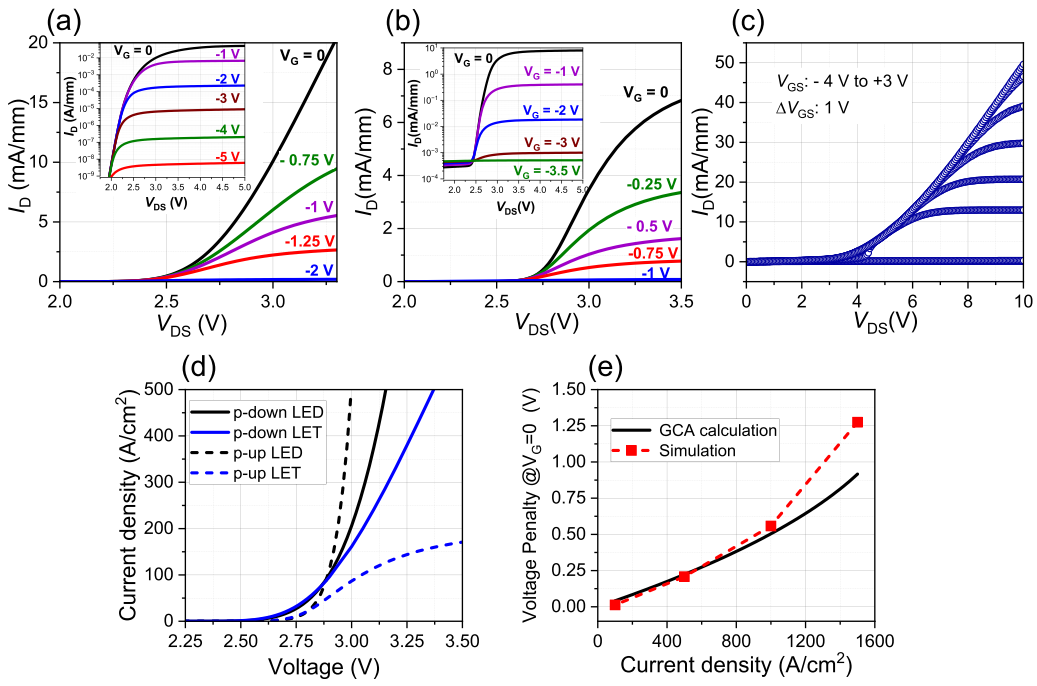

Figure 3. (a), (b) Simulated linear I_D–V_{DS} characteristics from $V_{GS} = 0$ to -5 V, inset: logscale I_D-V_{DS} from $V_{GS} = 0$ to $V_{GS} = -5$ *V* for (p-down, p-up) LET. (c) Preliminary measurements of $I_D$versus V_{DS} of the experimental device. (d) Overlayed *I–V* characteristics of both proposed LET devices and the reference TJ LEDs. (e) Simulation versus analytical model comparison of voltage penalty (excess voltage) due to the addition of a controlling transistor.

the gate contact were removed. Figure 3(d) shows the *I–V* characteristics of the proposed LETs and the reference stand-alone TJ LED previously mentioned. For the p-down LET, the integration of the gated structure to the standard p-down LED does not impact the diode performance up to the current density of 100 A cm^{-2}. At higher current densities, the device shows increased voltage drop due to the channel resistance. However, for the p-up LET, the excess voltage introduced by the transistor dramatically increases at current densities above 30 A cm^{-2}. This can be attributed to the proximity of the gate to the drain contact in p-up structure which resulted in channel pinch-off affected by the drain bias at low gate voltage. The excess voltage values at various current densities were extracted and are plotted versus current density for p-down LET in figure 3(e). For better understanding and validation, analytical calculations using the gradual channel approximation

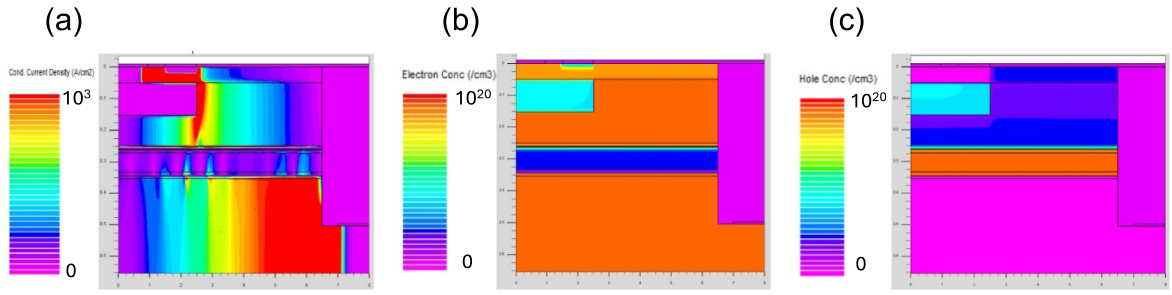

Figure 4. Contour plot of physical parameters in p-down LET at $V_{DS} = 2.9$ V (corresponding to 100 A cm^{-2} at $V_{GS} = 0$): (a) conduction current density (linear scale), (b) electron concentration (log scale), and (c) hole concentration (log scale).

were also done. As shown in figure 3(e), a good agreement was found between GCA-calculated excess voltage and simulated excess voltage at low (near zero at J_{LED} <100 A cm^{-2}) and moderate injection (0.2 V at 500 A cm^{-2}) regime. At high injection (>1 kA cm^{-2}), however, 2D device simulations predict a voltage penalty that is higher than that calculated from GCA.

The extra voltage penalty at high injection is due to current crowding near the drain side of the channel which can be solved by increasing the doping level and/or the thickness of the current spreading layer above the active emission area of the LED.

Figure 4 shows contour plots of conduction current density, electron, and hole concentrations at $J_{LED} = 100$ A cm^{-2}. It is clear that the current is spread over the active region as shown in figure 4(a) thanks to the design parameters of the current spreading layer. High carrier concentrations are depicted on both adjacent sides of the SQW in figures 4(b) and (c) enabling high carrier injection. Since the layers are relatively thin, the free carrier absorption is expected to be quite low. However, the impact of the gate and MESFET regions on the light extraction efficiency is an interesting topic for future investigation.

Figures 5(a) and (b) show the generated optical power spectral density as a function of the wavelength at $V_{DS} = 2.9$ V and $V_{DS} = 4$ V which drives a current density of 100 A cm^{-2} and 1 kA cm^{-2} in the on state ($V_{GS} = 0$), respectively. A blue shift is observed in high injection due to quantum-confined Stark effect (QCSE) which is common in InGaN QWs due to the applied electric field [40]. Total optical output power versus gate voltage shown in figure 5(c) is extracted by integrating the power spectrum in figures 5(a) and (b). When switching off the device, the emitted optical power is suppressed by a factor of ($\sim 1 \times 10^6$), which reflects the possibility of a true dimmed device in the off state and high dynamic range.

Estimated rise/fall time delays were obtained by performing transient simulations in Silvaco. The source and drain voltages were biased at 0 and 3 V, while a square signal (0, –5) V of 2 pulses with ramp time of 5 ns was applied at the gate terminal as shown in figure 6(a). The rise time of both the radiative recombination rate and the magnitude of drain current ($|I_d|$) were relatively fast (~2 ns), as expected, compared to the fall time where ~2 μs were needed to suppress the drain current by 5 orders of magnitude. On a closer look, however, when the device is switched off, the drain current drops abruptly (5 ns) by 4 orders of magnitude (to subzero values). Then, a relatively long (μs scale) recovery time is needed for the negative drain current to vanish as in regular pn junction diodes [41]. Given the estimated rise/fall time delays mentioned above, the transient characteristics of the proposed LET are suitable for micro-LED display applications.

An AC simulation was done in Silvaco to estimate the gate charge from the gate capacitance. Figure 6(b) shows the small-signal gate capacitance as a function of gate bias from $V_{gs} = 0$ V to $V_{gs} = -5$ V (giving $\sim 10^5$ on/off ratio). To calculate the gate charge, we integrated the gate capacitance over the switching range of V_{gs} at various gate lengths. Figure 6(c) shows Q_G as a function of L_G, with the gate voltage varied such that the current decreases from 10 A cm^{-2} to ~0. The simulated gate charge was estimated to be 7.2 pC/mm for $L_G = 1\,\mu$m and 3.2 pC/mm for $L_G = 0.4\,\mu$m. In comparison, the gate charge of the reference LED was estimated to be 27.97 pC/mm. This shows that the charge necessary to switch the gated LED is significantly lower than that needed for a standalone LED.

The results agree with the derived analytical formula:

$$Q_G = \frac{\pi a^2}{2}(qN_d) + qN_d a L_G \,, \tag{5}$$

where the first term represents the cylindrical charge at both edges of the gate contact, and the second term represents the charge under the gate. However, the model over-estimates the charge since, in reality, the depletion in the lateral direction is not as wide as in the normal direction which results in a non-perfect cylindrical depletion profile.

Reducing the gate length can enhance the switching characteristics of the device, however, the gate control over the channel might be affected by that reduction in the channel aspect ratio. Therefore, I_D–V_{DS} simulations were repeated for the device at various gate lengths from 0.4 μm up to 1 μm as shown in figure 6(d). The on current (at $V_{GS} = 0$ V) increases with decreasing L_G due to the reduction in channel resistance. In other words, at 100 A cm^{-2} the device voltage is decreased from 2.9 V to 2.78 V by reducing the gate length from 1 μm to

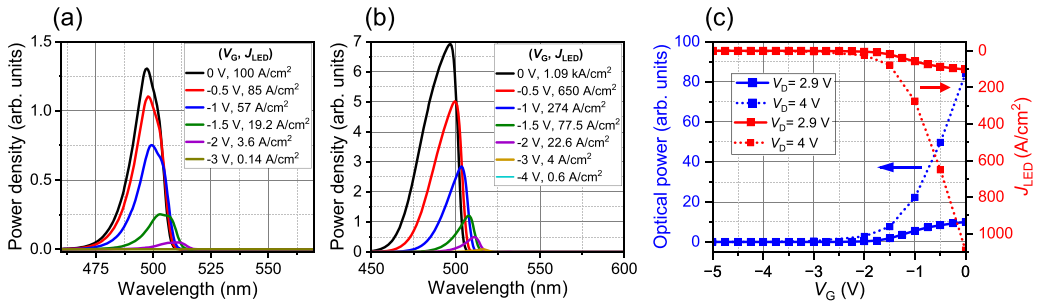

Figure 5. Simulated emission spectra at: (a) $V_{DS} = 2.9$ V (corresponding to 100 A cm^{-2} at $V_{GS} = 0$). (b) $V_{DS} = 4$ V (corresponding to 1 kA cm^{-2} at $V_{GS} = 0$). (c) Optical output power and gate current versus gate voltage at $V_{DS} = 2.9$ V and 4 V.

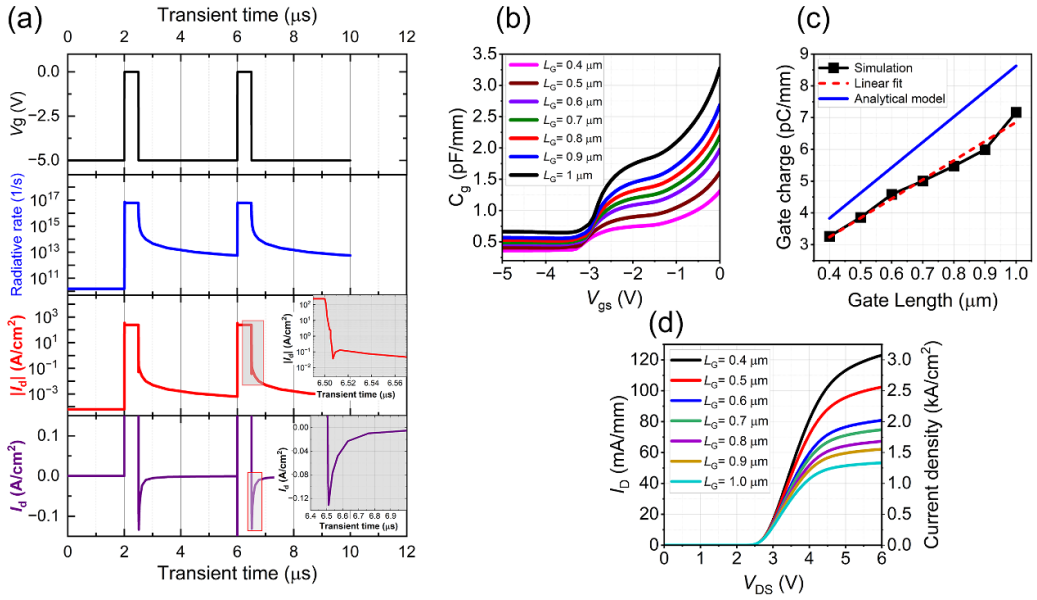

Figure 6. (a) Simulated transient response of the p-down LET at $V_S = 0$ V and $V_D = 3$ V.(b) Small-signal gate capacitance as a function of gate bias. (c) Extracted gate charge (Q_G) versus gate length (L_G) at 10 A cm^{-2}. (d) Simulated I_D–V_{DS} curves at $V_{GS} = 0$ V for various gate lengths (L_G).

0.4 μm, while the on-off current ratio is slightly reduced from $\sim 8 \times 10^5$ to $\sim 4 \times 10^5$. This shows that shorter gate lengths can provide sufficient on/off ratio while providing almost $\sim 9\times$ reduction in the gate switching charge.

4. Summary

To conclude, we designed a monolithically integrated MESFET controlled tunnel-injected 520 nm LED for micro-LED display systems. The gate of the MESFET designed here controls the electron flow in the LED active region which in turn controls the emission profile of the LED. The design enables high power and efficient voltage modulation of LED with a single epitaxial step. Simulation results show a high on-off current ratio ($>10^5$) at 100 A cm^{-2} and ($>10^6$) at 1 kA cm^{-2} for high-dynamic-range displays. We also showed that the transistor introduces near zero voltage penalty at 100 A cm^{-2} indicating a highly efficient operation. The low off current (<1 mA cm^{-2}) allows pixels to feature a true black state. Transient simulations estimated rise/fall time delays in the nanosecond scale enabling large micro-LED array multiplexing and high refresh rates. The switching charge for an integrated transistor LED proposed here is shown to be significantly lower than a stand-alone LED. We note here that while the 3-terminal device does introduce excess voltage over a stand-alone LED, it can greatly reduce the complexity of control circuits needed in micro-LED display applications.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

ORCID iD

Mohammad Awwad https://orcid.org/0000-0001-8756-9475

References

[1] Dupré L, Marra M, Verney V, Aventurier B, Henry F, Olivier F, Tirano S, Daami A and Templier F 2017 Processing and characterization of high resolution GaN/InGaN LED arrays at 10 micron pitch for micro display applications *Gallium Nitride Materials and Devices XII* (International Society for Optics and Photonics) vol 10104 (SPIE) p 1010422

[2] Anandan M 2008 *J. Soc. Inf. Disp.* **16** 287–310

[3] Li H, Chen X, Guo J and Chen H 2014 *Opt. Express* **22** 27203–13

[4] Nakamura S, Mukai T and Senoh M 1994 *Appl. Phys. Lett.* **64** 1687–9

[5] Nakamura S 2015 *Rev. Mod. Phys.* **87** 1139–51

[6] DenBaars S P *et al* 2013 *Acta Mater.* **61** 945–51

[7] Gong Z *et al* 2008 *J. Phys. D: Appl. Phys.* **41** 094002

[8] Jiang H X, Jin S X, Li J, Shakya J and Lin J Y 2001 *Appl. Phys. Lett.* **78** 1303–5

[9] Anwar A R, Sajjad M T, Johar M A, Hernández-Gutiérrez C A, Usman M and Łepkowski S P 2022 *Laser Photon. Rev.* **16** 2100427

[10] Lin J Y and Jiang H X 2020 *Appl. Phys. Lett.* **116** 100502

[11] Wong M S, Nakamura S and DenBaars S P 2019 *ECS J. Solid State Sci. Technol.* **9** 015012

[12] Tull B R, Basaran Z, Gidony D, Limanov A B, Im J S, Kymissis I and Lee V W 2015 *SID Symp. Dig. Tech. Pap.* **46** 375–7

[13] Zhang L, Ou F, Chong W C, Chen Y and Li Q 2018 *J. Soc. Inf. Disp.* **26** 137–45

[14] Peng D, Zhang K and Liu Z 2017 *IEEE J. Electron Devices Soc.* **5** 90–94

[15] Li Y, Tao J, Zhao Y, Wang J, Lv J, Qin Y, Liang J and Wang W 2019 *Appl. Opt.* **58** 8383–9

[16] Bower C A *et al* 2017 *Photon. Res.* **5** A23–A29

[17] Hartensveld M and Zhang J 2019 *IEEE Electron Device Lett.* **40** 427–30

[18] Memon M H *et al* 2024 *Nat. Electron.* **7** 279–87

[19] Yu H, Xiao S, Memon M H, Luo Y, Wang R, Li D, Shen C and Sun H 2014 *Laser Photon. Rev.* **18** 2300789

[20] Bharadwaj S, Lee K, Nomoto K, Hickman A, van Deurzen L, Protasenko V, Xing H G and Jena D 2020 *Appl. Phys. Lett.* **117** 031107

[21] Rahman S I, Jamal-Eddine Z, Dominic Merwin Xavier A M, Armitage R and Rajan S 2022 *Appl. Phys. Lett.* **121** 021102

[22] Akyol F, Nath D N, Gür E, Park P S and Rajan S 2011 *Jpn. J. Appl. Phys.* **50** 052101

[23] Rahman S I, Awwad M, Joishi C, Jamal-Eddine Z, Gunning B, Armstrong A and Rajan S 2024 *Appl. Phys. Lett.* **124** 221106

[24] Jamal-Eddine Z, Hasan S M N, Gunning B, Chandrasekar H, Crawford M, Armstrong A, Arafin S and Rajan S 2020 *Appl. Phys. Lett.* **117** 051103

[25] Akyol F, Krishnamoorthy S, Zhang Y, Johnson J, Hwang J and Rajan S 2016 *Appl. Phys. Lett.* **108** 131103

[26] Slawinska J, Muziol G, Siekacz M, Turski H, Hajdel M, Zak M, Feduniewicz-Zmuda A, Staszczak G and Skierbiszewski C 2022 *Opt. Express* **30** 27004–14

[27] Yıldırım N, Ejderha K and Turut A 2010 *J. Appl. Phys.* **108** 114506

[28] Yang E S 1972 Current saturation mechanisms in junction field-effect transistors (*Advances in Electronics and Electron Physics*) ed Marton L and Marton C 31 247–65

[29] Liu W 1999 *Fundamentals of III-V Devices: Hbts, Mesfets and Hfets/Hemts* (Wiley)

[30] Albrecht J D, Wang R P, Ruden P P, Farahmand M and Brennan K F 1998 *J. Appl. Phys.* **83** 4777–81

[31] Kaminski N and Hilt O 2014 *IET Circuits, Devices Syst.* **8** 227–36

[32] Bernardini F, Fiorentini V and Vanderbilt D 1997 *Phys. Rev.* B **56** R10024–7

[33] Neumann H 1995 *Cryst. Res. Technol.* **30** 910

[34] Wright A F 1997 *J. Appl. Phys.* **82** 2833–9

[35] Nam K B, Nakarmi M L, Li J, Lin J Y and Jiang H X 2003 *Appl. Phys. Lett.* **83** 878–80

[36] Götz W, Johnson N M, Chen C, Liu H, Kuo C and Imler W 1996 *Appl. Phys. Lett.* **68** 3144–6

[37] Miura N, Nanjo T, Suita M, Oishi T, Abe Y, Ozeki T, Ishikawa H, Egawa T and Jimbo T 2004 *Solid-State Electron.* **48** 689–95

[38] Levinshtein M, Rumyantsev S and Shur M 2001 *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, Sige* (A Wiley-Interscience Publication, Wiley)

[39] Zhou R, Ikeda M, Zhang F, Liu J, Zhang S, Tian A, Wen P, Li D, Zhang L and Yang H 2020 *J. Appl. Phys.* **127** 013103

[40] Turski H, Bharadwaj S, Xing H G and Jena D 2019 *J. Appl. Phys.* **125** 203104

[41] Tyagi M 2008 *Introduction to Semiconductor Materials and Devices* (Wiley India Pvt. Limited)