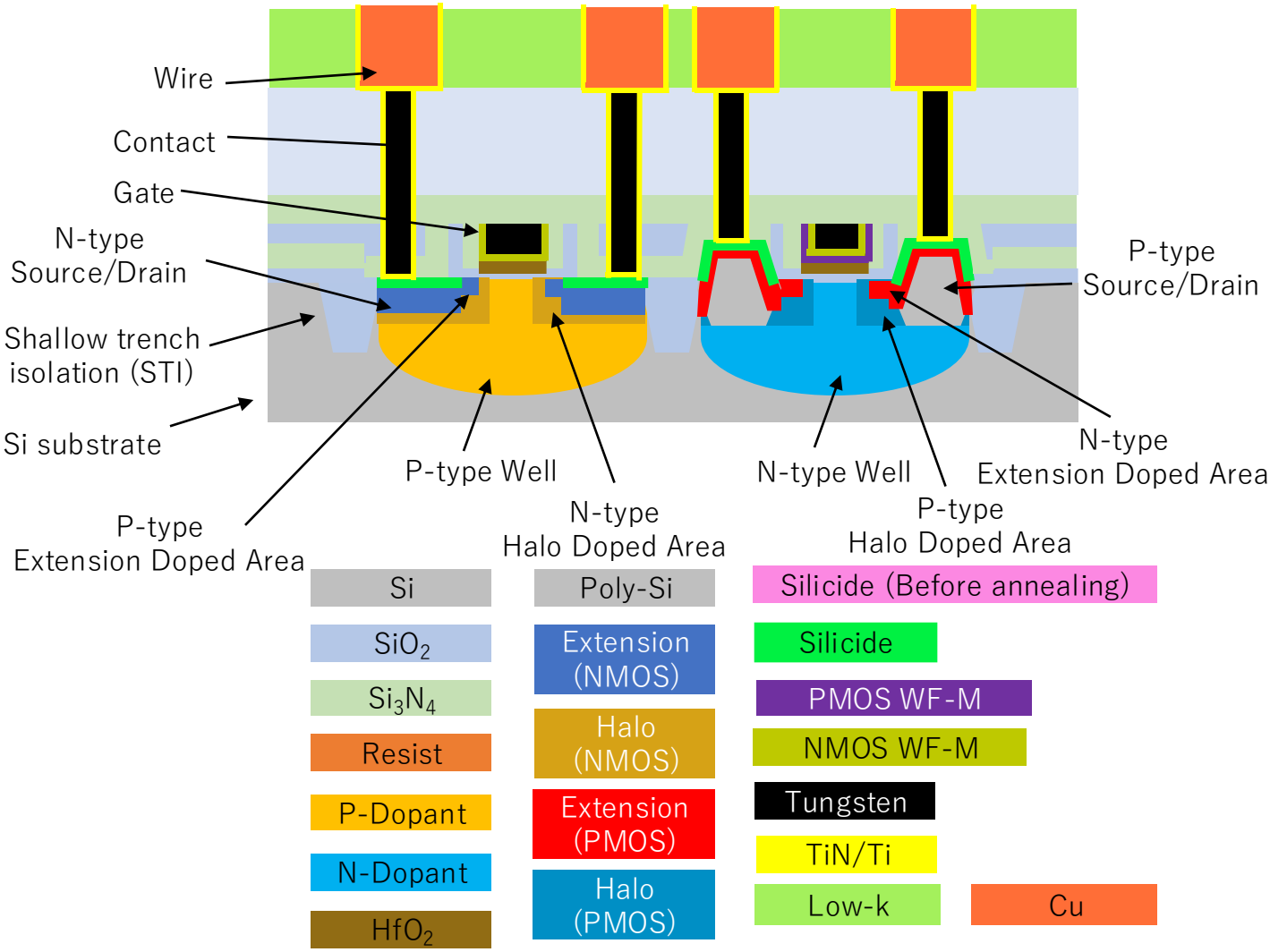
45 nm CMOS Fabrication Process Flow

Big picture of fabrication process flow

1. Si substrate preparation
2. Shallow Trench Isolation (STI) Formation
3. Well・Channel Formation
4. Dummy Gate Formation
5. Halo・Extension Formation
6. SiGe S/D Formation
7. Formation of a high-concentration diffusion layer
8. Silicide Formation
9. ILD Deposition
10. Dummy Gate Replacement
11. Gate Stack Formation
12. Contact Plug Formation
13. Wire・Via Formation



Si Substrate Preparation – Quality Check

Explanation

Check the quality of the substrates received from the supplier.

Why important ?

If the substrate preparation is flawed, the entire downstream process may be wasted. Therefore, it is essential to carefully verify

What, Why, How do we do in this process?

What	Why	How
Dopant concentration check	Affect built-in potential of PN junction, leading to fluctuate V_{th}	・Sheet Resistance ・SIMS
Crystallographic Orientation defect check	Affect carrier mobility	・XRD ・Photoluminescence
Bow and Wrap	Focus misalignment during exposure, leading CD variation	・Stylus profiler

Si Substrate Preparation - Cleaning

Explanation

Native, oxide, organic contaminants, and metal impurities are removed prior to starting the fabrication process

Why important ?

If there is contamination on the silicon substrate, it may become trapped beneath the gate, leading to defects. It can also alter etching and deposition characteristics, ultimately affecting yield.

Shallow Trench Isolation – Thermal Oxidation

Purpose : Sacrificial layer for ion implantation protecting product area against CMP

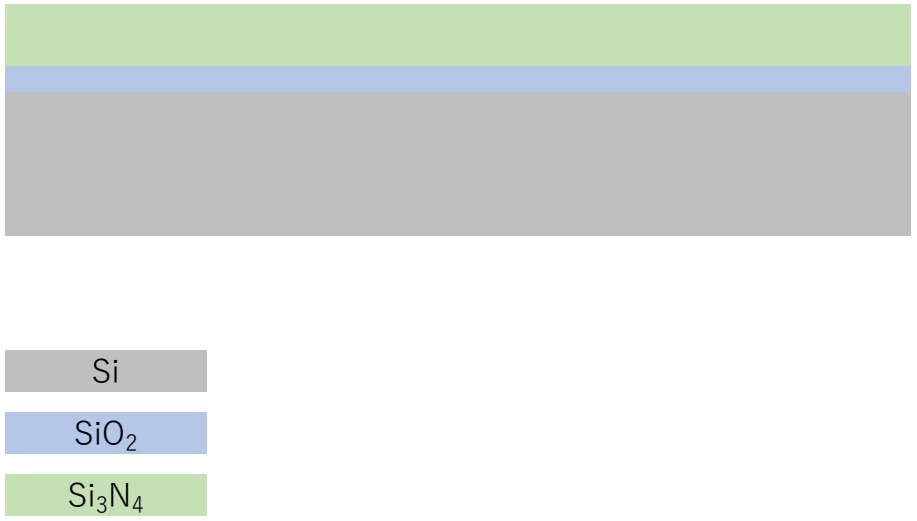
Method : Thermal Oxidation

Deposited material : Silicon Dioxide

Thickness : 10 nm

Metrology : Spectroscopy Ellipsometry

Shallow Trench Isolation – Stopping layer deposition



Purpose : Stopping layer against CMP

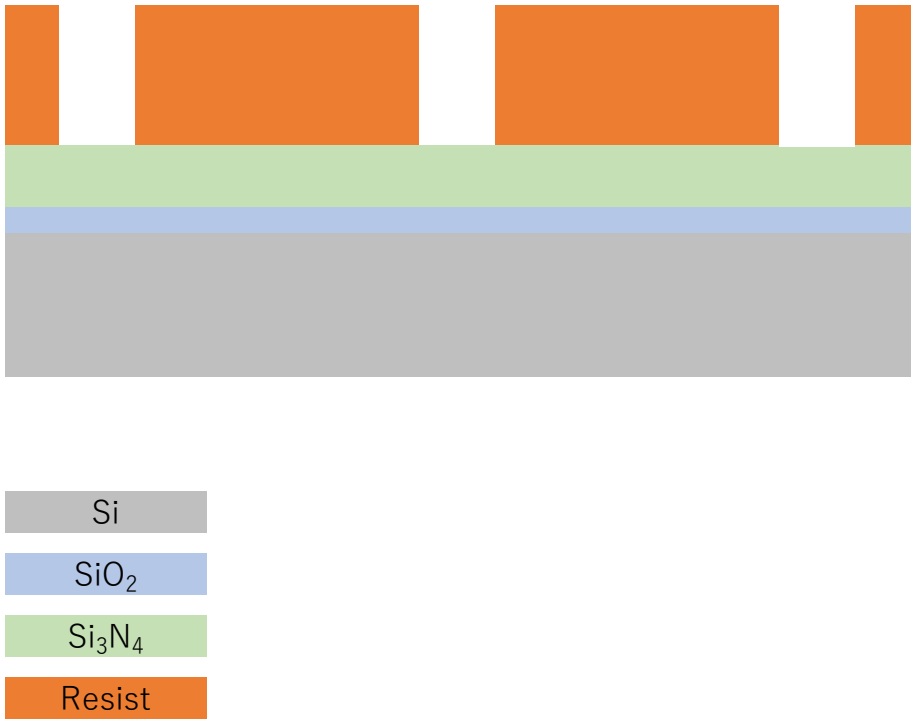
Method : Low Pressure CVD

Deposited material : Silicon Nitride

Thickness : 20~50 nm?

Metrology : Spectroscopy Ellipsometry

Shallow Trench Isolation – STI Patterning



Purpose : Form pattern on wafer

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300~800 nm

Metrology : Spectroscopy Interferometry

Shallow Trench Isolation – RIE Etching

Si

SiO_2

Si_3N_4

Resist

Purpose : Form Shallow Trench

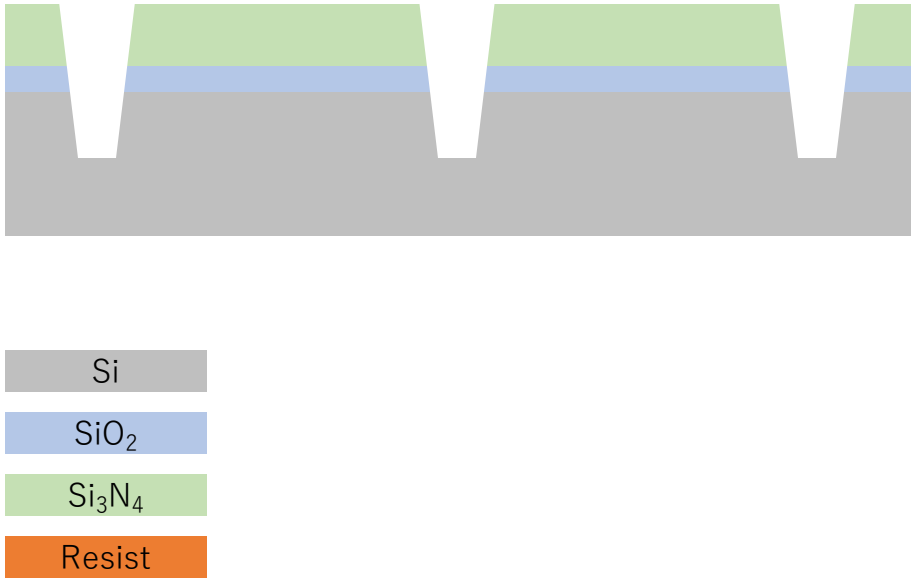
Method : RIE

Etched material : SiN/SiO2/Si

Thickness : 700 nm~2 μm

Metrology : Stylus Profiler

Shallow Trench Isolation – Resist Stripping



Purpose : Strip resist

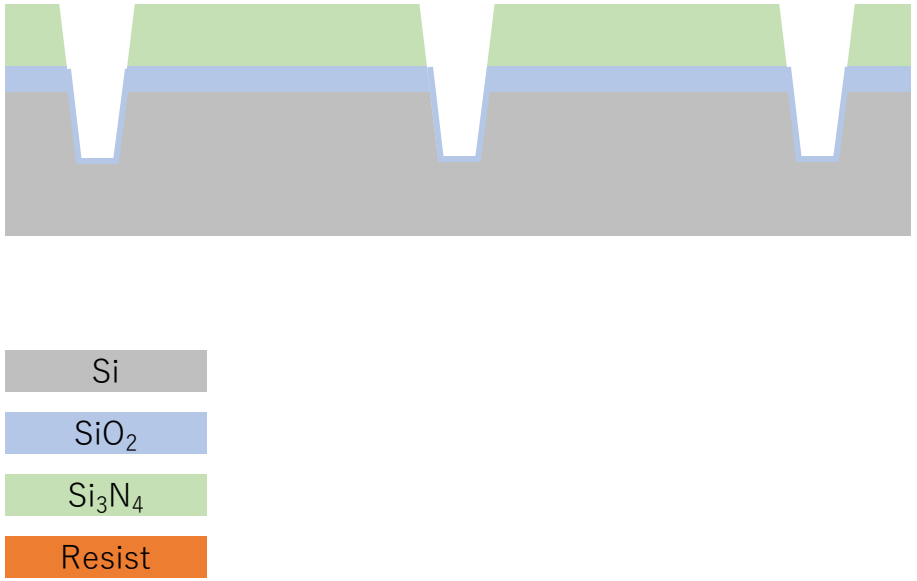
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

Shallow Trench Isolation – Shallow Trench Oxidation



Purpose :

・Eliminate any etch damage to a trench sidewall
・Rounds the upper corners of the trench.
→Minimizing the fringing field
・Form a high-quality interface between the Si trench sidewall

Method : Thermal Oxidation

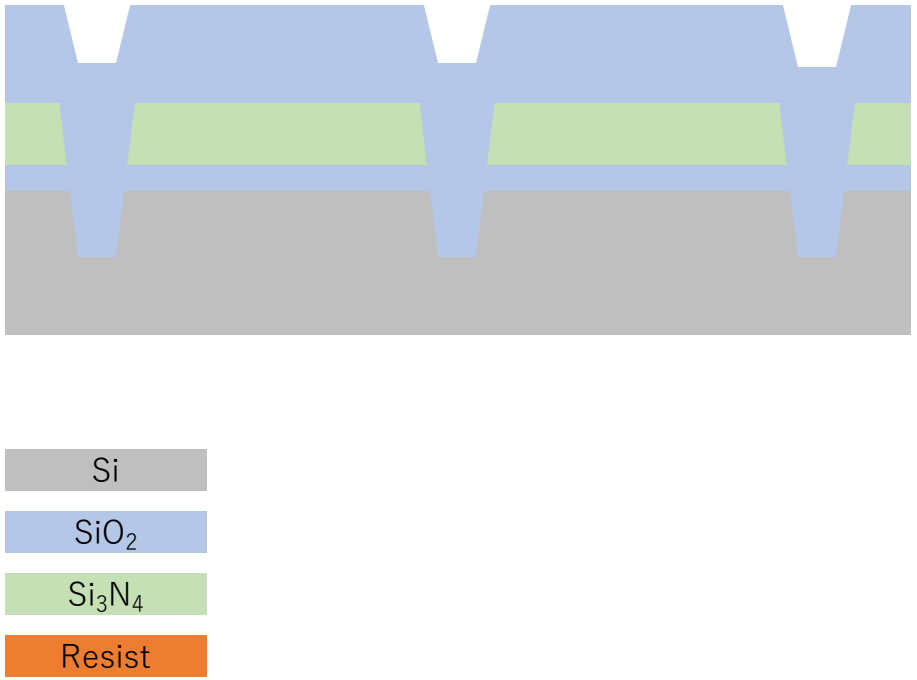
Etched material : SiO2

Thickness : 5 ~ 10 nm

Metrology : Surface Particle Inspection System

Ref: US Patent 20050205859 A1 “Shallow Trench Isolation Process”

Shallow Trench Isolation – SiO2 Deposition



Purpose : Overfill Trench

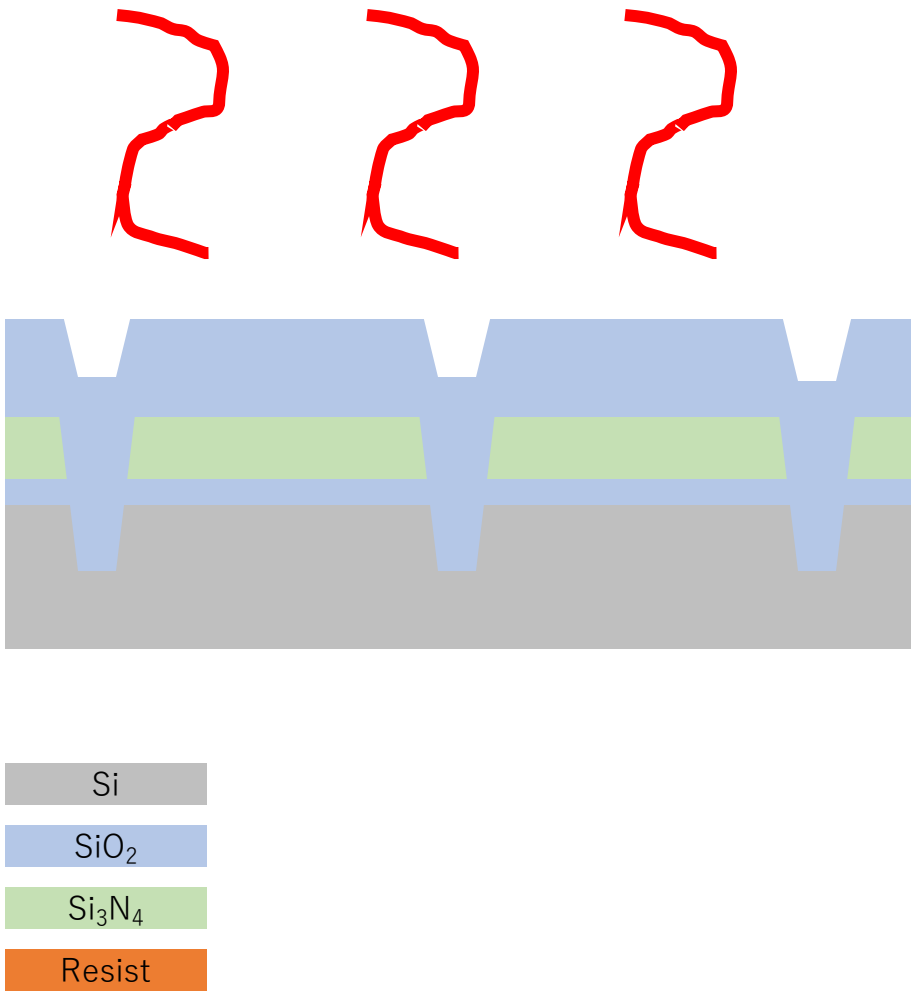
Method : TEOS CVD (TEOS is good coverage)

Deposited material : Silicon Dioxide

Thickness : 1.5 ~ 2.5 μm

Metrology : Spectroscopic Interferometry

Shallow Trench Isolation – Annealing

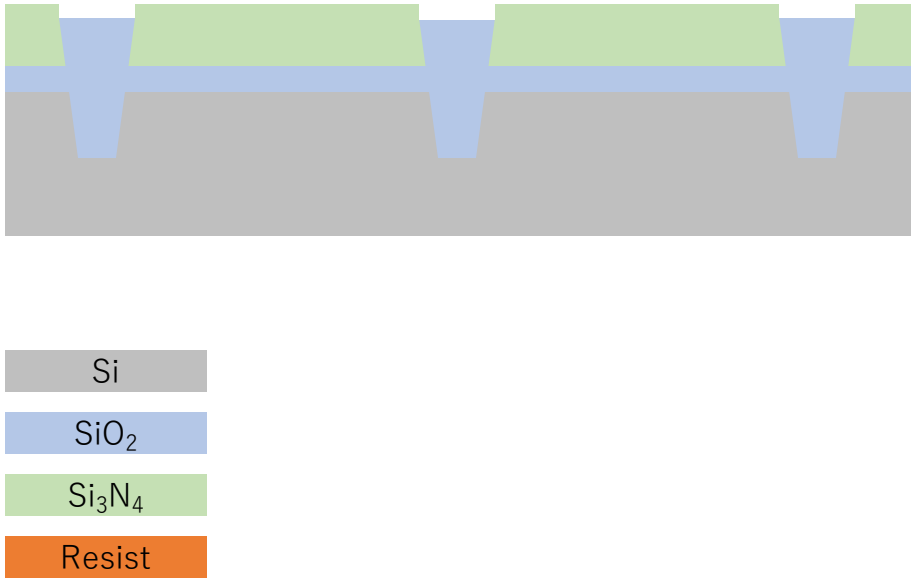


Purpose : To make it more resistant to be etched, since it will be exposed to HF-based etchants in later steps such as sacrificial layer removal

Method : Furnace annealing
(Vertical furnace annealing)

Temperature : Over 1000°C

Shallow Trench Isolation – Planarization



Purpose : Planarize surface for embedding Silicon dioxide into STI

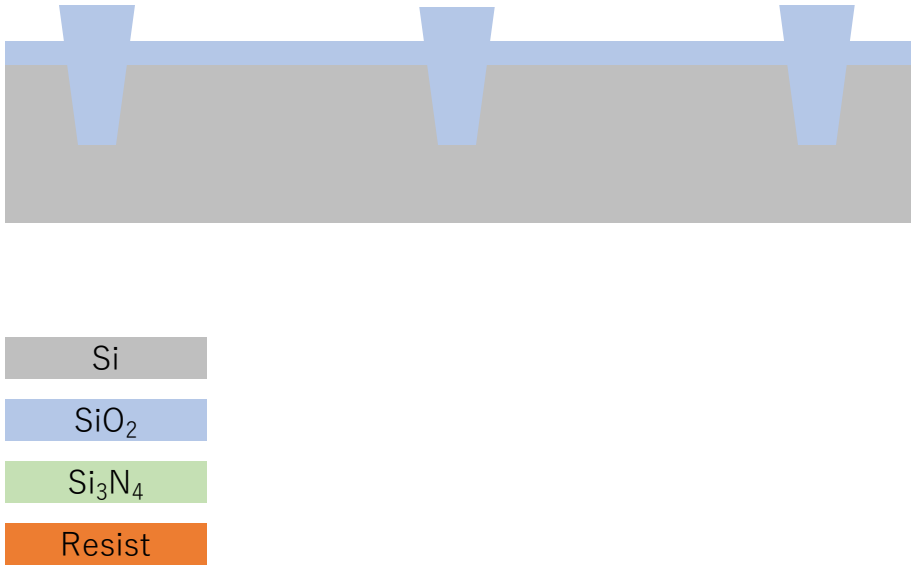
Method : Chemical Mechanical Polishing(CMP) (Colloidal silica, Alumina slurry)

Polished material : Silicon Dioxide

Thickness : 500 ~ 700 nm

Metrology : In-situ end point detection (Reflectivity, Torque)

Shallow Trench Isolation – Remove Stopping layer



Purpose : To remove Stopping layer

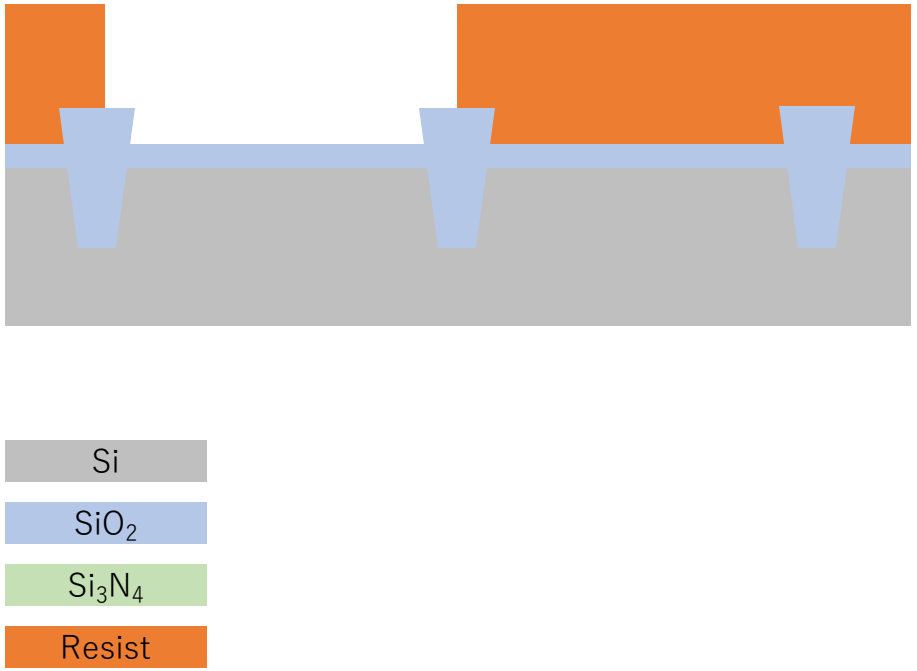
Method : Wet Etching (Hot Phosphorous acid)

Etched material : Silicon Nitride

Thickness : 20 ~ 50 nm

Metrology : Surface analysis (FT-IR, XPS)

Well Channel Formation – N-MOS Well Patterning



Purpose : Being able to protect from Ion implantation

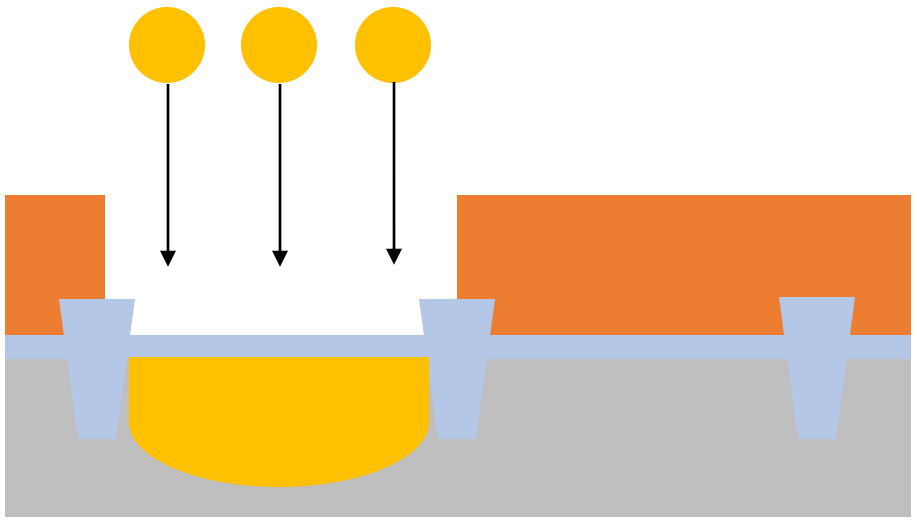
Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry

Well Channel Formation – N-MOS Well Ion Implantation



Si

SiO_2

Si_3N_4

Resist

P-Dopant

Purpose : Implant Dopant for forming N-MOS Well

Method : Ion Implantation

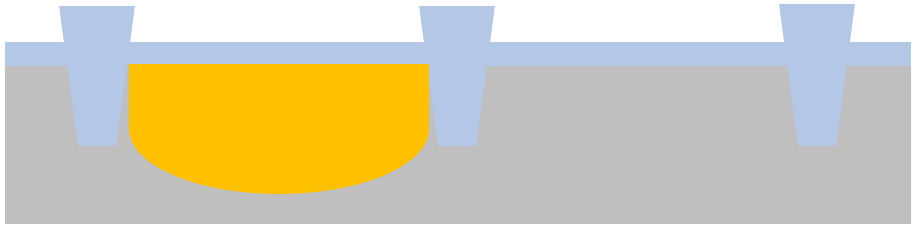
Implanted material : Boron

Concentration : $10^{16} \sim 10^{17}\ cm^{-3}$

Thickness : Few hundred nm ~ μm

Metrology : Secondary Ion Mass Spectroscopy (SIMS)

Well Channel Formation – N-MOS Well Pattern Stripping



Si

SiO_2

Si_3N_4

Resist

P-Dopant

Purpose : Strip resist

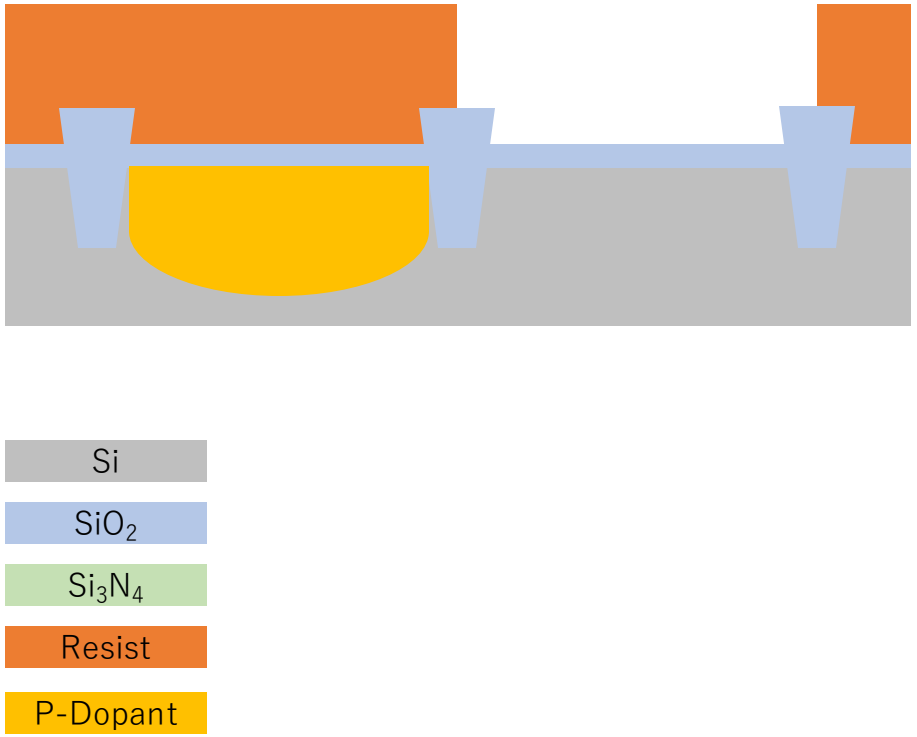
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

Well Channel Formation – P-MOS Well Patterning



Purpose : Being able to protect from Ion implantation

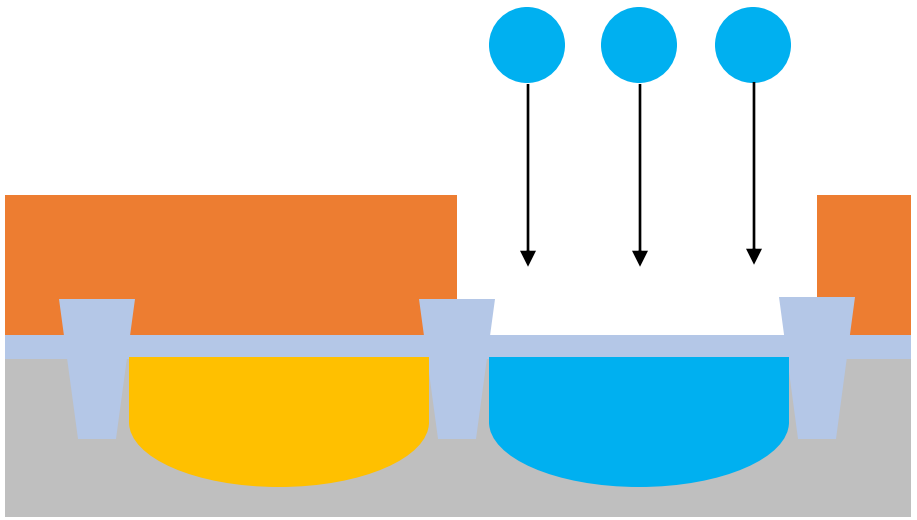
Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry

Well Channel Formation – P-MOS Well Ion Implantation



Si

SiO_2

Si_3N_4

Resist

P-Dopant

N-Dopant

Purpose : Implant Dopant for forming P-MOS Well

Method : Ion Implantation

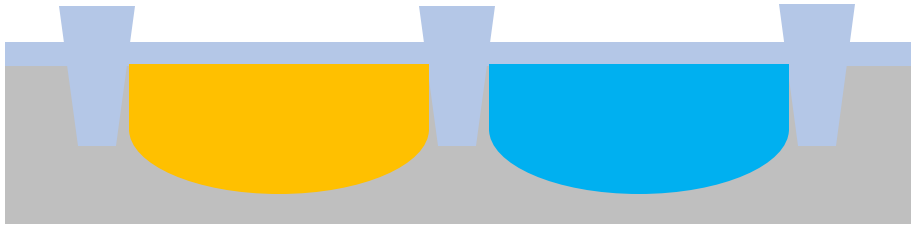
Implanted material : Phosphorous

Concentration : $10^{16} \sim 10^{17}\ cm^{-3}$

Thickness : Few hundred nm ~ μm

Metrology : Secondary Ion Mass Spectroscopy (SIMS)

Well Channel Formation – P-MOS Well Resist Stripping



Si

SiO_2

Si_3N_4

Resist

P-Dopant

N-Dopant

Purpose : Strip resist

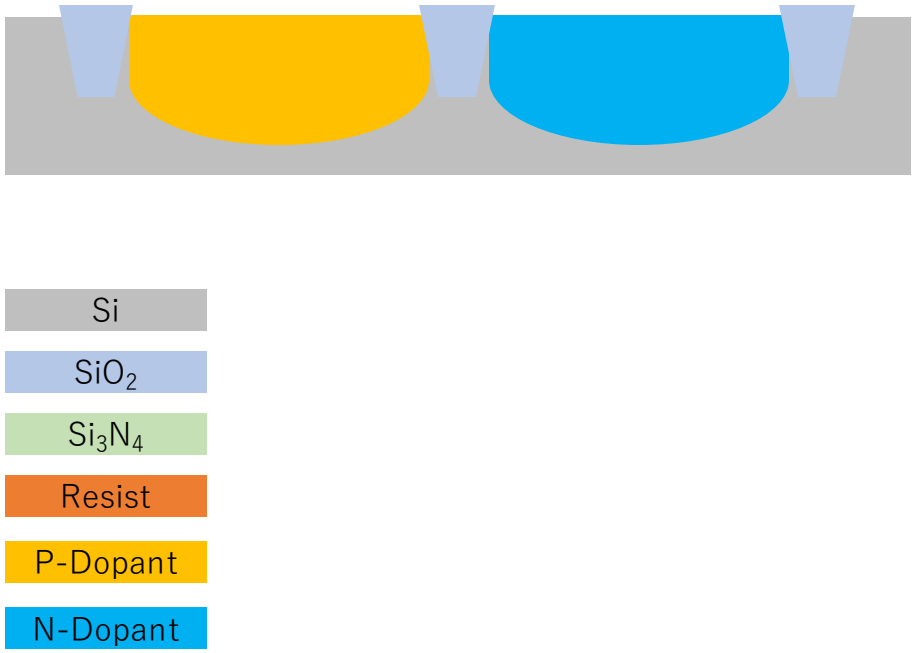
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

Well Channel Formation – Remove Sacrificial layer



Purpose : To Remove the sacrificial layer
(Because damaged by ion implantation)

Method : Wet Etching (BHF)

Etched material : Silicon dioxide

Thickness : 10 nm

Metrology : Surface analysis (FT-IR, XPS)

Dummy Gate Formation – Deposition of SiO2

Si

SiO_2

Si_3N_4

Resist

P-Dopant

N-Dopant

HfO_2

Purpose :
To suppress interface trap density at the Si/HfO_2 boundary and to preserve high carrier mobility for strong drive current and low ON-resistance.

Method : Thermal Oxidation

Deposited material : Silicon Dioxide (SiO_2)

Thickness : 0.5 nm

Metrology : Spectroscopic Ellipsometry(On line)
X-ray Refractometry (Off line)

Dummy Gate Formation – Deposition of a high-k dielectric layer

Si

SiO_2

Si_3N_4

Resist

P-Dopant

N-Dopant

HfO_2

Purpose :
High-k dielectrics improve C_{OX}, which leads to
・Lower ON-resistance, reduced power consumption
・Higher drive current.
etc.

Method : Atomic Layer Deposition (ALD)

Deposited material : Hafnium Oxide (HfO_2)

Thickness : few nm

Metrology : Spectroscopic Ellipsometry(On line)
X-ray Refractometry (Off line)

Dummy Gate Formation – Deposit Dummy Gate

Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Purpose : To form Dummy Gate
(Dummy Gate is removed and replaced with a metal gate.)

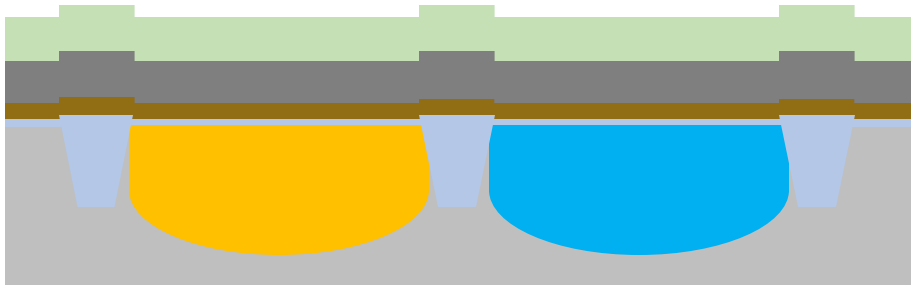
Method : LP-CVD

Deposited material : Poly-Si, a-Si

Thickness : 5 ~ 30 nm

Metrology : Spectroscopic Ellipsometry

Dummy Gate Formation – Deposit Cap Layer



Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Purpose :
Since it is a dummy silicon gate and will be removed later, a protective layer is deposited to prevent silicidation.

Method : LP-CVD

Deposited material : Silicon Nitride

Thickness : Few ten nm

Metrology : Spectroscopic Ellipsometry

Dummy Gate Formation – Gate patterning

Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Purpose : Gate patterning

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : Few hundred nm

Metrology : Spectroscopy Interferometry (Thickness)
CD-SEM (Dimension)

Dummy Gate Formation – Gate Etching

Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Purpose : Gate Etching (Isotropic etching)

Method : RIE

Etched material : Poly-Si, a-Si

Thickness : Few hundred nm

Metrology : Spectroscopy Interferometry (Thickness)
CD-SEM (Dimension)

Dummy Gate Formation – Stripping resist

Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Purpose : Strip resist

Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

Halo・Extension Formation – NMOS Patterning

Si
Poly-Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

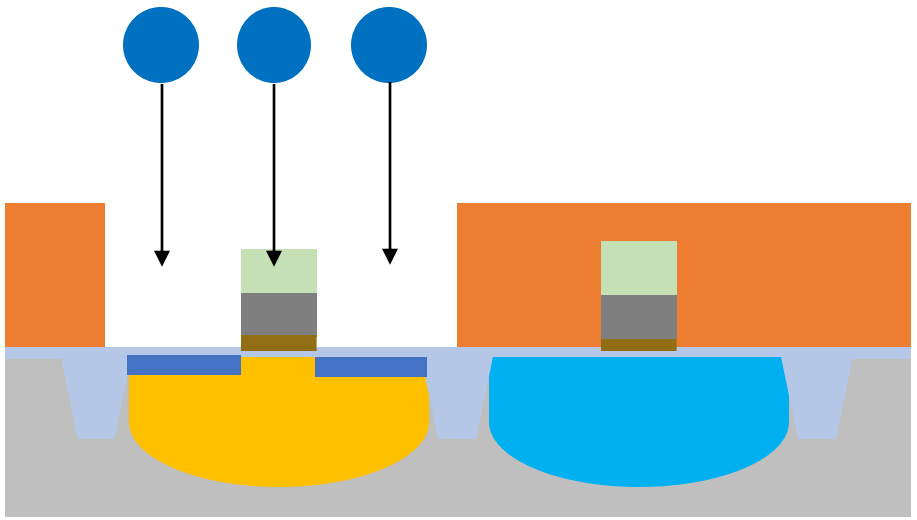
Purpose : Being able to protect from Ion implantation

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry



Si
Poly-Si
SiO_2
Extension (NMOS)
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

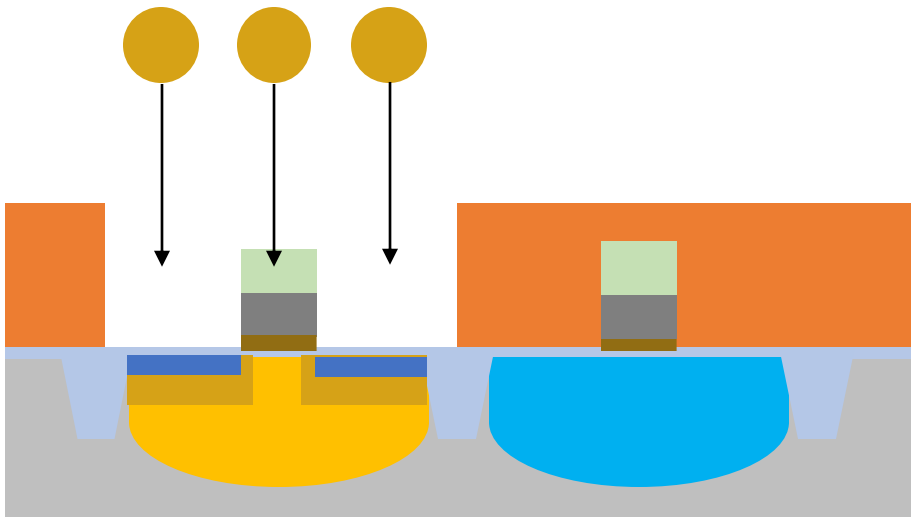
Purpose : To reduce the electric field near the drain junction, thereby mitigating hot carrier effects and improving device reliability.

Method : Ion implantation

Implanted material : Phosphorous

Concentration : ??~?? cm^{-3}

Metrology : Secondary Ion Mass Spectroscopy (SIMS)



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)

Purpose : To suppress short-channel effects, particularly the threshold voltage roll-off in scaled MOSFETs.

Method : Ion implantation

Implanted material : Boron

Concentration :??~?? cm^{-3}

Metrology : Secondary Ion Mass Spectroscopy (SIMS)

Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)

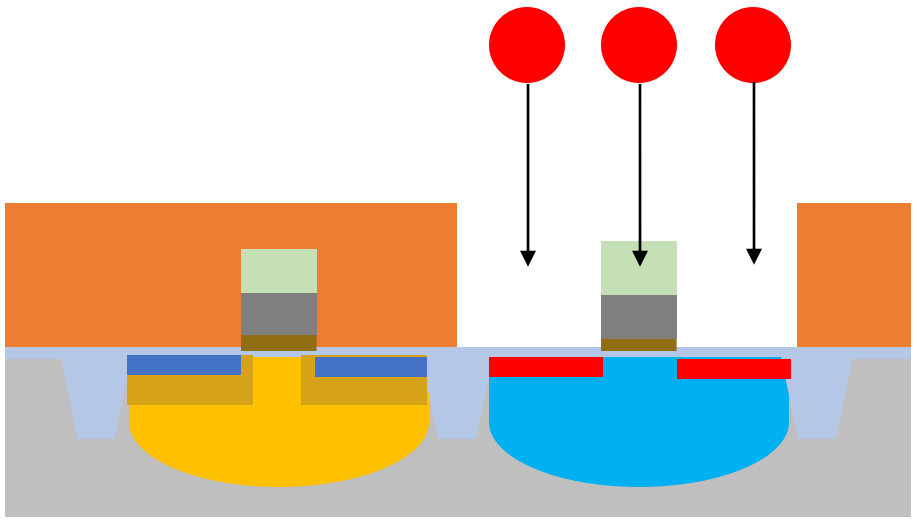
Purpose : Being able to protect from Ion implantation

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)

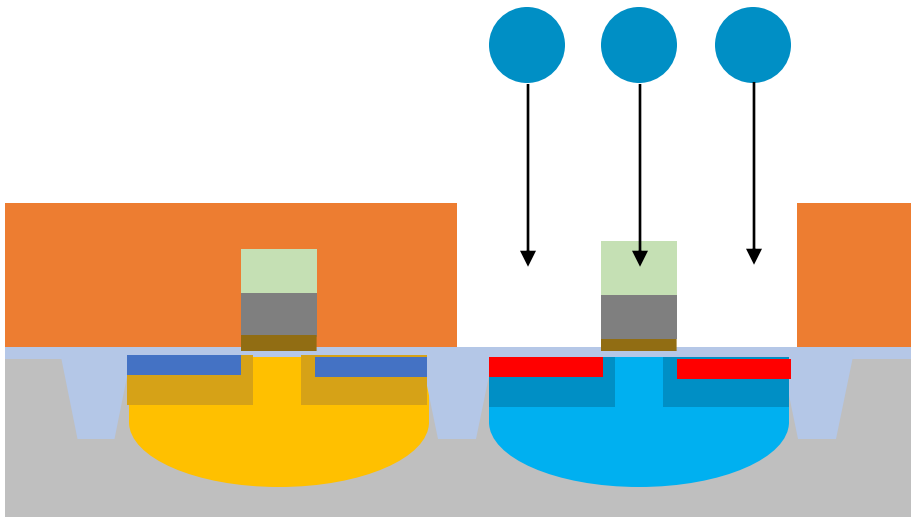
Purpose : To reduce the electric field near the drain junction, thereby mitigating hot carrier effects and improving device reliability.

Method : Ion implantation

Implanted material : Boron or BF_2

Concentration : ??~?? cm^{-3}

Metrology : Secondary Ion Mass Spectroscopy (SIMS)



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

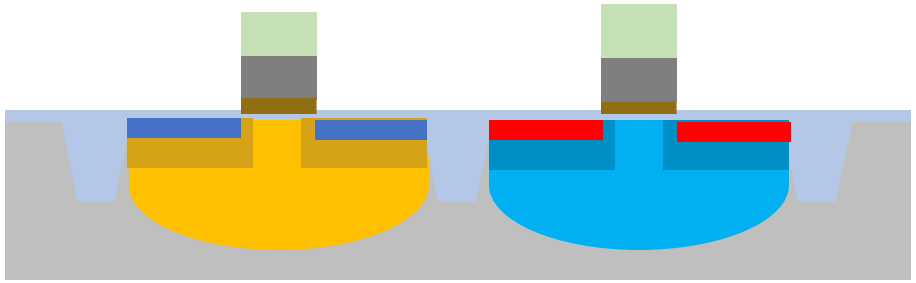
Purpose : To suppress short-channel effects, particularly the threshold voltage roll-off in scaled MOSFETs.

Method : Ion implantation

Implanted material : Phosphorous

Concentration : ??~?? cm^{-3}

Metrology : Secondary Ion Mass Spectroscopy (SIMS)



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

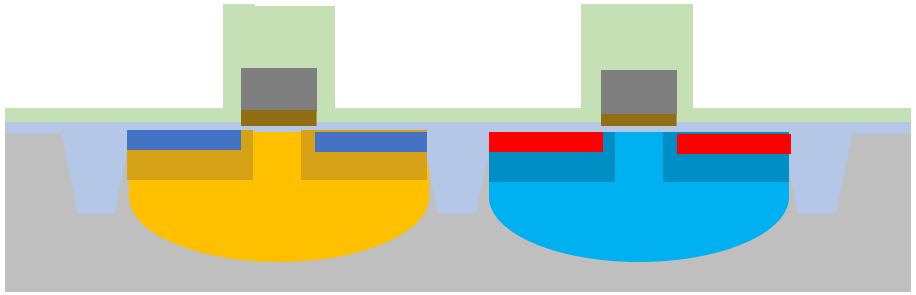
Purpose : Strip resist

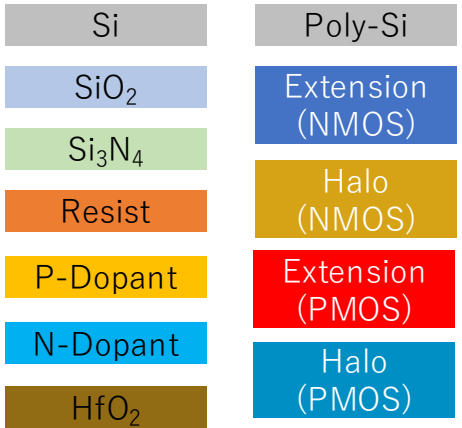
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System





Purpose : To form sidewall film for determining the channel length

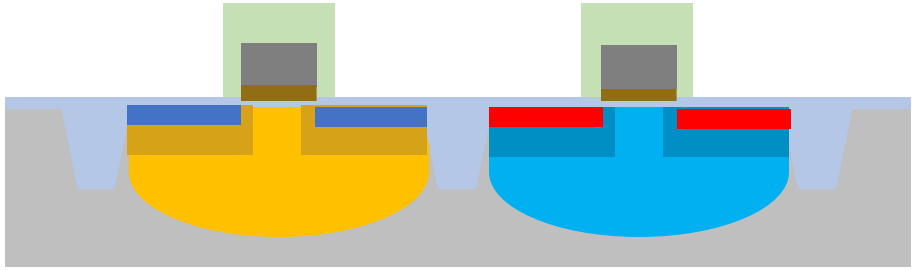
Method : TEOS CVD (is better)

Deposited material : Silicon Nitride

Thickness : Few hundred nm

Metrology : Spectroscopy interferometry

SiGe S/D Formation– Spacer Etching



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

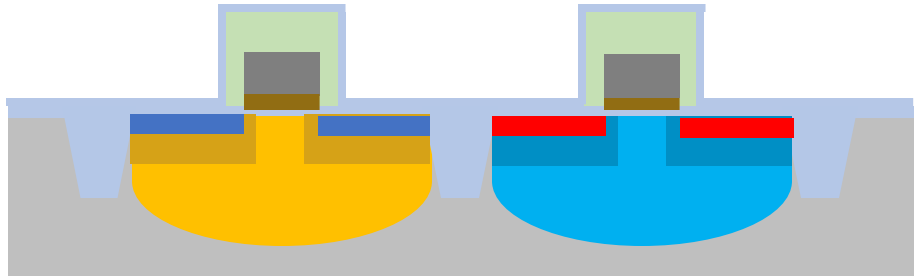
Purpose : To form sidewall film for determining the channel length

Method : RIE (as anisotropic as possible)

Etched material : Silicon Nitride

Thickness : Few hundred nm

Metrology : Spectroscopy interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : A hard mask must be deposited before Ge-Si epitaxy, as the photoresist cannot withstand the high temperatures typically required during these processes.

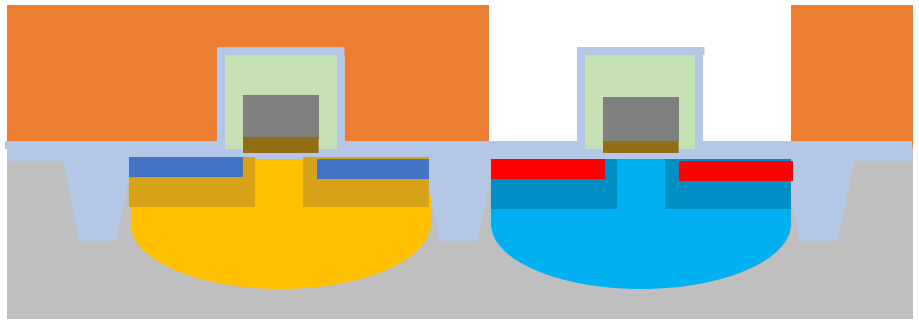
Method : Thermal Oxidation

Deposited material : Silicon Dioxide

Thickness : 10 nm

Metrology : Spectroscopy interferometry

SiGe S/D Formation– Hard mask patterning



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Being able to protect from etching

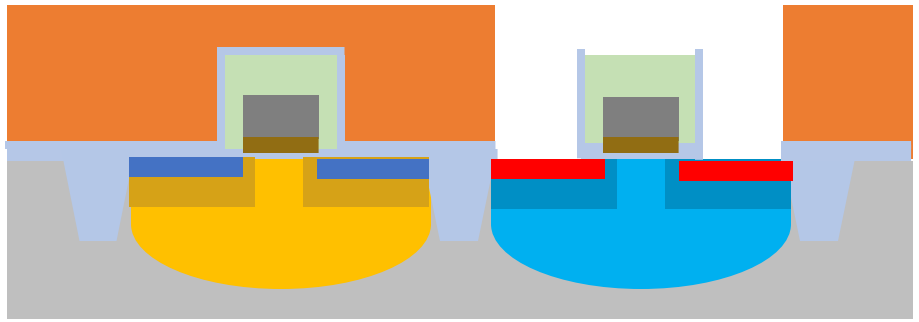
Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry

SiGe S/D Formation– Hard mask etching



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Being able to protect from etching

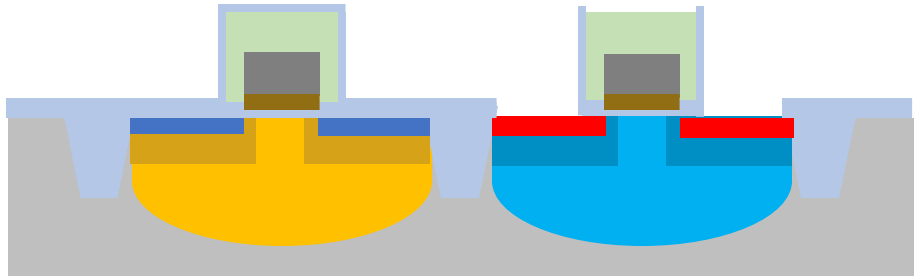
Method : Coating, Exposure, Development

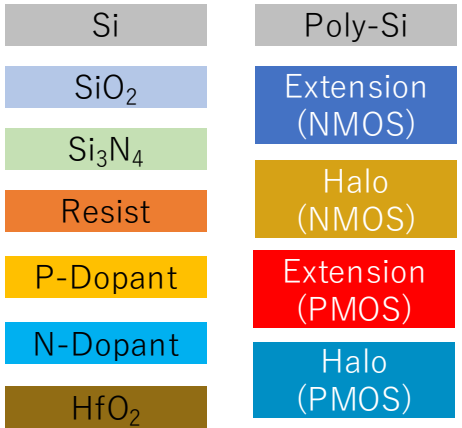
Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry

SiGe S/D Formation– Resist Stripping





Purpose : Strip resist

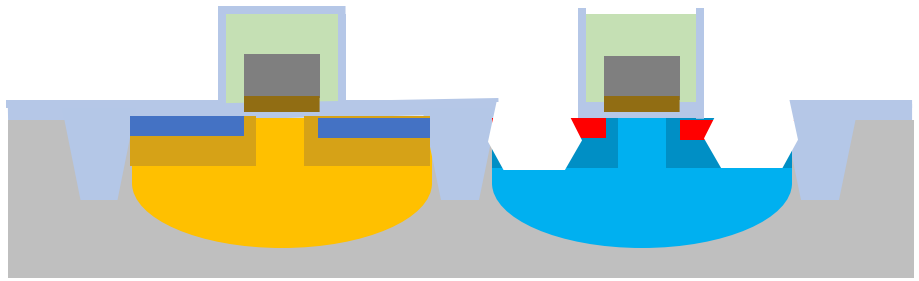
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

SiGe S/D Formation– Si Recess Etching



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : For making trench to embed the SiGe epitaxy growth

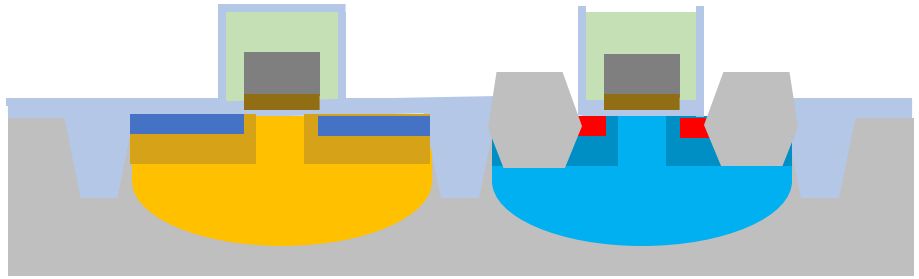
Method : Wet etching (TMAH, KOH?)

Etched material : Si on PMOS side

Thickness : Few ten nm (60nm?)

Metrology : TEM

SiGe S/D Formation– SiGe epitaxy growth



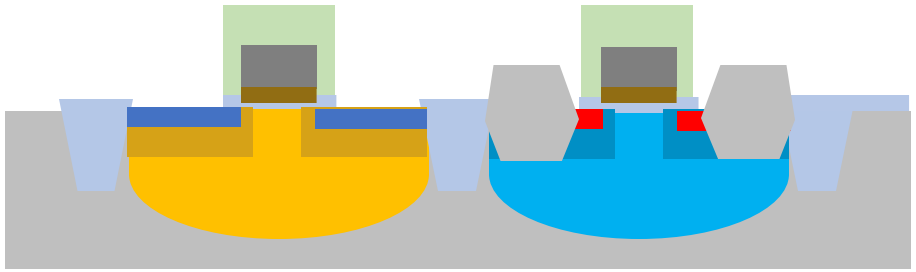
Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Embedding SiGe in the source/drain regions introduces uniaxial compressive strain, which boosts hole mobility in PMOS transistor.

Method : Epitaxial Growth

Deposited material : SiGe

SiGe S/D Formation– Remove hard mask



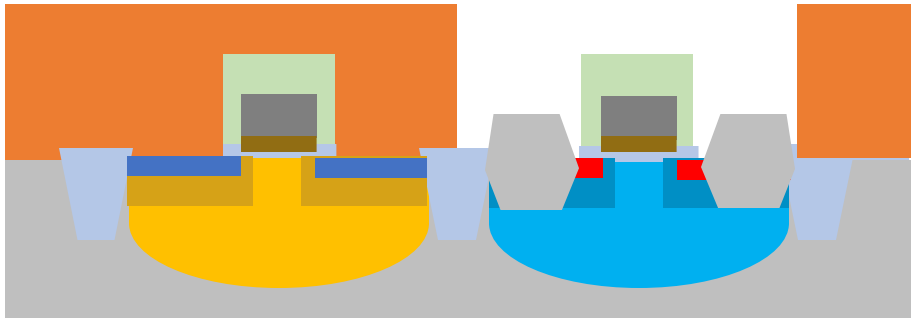
Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : To remove hard

Method : Wet Etching (BHF)

Etched material : 10nm

SiGe S/D Formation– Patterning



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Being able to protect from Ion implantation

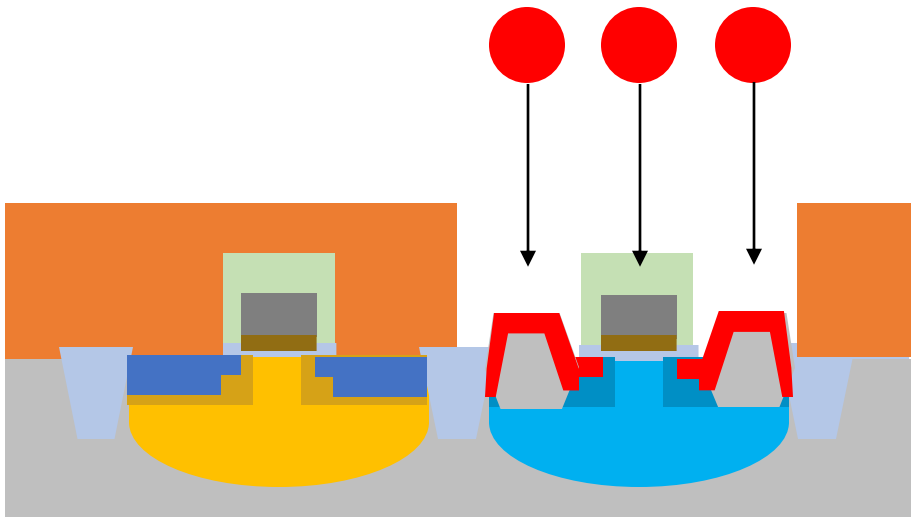
Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry

SiGe S/D Formation– Source and Drain ion implantation



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : To form Source and Drain ion implantation.

Method : Ion implantation

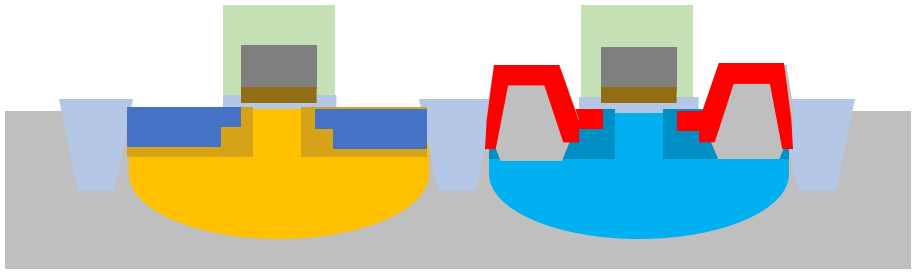
Implanted material : Arsenic, Boron difluoride

Concentration : 10^{20} cm^{-3}

Metrology : Secondary Ion Mass Spectroscopy (SIMS)

※N-MOS ion implantation is omitted

SiGe S/D Formation– Resist strip



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Strip resist

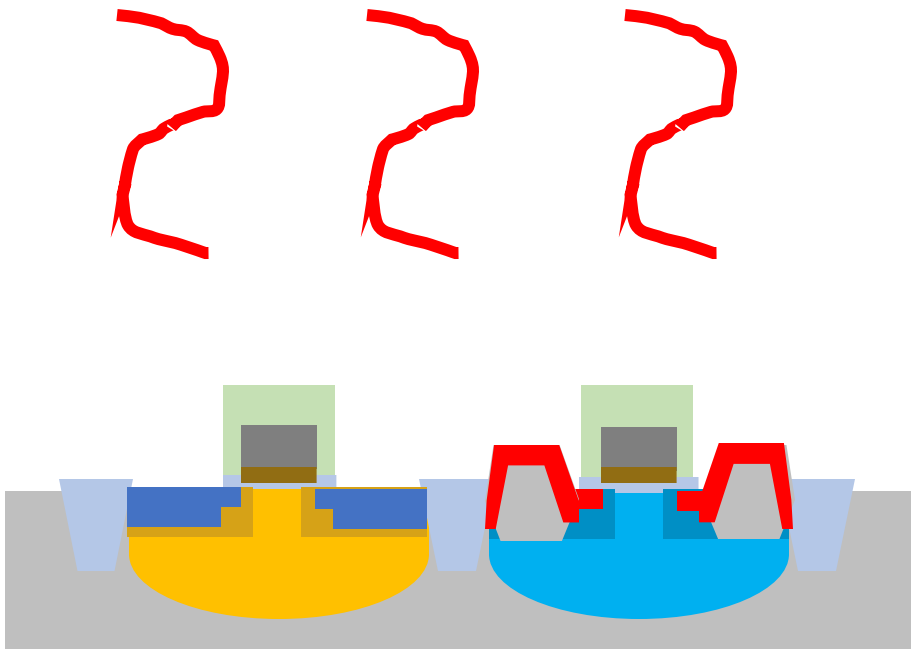
Method : O2 ashing

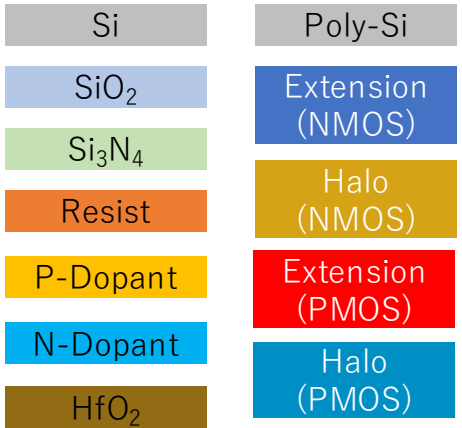
Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

SiGe S/D Formation– Annealing



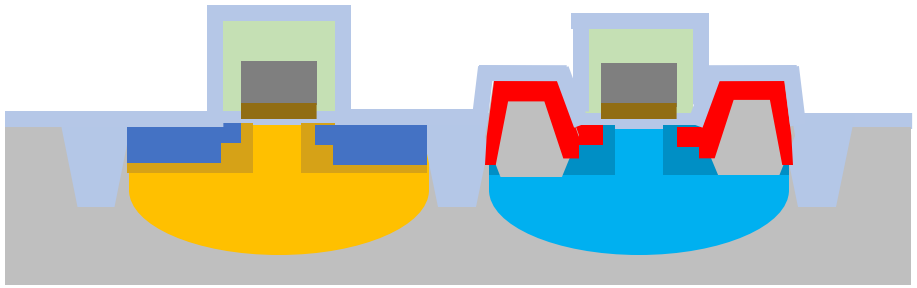


Purpose : Annealing activates the dopants by using heat, allowing them to move into the silicon lattice and become electrically active.

Method : Furnace annealing
(Vertical furnace annealing)

Temperature : Over 1000°C

Silicide Formation – Deposit Hard mask



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

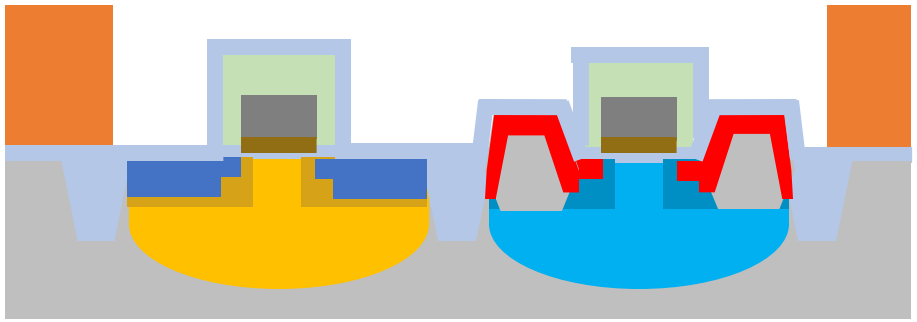
Purpose : To form hard mask for silicide

Method : CVD (TEOS)

Deposited material : Silicon Dioxide

Thickness : 80 ~ 120 nm

Metrology : Spectroscopy interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

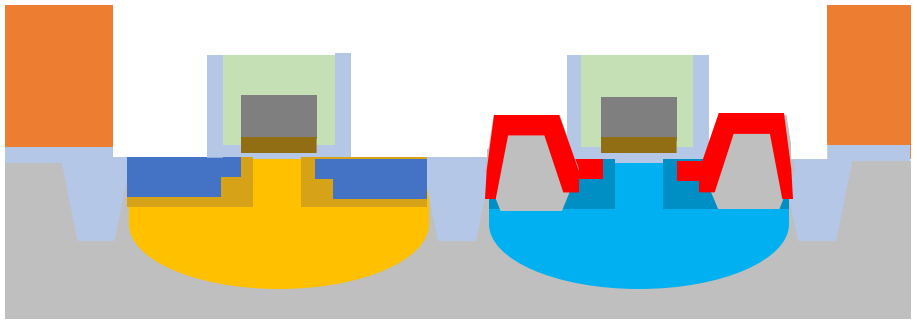
Purpose : Being able to protect from etching

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Spectroscopy Interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Being able to protect from etching

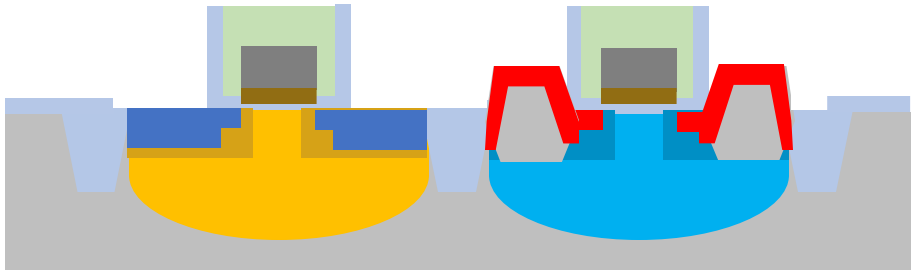
Method : RIE

Deposited material : Silicon Dioxide

Thickness : 80 ~ 120 nm

Metrology : Spectroscopy Interferometry

Silicide Formation – Resist Striping



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Purpose : Strip resist

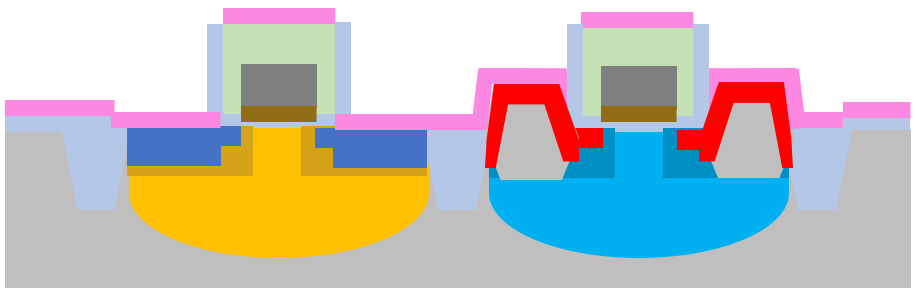
Method : O2 ashing

Etched material : Photoresist

Thickness : 300 ~ 800 nm

Metrology : Surface Particle Inspection System

Silicide Formation – Deposit silicide metal



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)

Purpose : Silicide materials are deposited by sputtering to react with silicon and form low-resistance metal silicide contacts during annealing.

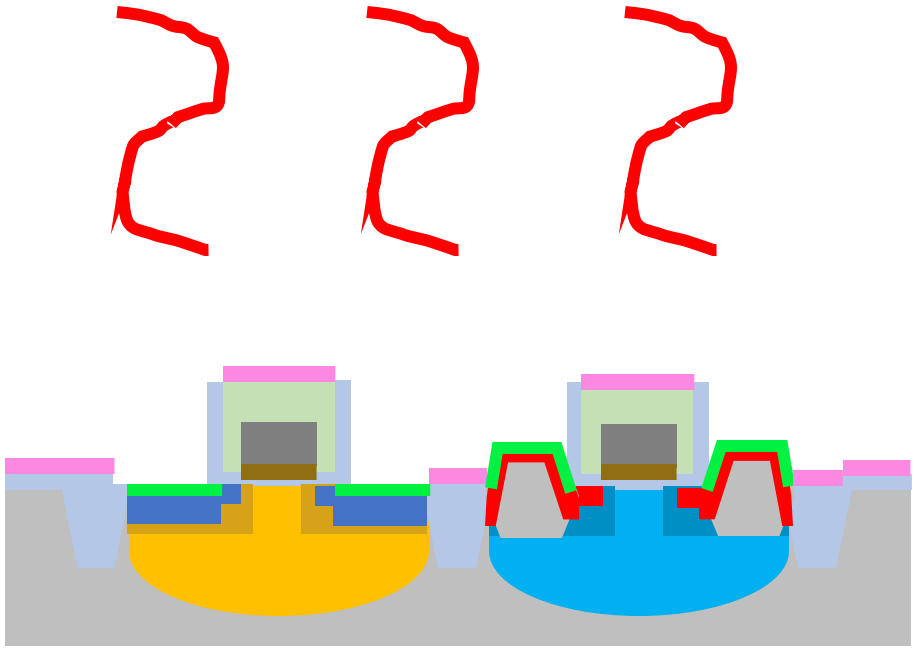
Method : Sputtering

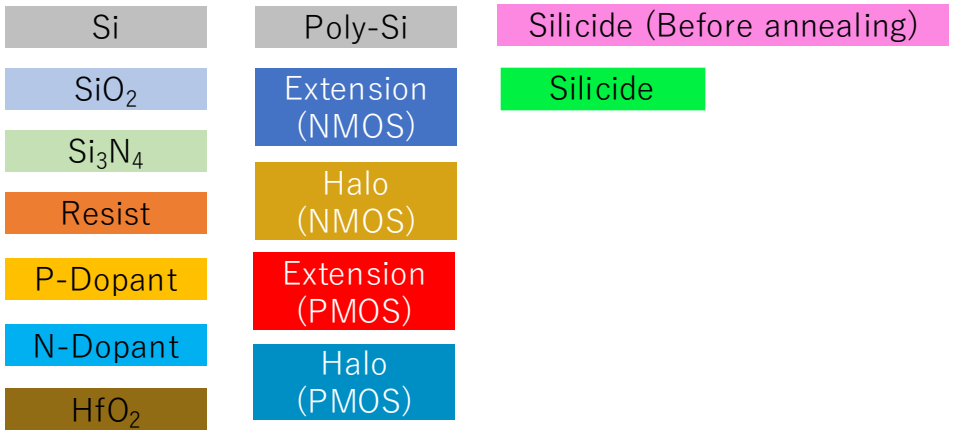
Deposited material : Ti, Co or Ni etc.

Thickness : 30 ~ 80 nm

Metrology : Ellipsometry, XRR, XRF

Silicide Formation – 1st Annealing





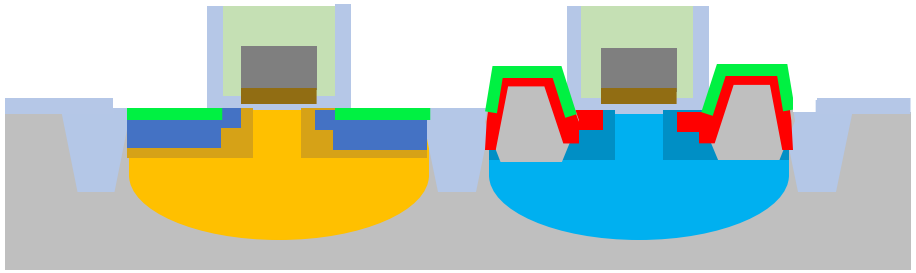
Purpose : Initiate the reaction between the deposited metal and the underlying silicon to form a preliminary silicide phase
(C49 phase which is high resistivity).

Method : Furnace annealing

Deposited material : Si + Silicide material
(Ti, Co, Ni)

Temperature : 600 ~ 700°C

Silicide Formation – Wet Etching



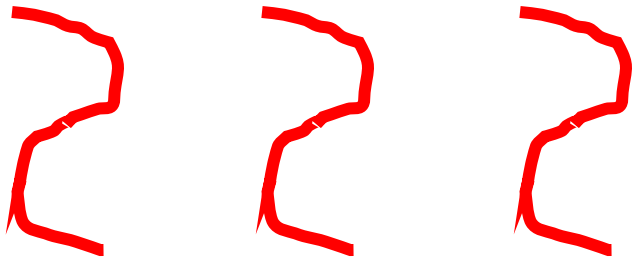
Si
Poly-Si
Silicide (Before annealing)
SiO_2
Extension (NMOS)
Silicide
Si_3N_4
Halo (NMOS)
Resist
Extension (PMOS)
P-Dopant
Halo (PMOS)
N-Dopant
HfO_2

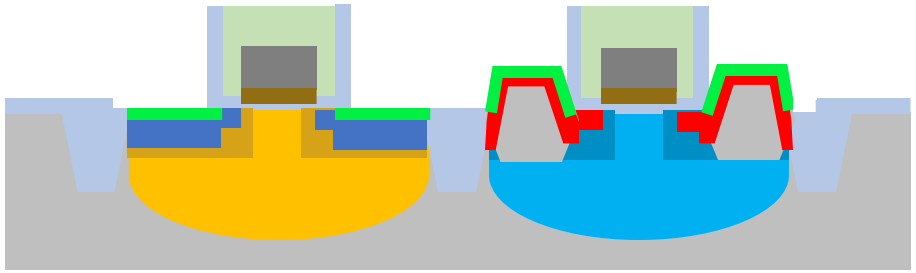
Purpose : To eliminate only the non-silicide area

Method : Wet etching ($HF + H_2O_2$)

Etched material : Silicide material

Silicide Formation – 2nd Annealing





Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2

Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)

Silicide (Before annealing)
Silicide

Purpose : To convert the high-resistance C49 phase into the low-resistance C54 phase.

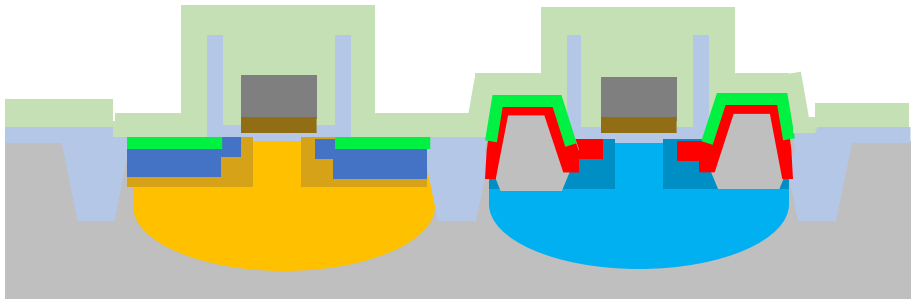
Method : Furnace annealing

Deposited material : Silicide material

Temperature : 700 ~ 900°C

Note: Why this flow?
(1st anneal → Wet etching → 2nd anneal)
This sequence helps prevent unintended silicide formation and reduces the risk of electrical failure.

ILD Deposition – Linear SiN deposition



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide

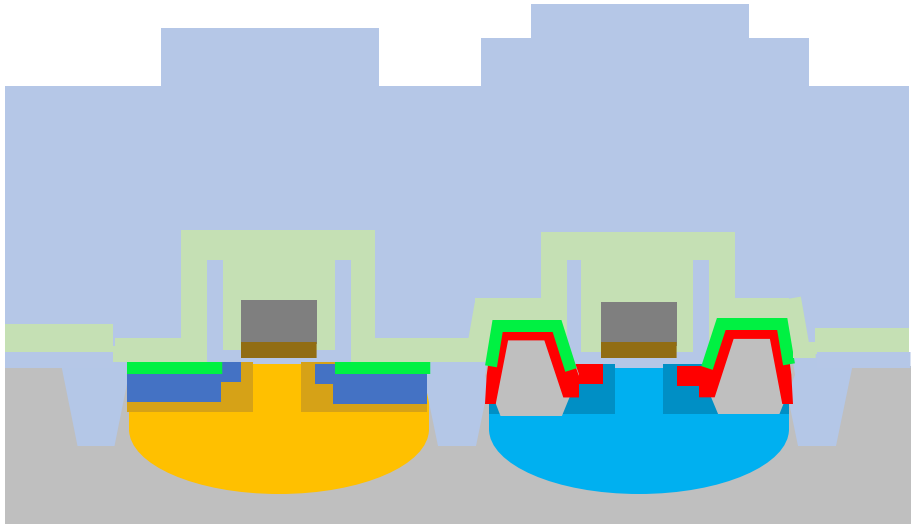
Purpose : Strain engineering for transistors
Etch stop layer during contact formation

Method : CVD

Deposited material : Silicide Nitride

Thickness : 5 ~ 30 nm

Metrology : Spectroscopic Ellipsometry



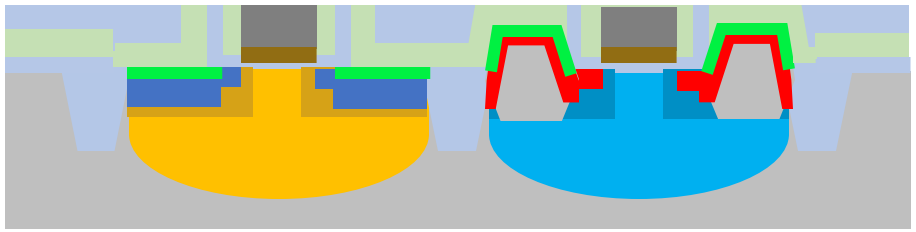
Purpose : Deposit ILD

Method :LPCVD, SOG

Deposited material : Silicon Dioxide

Thickness : Few hundred nm

Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide



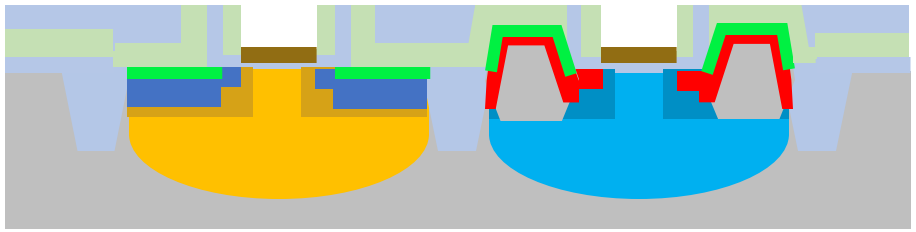
Purpose : CMP is performed until the dummy gate is exposed in order to replace it.

Method : CMP

Planarized material : Silicon Dioxide/Silicon Nitride

Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide

Dummy Gate Replacement – Wet Etching



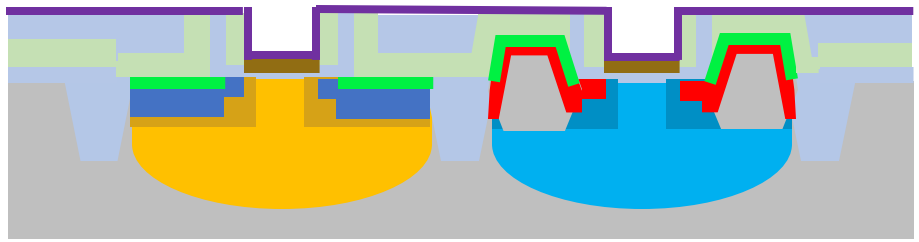
Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide

Purpose : Gate material is removed for replacement

Method : Wet Etching

Etched material : Poly-Si

Etchant : Alkaline TMAH solution
under ultrasonic treatment



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M

Purpose : Work function metals are deposited to tune the threshold voltage of NMOS and PMOS transistors by aligning their work function with the semiconductor bands

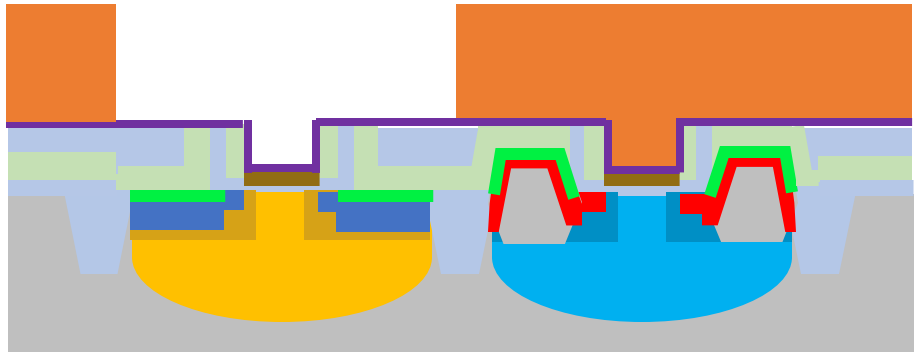
Method : Sputtering, ALD

Deposited material : TiN

Thickness : Few nm

Metrology: XRR

Gate Stack Formation– Patterning



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M

Purpose : To cover PMOS area in order to remove the work function metal on the NMOS side.

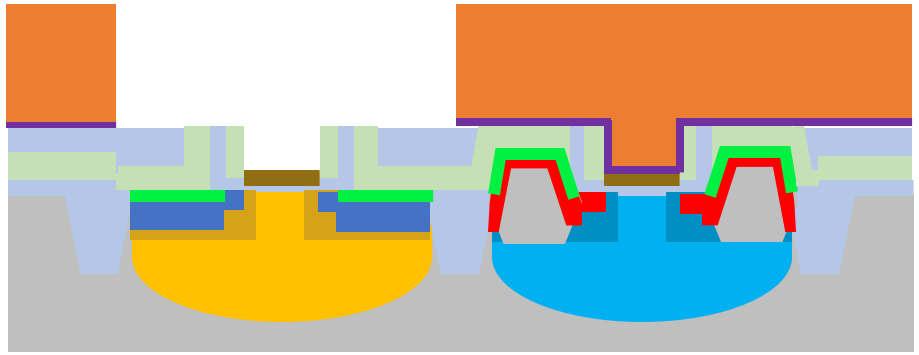
Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : 200 ~ 300 nm

Metrology : Spectroscopy Interferometry

Gate Stack Formation– Remove NMOS Work function metal



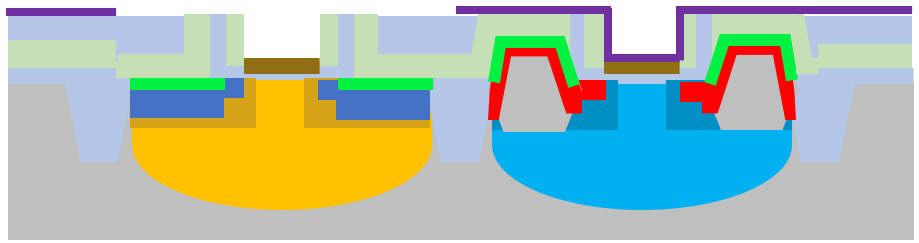
Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M

Purpose : To cover PMOS area in order to remove the work function metal on the NMOS side.

Method : Wet etching

Etched material : PMOS work function metal

Gate Stack Formation– Remove Photoresist



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M

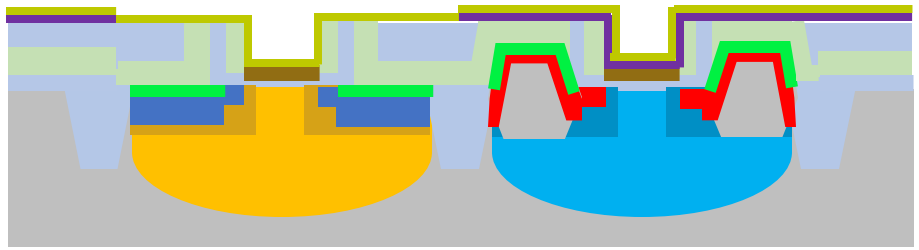
Purpose : Strip resist

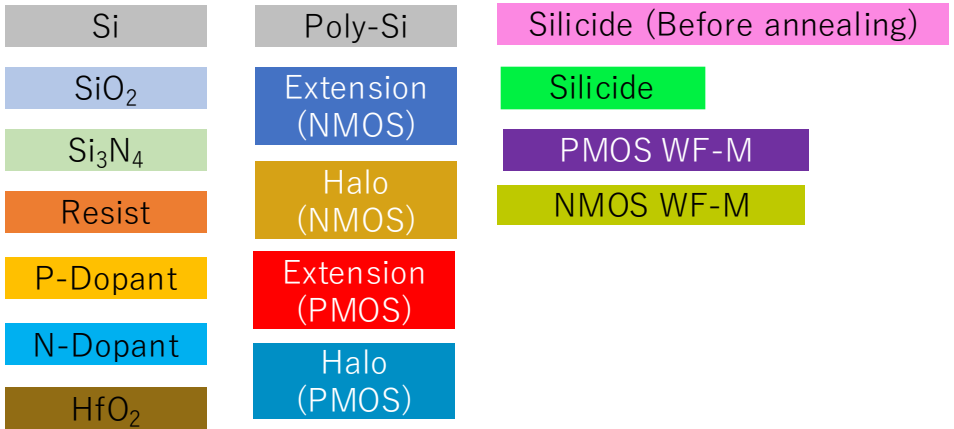
Method : O2 ashing

Etched material : Photoresist

Thickness : 200 ~ 300 nm

Metrology : Surface Particle Inspection System





Purpose : Work function metals are deposited to tune the threshold voltage of NMOS and PMOS transistors by aligning their work function with the semiconductor bands

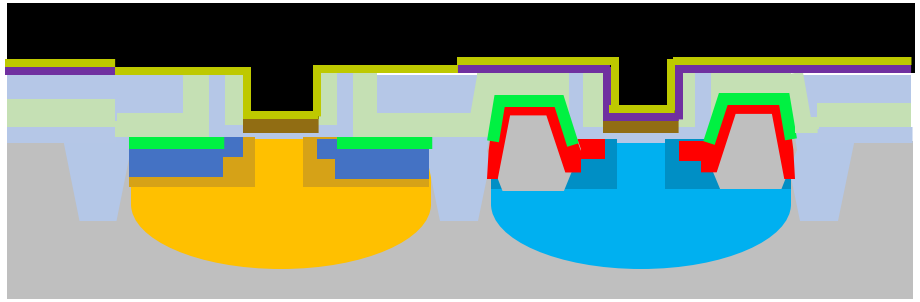
Method : Sputtering, ALD

Deposited material : TiAl/TiAlN

Thickness : Few nm

Metrology: XRR

Gate Stack Formation– Embed Gate Metal



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Purpose : To form gate metal

Method : CVD, ALD

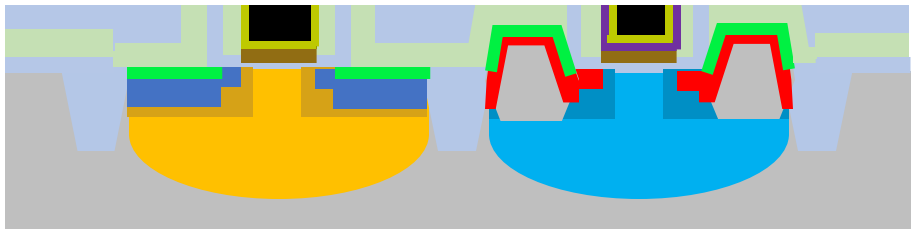
Deposited material : Tungsten

Thickness : 120~200 nm

Purpose : To embed gate metal

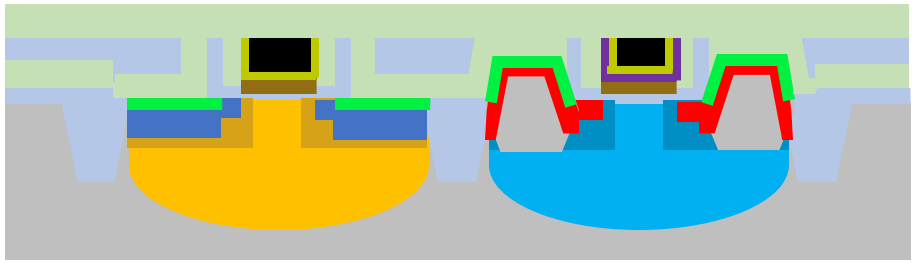
Method : CMP

Planarized material : Tungsten(W)



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Contact Plug Formation– Etch Stop Layer Deposition



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Purpose : To stabilize the process, an etch stop layer is introduced to ensure stable etching.

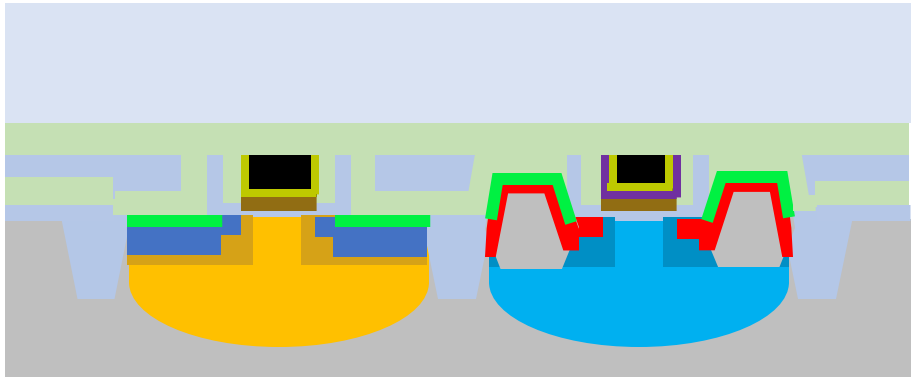
Method : CVD

Deposited material : Silicon Nitride

Thickness : 10~20 nm

Metrology : Spectroscopic Ellipsometry

Contact Plug Formation– ILD Deposition



Purpose : Deposit ILD

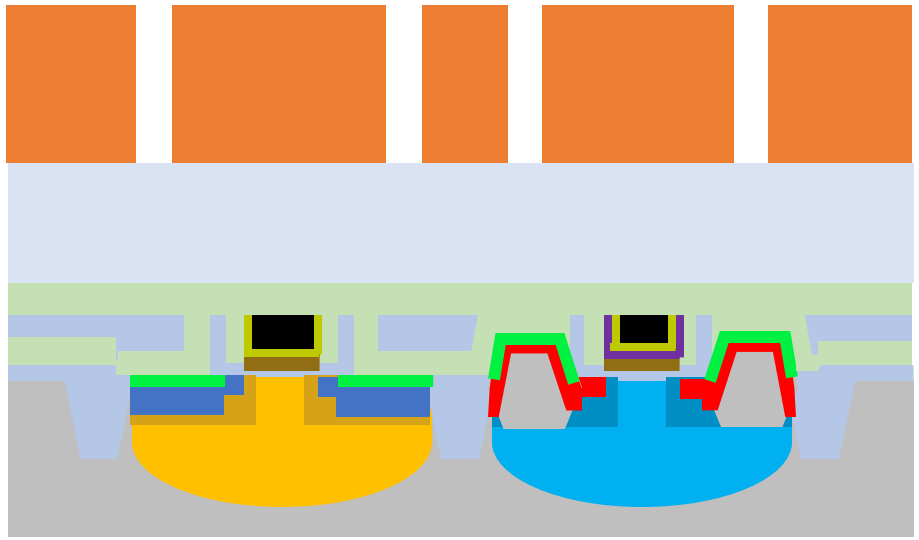
Method : LPCVD, SOG

Deposited material : Silicon Dioxide

Thickness : Few hundred nm

Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Contact Plug Formation– Contact Patterning



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

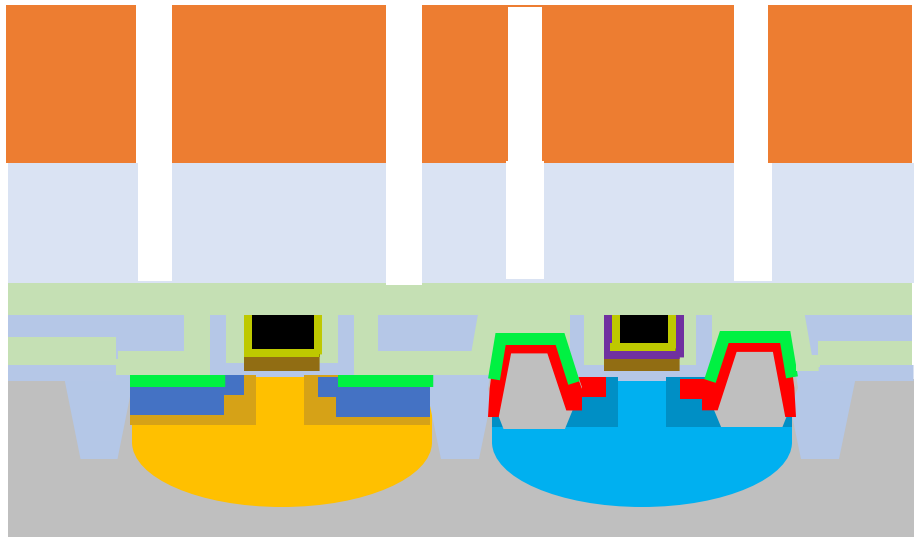
Purpose : Protect from RIE etching

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : Few μm

Metrology : Spectroscopy Interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Purpose : To stabilize the process, the etching is temporarily stopped at the etch stop layer.

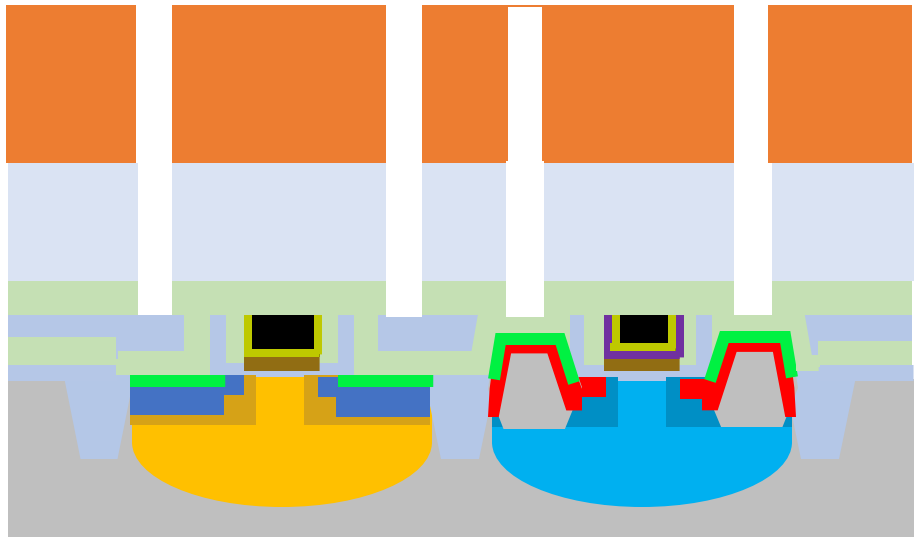
Method : RIE (CHF_3 Gas)

Etched material : Silicon dioxide

Thickness : Few hundred nm

Metrology : Stylus profiler

Contact Plug Formation– Contact Etching 2



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

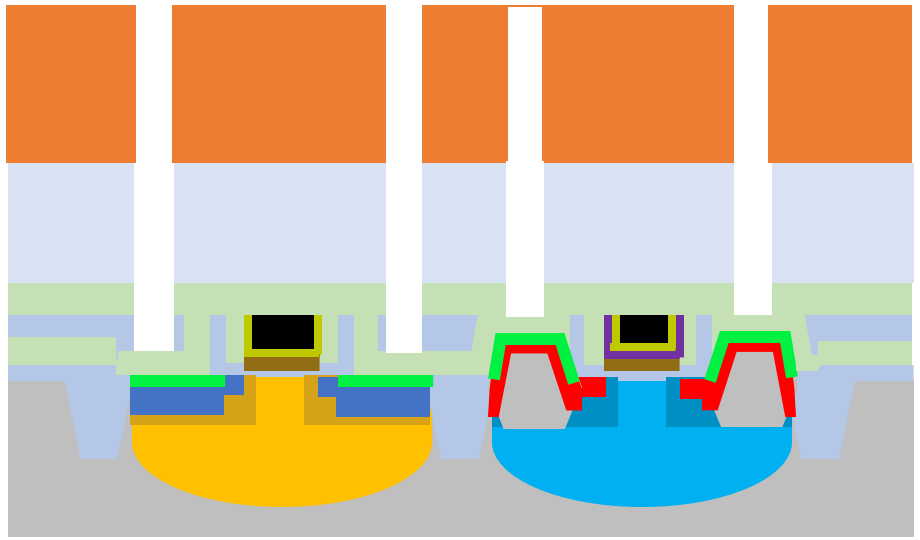
Purpose : To stabilize the process, the etching is temporarily stopped at the etch stop layer.

Method : RIE

Etched material : Silicon Nitride

Thickness : 10~20 nm

Metrology : Stylus profiler



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

Purpose : To stabilize the process, the etching is temporarily stopped at the etch stop layer.

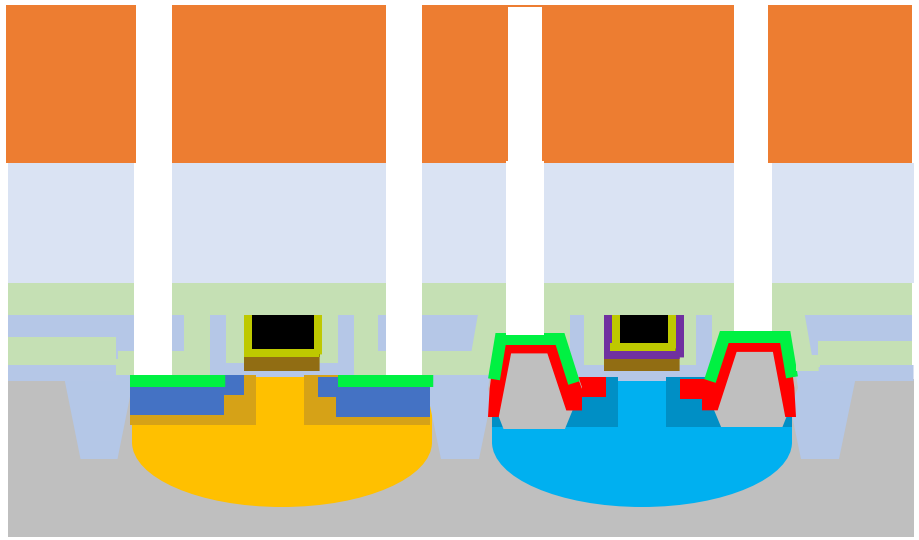
Method : RIE

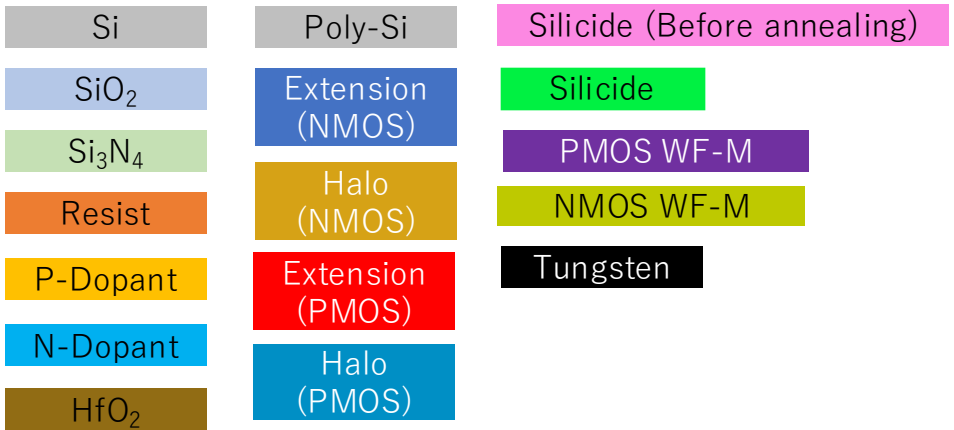
Etched material : Silicon dioxide

Thickness : Few hundred nm

Metrology : Stylus profiler

Contact Plug Formation– Contact Etching 4





Purpose : To stabilize the process, the etching is temporarily stopped at the etch stop layer.

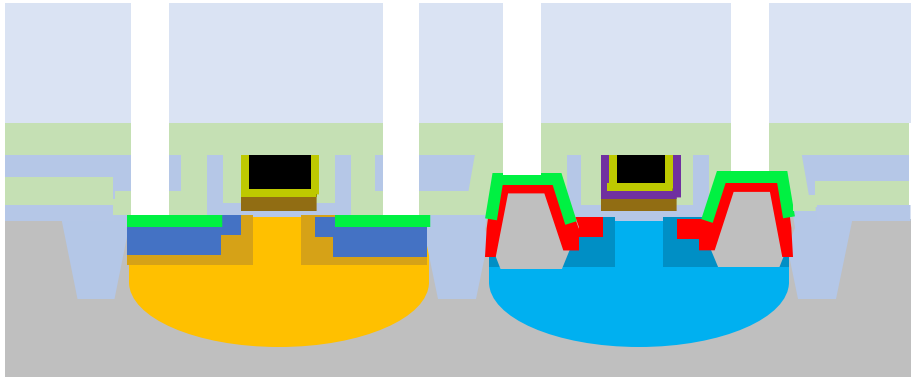
Method : RIE

Etched material : Silicon Nitride

Thickness : 5 ~ 30 nm

Metrology : Stylus profiler

Contact Plug Formation– Photoresist Stripping



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten

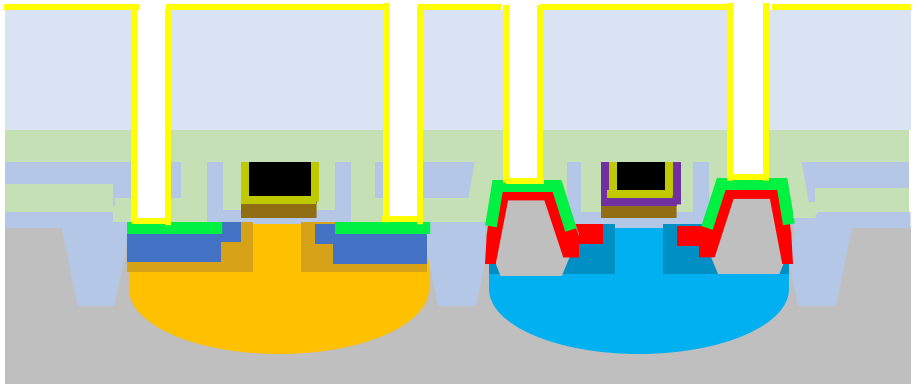
Purpose : Strip resist

Method : O2 ashing

Etched material : Photoresist

Thickness : Few μm

Metrology : Surface Particle Inspection System



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti

Purpose : Prevent Tungsten from diffuse with Silicon. Deposit Barrier layer

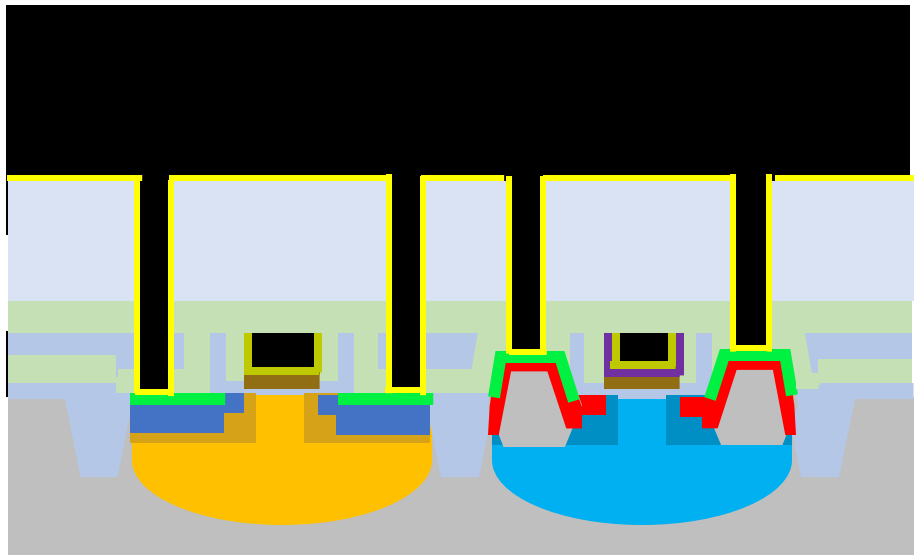
Method : CVD (is better because good coverage)

Deposited material : TiN/Ti

Thickness : Few ten nm

Metrology :
Thickness → Spectroscopy Ellipsometry, XRR,XRF
Coverage → FIB, SEM, TEM

Wire・Via Formation – Tungsten layer Deposition



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti

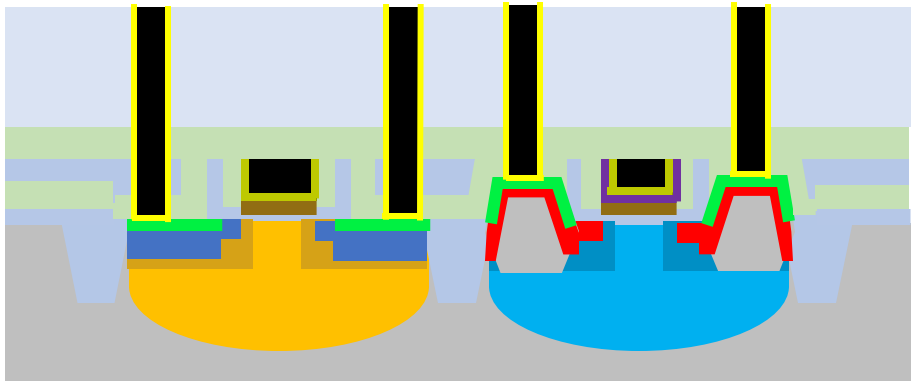
Purpose : Deposit Wiring layer

Method : CVD (is better because good coverage)

Deposited material : Tungsten

Thickness : Few hundred nm ~ few μm

Metrology :
Thickness → Spectroscopy Ellipsometry, XRR,XRF
Coverage → FIB, SEM, TEM



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti

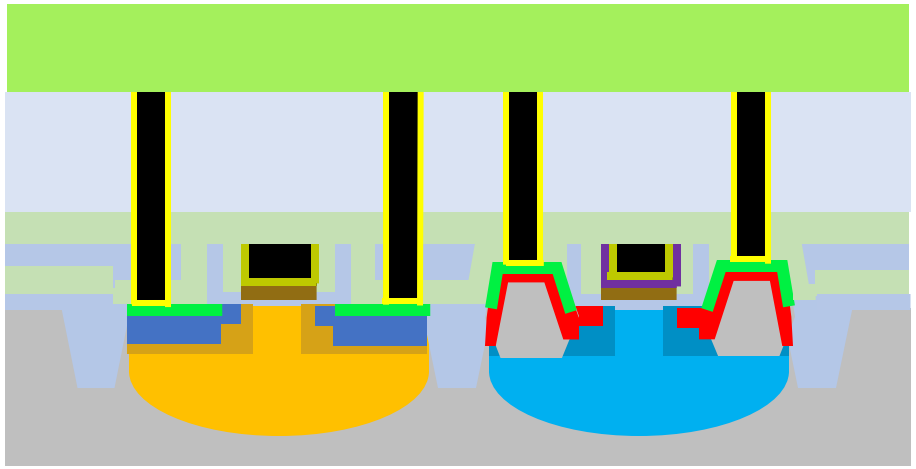
Purpose : To embed tungsten into contact hole

Method : CMP (Al_2O_3, H_2O_2 slurry)

Planarized material : Tungsten

Thickness : Few hundred nm ~ few μm

Metrology :
Thickness → Spectroscopy Ellipsometry, XRR,XRF
Coverage → FIB, SEM, TEM



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti
Low-k

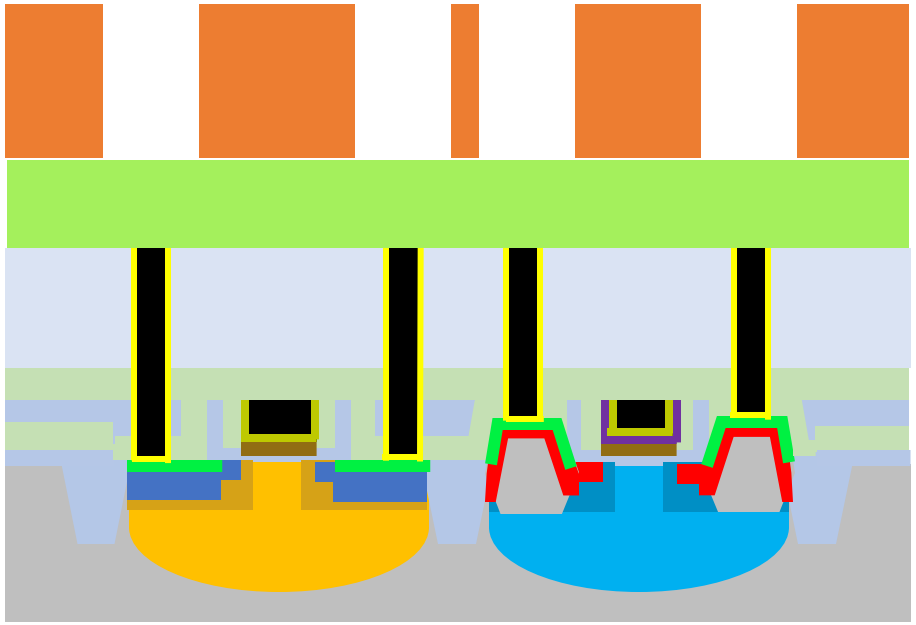
Purpose : To provide insulation between metal layers

Method : PE-CVD

Planarized material : FSG, SIOC, p-SIOC

Thickness : Few hundred nm ~ few μm

Metrology :
Thickness → Spectroscopy Ellipsometry, XRR,XRF
Density → Spectroscopy Ellipsometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti
Low-k

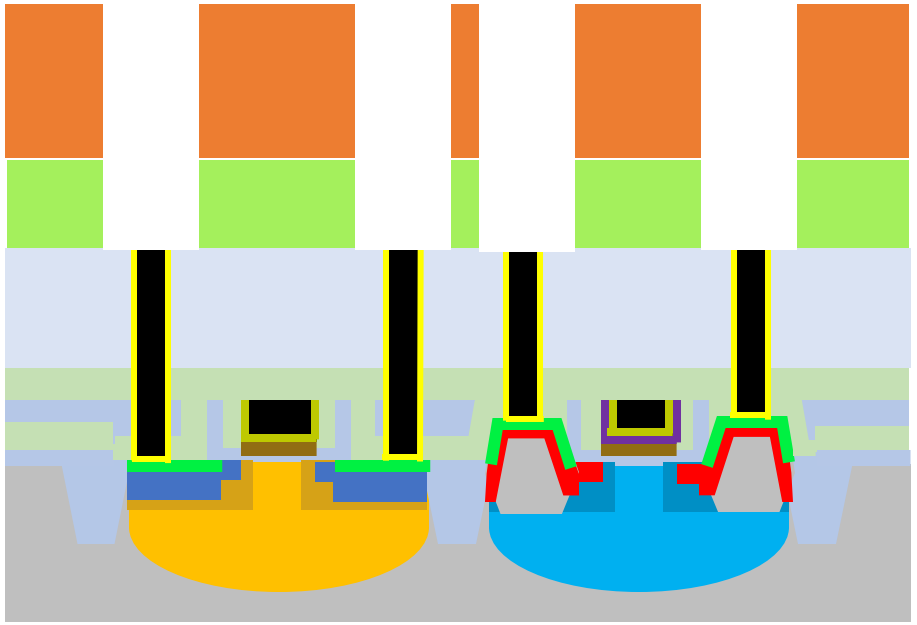
Purpose : Being able to protect from RIE

Method : Coating, Exposure, Development

Deposited material : Photoresist

Thickness : Few μm

Metrology : Spectroscopy Interferometry



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti
Low-k

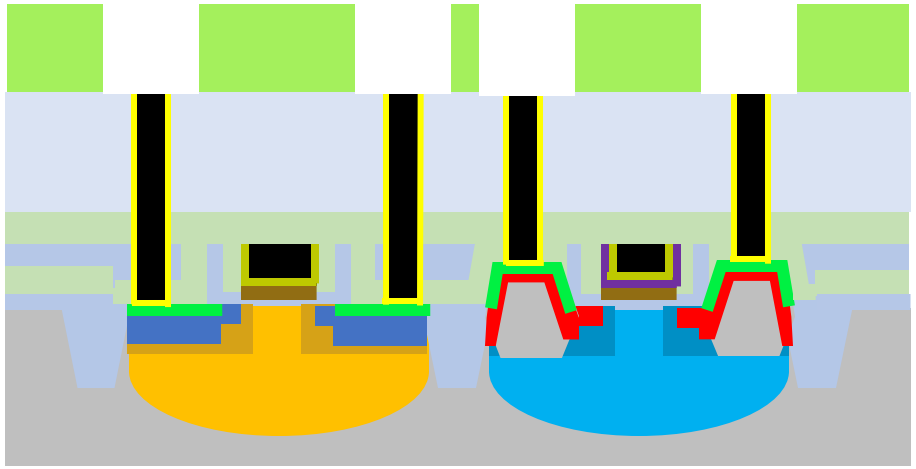
Purpose : To ensure that the semiconductor operates properly by allowing electrical signals and power to flow between components.

Method : RIE

Etched material : FSG, SIOC, p-SIOC

Thickness : Few hundred nm ~ few μm

Metrology : Sylus profiler



Si
SiO_2
Si_3N_4
Resist
P-Dopant
N-Dopant
HfO_2
Poly-Si
Extension (NMOS)
Halo (NMOS)
Extension (PMOS)
Halo (PMOS)
Silicide (Before annealing)
Silicide
PMOS WF-M
NMOS WF-M
Tungsten
TiN/Ti
Low-k

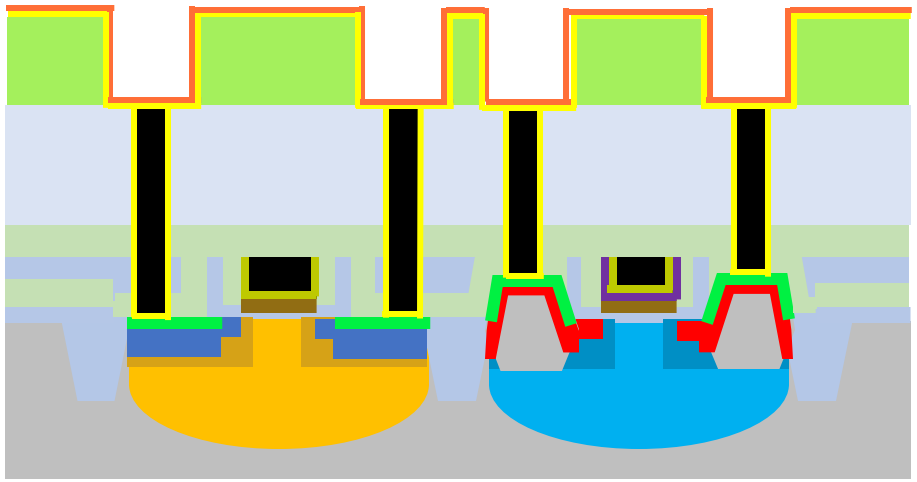
Purpose : Strip resist

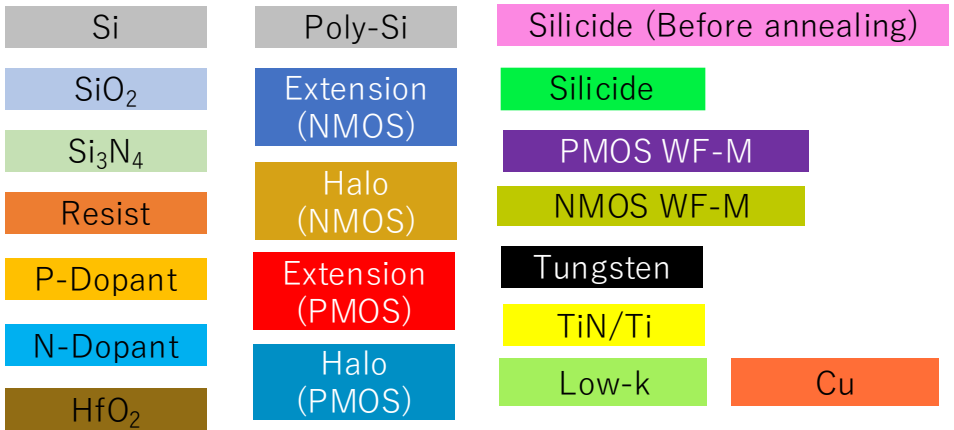
Method : O2 ashing

Etched material : Photoresist

Thickness : Few hundred nm ~ few μm

Metrology : Surface Particle Inspection System





Purpose : Prevent copper from diffuse, erosion.

Method : Sputtering

Deposited material : TiN/Ti/Cu

TiN→ Barrier metal

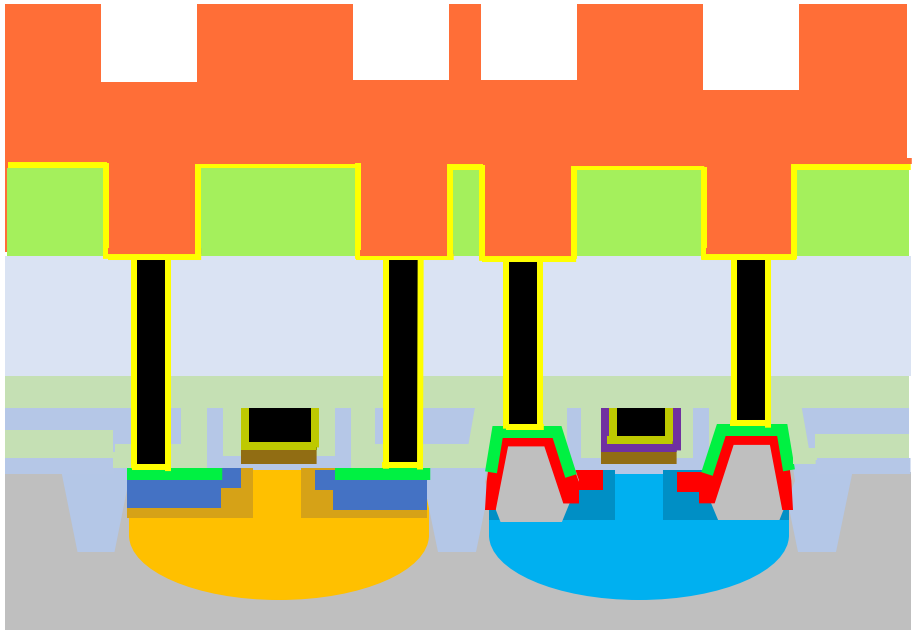
Ti →Adhesion layer

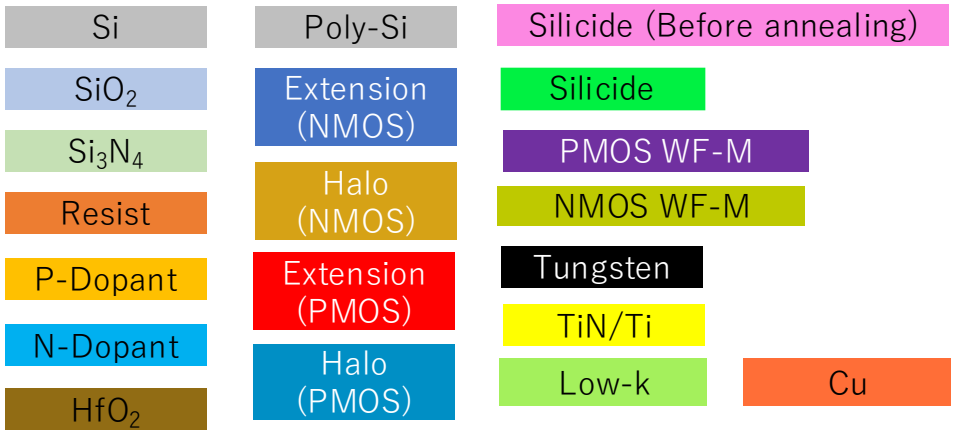
Cu→ Copper underlayer

Thickness : Few ten nm

Metrology :

Coverage → FIB, SEM, TEM





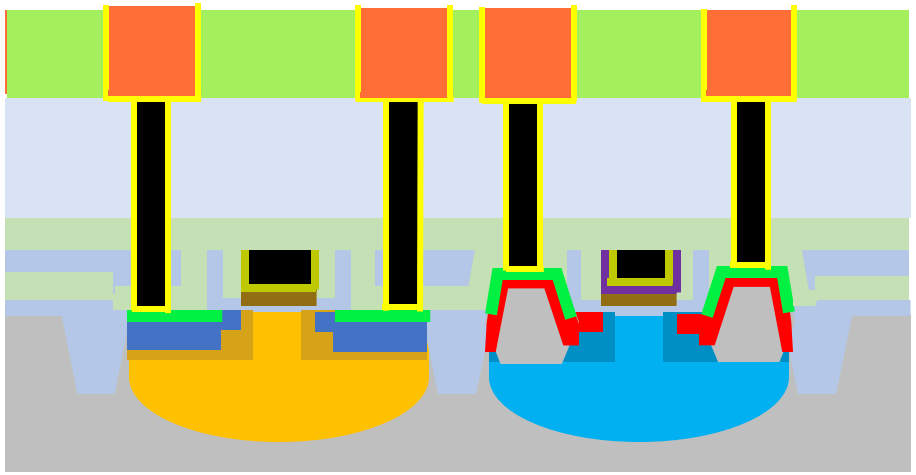
Purpose : Filling copper to form wire

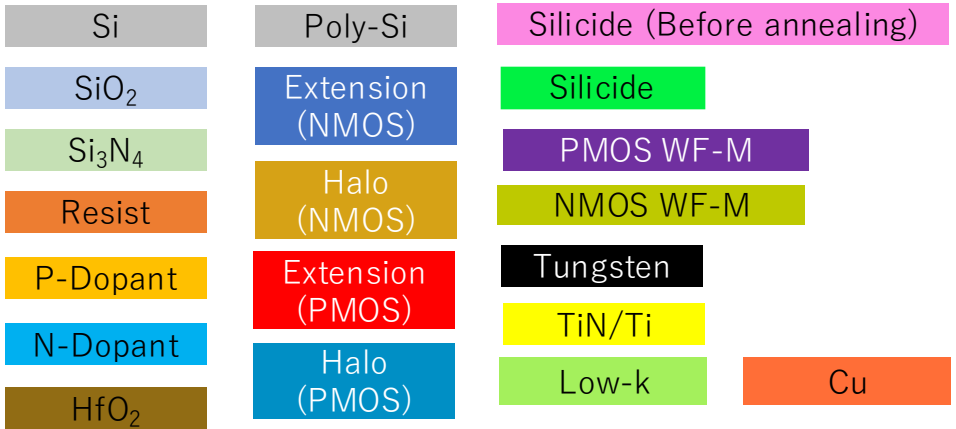
Method : Electroplating (Copper sulfate plating)

Deposited material : Cu

Thickness : Few μm

Metrology :
Thickness → XRF





Purpose : To embed copper into contact wire

Method : CMP (Colloidal Silica, H_2O_2 slurry)

Planarized material : Copper

Thickness : Few μm

Metrology :
Thickness → XRF
Coverage → FIB, SEM, TEM