Bastian Hagedorn

Einsteinstraße 62
48149 Münster, Germany
☎ *+49 (0) 251 83-32746*
✉ *b.hagedorn@wwu.de*

University Education

since 2016 **Ph.D. studies**, *University of Münster*, Münster, Germany.
Supervisor: Prof. Sergei Gorlatch
My PhD research focuses on high-performance GPU code generation using Lift by tackling the growing problem of achieving high efficiency when programming the ever changing hardware of today and tomorrow. I'm one of the main developers of the Lift project which has recently emerged as a promising compilation framework to achieve performance portability. Lift defines a small set of reusable parallel primitives that DSL writers can easily build upon. Lift's key novelty is its ability to automatically explore the optimization space by using as a system of extensible rewrite rules which encode specific optimizations.

2014 – 2016 **Master of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: excellent with distinction (90%).*
Thesis title: An Extension of a Functional Intermediate Language for Parallelizing Stencil Computations and its Optimizing GPU Implementation Using OpenCL.
Grade for thesis: excellent

2011 – 2014 **Bachelor of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: very good (81%).*
Thesis title: Implementation of a Multicast Module for the Floodlight SDN-Controller
Grade for thesis: excellent

Research Visits

07/2018 – 09/2018 **Deep Learning Compiler Engineer Intern (3 months)**, *NVIDIA*, Redmond, WA, USA.
During this internship, I was working on an embedded DSL, IR and compiler for optimizing deep learning applications. I focused especially on CUDA code generation for highly optimized matrix multiplication algorithms. My work on this project simplified managing the deep compute and memory hierarchy on modern GPUs and enabled using program synthesis for design space exploration.

02/2018 – 04/2018 **Visiting researcher (2 months)**, *University of Glasgow*, Glasgow, UK.
Funded by HPC-Europa3
During this visit, I investigated the implementation of performance portable HPC applications with Lift including the automatic fusion of multiple compute kernels using rewrite rules. I focused on geometric multigrid methods and the Irish Centre for High-End Computing (ICHEC) supported my visit by providing access to their GPU hardware.

07/2017 – 09/2017 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by HiPEAC
During this visit, I combined modern auto-tuning techniques with the current Lift code generator. I also evaluated Lift's functional compilation approach compared to state-of-the-art polyhedral compilation. A paper describing the results of this and our previous collaborations has won the *best paper award* at the prestigious International Symposium on Code Generation and Optimization (CGO) [2]

02/2017 – 03/2017 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by EuroLab-4-HPC
During this visit, I extended the Lift compiler, developed at the University of Edinburgh, to enable automatic exploration of stencil-specific optimizations.

04/2016 – 05/2016 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by EuroLab-4-HPC
During this visit, I extended the Lift compiler to enable the generation of high-performance stencil code for GPUs.

09/2015 **Visiting researcher (3 weeks)**, *HUST University*, Wuhan, China.
Funded by the EC's 7th Framework Programme MONICA for accelerating the transfer and deployment of research knowledge between European countries and China. During this visit, I implemented an experimental setup for SDN-based multicast, and prepared a research paper on this topic [4]

Publications

2019 [1] P. M. Phothilimthana, A. S. Elliott, A. Jangda, **B. Hagedorn**, H. Barthels, R. Bodik, and V. Grover. "Swizzle Inventor: Data Movement Synthesis for GPU Kernels". In: *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS (under review)*. 2019.

2018 [2] **B. Hagedorn**, L. Stoltzfus, M. Steuwer, S. Gorlatch, and C. Dubach. "High Performance Stencil Code Generation with Lift". In: *Proceedings of the 2018 International Symposium on Code Generation and Optimization, CGO 2018, Vienna, Austria (**Best Paper Award**)*. 2018, pp. 100–112. DOI: 10.1145/3168824.

2017 [3] **B. Hagedorn**, M. Steuwer, and S. Gorlatch. "A Transformation-Based Approach for Developing High-Performance GPU Programs". In: *Perspectives of System Informatics - 12th International Andrei Ershov Informatics Conference, PSI 2017*. Lecture Notes in Computer Science. Springer, 2017.

2016 [4] T. Humernbrum, **B. Hagedorn**, and S. Gorlatch. "Towards Efficient Multicast Communication in Software-Defined Networks". In: *2016 IEEE 36th International Conference on Distributed Computing Systems Workshops (ICDCSW)*. June 2016, pp. 106–113. DOI: 10.1109/ICDCSW.2016.15.

2015 [5] M. Haidl, **B. Hagedorn**, and S. Gorlatch. "Programming GPUs with C++14 and Just-In-Time Compilation". In: *Parallel Computing: On the Road to Exascale, Proceedings of the International Conference on Parallel Computing, ParCo 2015, 1-4 September 2015, Edinburgh, Scotland, UK*. 2015, pp. 247–256.

[6] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. "High Quality Information Delivery: Demonstrating the Web in Your Pocket for Cineast Tourists". In: *Proceedings of the BTW 2015*. 2015, pp. 667–670.

2014 [7] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. "Implementing the WiPo architecture". In: *E-Commerce and Web Technologies*. Springer, 2014, pp. 1–12.

Presentations

10/2018 Talk: *High Performance Geometric Multigrid Operations in Lift*.
HPC-Europa3 Transnational Access Meeting (TAM), Edinburgh, UK

04/2018 Talk: *High Performance Stencil Code Generation with Lift*.
Workshop on Compilers for Parallel Computing (CPC), Dublin, Ireland

04/2018 Invited Talk: *High Performance Stencil Code Generation with Lift*.
Dependable Systems Group, Heriot-Watt University Edinburgh, UK

04/2018 Tutorial: *Lift: Performance Portable Parallel Code Generation via Rewrite Rules*.
International Symposium on Performance Analysis of Systems and Software (ISPASS), Belfast, UK

03/2018 Talk: *High Performance Stencil Code Generation with Lift*.
Scottish Programming Language Seminar (SPLS), University of Glasgow, UK

02/2018 Talk: *High Performance Stencil Code Generation with Lift*.
International Symposium on Code Generation and Optimization (CGO), Vienna, Austria

02/2018 Invited Talk: *High Performance Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

03/2017 Invited Talk: *Performance Portable Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

Research Projects

I have been actively contributing to the following research projects.

since 04/2016 **Lift**, *A Novel Approach to Achieving Performance Portability on Accelerators*.
Ongoing research, *www.lift-project.org*
I am one of the main contributors focusing on implementing stencil computations in Lift. I extended the functional Lift IR and enabled the generation of efficient OpenCL kernels for stencil-based applications. The Lift project is a novel approach to generate high-performance OpenCL kernels from high-level functional programs.

04/2015 **PACXX**, *Programming Accelerators with C++*.
Ongoing research
I developed an LLVM analysis pass for the PACXX compiler and ported HPC applications to the PACXX programming model resulting in a publication [5]. PACXX is a unified HPC programming model for programming accelerators (GPUs etc.) using pure C++ by implementing a custom compiler (based on the LLVM framework) and a runtime system.

10/2013 **OFERTIE EU Project**, *OpenFlow Experiment in Real-Time Internet Edutainment*.
- 09/2014 I configured the SDN testbed at the University of Münster, conducted several SDN-based experiments and extended the monitoring interface of the Real-Time Framework (RTF) The OFERTIE project aims to use SDN approaches to improve delivery of Real-Time Online Interactive Applications (ROIA).

Attended Academic Events

2018 TAM - *HPC-Europa3 Transnational Access Meeting*, Edinburgh, UK

CPC - *20th Workshop on Compilers for Parallel Computing*, Dublin, Ireland

ISPASS - *International Symposium on Performance Analysis of Systems and Software*, Belfast, UK

SPLS - *Scottish Programming Languages Seminar*, Glasgow, UK

CGO - *International Symposium on Code Generation and Optimization*, Vienna, Austria

2017 Compiler and Programming Language Summit (organized by Google), Munich, Germany

ACASES Summer School (organized by HiPEAC) - *Thirteenth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems*, Fiuggi, Italy

PUMPS Summer School - *Eighth edition of the Programming and Tuning Massively Parallel Systems summer school*, Barcelona, Spain

SPLS - *Scottish Programming Languages Seminar*, St. Andrews, UK

2016 HLPP conference - *9th International Symposium on High-Level Parallel Programming and Applications*, Münster, Germany

UKMAC - *UK Many-Core Developer Conference*, Edinburgh, UK

WadlerFest/LFCS30 - *30th Aniversery of the Laboratory for Foundations of Computer Science*, Edinburgh, UK

2015 PRACE Course - *Advanced Parallel Programming with MPI and OpenMP*, Jülich, Germany

PRACE Course - *Node-Level Performance Engineering*, Stuttgart, Germany

Reviewer

2019 CGO 2019 artifact evaluation commitee

2018 CGO 2018 artifact evaluation commitee

LCTES 2018 artifact evaluation commitee

2016 – 2018 I have been active as an external reviewer for the following conferences and journals: *Principles and Practice of Parallel Programming (PPoPP), the International Parallel and Distributed Processing Symposium (IPDPS), the International Journal of Parallel Programming (IJPP)*, the *Journal of Supercomputing*, the journal *Concurrency and Computation: Practice and Experience*, the Journal of Applied Geophysics (APPGEO), the Parallel Computing Technologies (PaCT), the Parallel Computing Conference (ParCo), the UKRCON and the PSI.

Teaching

Winter 2019 Teaching assistant for the course: *Operating systems*

Winter 2019 Teaching assistant for the course: *Introduction to programming with Java and Haskell*

Summer 2018 Course design and Lecturer: *Introduction to programming with C and C++*

Summer 2018 Teaching assistant for the course: *Parallel Programming: Multi-Core and GPU*

Winter 2017 Teaching assistant for the course: *Operating systems*

Winter 2017 Teaching assistant for the course: *Introduction to programming with Java and Racket*

Summer 2017 Course design and Lecturer: *Introduction to programming with C and C++*

Summer 2017 Supervised a student project: *Automatic program optimization for modern many-core systems*

Winter 2016 Teaching assistant for the course: *Operating systems*

Winter 2015 Student assistant for the course: *Operating systems*

Summer 2015 Student assistant for the course: *Computer architectures*

Winter 2014 Student assistant for the course: *Operating systems*

Supervised Undergraduate and Master Students

since 02/2018 Johannes Lenfers (Master): *Implementing Compiler Auto-Tuning Strategies for Design Space Exploration of Lift Programs*

02/2018 Bastian Köpcke (Master): *Efficient GPU Code Generation for FFT Computations in Lift*

01/2018 Martin Lücke (Master): *Efficient Implementation and Optimization of Geometric Multi-Grid Operations in the Lift Framework*

03/2018 Clemens Hesse-Edenfeld (Undergraduate): *Integrating Performance Models for Stencil Computations in Lift*

03/2018 Alexander Dirk Holthaus (Master): *Development of an Analytical Tool for Visualizing and Optimizing Memory Accesses in GPU Kernels*

03/2018 Maurice Heine (Undergraduate): *Implementation of a Visualization Tool for Lift Programs*