

Bastian Hagedorn

Einsteinstraße 62
48149 Münster, Germany
✉ b.hagedorn@wwu.de

University Education

- since 2016 **Ph.D. studies**, *University of Münster*, Münster, Germany.
Supervisor: Prof. Sergei Gorlatch, Prof. Michel Steuwer (University of Glasgow)
Tackling ambitious problems ranging from artificial intelligence to autonomous driving creates significantly increasing demands in computational power as well as efficient software. I develop novel compilation techniques which will allow to generate high-performance programs for the rapidly changing landscape of specialized hardware accelerators. I am especially interested in performance optimizations encoded as semantics preserving rewrite rules whose application is controlled by a novel strategy language. By combining high-level programming abstractions with application and hardware knowledge, I aim to shape the next generation of optimizing compilers for today's and tomorrow's hardware.
- 2014 – 2016 **Master of Science in computer science**, *University of Münster*, Münster, Germany,
Final grade in computer science: excellent with distinction (90%).
Thesis title: An Extension of a Functional Intermediate Language for Parallelizing Stencil Computations and its Optimizing GPU Implementation Using OpenCL.
Grade for thesis: excellent
- 2011 – 2014 **Bachelor of Science in computer science**, *University of Münster*, Münster, Germany,
Final grade in computer science: very good (81%).
Thesis title: Implementation of a Multicast Module for the Floodlight SDN-Controller
Grade for thesis: excellent

Awards and Grants

- 09/2019 **Heidelberg Laureate Forum 2019**, *Invited Participation*, Invited to attend this highly prestigious forum with laureates of ACM A.M. Turing Award, Abel Prize, Fields Medal and Nevanlinna Prize. **Only 100 spaces** available for computer science.
- 12/2018 **NVIDIA Graduate Fellowship 2019**, 50.000\$, One of ten recipients world wide, selected as the only student from a European university.
- 02/2018 **Best Paper Award**, *ACM International Symposium on Code Generation and Optimization (CGO) 2018*, Selected as the best paper out of 103 submissions.
- since 2016 **Four Travel Grants**, *HPC-Europa3*, *HiPEAC*, 2x *EuroLab-4-HPC*, total approx. 12.500€.

Research Visits

- 11/2019 **Visiting researcher (2 weeks)**, *University of Glasgow*, Glasgow, UK.
During this visit, I prepared a publication about Elevate. We especially investigated how to implement TVM's scheduling language in terms of composable rewrite rules using Elevate.
- 12/2018 **Deep Learning Compiler Engineer (7 months)**, *NVIDIA*, Würselen, Germany.
- 06/2019 During this time, I extended the IR developed during my Internship in the US, focusing on code generation targeting NVIDIA's tensor cores in order to accelerate low-precision deep learning applications on GPUs.

- 07/2018 **Deep Learning Compiler Engineer Intern (3 months)**, NVIDIA, Redmond, WA, USA.
 – 09/2018 During this internship, I was working on an embedded DSL, IR and compiler for optimizing deep learning applications. I focused especially on CUDA code generation for highly optimized matrix multiplication algorithms. My work on this project simplified managing the complex compute and memory hierarchy on modern GPUs and enabled using program synthesis for design space exploration.
- 02/2018 **Visiting researcher (2 months)**, University of Glasgow, Glasgow, UK.
 – 04/2018 Funded by HPC-Europa3
 During this visit, I investigated the implementation of performance portable HPC applications with Lift including the automatic fusion of multiple compute kernels using rewrite rules. I focused on geometric multigrid methods. The Irish Centre for High-End Computing (ICHEC) supported my visit by providing access to their GPU hardware.
- 07/2017 **Visiting researcher (2 months)**, University of Edinburgh, Edinburgh, UK.
 – 09/2017 Funded by HiPEAC
 During this visit, I combined modern auto-tuning techniques with the current Lift code generator. I also evaluated Lift’s functional compilation approach compared to state-of-the-art polyhedral compilation. A paper describing the results of this and our previous collaborations has won the *best paper award* at the prestigious ACM International Symposium on Code Generation and Optimization (CGO) [4]
- 02/2017 **Visiting researcher (2 months)**, University of Edinburgh, Edinburgh, UK.
 – 03/2017 Funded by EuroLab-4-HPC
 During this visit, I extended the Lift compiler, developed at the University of Edinburgh, to enable automatic exploration of stencil-specific optimizations.
- 04/2016 **Visiting researcher (2 months)**, University of Edinburgh, Edinburgh, UK.
 – 05/2016 Funded by EuroLab-4-HPC
 During this visit, I extended the Lift compiler to enable the generation of high-performance stencil code for GPUs.
- 09/2015 **Visiting researcher (3 weeks)**, HUST University, Wuhan, China.
 Funded by the EC’s 7th Framework Programme MONICA for accelerating the transfer and deployment of research knowledge between European countries and China. During this visit, I implemented an experimental setup for SDN-based multicast, and prepared a research paper on this topic [6]

Publications

- 2020 [1] T. Remmelg, **B. Hagedorn**, L. Li, M. Steuwer, S. Gorlatch, and C. Dubach. “High-Level Hardware Feature Extraction for GPU Performance Prediction of Stencils”. In: *Proceedings of the Annual Workshop on General Purpose Processing Using Graphics Processing Unit (GPGPU)*. 2020.
- 2019 [2] L. Stoltzfus, **B. Hagedorn**, M. Steuwer, S. Gorlatch, and C. Dubach. “Tiling Optimizations for Stencil Computations Using Rewrite Rules in Lift”. In: *ACM Trans. Archit. Code Optim.* 16.4 (Dec. 2019).
- [3] P. M. Phothisilimthana, A. S. Elliott, A. Wang, A. Jangda, **B. Hagedorn**, H. Barthels, S. J. Kaufman, V. Grover, E. Torlak, and R. Bodik. “Swizzle Inventor: Data Movement Synthesis for GPU Kernels”. In: *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS*. 2019.
- 2018 [4] **B. Hagedorn**, L. Stoltzfus, M. Steuwer, S. Gorlatch, and C. Dubach. “High Performance Stencil Code Generation with Lift”. In: *Proceedings of the 2018 International*

Symposium on Code Generation and Optimization, CGO 2018, Vienna, Austria (Best Paper Award, Most cited paper of CGO'18). 2018, pp. 100–112. DOI: 10.1145/3168824.

- 2017 [5] **B. Hagedorn**, M. Steuwer, and S. Gorlatch. “A Transformation-Based Approach for Developing High-Performance GPU Programs”. In: *Perspectives of System Informatics - 12th International Andrei Ershov Informatics Conference, PSI 2017*. Lecture Notes in Computer Science. Springer, 2017.
- 2016 [6] T. Humernbrum, **B. Hagedorn**, and S. Gorlatch. “Towards Efficient Multicast Communication in Software-Defined Networks”. In: *2016 IEEE 36th International Conference on Distributed Computing Systems Workshops (ICDCSW)*. June 2016, pp. 106–113. DOI: 10.1109/ICDCSW.2016.15.
- 2015 [7] M. Haidl, **B. Hagedorn**, and S. Gorlatch. “Programming GPUs with C++14 and Just-In-Time Compilation”. In: *Parallel Computing: On the Road to Exascale, Proceedings of the International Conference on Parallel Computing, ParCo 2015, 1-4 September 2015, Edinburgh, Scotland, UK*. 2015, pp. 247–256.
- [8] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. “High Quality Information Delivery: Demonstrating the Web in Your Pocket for Cineast Tourists”. In: *Proceedings of the BTW 2015*. 2015, pp. 667–670.
- 2014 [9] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. “Implementing the WiPo architecture”. In: *E-Commerce and Web Technologies*. Springer, 2014, pp. 1–12.

Presentations

- 01/2020 Talk: *Elevate - A Language for Describing Optimization Strategies*.
NVIDIA, Redmond WA, USA
- 04/2019 Talk: *High Performance Matrix Multiplication using Tensor Cores*.
NVIDIA, Redmond WA, USA
- 03/2019 Talk: *Elevate - A Language for Expressing Optimization Strategies*.
Scottish Programming Language Seminar (SPLS), University of St. Andrews, UK
- 12/2018 Talk: *High Performance Code Generation for Matrix Multiplication and Machine Learning*.
NVIDIA, Redmond WA, USA
- 10/2018 Talk: *High Performance Geometric Multigrid Operations in Lift*.
HPC-Europa3 Transnational Access Meeting (TAM), Edinburgh, UK
- 04/2018 Talk: *High Performance Stencil Code Generation with Lift*.
Workshop on Compilers for Parallel Computing (CPC), Dublin, Ireland
- 04/2018 Invited Talk: *High Performance Stencil Code Generation with Lift*.
Dependable Systems Group, Heriot-Watt University Edinburgh, UK
- 04/2018 Tutorial: *Lift: Performance Portable Parallel Code Generation via Rewrite Rules*.
International Symposium on Performance Analysis of Systems and Software (ISPASS), Belfast, UK
- 03/2018 Talk: *High Performance Stencil Code Generation with Lift*.
Scottish Programming Language Seminar (SPLS), University of Glasgow, UK
- 02/2018 Talk: *High Performance Stencil Code Generation with Lift*.
International Symposium on Code Generation and Optimization (CGO), Vienna, Austria

- 02/2018 Invited Talk: *High Performance Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK
- 03/2017 Invited Talk: *Performance Portable Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

Research Projects

I have been actively contributing to the following research projects.

- since **Elevate**, *A Language for Describing Program Transformations*.
07/2019 Ongoing research, <https://github.com/elevate-lang>
I am leading the development of Elevate, a language enabling the specification of composable program transformations. Using simple combination and traversal operators, Elevate allows to build domain-specific program optimizations as semantics preserving rewrite rules for arbitrary ASTs.
- since **Lift**, *A Novel Approach to Achieving Performance Portability on Accelerators*.
04/2016 Ongoing research, www.lift-project.org
I am one of the main contributors focusing on implementing stencil computations in Lift. I extended the functional Lift IR and enabled the generation of efficient OpenCL kernels for stencil-based applications. The Lift project is a novel approach to generate high-performance OpenCL kernels from high-level functional programs.
- 04/2015 **PACXX**, *Programming Accelerators with C++*.
I developed an LLVM analysis pass for the PACXX compiler and ported HPC applications to the PACXX programming model resulting in a publication [7]. PACXX is a unified HPC programming model for programming accelerators (GPUs etc.) using pure C++ by implementing a custom compiler (based on the LLVM framework) and a runtime system.
- 10/2013 **OFERTIE EU Project**, *OpenFlow Experiment in Real-Time Internet Edutainment*.
- 09/2014 I configured the SDN testbed at the University of Münster, conducted several SDN-based experiments and extended the monitoring interface of the Real-Time Framework (RTF) The OFERTIE project aims to use SDN approaches to improve delivery of Real-Time Online Interactive Applications (ROIA).

Reviewer

- 2020 CGO 2020 artifact evaluation chair
ASPLOS 2020 artifact evaluation committee
- 2019 CGO 2019 artifact evaluation committee
- 2018 CGO 2018 artifact evaluation committee
LCTES 2018 artifact evaluation committee
- since 2016 I have been active as an external reviewer for the following conferences and journals: *Principles and Practice of Parallel Programming (PPoPP)*, the *International Parallel and Distributed Processing Symposium (IPDPS)*, the *International Journal of Parallel Programming (IJPP)*, the *Journal of Supercomputing*, the journal *Concurrency and Computation: Practice and Experience*, the *Journal of Applied Geophysics (APPGEO)*, the *Parallel Computing Technologies (PaCT)*, the *Parallel Computing Conference (ParCo)*

Teaching

- Winter '20 Teaching assistant for the course: *Parallel Systems*
- Winter '20 Supervised a student project: *Developing a CUDA backend for Lift targeting TensorCores*

- Winter '19 Teaching assistant for the course: *Operating systems*
- Winter '19 Teaching assistant for the course: *Introduction to programming with Java and Haskell*
- Summer '18 Course design and Lecturer: *Introduction to programming with C and C++*
- Summer '18 Teaching assistant for the course: *Parallel Programming: Multi-Core and GPU*
- Winter '17 Teaching assistant for the course: *Operating systems*
- Winter '17 Teaching assistant for the course: *Introduction to programming with Java and Racket*
- Summer '17 Course design and Lecturer: *Introduction to programming with C and C++*
- Summer '17 Supervised a student project: *Automatic program optimization for modern many-core systems*
- Winter '16 Teaching assistant for the course: *Operating systems*
- Winter '15 Student assistant for the course: *Operating systems*
- Summer '15 Student assistant for the course: *Computer architectures*
- Winter '14 Student assistant for the course: *Operating systems*

Supervised Undergraduate and Master Students

- 12/2018 Johannes Lenfers (Master): *Implementing Compiler Auto-Tuning Strategies for Design Space Exploration of Lift Programs*
- 02/2018 Bastian Köpcke (Master): *Efficient GPU Code Generation for FFT Computations in Lift*
- 01/2018 Martin Lücke (Master): *Efficient Implementation and Optimization of Geometric Multi-Grid Operations in the Lift Framework*
- 03/2018 Clemens Hesse-Edenfeld (Undergraduate): *Integrating Performance Models for Stencil Computations in Lift*
- 03/2018 Alexander Dirk Holthaus (Master): *Development of an Analytical Tool for Visualizing and Optimizing Memory Accesses in GPU Kernels*
- 03/2018 Maurice Heine (Undergraduate): *Implementation of a Visualization Tool for Lift Programs*