Bastian Hagedorn

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University Education

since 2016 **Ph.D. studies**, *University of Münster*, Münster, Germany.
Supervisor: Prof. Sergei Gorlatch
My PhD research focuses on performance-portable stencil code generation using Lift by tackling the growing problem of achieving high efficiency when programming the ever changing hardware of today and tomorrow. The Lift project has recently emerged as a promising compilation framework to achieve performance portability. Lift defines a small set of reusable parallel primitives that DSL writers can easily build upon. Lift's key novelty is its ability to automatically explore the optimization space by using as a system of extensible rewrite rules which encode specific optimizations.

2014 – 2016 **Master of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: excellent with distinction (90%)*.
Thesis title: An Extension of a Functional Intermediate Language for Parallelizing Stencil Computations and its Optimizing GPU Implementation Using OpenCL.
Grade for thesis: excellent

2011 – 2014 **Bachelor of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: very good (81%)*.
Thesis title: Implementation of a Multicast Module for the Floodlight SDN-Controller
Grade for thesis: excellent

Research Visits

02/2018 – 04/2018 **Visiting researcher (2 months)**, *University of Glasgow*, Glasgow, UK.
Funded by HPC-Europa3
During this visit, I investigate the implementation of performance portable HPC applications with Lift. I will focus on two HPC applications: room acoustics simulations and ground penetrating radar. The Irish Centre for High-End Computing (ICHEC) is supporting my visit by providing access to their GPU hardware and I closely collaborate with the entire Lift team at the Universities of Glasgow and Edinburgh.

07/2017 – 09/2017 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by HiPEAC
During this visit, I combined modern auto-tuning techniques with the current Lift code generator. I also evaluated Lift's functional compilation approach compared to state-of-the-art polyhedral compilation. A paper describing the results of this and our previous collaborations is nominated for the best paper award at the prestigious International Symposium on Code Generation and Optimization (CGO) [1]

02/2017 – 03/2017 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by the EuroLab-4-HPC
During this visit, I extended the Lift compiler, developed at the University of Edinburgh, to enable automatic exploration of stencil-specific optimizations.

04/2016 – 05/2016 **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by the EuroLab-4-HPC
During this visit, I extended the Lift compiler to enable the generation of high-performance stencil code for GPUs.

09/2015 **Visiting researcher (3 weeks)**, *HUST University*, Wuhan, China.
Funded by the EC's 7th Framework Programme MONICA for accelerating the transfer and deployment of research knowledge between European countries and China. During this visit, I implemented an experimental setup for SDN-based multicast, and prepared a research paper on this topic [3]

Publications

2018 [1] **B. Hagedorn**, L. Stoltzfus, M. Steuwer, S. Gorlatch, and C. Dubach. "High Performance Stencil Code Generation with Lift". In: *International Symposium on Code Generation and Optimization, CGO 2018 (**Best Paper Finalist**)*. 2018.

2017 [2] **B. Hagedorn**, M. Steuwer, and S. Gorlatch. "A Transformation-Based Approach for Developing High-Performance GPU Programs". In: *Perspectives of System Informatics - 12th International Andrei Ershov Informatics Conference, PSI 2017*. Lecture Notes in Computer Science. Springer, 2017.

2016 [3] T. Humernbrum, **B. Hagedorn**, and S. Gorlatch. "Towards Efficient Multicast Communication in Software-Defined Networks". In: *2016 IEEE 36th International Conference on Distributed Computing Systems Workshops (ICDCSW)*. June 2016, pp. 106–113. DOI: 10.1109/ICDCSW.2016.15.

2015 [4] M. Haidl, **B. Hagedorn**, and S. Gorlatch. "Programming GPUs with C++14 and Just-In-Time Compilation". In: *Parallel Computing: On the Road to Exascale, Proceedings of the International Conference on Parallel Computing, ParCo 2015, 1-4 September 2015, Edinburgh, Scotland, UK*. 2015, pp. 247–256.

[5] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. "High Quality Information Delivery: Demonstrating the Web in Your Pocket for Cineast Tourists". In: *Proceedings of the BTW 2015*. 2015, pp. 667–670.

2014 [6] F. Stahl, A. Godde, **B. Hagedorn**, B. Köpcke, M. Rehberger, and G. Vossen. "Implementing the WiPo architecture". In: *E-Commerce and Web Technologies*. Springer, 2014, pp. 1–12.

Presentations

03/2018 Talk: *High Performance Stencil Code Generation with Lift*.
Scottish Programming Language Seminar (SPLS), University of Glasgow, UK

02/2018 Talk: *High Performance Stencil Code Generation with Lift*.
International Symposium on Code Generation and Optimization (CGO), Vienna, Austria

02/2018 Invited Talk: *High Performance Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

03/2017 Invited Talk: *Performance Portable Stencil Code Generation with Lift*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

Research Projects

I have been actively contributing to the following research projects.

since 04/2016 **Lift**, *A Novel Approach to Achieving Performance Portability on Accelerators*.
Ongoing research, *www.lift-project.org*
I am one of the main contributors focusing on implementing stencil computations in Lift. I extended the functional Lift IR and enabled the generation of efficient OpenCL kernels for stencil-based applications. The Lift project is a novel approach to generate high-performance OpenCL kernels from high-level functional programs.

04/2015 **PACXX**, *Programming Accelerators with C++*.
Ongoing research
I developed an LLVM analysis pass for the PACXX compiler and ported HPC applications to the PACXX programming model resulting in a publication [4]. PACXX is a unified HPC programming model for programming accelerators (GPUs etc.) using pure C++ by implementing a custom compiler (based on the LLVM framework) and a runtime system.

10/2013 - 09/2014 **OFERTIE EU Project**, *OpenFlow Experiment in Real-Time Internet Edutainment*.
I configured the SDN testbed at the University of Münster, conducted several SDN-based experiments and extended the monitoring interface of the Real-Time Framework (RTF) The OFERTIE project aims to use SDN approaches to improve delivery of Real-Time Online Interactive Applications (ROIA).

Attended Academic Events

2018 SPLS - *Scottish Programming Languages Seminar*, Glasgow, UK

CGO - *International Symposium on Code Generation and Optimization*, Vienna, Austria

2017 Compiler and Programming Language Summit (organized by Google), Munich, Germany

ACASES Summer School (organized by HiPEAC) - *Thirteenth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems*, Fiuggi, Italy

PUMPS Summer School - *Eighth edition of the Programming and Tuning Massively Parallel Systems summer school*, Barcelona, Spain

SPLS - *Scottish Programming Languages Seminar*, St. Andrews, UK

2016 HLPP conference - *9th International Symposium on High-Level Parallel Programming and Applications*, Münster, Germany

UKMAC - *UK Many-Core Developer Conference*, Edinburgh, UK

WadlerFest/LCFS30 - *30th Aniversery of the Laboratory for Foundations of Computer Science*, Edinburgh, UK

2015 PRACE Course - *Advanced Parallel Programming with MPI and OpenMP*, Jülich, Germany

PRACE Course - *Node-Level Performance Engineering*, Stuttgart, Germany

Reviewer

2018 CGO 2018 artifact evaluation commitee

2016 – 2018 I have been active as an external reviewer for the following conferences and journals: *Principles and Practice of Parallel Programming (PPoPP), the International Journal of Parallel Programming (IJPP)*, the *Journal of Supercomputing*, the journal *Concurrency and Computation: Practice and Experience*, the Journal of Applied Geophysics (APPGEO), the Parallel Computing Technologies (PaCT), the Parallel Computing Conference (ParCo), the UKRCON and the PSI.

Teaching

Summer 2018	Course design and Lecturer: *Introduction to programming with C and C++*
Summer 2018	Teaching assistant for the course: *Parallel Programming: Multi-Core and GPU*
Winter 2017	Teaching assistant for the course: *Operating systems*
Winter 2017	Teaching assistant for the course: *Introduction to programming with Java and Racket*
Summer 2017	Course design and Lecturer: *Introduction to programming with C and C++*
Summer 2017	Supervised a student project: *Automatic program optimization for modern many-core systems*
Winter 2016	Teaching assistant for the course: *Operating systems*
Winter 2015	Student assistant for the course: *Operating systems*
Summer 2015	Student assistant for the course: *Computer architectures*
Winter 2014	Student assistant for the course: *Operating systems*

Supervised Undergraduate and Master Students

since 02/2018	Johannes Lenfers (Master): *Implementing Compiler Auto-Tuning Strategies for Design Space Exploration of Lift Programs*
since 02/2018	Bastian Köpcke (Master): *Efficient GPU Code Generation for FFT Computations in Lift*
since 01/2018	Maurice Heine (Undergraduate): *Implementation of a Visualization Tool for Lift Programs*
since 01/2018	Martin Lücke (Master): *Efficient Implementation and Optimization of Geometric Multi-Grid Operations in the Lift Framework*

Technical Skills

Programming Languages	**Scala, C/C++, Java**. Experiences: Stencil support for Lift compiler (Scala), Multicast Module for the Floodlight SDN Controller (Java), Measurement library for OpenCL (C++), Implementation of the WiPo architecture (Java), Monitoring interface extension of RTF (C++)
Parallel Programming	**OpenCL, CUDA, OpenMP**. Experiences: Performance portability evaluation of OpenCL Kernels on Intel Xeon (Phi) and NVIDIA Tesla. JIT compilation of a DSL using LLVM and CUDA Driver API
Compiler Tools	**LLVM**. Experiences: Analysis Pass for the PACXX Compiler, Compiler frontend for self-defined DSL for data parallel applications based on algorithmic skeletons