Bastian Hagedorn

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University Education

since 2016   **Ph.D. studies**, *University of Münster*, Münster, Germany.
Supervisor: Prof. Sergei Gorlatch
Main research interests: High-level programming abstractions for high-performance computing applications, Programming of modern multi- and many-core processors

2014 – 2016   **Master of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: excellent with distinction (90%)*.
Thesis title: An Extension of a Functional Intermediate Language for Parallelizing Stencil Computations and its Optimizing GPU Implementation Using OpenCL.
In this thesis, I extended the LIFT compiler to enable the generation of high-performance stencil code for GPUs from a high-level functional program *Grade for thesis: excellent*

2011 – 2014   **Bachelor of Science in computer science**, *University of Münster*, Münster, Germany, *Final grade in computer science: very good (81%)*.
Thesis title: Implementation of a Multicast Module for the Floodlight SDN-Controller
In this thesis, I extended the Floodlight network controller with a module which enables a novel apporach to multicast communication in software-defined networks. *Grade for thesis: excellent*

Research Visits

02/2017 – 03/2017   **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by the EuroLab-4-HPC
During this visit, I extended the LIFT compiler which is developed at the University of Edinburgh to enable performance-portable generation of stencil code across several GPU architectures.

04/2016 – 05/2016   **Visiting researcher (2 months)**, *University of Edinburgh*, Edinburgh, UK.
Funded by the EuroLab-4-HPC
During this visit, I extended the LIFT compiler to enable the generation of high-performance stencil code for GPUs.

12/2015   **PRACE course participant**, *Jülich Supercomputing Centre*, Jülich, Germany.
Course: Advanced Parallel Programming with MPI and OpenMP
Content: Nonblocking Communication, Virtual Topologies, OpenMP-4.0 Extensions, Parallel programming models on hybrid systems

09/2015   **Visiting researcher (3 weeks)**, *HUST University*, Wuhan, China.
Funded by the EC's 7th Framework Programme MONICA for accelerating the transfer and deployment of research knowledge between European countries and China. During this visit, I implemented an experimental setup for SDN-based multicast, and prepared a research paper on this topic which is about to appear.

07/2015 **PRACE course participant**, *High Performance Computing Centre Suttgart*, Stuttgart, Germany.
Course: Node-Level Performance Engineering
Content: Parallel hardware architectures, Roofline performance model, benchmarking and profiling tools for high-performance systems and applications

Presentations

03/2017 Invited Talk: *Performance Portable Stencil Code Generation with LIFT*.
Research Group on Compiler and Architecture Design, University of Edinburgh, UK

Research Projects

04/2016 **LIFT**, *A Novel Approach to Achieving Performance Portability on Accelerators*.
Ongoing research, *www.lift-project.org*
The Lift project is a novel approach to generate high-performance OpenCL kernels from high-level functional programs. My contribution to the project focuses on stencil computations. I extended the functional LIFT IR and enabled the generation of efficient OpenCL kernels for stencil-based applications.

04/2015 **PACXX**, *Programming Accelerators with C++*.
Ongoing research
PACXX is a unified HPC programming model for programming accelerators (GPUs etc.) using pure C++ by implementing a custom compiler (based on the LLVM framework) and a runtime system. I developed an analysis pass for the PACXX compiler and ported HPC applications to the PACXX programming model resulting in a publication [1].

10/2013 - **OFERTIE EU Project**, *OpenFlow Experiment in Real-Time Internet Edutainment*.
09/2014 The OFERTIE project aims to use SDN approaches to improve delivery of Real-Time Online Interactive Applications (ROIA). As a student assistant, I configured the SDN testbed at the University of Münster, conducted several SDN-based experiments and extended the monitoring interface of the Real-Time Framework (RTF)

Teaching

Summer 2017 Lecturer for the course: *Introduction to programming with C and C++*

Summer 2017 Supervised a student project: *Automatic program optimization for modern many-core systems*

Winter 2016 Teaching assistant for the course: *Operating systems*

Winter 2015 Student assistant for the course: *Operating systems*

Summer 2015 Student assistant for the course: *Computer architectures*

Winter 2014 Student assistant for the course: *Operating systems*

Technical Skills

Programming **Scala, C/C++, Java**.
Languages Experiences: Stencil support for Lift compiler (Scala), Multicast Module for the Floodlight SDN Controller (Java), Measurement library for OpenCL (C++), Implementation of the WiPo architecture (Java), Monitoring interface extension of RTF (C++)

Parallel **OpenCL, CUDA, OpenMP**.
Programming Experiences: Performance portability evaluation of OpenCL Kernels on Intel Xeon (Phi) and NVIDIA Tesla. JIT compilation of a DSL using LLVM and CUDA Driver API

Compiler	**LLVM**.
Tools	Experiences: Analysis Pass for the PACXX Compiler, Compiler frontend for self-defined DSL for data parallel applications based on algorithmic skeletons
OS	**Linux, Mac OS X**.

Reviewer

2016 – 2017 I have been active as an external reviewer for the following conferences and journals: *International Journal of Parallel Programming (IJPP)*, the *Journal of Supercomputing*, the journal *Concurrency and Computation: Practice and Experience*, the Parallel Computing Technologies (PaCT), the Parallel Computing Conference (ParCo), the UKRCON and the PSI.

Attended Conferences

2017 SPLS - *Scottish Programming Languages Seminar*, Edinburgh, UK

2016 HLPP - *9th International Symposium on High-Level Parallel Programming and Applications*, Münster, Germany

2016 UKMAC - *UK Many-Core Developer Conference*, Edinburgh, UK

2016 WadlerFest/LCFS30 - *30th Aniversery of the Laboratory for Foundations of Computer Science*, Edinburgh, UK

Publications

[1] Michael Haidl, Bastian Hagedorn, and Sergei Gorlatch. Programming GPUs with C++ 14 and just-in-time compilation. volume 27, page 247. IOS Press, 2016.

[2] T. Humernbrum, B. Hagedorn, and S. Gorlatch. Towards efficient multicast communication in software-defined networks. In *2016 IEEE 36th International Conference on Distributed Computing Systems Workshops (ICDCSW)*, pages 106–113, June 2016.

[3] Florian Stahl, Adrian Godde, Bastian Hagedorn, Bastian Köpcke, Martin Rehberger, and Gottfried Vossen. Implementing the WiPo architecture. In *E-Commerce and Web Technologies*, pages 1–12. Springer, 2014.

[4] Florian Stahl, Adrian Godde, Bastian Hagedorn, Bastian Köpcke, Martin Rehberger, and Gottfried Vossen. High quality information delivery: Demonstrating the web in your pocket for cineast tourists. In *Proceedings of the BTW 2015*, pages 667–670, 2015.

[5] Florian Stahl, Adrian Godde, Bastian Hagedorn, Bastian Köpcke, Martin Rehberger, and Gottfried Vossen. Implementing the WiPo architecture. ERCIS Working Papers 20, Westfälsche Wilhelms-Universität Münster (WWU), 2014.