
STM32
CubeMX

1. Description

1.1. Project

Project Name	OTB-Backplane
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	06/01/2021

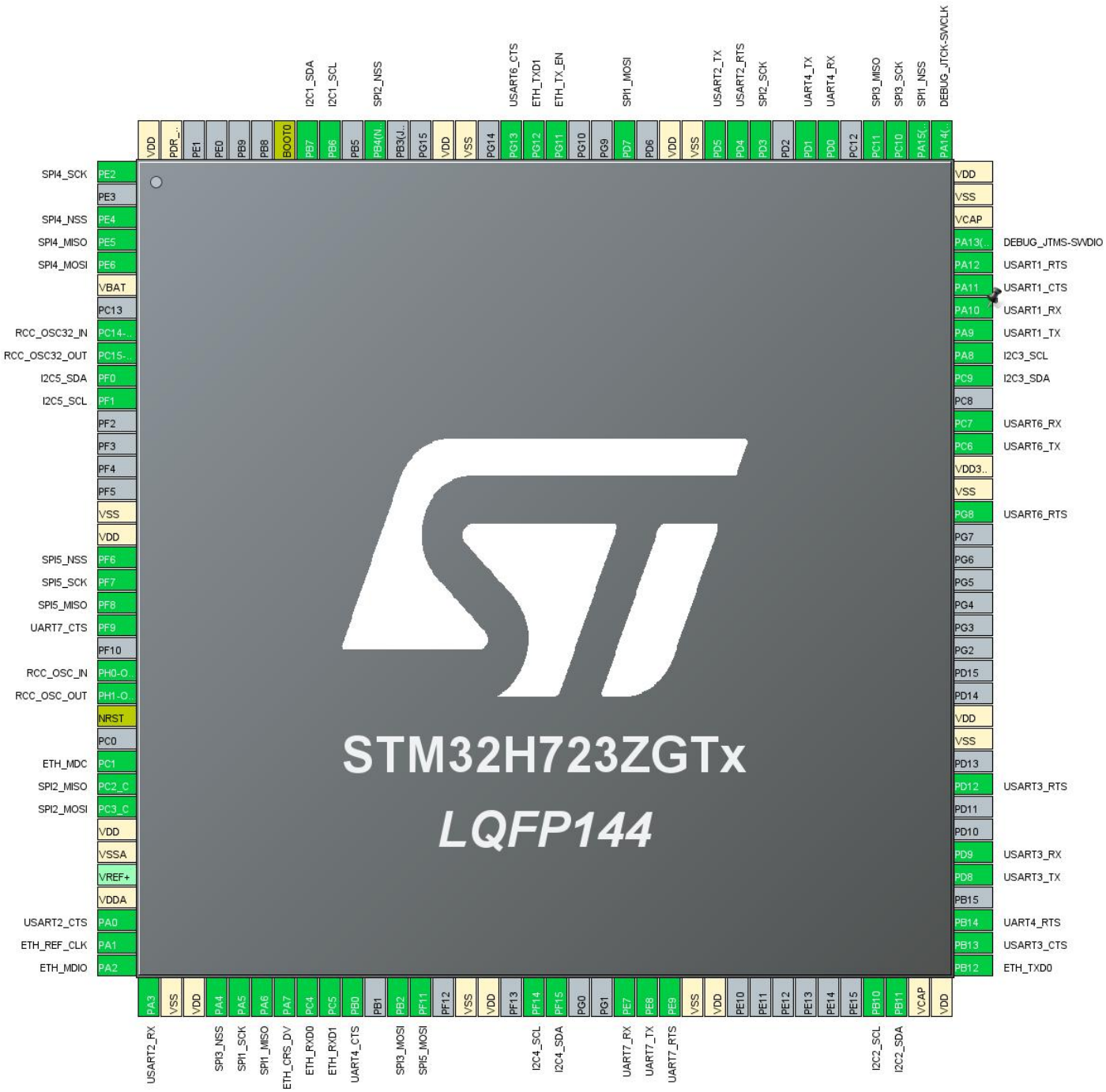
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



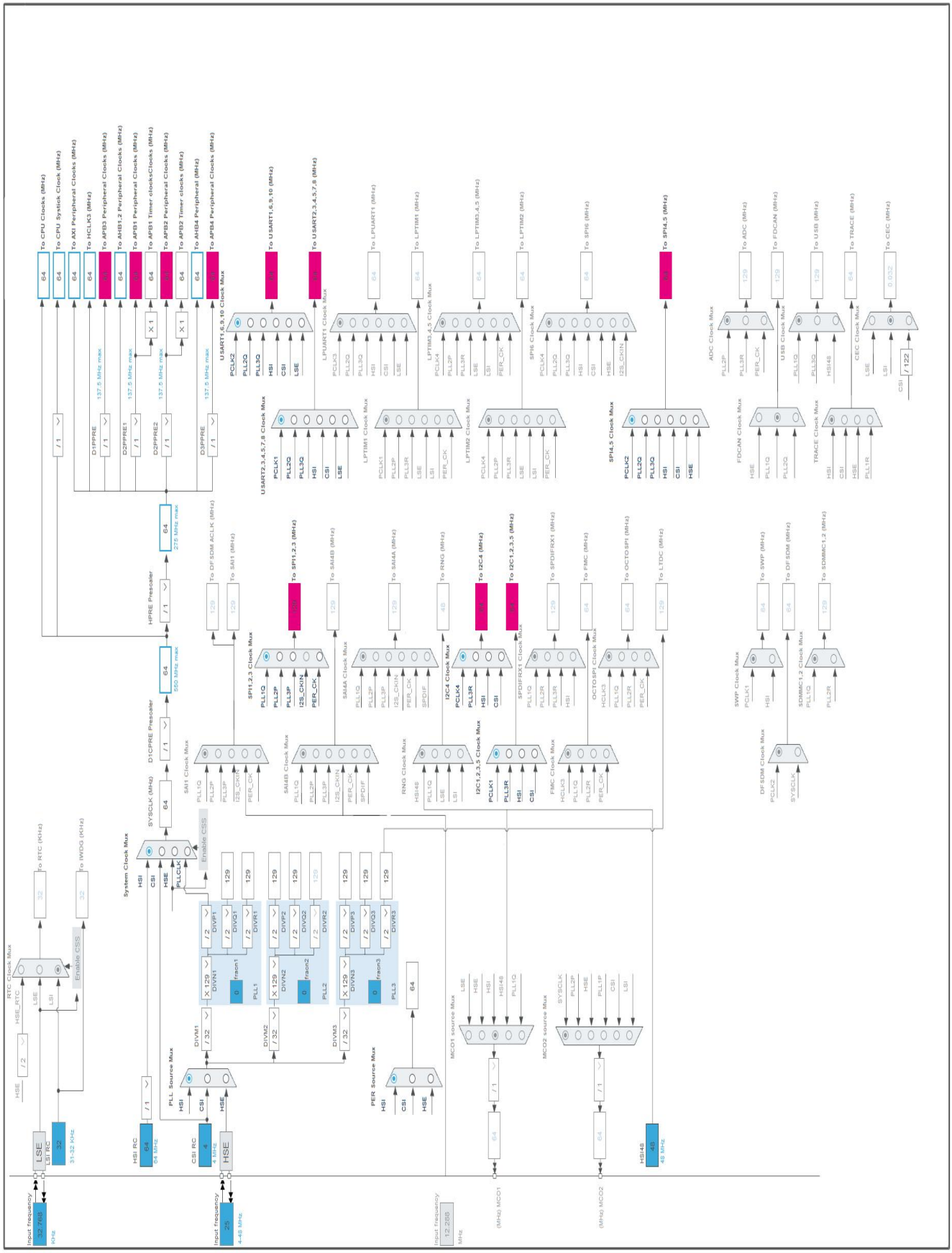
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
3	PE4	I/O	SPI4_NSS	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C5_SDA	
11	PF1	I/O	I2C5_SCL	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	SPI5_NSS	
19	PF7	I/O	SPI5_SCK	
20	PF8	I/O	SPI5_MISO	
21	PF9	I/O	UART7_CTS	
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
28	PC2_C	I/O	SPI2_MISO	
29	PC3_C	I/O	SPI2_MOSI	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	USART2_CTS	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI3_NSS	
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PB0	I/O	UART4_CTS	
48	PB2	I/O	SPI3_MOSI	
49	PF11	I/O	SPI5_MOSI	
51	VSS	Power		
52	VDD	Power		
54	PF14	I/O	I2C4_SCL	
55	PF15	I/O	I2C4_SDA	
58	PE7	I/O	UART7_RX	
59	PE8	I/O	UART7_TX	
60	PE9	I/O	UART7_RTS	
61	VSS	Power		
62	VDD	Power		
69	PB10	I/O	I2C2_SCL	
70	PB11	I/O	I2C2_SDA	
71	VCAP	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	USART3_CTS	
75	PB14	I/O	UART4_RTS	
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
81	PD12	I/O	USART3_RTS	
83	VSS	Power		
84	VDD	Power		
93	PG8	I/O	USART6_RTS	
94	VSS	Power		
95	VDD33USB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
99	PC9	I/O	I2C3_SDA	
100	PA8	I/O	I2C3_SCL	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	USART1_CTS	
104	PA12	I/O	USART1_RTS	
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
110	PA15(JTDI)	I/O	SPI1_NSS	
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	SPI3_MISO	
114	PD0	I/O	UART4_RX	
115	PD1	I/O	UART4_TX	
117	PD3	I/O	SPI2_SCK	
118	PD4	I/O	USART2_RTS	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	SPI1_MOSI	
126	PG11	I/O	ETH_TX_EN	
127	PG12	I/O	ETH_TXD1	
128	PG13	I/O	USART6_CTS	
130	VSS	Power		
131	VDD	Power		
134	PB4(NJTRST)	I/O	SPI2_NSS	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
143	PDR_ON	Power		
144	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	OTB-Backplane
Project Folder	C:\projetLocal\Open-test-bench\Software\Embedded\Backplane
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ETH_Init	ETH
4	MX_I2C1_Init	I2C1
5	MX_I2C2_Init	I2C2
6	MX_I2C3_Init	I2C3
7	MX_I2C4_Init	I2C4
8	MX_I2C5_Init	I2C5
9	MX_SPI1_Init	SPI1
10	MX_SPI2_Init	SPI2
11	MX_SPI3_Init	SPI3

Rank	Function Name	Peripheral Instance Name
12	MX_SPI4_Init	SPI4
13	MX_SPI5_Init	SPI5
14	MX_UART4_Init	UART4
15	MX_UART7_Init	UART7
16	MX_USART1_UART_Init	USART1
17	MX_USART2_UART_Init	USART2
18	MX_USART3_UART_Init	USART3
19	MX_USART6_UART_Init	USART6

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723ZGTx
Datasheet	DS13313_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

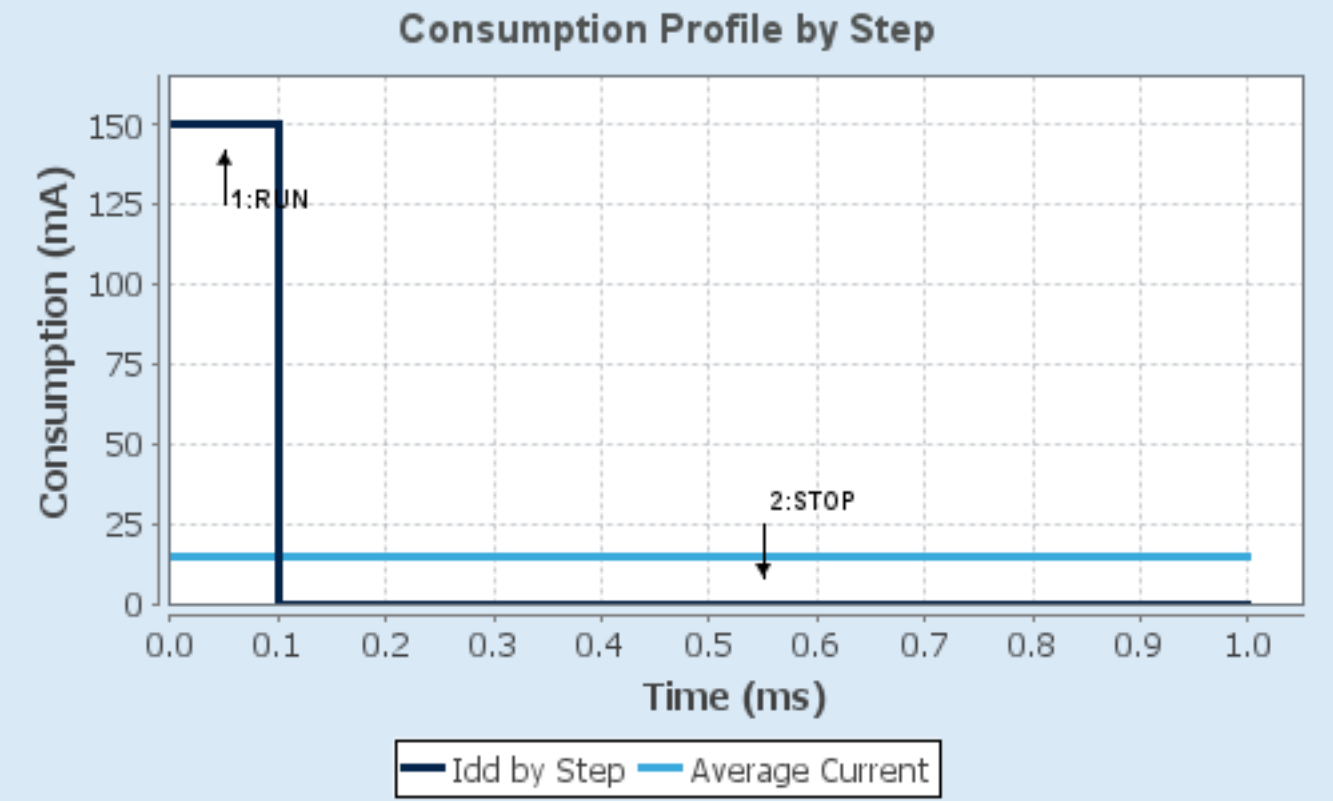
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS_OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	105.2	124.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. DEBUG

Debug: Serial Wire

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. I2C3

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit

Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. I2C4

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. I2C5

I2C: I2C

7.7.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled

General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range

7.9. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2

Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.10. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low

Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.11. SPI3

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.12. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.13. SPI5

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.14. SYS

Timebase Source: SysTick

7.15. UART4

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. UART7

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.17. USART1

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USART3

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

7.20. USART6

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C4	PF14	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C5	PF0	I2C5_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C5_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-	RCC_OSC_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_IN					
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15(JTDI)	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC3_C	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4(NJTRST)	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI3	PA4	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI5	PF6	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF11	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PB0	UART4_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	UART4_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD0	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PF9	UART7_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	UART7_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	USART1_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USART1_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA0	USART2_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD4	USART2_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB13	USART3_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	USART3_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PG8	USART6_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	USART6_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
SPI3 global interrupt	unused		
UART4 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
SPI4 global interrupt	unused		
SPI5 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
HSEM1 global interrupt	unused		
I2C5 event interrupt	unused		
I2C5 error interrupt	unused		

8.5.2. NVIC Code generation

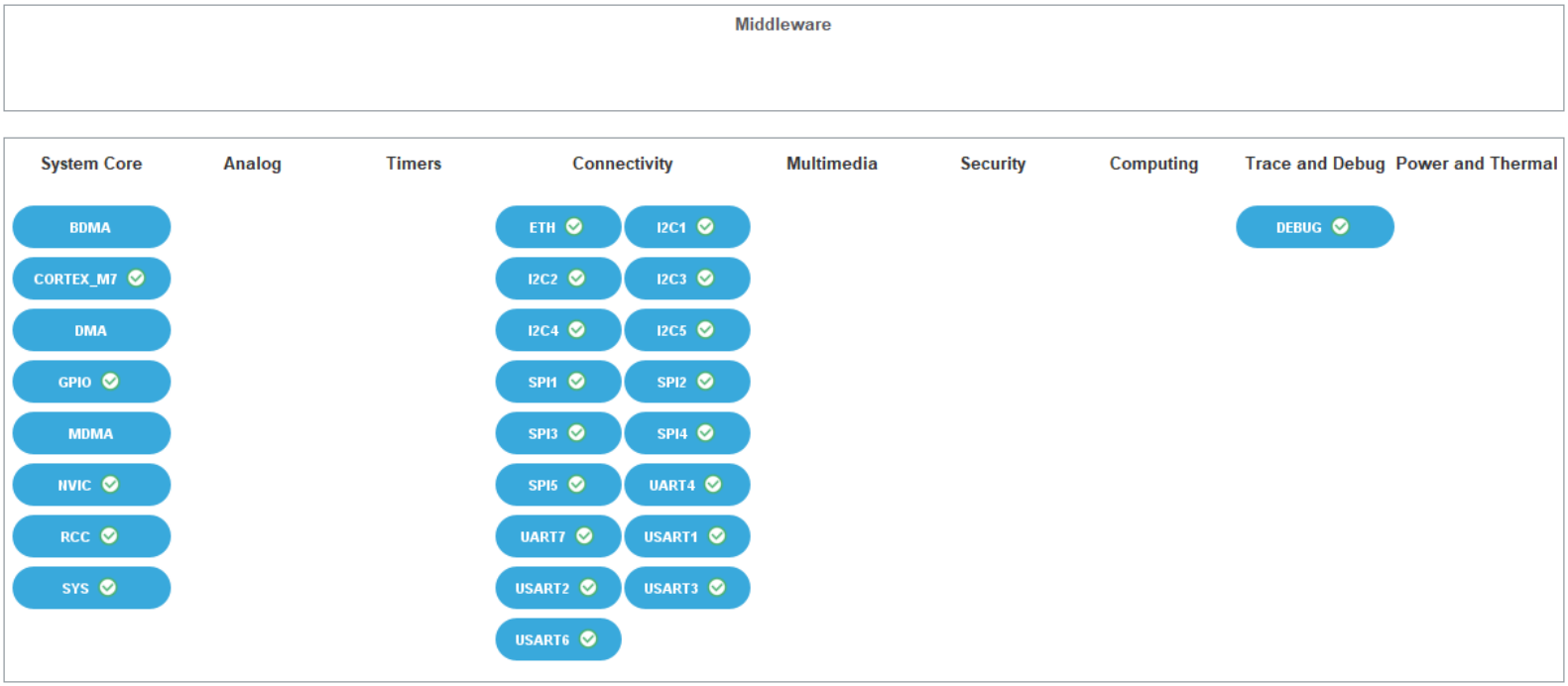
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00701028.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00603761.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00625312.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf

Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00407776.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00663674.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf